High resolution electric field imaging using ultra-low capacitance probes

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Declaration

I hereby declare that this thesis has not been and will not be submitted in whole or in part to another University for the award of any other degree

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SUMMARY

Imaging of material properties by direct measurement of electric field allows the non-contact determination of a number of important properties. The development of ultra-low capacitance probes for high spatial resolution measurements, based on the Electric Potential Sensor, forms the bulk of the work in this thesis. This sensor's unique and low capacitance design enables the use of smaller sense electrodes, down to 6 μm, while still maintaining a relatively wide signal bandwidth. The imaging techniques presented have significant advantages over other methods where mesoscopic spatial resolution is required. Three distinct measurement modes are explored which variously allow the imaging of surface topography, dielectric constant, static charge density and electrical conductivity.

The Electric Potential Sensor is a generic sensing technology developed at the University of Sussex. Details of various sensor designs and the applications of the sensors to the imaging of electric potentials has been published previously and demonstrated for the non-destructive testing of composites and the imaging of signals in digital integrated circuits. These previous investigations have been limited primarily by shortcomings in the probe design, particularly the sensitivity, spatial resolution, stability, and versatility.

An ultra-low capacitance probe is designed using discrete transistors. The characterisation and application of this sensor to high resolution imaging is described. Results, using this design, are presented for the first microscopic charge imaging system to provide time dependent charge density information. In addition, the use of both phase and amplitude for information obtained from a.c. signals is demonstrated. The wider application of this sensor to other measurements is discussed, including the remote electrocardiograph and the contact electromyogram. In each case the benefits of increased dynamic range and reduced input capacitance are demonstrated. By investigating the implementation of the sensors using discrete transistors, the additional possibility of producing a CMOS integrated sensor is explored.

Acknowledgements

It is with great pleasure and humble thanks that I arrive at this point where I may acknowledge the invaluable guidance of my supervisors, both those formally identified as such and the many others who have contributed along the way. Their gentle encouragement, and above all their tactful and wise recognition of both difficulty and ability, have allowed me to achieve so much that I never thought possible.

Huge thanks to Claire for her patience, tolerance and support over the last year whilst 'the thesis' always won the better part of my time.

To Martin, Sam, Tash, Ahmet, Shrijit, Dave and all the other colleagues, students, technicians and teachers who have been truly invaluable over the past 4 years I extend a truly gargantuan, over the top and truly genuine 'thanks very much indeed'.

One doesn't wish to become too sentimental, but it is a rare occasion indeed that one is given the space to formally thank those whom without which, this would really not have been possible. And so I thank my parents Tom and Annemarie, who have selflessly worked so hard for many years on my behalf.

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1 INTRODUCTION

There has been much work in recent years concerning the application of high impedance sensors to several diverse fields, including medicine, security, materials science and fundamental physics. Over the past ten years at the University of Sussex a high impedance sensing technology known as the electric potential sensor (EPS) has been developed. Some of the application areas, particularly electrophysiology, have reached a level of maturity in the laboratory and now must be translated to commercial production.

In moving to a commercial product it is necessary to prepare sensor designs for widespread production. In the interests of reducing cost and optimising performance, the implementation of high impedance sensors in commercial integrated circuit processes is required. Cementing the specification and understanding of these devices into a set of hard specifications is necessary in order to successfully transfer the technology outside of the laboratory. This has been a key motivation for much of the work described in this thesis.

Prior work on the EPS has been driven by the exploration of the diverse applications of this technology. Early work at Sussex demonstrated the application of these high impedance sensors to electrophysiological measurements such as the electrocardiogram. Later, the applications were expanded across the breadth of electrophysiological measurements, and further into materials testing. Each of these major application areas

will be visited throughout this thesis. One notable area of EPS research that will not be addressed here is the application of high impedance sensors in the radio frequency domain, a significant area of research typified by the work of Prance & Aydin (Prance and Aydin, 2007b).

There is little need to further introduce the electric potential sensor here, since this is the subject of chapter 2. This chapter is indeed rather more than an introduction, representing an expanded and more complete discussion of the operation and design of electric potential sensors than has previously been attempted in the field. Electrical models of the electric potential sensor are developed, which consider the input impedance, bandwidth and noise performance that are related to the feedback techniques employed in constructing these high impedance amplifiers. The study of the fundamentals of the EPS sensor and subsequent compilation of this material into chapter 2 represents the most significant contribution to the field made by this thesis work.

Following this generalised and detailed treatment of the electric potential sensor, chapter 3 develops the experimental justification for the preceding theoretical analysis. This experimental work is given with a thorough discussion of the methods and the tools used in characterising the electric potential sensor; the development of such methods having been a major part of this experimental work.

In chapter 4 the development of specialized EPS circuits from discrete transistor circuit elements is described. These discrete circuits, having been developed as part of this thesis work and considered a major contribution to the field, are used to produce the ultra-low capacitance sensors of the title. This approach marks a departure from the work of previous EPS experiments at Sussex, where the sensors have generally been constructed from integrated circuit operational amplifiers. The relevant transistor parameters are discussed, and several circuits for EP sensors are described.

The results of a series of experiments which capitalize on the performance of these discrete EP sensors are given in chapter 5. These are: the remote measurement of cardiological activity in unshielded environments; and the surface electromyogram

(sEMG) at high spatial resolution. In addition to these experiments, results from characteristic measurements are given for a discrete transistor EPS.

The ultra low capacitance sensors which have been described are particularly suited to microscopic imaging applications. Thus, chapter 6 describes an extended experimental investigation into the use of such sensors for a group of 3 electric potential microscopy methods which have application in materials testing, as well as a less immediately obvious application in forensics.

2 THE ELECTRIC POTENTIAL SENSOR

2.1 The EPS sensing technology

Electric Potential Sensor (EPS) is the name coined to describe a generic sensing technology developed at the University of Sussex. The technology represents the culmination of several high impedance amplifier techniques with a broad range of measurement methods. An EPS sensor is, of itself, not much more than a high-impedance amplifier which may be constructed using several, or perhaps none, of the special techniques employed at the University of Sussex. Such an amplifier can only be described as an EPS once it has been supplemented with an input electrode structure and has the requisite electrical characteristics to make non-invasive measurements of electric potential. This last requirement is often only met in a given measurement scenario by the application of all of these high impedance techniques. An electric potential sensor is therefore defined as a solid state device which measures electric potential non-invasively by capacitive coupling. In this context the term non-invasive is used in a manner best demonstrated by referring to a device analogous to the EPS; the magnetometer. These devices are available in a variety of configurations, capable of measuring very small or very large magnetic fields. A magnetometer can be considered non-invasive both in the sense that it causes very little disturbance to the gross magnetic field which it is intended to measure, and that it need not be coupled directly to the source. An EPS should perform a similar function for electric field measurement. Many of the applications in which electric potential sensing technology has been deployed

represent unique measurement opportunities that in many cases have not previously been possible, or indeed attempted.

It will be extremely valuable to the reader to immediately clarify what an EPS consists of, and so, in figure 2-1, a schematic for an amplifier circuit which has some basic electric potential sensing capability is provided—and is therefore close to being designated an Electric Potential Sensor. The circuit consists of an operational amplifier (op-amp) configured as a unity gain voltage buffer. The op-amp chosen here has been selected for its low input bias current (60 fA) and relatively low input capacitance (1 pF). The high impedance input node of the circuit is connected to an electrode, represented in the schematic as one half of a capacitor. The choice of this symbol is a useful one, as will shortly become apparent. A high value resistor has been connected from the input node to ground, in order to provide a DC bias point of approximately 0 V. The value of the resistor has been chosen to maintain high input impedance, whilst also limiting the DC offset produced by the input bias current of the op-amp. The input electrode provides a means for a source of electric potential to capacitively couple to the input of the amplifier. This could be a voltage source which is connected to its own electrode, such as a function generator connected to a metal plate; or the source could be heart muscle cells, generating an electric potential during de-polarisation, with the entire human body acting as an electrode. An alternative interpretation of the sensor-source

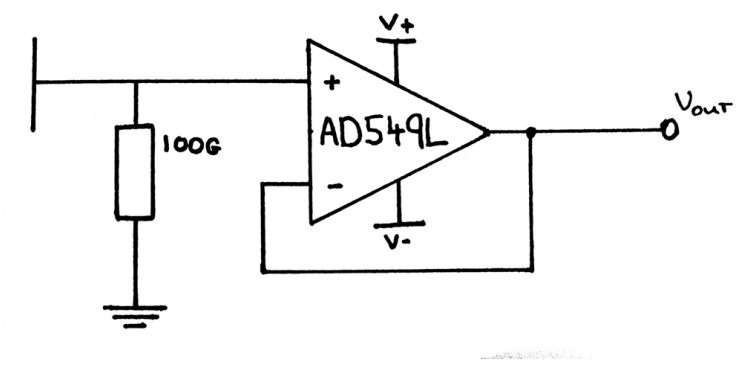


Figure 2-1: An amplifier circuit capable of electric potential sensing. A low input-bias current operational amplifier has been used in a non-inverting voltage buffer configuration. Positive and negative supplies are required for symmetric signal swings. A high valued resistor provides DC biasing of the input at 0 V. An input electrode is represented by a symbol intended to represent one plate of a capacitor.

coupling considers the self-capacitance of the input electrode coupling to an electric field. By adding such a source of potential—with its associated electrode—to the diagram given in figure 2-1, the half-capacitor symbol would be completed.

Clearly, since the input signal is capacitively coupled to the amplifier circuit, the input impedance of the amplifier is of paramount importance in determining sensitivity. The remainder of this chapter is largely concerned with discussing a series of techniques which have been found to deliver amplifier circuits with very high input impedance whilst retaining low noise. These techniques represent the core of the EPS technology.

2.2 Source Coupling

There are uncountable sources of electrical potential that an experimenter might wish to measure using an EP sensor. It is useful to categorize these various sources where possible, since they may define the type of sensor and electrode used. The chief qualifier which determines the nature of the measurement is not so much the source of potential itself, but rather how strongly or weakly it is capacitively coupled to the source. The terms strong or weak are used to describe the two extreme cases of source sensor coupling, in terms of the relationship between the source coupling capacitance and the sensor input capacitance. Since a typical sensor might have an input capacitance of around 1 pF (Prance et al., 2000) then any source which is coupled to the sensor by a capacitance much less than 1 pF would be considered weakly coupled. In the opposite situation, where the coupling capacitance is comparable to or much larger than the sensor input capacitance, then the measurement is described as strongly coupled. This designation is based on the ratio of these two capacitances since the coupling capacitance and the input capacitance of the sensor form a capacitive potential divider. The relationship between the sensor input impedance and the source coupling capacitance, and its affect on sensitivity, will be discussed further in the following section.

In a weakly coupled system the potential measured by the EP sensor will be attenuated with respect to the source potential. The success of a weakly coupled measurement will depend on a variety of factors, including: the amplitude and frequency of the source potential; the magnitudes, frequencies, and coupling capacitances of other ‘noise’ potentials; the input capacitance of the sensor; and the electrical noise of the sensor.

If the contribution of external noise sources is briefly ignored, then a few simple remarks may be made on weakly coupled measurements. When the source potential is large compared to the input voltage range of the sensor, then the attenuation due to weak coupling is not so important. Indeed, this property becomes particularly useful when potentials of many hundreds or thousands of volts are to be measured by a low-voltage sensor. When the source potential is much smaller, then the resolution of the measurement may be compromised. In the extreme, the source potential may be entirely undetectable due to the inherent electrical noise of the sensor. In some situations it may be possible to use a larger input electrode, thereby increasing the coupling capacitance. If this cannot be allowed, perhaps due to packaging issues, or the need for a spatially resolved measurement, then the only solution is to seek to improve the sensor input impedance, noise performance, or both.

In weakly coupled measurements it is often possible for external sources of potential to couple to the sensor. Two stratagems may be employed to overcome this: the experimenter may seek to reduce the coupling of the noise source to the sensor, either by changing the measurement geometry or by some other means; or the desired signal may be extracted from the noisy signal by signal processing. In some cases it will be impossible to make a satisfactory measurement if the amplitude of the noise source at the sensor input is significantly larger than that of the signal source. This is especially the case when the sensor is saturated by the noise potential, as can be the case with mains borne noise. Some external noise sources may be removed by applying signal processing techniques to the sensor output signal. The complexity of implementation and the ultimate success of these techniques will depend on the frequency- and time-domain characteristics of both the source potential and noise potentials present. One

common noise potential encountered in remote measurements is produced by the mains power circuit. Fortunately the continuous and relatively fixed frequency bands over which this noise source emits can be effectively filtered (Prance et al., 2007) (Beardsmore-Rust et al., 2009c). An undesirable signal due to the movement of humans close to the sensor is, however, not so well defined in time and frequency domains and is consequently difficult to remove in post-processing. Conversely, if the source potential can be well defined in the frequency domain then it is possible to tightly limit the bandwidth of the sensor to this region of interest. This is the case in ECG measurement, where a monitoring (rather than diagnostic) quality ECG can be recorded in the frequency band 0.5-30Hz (Bailey et al., 1990). By filtering in this band noise signals due to mains wiring, as well as the most significant movement artefacts, can be effectively removed.

In strongly coupled measurements the sensor and source of potential are often in mechanical contact. The strong capacitive coupling is significantly larger than the coupling to any external noise sources, effectively screening noise, and the mechanical coupling eliminates noise due to relative movement of sensor and source. The only noise sources which therefore remain are the electrical noise of the sensor and any other noise potentials on the source itself. Despite the mechanical contact between sensor and source, it is important that resistive contact is not permitted between the two since this would usually have the effect of improperly biasing the sensor or allowing undesirable DC and low frequency potentials to affect the measurement. The input electrode is usually coated with an insulating film so that it may be applied in contact with the source potential and couple only capacitively to it. This film may be an oxide layer or a plastic film such as PTFE.

2.3 Input impedance and its effect on sensitivity

A simple model of an EP sensor consists of an 'ideal' voltage buffer, with a resistor and a parallel capacitor shunting the input signal to ground. This circuit is similar to that given in figure 2-1, but it considers the entire contribution of both real and parasitic circuit elements. This model is used in order to assess the interaction of the coupling capacitance and the input impedance of the sensor. The input resistor and capacitor represent the lumped contributions of various resistive leakage paths and capacitive shunts. The combination of these two components forms the input impedance of the sensor.

When a capacitor is used to couple a voltage source to the EPS, the circuit shown in figure 2-2 is produced. This capacitor may be a traditional leaded component, or it may be the electrode-source capacitance in a real EPS measurement. The input capacitor which connects the EPS to an external source is referred to as C_C. When C_C is known the values of the two unknown components can be found. These components are denoted C_{IN} and R_{IN} respectively, with the subscript *IN* indicating that these correspond to the input impedance of the EPS. The total input impedance of the sensor, Z_{IN}, is therefore simply expressed as the parallel combination of these, $Z_{IN} = C_{IN}||R_{IN}$.

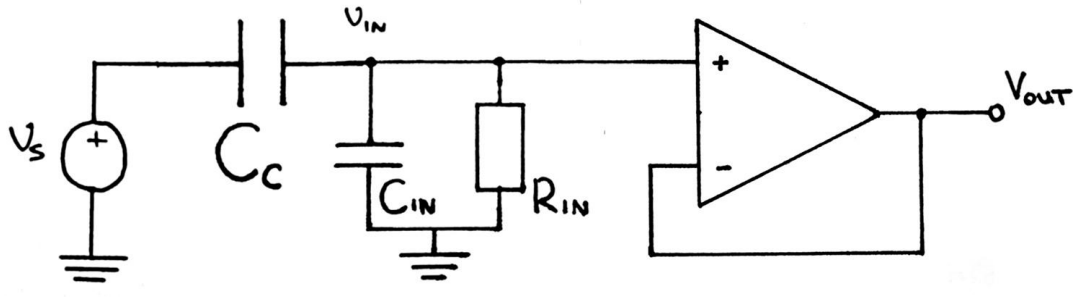


Figure 2-2: EPS input stage equivalent circuit. A signal voltage source, V_S is connected to the EPS input via a coupling capacitance C_C. The EPS has an input impedance represented by C_{IN} and R_{IN}, which shunt the input node, V_{IN}, to ground. V_{IN} is buffered by an ideal voltage buffer.

The circuit described in figure 2-2 has a frequency response characteristic of a shelving high-pass filter. This response is illustrated in figure 2-3. Analysis of the circuit is simplified by considering the two separate cases where the behaviour is either dominated by C_{IN} or R_{IN}. Above a certain corner frequency, denoted ω_c, the reactance of the input capacitance C_{IN} is much lower than the resistance R_{IN}. In this case the effect of R_{IN} is negligible, and the circuit behaves as a capacitive potential divider, with a correspondingly flat response in this region. For the low frequency case, where the reactance of C_{IN} is large such that R_{IN} dominates the response, then a high-pass filter is formed by the combination of R_{IN} and C_C. This two-case approach can be used extensively throughout the analysis, design and use of EP sensors.

Despite the utility of this two-case approach in understanding the response of the EPS circuit, it is necessary to consider the circuit as a whole in order to describe the response in the transition region. By describing the behaviour in the transition region a relationship between the corner frequency, ω_c, and the values of C_{IN} and R_{IN} can be found.

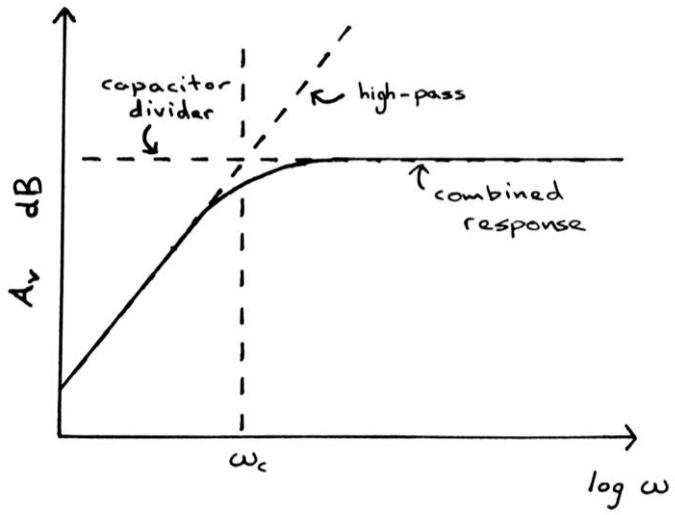


Figure 2-3: Simplified frequency response of the circuit given in Figure 2-2. Dashed lines have been used to show the response due to the two separate components of the sensor input impedance. The solid line represents the combined response. A capacitive potential divider is formed between C_{IN} and C_C producing a flat response. A high-pass filter is formed between R_{IN} and C_C.

Since the amplifier is modelled as an ideal buffer characterised by the following equation,

$$v_o = v_{IN}$$

the transfer function of the circuit, in s-space, can be stated as follows

$$\frac{v_o}{v_s} = T(s) = \frac{Z_{IN}}{Z_{C_c} + Z_{IN}}$$

where Z_{IN} is as previously defined and Z_{C_c} is the impedance of the input coupling capacitor, C_c. The conventional Laplace transform is used, where $s = j\omega$. The proceeding analysis is simplified if the transfer function is instead written in terms of admittance, Y, where $Y = 1/Z$, and conductance, G, where $G = 1/R$. The transfer function then becomes

$$T(s) = \frac{Y_{C_c}}{Y_{C_c} + \mathrm{Y}_{IN}}$$

with the two admittances,

$$Y_{C_c} = sC_c$$

$$Y_{IN} = sC_{IN} + G_{IN}$$

which gives equation 2.1, the complete transfer function,

$$T(s) = \frac{\mathrm{s}C_c}{s(C_c + \mathrm{C}_{IN}) + \mathrm{G_{IN}}} \qquad 2.1$$

This bilinear expression is a first order function of s, whose coefficients are real constants, and so has the expected single pole-zero. It is referred to as bilinear since it is the combination of two straight line graphs, or first order polynomials. These two straight lines correspond to the separate contributions discussed earlier and illustrated in figure 2-3. A bilinear function can be written as composed of two functions, $N(s)$ and $D(s)$, the numerator and denominator polynomials respectively, with coefficients b_n and a_n (Schaumann and Van Valkenburg, 2001).

$$T(s) = \frac{N(s)}{D(s)} = \frac{b_1 s + b_0}{a_1 s + a_0} \tag{2.2}$$

equation 2.2 can be rewritten in the form

$$T(s) = \frac{N(s)}{D(s)} = \frac{b_1}{a_1}\frac{s + b_0/b_1}{s + a_0/a_1} = K\frac{s + z_1}{s + p_1} \tag{2.3}$$

where z_1 corresponds to the zero of $T(s)$ and p_1 is the pole. The transfer function of equation 2.1 can be brought into the standard form of equation 2.3,

$$T(s) = \frac{C_c}{C_{IN} + C_c}\ \frac{s}{s + G_{IN}/(C_{IN} + C_c)} \tag{2.4}$$

revealing the location of the pole and zero in the s-plane as the roots of the denominator and numerator polynomials respectively. A zero is found at $s = -z_1$,

$$s = -z_1 = 0$$

with a corresponding pole at $s = -p_1$

$$s = -p_1 = -G_{IN}/(C_{IN} + C_c)$$

This pole corresponds directly to the corner frequency

$$\omega_c = p_1 = G_{IN}/(C_{IN} + C_c)$$

which can now be rewritten in more convenient units

$$f_c = \frac{\omega_c}{2\pi} = \frac{1}{2\pi R_{IN}(C_{IN} + C_c)} \tag{2.5}$$

The single pole and single zero indicates a first order, high-pass frequency response, with the corner frequency f_c defining the half-power (-3 dB) output.

A simplified equation for the case where the signal frequency, ω, is much greater than ω_c can be derived from the transfer function. Under this condition the following can be stated,

$$\frac{1}{R_{IN}(C_{IN} + C_c)} \ll s \qquad\qquad for\ \omega \gg \omega_c$$

equation 2.4 can then be written as

$$T(s) \cong \frac{C_c}{C_{IN} + C_c} \quad for\ \omega \gg \omega_c \qquad 2.6$$

Equation 2.6 is of course the capacitive potential divider equation, with no pole or zero, and so the expected behaviour is found at these frequencies.

In the previous discussion the gain of the ideal amplifier shown in figure 2-2 has been assumed to be unity. In many sensor applications this input amplifier stage may have gain greater than unity, and indeed it may be followed by subsequent high-gain stages. In this case the total gain of the amplifier must be found and used to refer the output voltage back to the voltage at the input node of the sensor before input impedance can be determined.

The value of input impedance represents the source loading that the sensor presents. It therefore determines the sensitivity to a given source potential when coupled through a coupling capacitance C_C. If the high frequency limit where C_{IN} dominates is considered, (as it should be, since it is usually undesirable to operate a sensor at a frequency below ω_c) then the sensitivity is found to depend on C_C and C_{IN} only. Equation 2.6 therefore formalizes the previous discussion of the sensitivity to a given source.

2.4 Positive feedback techniques for boosting input impedance

Three related techniques are discussed here which are applied to achieve high input impedance in EP sensors. These 3 techniques are guarding, neutralization and bootstrapping. All involve the application of a potential to a two-terminal device such that the voltage across the device is minimized. The subsequently reduced current can be interpreted as an increase in the *effective* impedance. The 3 techniques will be discussed separately and the concept of effective impedance explored.

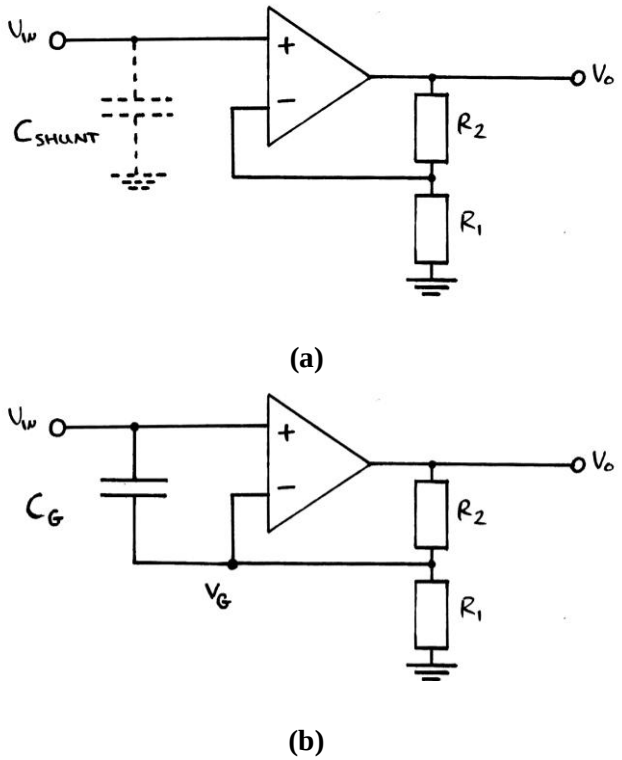


Figure 2-4: Amplifier with additional input shunt capacitance represented by C_{SHUNT}. In (a) this shunt capacitance increases the input capacitance of the (ideal) amplifier. In (b) this capacitance has been connected to a low impedance node at unity gain with respect to the input network. The capacitance is relabelled C_G since it is now a guarded capacitance.

2.4.1 Guarding

When an amplifier is assembled on a printed circuit board, or has any form of connection made to its input, a parasitic shunt capacitance, C_{SHUNT}, is added, usually between the input of the amplifier and ground. This capacitor may be formed through PCB trace capacitance to a ground plane, the shield capacitance of a coaxial cable, some combination of these two, or any others. The total shunt capacitance on the input of the ideal op-amp is represented by C_{SHUNT} in Figure 2-4a.

When C_{SHUNT} is disconnected from ground and instead connected to a low impedance node in the circuit at a potential equal to that of the input, as shown in Figure 2-4b, C_{SHUNT} is *guarded* and the input capacitance of the amplifier is decreased (Keithley Instruments Inc., 1998). This shunt capacitance is now denoted C_G to recognise that it is a guard capacitance. Since no current flows through the inputs of the ideal op-amp, the input current of the amplifier is due to C_G only and is given by equation 2.7;

$$i_{IN} = v_{C_G} s C_G$$

$$i_{IN} = (v_{IN} - v_G)\, s C_G \qquad 2.7$$

When v_G is equal to v_{IN} then the current i_{IN} is zero and C_G no longer has any loading effect. Equation 2.7 can be rewritten as

$$i_{IN} = v_{IN}(1 - A_G)\, s C_G \qquad 2.8$$

Where A_G represents the gain applied between v_{IN} and v_G. For the ideal op-amp in Figure 2-4b, A_G is equal to 1. An effective guard capacitance, $C_{G,eff}$, can then be defined as

$$C_{G,eff} = (1 - A_G) C_G \qquad 2.9$$

So that equation 2.8 becomes

$$i_{IN} = v_{IN} s C_{G,eff} \qquad 2.10$$

By defining $C_{G,eff}$ it is possible to intuitively assess the effect of the guarded shunt capacitance on the input of the amplifier. If A_G is exactly 1 then $C_{G,eff}$ = 0 and the capacitance is perfectly guarded – it has no capacitive loading of any source impedance connected to the amplifier input.

Defining an effective capacitance may seem an overly indulgent piece of mathematics, and may even seem sloppy. However, if the charge required to produce a given output voltage on the guarded input capacitance is calculated, it would be seen that the definition of effective input capacitance is quite reasonable. The value of $C_{G,eff}$ can be used in the model EPS circuit given in Figure 2-2 and characterised by the transfer function of equation 2.1 to find the response of the guarded amplifier.

When A_G is greater than one, $C_{G,eff}$ will have a negative value. This result is not as confusing as it may first seem. This concept is explored in the following section on neutralization.

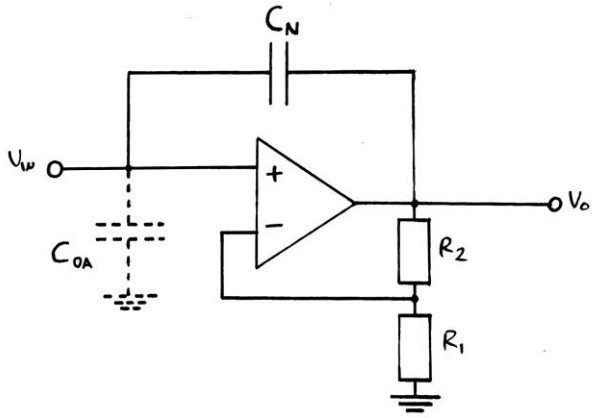


Figure 2-5: Amplifier with the common-mode input capacitance of the op-amp, C_{OA}, included. A neutralizing capacitor, C_N, is connected between the input and low impedance output of the amplifier.

2.4.2 Neutralization

By increasing the gain of the guard circuit above unity, additional shunt capacitances can be neutralized (Graeme, 1973). In figure 2-5, C_N cancels the input current which is shunted by the common-mode input capacitance of the op-amp, C_{OA}. Figure 2-5 follows from Figure 2-4, with the parasitic input capacitance C_{OA} added to the ideal amplifier model.

An expression for the total input capacitance can be found by considering the currents through C_{OA} and C_N

$$i_{C_{OA}} = V_{IN} s C_{OA}$$

$$i_{C_N} = (v_{IN} - v_o) s C_N$$

The output voltage is related to the input by,

$$v_o = A_{CL}\, v_{IN} \qquad 2.11$$

where A_{CL} is the closed loop transfer function of the operational amplifier circuit. For the ideal non-inverting amplifier of figure 2-5, A_{CL} is given by

$$A_{CL} = \frac{v_o}{v_{IN}} = \left(1 + \frac{R_2}{R_1}\right) \qquad 2.12$$

Using the principle of superposition at the input node, an expression for the input current, i_{IN}, in terms of the amplifier gain can be found

$$i_{IN} = v_{IN}s\big(C_{OA} - C_N(A_{CL} - 1)\big) \qquad 2.13$$

C_{OA} and C_N can now be replaced by a single effective capacitor representing the input capacitance of the amplifier. This input capacitance has the value,

$$C_{IN} = C_{OA} - C_N(A_{CL} - 1) \qquad 2.14$$

Equation 2.12 can be substituted into equation 2.14 to find an expression for C_{IN} of the circuit given in Figure 2-5, though it is preferred to retain the form of equation 2.14 for application to the generalised case where A_{CL} can be used to represent any transfer function between the input node and the neutralising capacitor.

When A_{CL} is given the value 1 then the neutralising capacitor is merely guarded and the same result is found as for the previous discussion. When A_{CL} is set appropriately the input capacitance of the amplifier can be reduced to zero. However, if the input capacitance is allowed to have a negative value, then the circuit will be unstable and oscillation will result. For this reason, it is impossible to achieve an input capacitance of zero in practical circuits. The degree to which neutralization can be achieved will be limited by the gain error of the amplifier and the stability and initial accuracy of the neutralizing and shunt capacitors.

2.4.3 Bootstrapping

The technique known as bootstrapping applies precisely the same principles as in guarding, but in this thesis the distinction is made when the technique is applied to resistive components.

The circuit of Figure 2-6a has an input resistance set by R_{IN} (the input resistance of the ideal op-amp is assumed to be infinite.) The input impedance of the circuit can be increased by connecting $R_{IN}$to a low impedance node in the circuit at a potential equal to that of the input, as in Figure 2-6b. By finding the current that flows through R_{IN} an

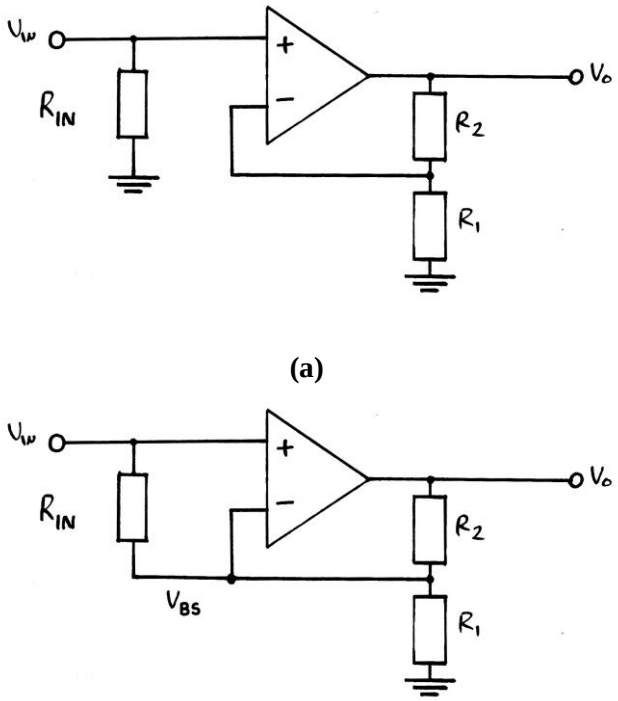


Figure 2-6: Amplifier with input resistor R_{IN}. (a) the resistor is connected to ground and sets the amplifier input impedance. (b) R_{IN} is bootstrapped by v_{BS} so that the input impedance of the amplifier is increased.

expression for the input impedance can be derived in the same manner as for the case where an input shunt capacitor is guarded.

The input current of the amplifier in Figure 2-6b is due to R_{IN} only and is given by equation 2.15

$$i_{IN} = \frac{v_{IN} - v_{BS}}{R_{IN}} \qquad 2.15$$

The input current will be zero when v_{BS} is equal to v_{IN}. In keeping with the treatment of guarding, an equation for an effective input resistance will now be found in terms of the gain applied between v_{IN} and v_{BS}, which is denoted A_{BS}. Equation 2.15 is rewritten in terms of A_{BS}

$$i_{IN} = \frac{v_{IN}(1 - A_{BS})}{R_{IN}} \qquad 2.16$$

so that an effective resistance can be defined, $R_{IN,eff}$, given by equation 2.17

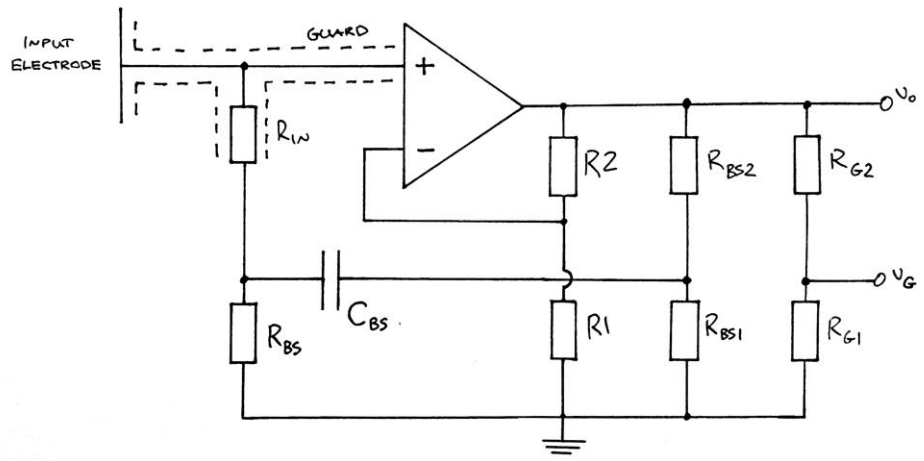
$$R_{IN,eff} = \frac{R_{IN}}{(1 - A_{BS})} \tag{2.17}$$

Whilst an infinite effective input resistance can be achieved by setting A_{BS} equal to one, similar limitations are applied to practical circuits as in the case of neutralisation, and so only an order of magnitude improvement of the value of R_{IN} is commonly achieved.

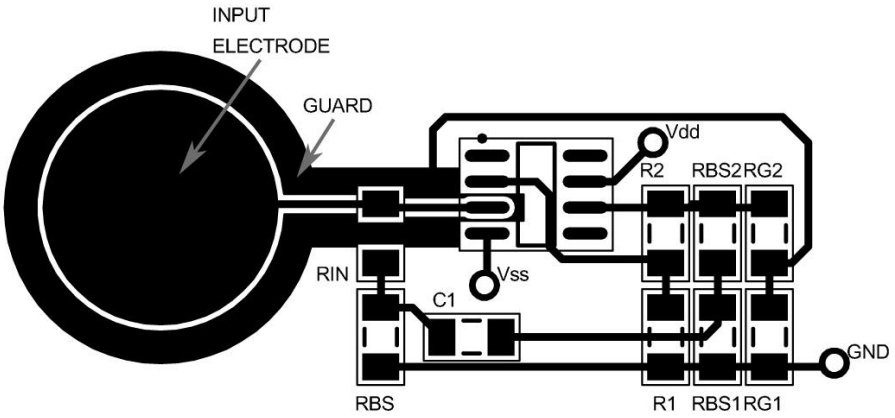
2.5 Application of high-impedance positive feedback techniques to non-ideal EPS circuits

In order to further explore the behaviour of the 3 positive feedback techniques the circuit of Figure 2-7a is considered. This schematic represents a basic, though functionally complete EP sensor. With appropriate choice of device for the operational amplifier this circuit can achieve good levels of performance for a range of applications. Figure 2-7b shows a printed circuit layout to illustrate the arrangement of input electrode and guard structure.

R_2 and R_1 set the gain of the non-inverting operational amplifier. R_{BS2} and R_{BS1} set the level of feedback for the bootstrapping of R_{IN}. The input guard is connected to v_G, which is set at a portion of the output voltage by $R_{G2}$and R_{G1}. v_G can therefore be set to provide only guarding of the input node, or it can be used to neutralize additional input capacitances.



(a)



(b)

Figure 2-7: (a) Schematic diagram of a basic EPS sensor with positive feedback. $R2$ and $R1$ set the overall gain of the operational amplifier. R_{BS2}, R_{BS1} and R_{G2}, R_{G1} set the bootstrap and guard feedback level respectively. (b) Illustrative printed circuit layout of EP sensor showing top copper and silkscreen layers. The entire input area is surrounded by a guard area, connected to v_G.

In Figure 2-7a, the capacitance between input and guard circuit has not been drawn. Figure 2-8 shows a modified schematic with the parasitic capacitances added and some of the circuit components reduced to blocks. A defined coupling capacitance, C_C and a source potential, v_s has also been added. The non-inverting op-amp has been replaced by an amplifier block having a frequency dependent transfer function $A_v(s)$. A parasitic shunt capacitance C_{SHUNT} is included which may represent any unguarded input capacitance. C_{SHUNT} may include contributions from the common mode input capacitance of the op-amp as well as board-level parasitics. The voltage dividers of Figure 2-7 have been replaced with constant multiplier blocks. The constants k_G and

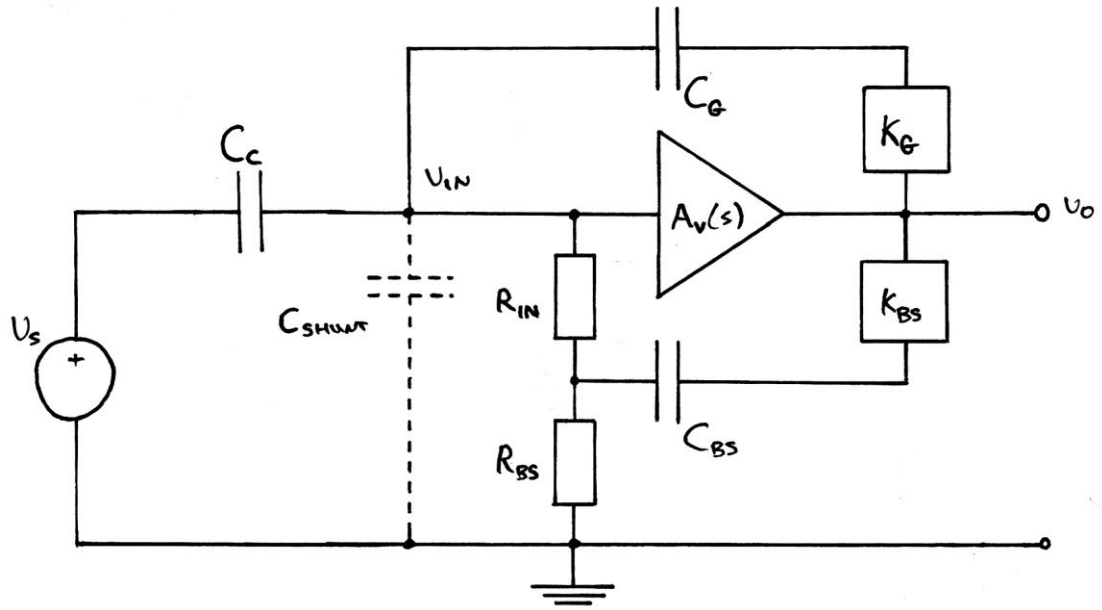


Figure 2-8: Simplified schematic of the basic EPS sensor. A source potential is coupled to the EPS input via a capacitance C_C. C_G is guarded by a fraction of the output potential set by k_G. Similarly, R_{IN} is bootstrapped at AC through C_{BS} by a fraction of the output set by k_{BS}. The amplifier is modelled as a voltage controlled voltage source with transfer function $A_v(s)$.

k_{BS} may take any real value between 0 and 1. This simplified schematic will form the basis of further analyses.

2.5.1 Bootstrapping of the AC-coupled EPS circuit

The input resistor R_{IN} is the biasing component for the non-inverting operational amplifier of Figure 2-8, and sets the DC input impedance. The series combination of R_{IN} and R_{BS} provides a path to ground for the (DC) input bias current of the operational amplifier and sets the operating point of the circuit. The value of these two resistors should be chosen to minimize the input offset voltage (due to the input bias current of the operational amplifier) to a tolerable level, whilst offering a high input resistance and hence low corner frequency. It should be noted that most JFET or MOSFET input operational amplifiers have a positive input bias current which flows *out* of the gate of the input transistor, though data sheets of various manufacturers may define the polarity of this current in various ways. This current results in a positive input offset voltage across the input resistance.

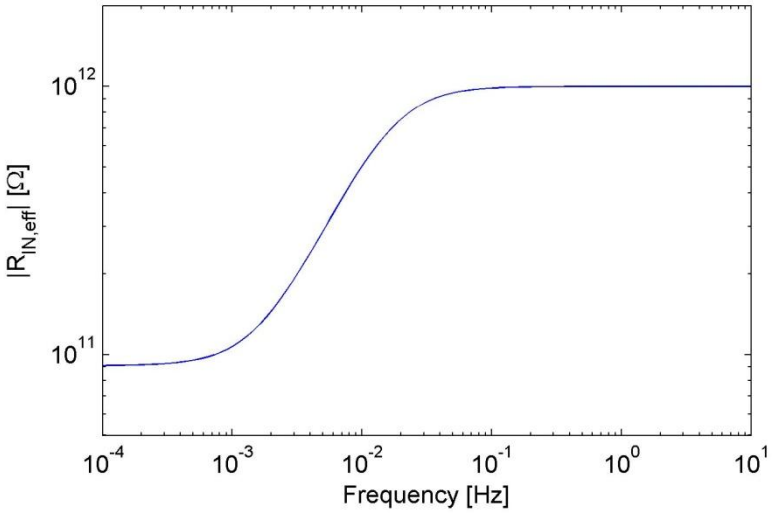


Figure 2-9: Bootstrapped input impedance of the circuit shown in Figure 2-7a. The DC value of R_{IN} is $100\,G\Omega$ $(= 10^{11}\Omega)$, with the following component values; $R_{BS} = 100\,M\Omega$, $C_{BS} = 1\,\mu F$. k_{BS} is set to 0.9.

The input resistor must be connected to a DC biasing potential (usually ground) since the EPS input is AC coupled. This precludes the direct connection of this biasing resistor to a low impedance node at the same AC *and* DC potential as the input, as is the case in Figure 2-6b. Instead, bootstrapping must be applied only at (low) AC frequencies. The circuit of Figure 2-8 achieves this by providing the bootstrapping potential through a capacitor. The DC resistance is set by the series combination of R_{IN} and R_{BS}. The AC impedance can be found from equation 2.17 with A_{BS} chosen to reflect the transfer function of the circuit which includes the high-pass filter formed by R_{BS} and C_{BS}.

Figure 2-9 illustrates the response of this circuit using some typical values. The following expression is used for A_{BS}, using the notation given in Figure 2-8,

$$A_{BS}(s) = A_v(s) k_{BS} \frac{R_{BS} C_{BS} s}{1 + R_{BS} C_{BS} s} \qquad 2.18$$

where k_{BS} is a constant chosen to set the overall level of feedback, and $A_v(s)$ is set to 1. It is important to note from Figure 2-9 that R_{IN} is not properly bootstrapped until a frequency significantly above the corner frequency set by R_{BS} and C_{BS}, which is 1.5 mHz in this example, due to the phase shift of this network. Above this frequency R_{IN} is bootstrapped to 10 times its original value.

2.5.2 Non-ideal voltage followers and guarding

Equation 2.9 defines an effective guard capacitance, $C_{G,eff}$, and is repeated here

$$C_{G,eff} = (1 - A_G)C_G \qquad 2.9$$

The input-guard gain, A_G, will produce perfect guarding when its value is precisely one. This naturally begs the question, how closely might an A_G of 1 be achieved in a practical circuit? The first point which has already been noted is that a value of A_G greater than unity is likely to result in oscillation unless there is additional shunt capacitance on the input. Though it is often desirable to use A_G greater than 1 to achieve neutralization of this additional shunt capacitance, there are many situations where it is preferred to achieve perfect guarding in order to guarantee stability when this shunt capacitance might be expected to change. Fortunately, a simple op-amp voltage follower can guarantee gain close to, though always less than, unity. In order to determine just how close to unity, the transfer function of the voltage follower given in Figure 2-10 will be briefly considered. For any op-amp, v_o is defined as

$$v_o = A_{OL}(V_+ - V_-) \qquad 2.19$$

Where A_{OL} is the open-loop gain of the device used. For the standard voltage follower circuit the following can be defined,

$$v_- = v_o\,, v_+ = v_s \qquad 2.20$$

Equation 2.19 is solved to find the transfer function

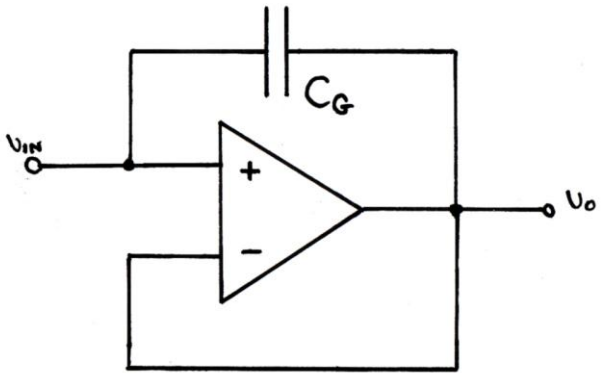


Figure 2-10: An op-amp voltage follower with guard capacitance C_G.

$$\frac{v_0}{v_{IN}} = \frac{A_{OL}}{1 + A_{OL}} \qquad 2.21$$

Equation 2.21 tells us that the voltage follower circuit has a gain which is inversely proportional to the open-loop gain of the op-amp used. When this voltage follower is used to drive the guard capacitance, this small gain error will produce a residual effective capacitance, that is to say the effective guard capacitance will not be reduced to zero. By substituting equation 2.21 into Equation 2.9, it is possible to find an expression for the effective capacitance of a guard capacitance driven by an op-amp voltage follower as in Figure 2-10.

$$C_{G,eff} = C_G \left(\frac{1}{1 + A_{OL}} \right) \qquad 2.22$$

Equation 2.22 can be used to examine a typical case. A_{OL} for common op-amps is commonly quoted to lie in the range 10^4 to 10^6, so for the purposes of illustration a value of 10^4 is chosen and applied to a guard capacitance of $C_G = 10\ pF$. From equation 2.22 a value of $C_{G,eff}$ of approximately 1 fF is found. This will be quite acceptable for most capacitive sensing applications, and will generally be significantly less than the input capacitance which remains as a result of parasitics which cannot be guarded. It should be concluded that equation 2.22 tells us that it is not possible to turn a very poor amplifier into one which is suited to capacitive sensing, though good amplifiers can be turned into *very* good capacitive sensors. Voltage followers nonetheless remain attractive as candidates for the input stage of an EPS since they eliminate the need for the careful trimming of feedback resistor values required in non-inverting and inverting amplifier circuits. The voltage follower will provide near-ideal guarding (and bootstrapping) signals without the risk of instability when gain is not carefully trimmed. This advantage of course comes at the cost of low input stage gain, which may be undesirable.

A second order effect can be added to equation 2.22 which addresses the frequency dependence of A_{OL}. For common op-amps A_{OL} decreases rapidly from a very low

frequency, typically around 10 Hz. The gain error at high frequencies is therefore increased with a subsequent increase in the guarded input capacitance.

2.5.3 Bandwidth limiting in guarded amplifiers

In Figure 2-8 the guard capacitance C_G is buffered by an amplifier having a frequency dependent transfer function defined by $A_v(s)$. By considering the transfer function of this circuit the bandwidth limiting effects of guarding can be evaluated. Following the same derivation as in section 2.5.2, an expression for the frequency dependent closed-loop gain of the non-inverting amplifier circuit can be found by considering the dominant pole in the open loop gain response of the amplifier (Surtihadi and Oljaca, 2010). Whilst this approach is the most accurate, for the purposes of this discussion it is sufficient to simply describe the amplifier as having a closed loop gain with a single pole at the angular frequency defined as ω_{GBW}/k_A, where ω_{GBW} is the gain-bandwidth product of the amplifier and k_A is the closed loop gain, as set by the ratio $1 + R2/R1$ in Figure 2-7. The transfer function for the amplifier in Figure 2-8 is therefore

$$A_v(s) = \frac{k_A}{1 + \frac{k_A s}{\omega_{GBW}}} \tag{2.23}$$

This function will now be used to find the complete transfer function of the circuit in Figure 2-8. Since this analysis is concerned with revealing only the upper frequency roll-off, the bootstrapping of R_{IN} may be neglected. k_{BS} is therefore set to zero, with the additional assumption that $R_{BS} \ll R_{IN}$ applied so that only R_{IN} contributes to the resistive part of the amplifier input impedance. Considering the currents at the input node of the circuit in Figure 2-8, and collecting terms gives equation 2.24

$$v_{IN}(G_{IN} + sC_{SHUNT}) + (v_{IN} - v_s)sC_c + (v_{IN} - v_G)sC_G = 0$$

$$v_{IN}(G_{IN} + sC_{SHUNT} + sC_c + sC_G) = v_s sC_c + v_G sC_G \tag{2.24}$$

the following have been defined,

$$v_G = k_G v_o \tag{2.25}$$

$$v_o = A_v(s)v_{IN} \tag{2.26}$$

which can be substituted into equation 2.24, before solving for v_o/v_s,

$$\frac{v_0}{v_s} = \frac{sC_c}{\frac{G_{IN} + sC_{SHUNT} + sC_c + sC_G}{A_v(s)} - k_G sC_G} \tag{2.27}$$

Finally equation 2.23 is substituted into 2.27 and the terms collected to give the complete transfer function

$$\frac{v_o}{v_s} = \frac{sC_c}{s^2\left(\frac{C_{SHUNT} + C_c + C_G}{\omega_{GBW}}\right) + s\left(\frac{G_{IN}}{\omega_{GBW}} + \frac{C_{SHUNT} + C_c + C_G}{k_A} - k_G C_G\right) + \frac{G_{IN}}{k_A}} \tag{2.28}$$

The numerator polynomial reveals that the transfer function has a single zero, corresponding to the single pole high-pass response, with the two denominator roots corresponding to two high and low frequency poles. The pole which determines the high frequency roll-off, from equation 2.28, is given below

$$s = -p = -\omega_{GBW}\left(\frac{k_G C_G}{C_{SHUNT} + C_c + C_G} - \frac{1}{k_A}\right) \tag{2.29}$$

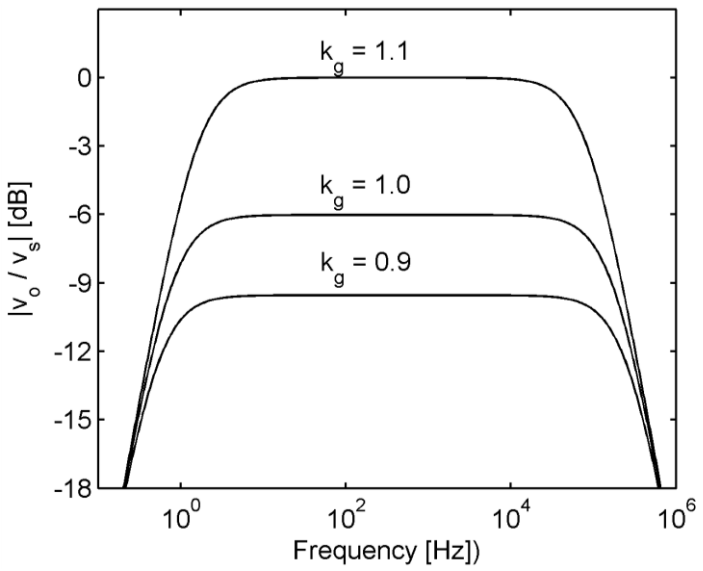


Figure 2-11: Magnitude response of equation 2.28 for several levels of guarding, with $C_C = 1\,pF$, $C_{SHUNT} = 1pF$, $C_G = 10\,pF$ and $R_{IN} = 100\,G\Omega$. k_A is set to 1 and $\omega_{GBW} = 2\pi \times 1 \times 10^6$ ($= 1$ MHz) . k_G is varied across a range which reflects partial and then full guarding of C_G, and finally neutralization of C_{SHUNT}.

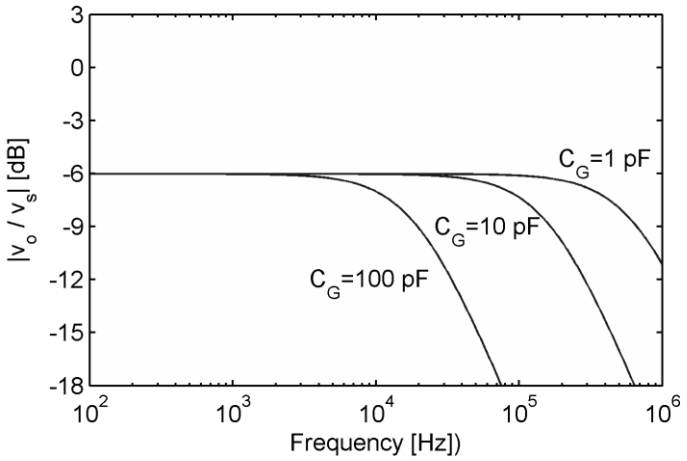


Figure 2-12: Magnitude response of equation 2.28 for several levels of guard capacitance, C_G. k_G = 1 and all other values are identical to those given in Figure 2-11.

The upper corner frequency, determined by equation 2.29, is proportional to the gain-bandwidth product of the op-amp employed, as expected, and so the first step in designing a high-bandwidth EP sensor will be the selection of an op-amp having a large gain-bandwidth product. However, the bandwidth is also strongly dependent on the level of guarding used, and the ratio of the guard capacitance to the sum of all input capacitances. Since the band-limited output of the op-amp is the positive feedback signal for the guarding of C_G, then it can only be effectively guarded within this limited band. The bandwidth of the guarded sensor is therefore usually somewhat less than might be expected from the gain-bandwidth of the op-amp alone. The extent to which this effect is encountered will depend on the level of guarding and/or neutralization which is employed, as illustrated in Figure 2-11, and also the value of C_G, the total capacitance which is guarded, as illustrated in Figure 2-12. The use of large amplifier gains will further limit the overall bandwidth of the sensor. In general, large sensor bandwidth is achieved by ensuring that C_G is minimized, in addition to the use of high speed amplifiers in a low-gain configuration.

This band-limiting effect was noted when performing a remote ECG experiment (see section 5.2) with large (7 cm diameter) electrode structures. Initially, this large electrode was used with a back-side guard electrode. This large parallel plate produces a significant guard capacitance of approximately 120 pF, and a subsequently limited bandwidth of only several kHz. A reduced-capacitance electrode structure having a

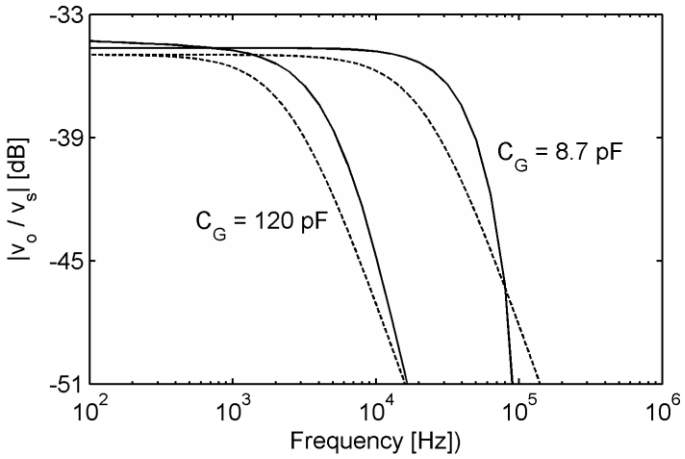


Figure 2-13: Measured magnitude response of an EPS sensor with two different electrode structures having significantly different values of C_G. Solid lines represent measured data, and dashed lines are calculated from equation 2.28 with the given values of C_G and all other values determined by direct measurement.

more moderate 8.7 pF of guard capacitance results in an order of magnitude increase in bandwidth, as shown in Figure 2-13. The bandwidth of the sensor is well predicted by the model represented by equation 2.28, as demonstrated in the figure. C_G has been determined for each electrode by direct measurement using a capacitance meter, and all other model parameters have been determined by direct measurement of the sensor (see section 3). Two amplification stages, each with a gain-bandwidth of 1 MHz, are responsible for the second order roll-off in the measured data, whilst the model only accounts for a single-pole response.

A second bandwidth-limiting effect is encountered in common EPS circuit designs which is equally deserving of attention. This discussion has so far considered a voltage-follower amplifier which directly drives the guard capacitance from its low impedance output. Returning to the circuit of Figure 2-7a it is seen that in a non-inverting amplifier configuration (i.e., with voltage gain) the guard drive signal is an attenuated version of the output signal. This guard drive signal is derived from a resistive voltage divider, and so has an output impedance given by the parallel combination of R_{G1} and R_{G2}. The guard plane has a capacitance to the input node of the circuit, discussed previously and denoted C_G, and it also has a shunt capacitance to ground, which will be denoted $C_{G,SHUNT}$. These capacitances load the output of the voltage divider, and so have the

effect of introducing an additional pole in the response of the guard circuit. This may result in a further reduction in sensor output bandwidth. For common EPS circuits assembled on a printed circuit board and with a ground plane surrounding the input guard area, $C_{G,SHUNT}$ may have a value from tens to hundreds of pico-Farads. With a $100\ k\Omega$ potentiometer used as the guard circuit attenuator a low pass corner in the kHz range is formed. Since this low-pass filter is inside the guard feedback loop it may have a drastic effect on the output response of the sensor. In the general case then, $C_{G,SHUNT}$ should be minimized by careful board layout techniques, and where wide sensor bandwidth is desired the guard should be driven by the output of a low impedance buffer. The effect on the output response of the sensor can be found by replacing k_G of equation 2.28 with the transfer function of the voltage divider with a capacitive load. This frequency dependent $k_G(s)$ is given below

$$k_G(s) = \frac{1}{1 + \frac{R_{G2}}{R_{G1}} + sR_{G2}C_{G,SHUNT}} \qquad 2.30$$

substituting this function into the expression for the low pass pole given in equation 2.29 to find the new, lower, pole.

2.6 Noise

An understanding of the noise sources present in the EPS circuit is best served by beginning with a treatment of the noise sources present in the basic EPS input stage, utilising the model of an idealised noiseless op-amp having equivalent input current and voltage noise sources. Only after this can the additional complications of the positive feedback techniques be considered. Furthermore, a discussion of the parameters which determine the noise performance of an EPS circuit is meaningless without discussing how those same parameters might affect the signal sensitivity (and therefore signal-to-noise ratio), and so this section is concluded with such a discussion. In section 3.5.2

experimental data for an EPS circuit will be given and compared with the theoretical model developed here. In chapter 4 the idealised op-amp of the present treatment will be replaced with an input transistor so that the underlying noise sources which contribute to the equivalent input current and voltage noise can be considered.

Before beginning, a few definitions should be given. This text does not break from convention, but it is sensible nonetheless to define the units and symbols which will be used. A noise voltage is given the symbol e and has units of Volts rms. This noise voltage may be represented by a Power Spectral Density (PSD) (Connor, 1973), which has units of V^2/Hz and represents the noise power delivered in a 1 Hz bandwidth. Similarly, a Voltage Spectral Density (VSD) may be defined, which is found simply by taking the square root of the PSD and hence has units of $V/\sqrt{Hz}$. Finally, a noise current, i, in units of Amps, can be described in terms of a spectral density having units $A/\sqrt{Hz}$

2.6.1 Noise in the EPS input circuit

The EPS equivalent input stage of Figure 2-2 has been redrawn in Figure 2-14 with the noise sources included. The ideal (noiseless) op-amp has an equivalent input voltage noise source, e_n, in series with its non-inverting input, and a corresponding equivalent input current noise source, i_n, connected between the input and ground (Mancini, 2002). These external noise sources are *equivalent* to the total noise contributions internal to the op-amp. Most op-amp manufacturers' data sheets give values for these two sources

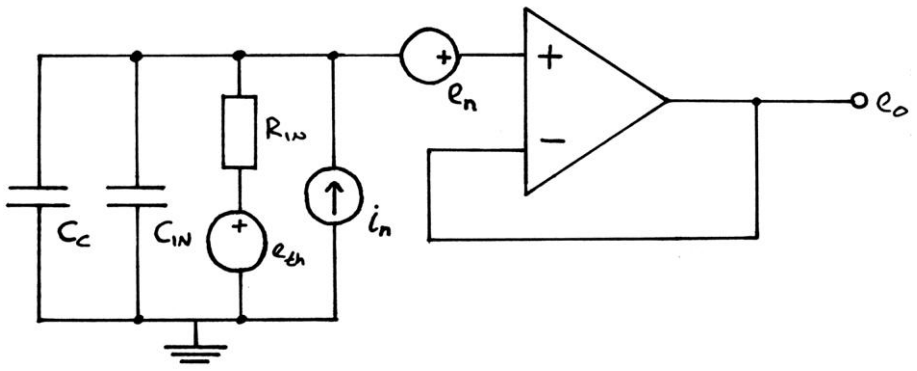


Figure 2-14: EPS input stage equivalent circuit with noise sources included.

and define them in an identical manner (Jung, 2002). Since the input current noise generates an output voltage proportional to the impedance through which it flows, then it is evident that its value is of the utmost important in high impedance amplifiers. For JFET input devices, the current noise is simply the shot noise of the input bias current, and so the spectral density of this noise current can be found from the relation

$$i_n = \sqrt{2q_e I_B}$$

where I_B is the input bias current and q_e is the charge on an electron. The relation is only true when the majority of the input bias current is due to the input transistor of the amplifier only (and only for JFET devices), and not when the amplifier employs input current cancellation circuitry or other resistive leakage paths dominate. The designer should therefore rely on datasheet values for current noise when available.

The third noise source in this circuit is e_{th}, and is due to the thermal noise of the input resistance R_{IN}. The spectral density of this thermal voltage noise can be calculated using Nyquist's relation

$$e_{th} = \sqrt{4k_B T R_{IN}}$$

where k_B is Boltzmann's constant ($k_b = 1.38 \times 10^{-23}\ m^2\ kg\ s^{-1}\ K^{-1}$) and T is the absolute temperature in Kelvin. This thermal noise can equivalently be represented by a current noise generator, i_{th}, which is placed in parallel with R_{IN}, in which case the spectral density of the thermal current noise is given (by Norton's theorem) as

$$i_{th} = \sqrt{\frac{4k_B T}{R_{IN}}}$$

either interpretation, of the input resistor as a voltage or a current noise generator, is therefore correct. Note that the capacitors in the circuit are not themselves noise generators, since Nyquist's relation is dependent only on the real part of impedance.

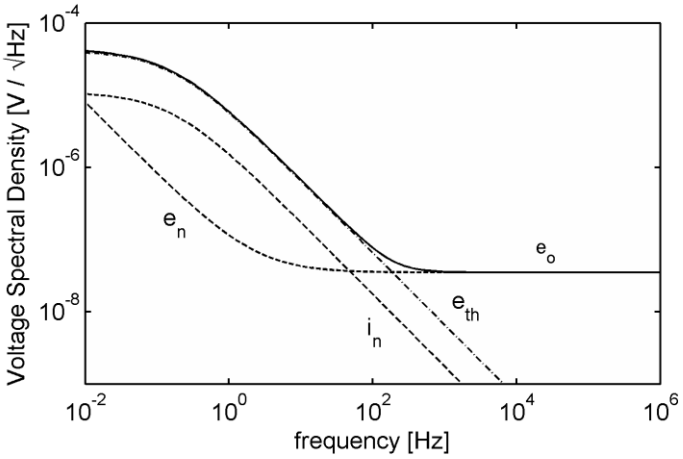


Figure 2-15: Individual contributions (dashed lines) of the amplifier voltage noise e_n, amplifier current noise i_n, and resister thermal noise e_{th} to the total EPS output noise e_o (solid line) for a weakly coupled, typical low noise, high input impedance op-amp at $T = 310\ K$ calculated from equation 2.32.

The thermal noise generator e_{th} produces an output noise voltage over the series circuit of R_{IN} and the two parallel capacitances C_{IN} and C_C, and so produces a contribution to the total output noise voltage spectral density, e_o, that is denoted $e_{o,th}$

$$e_{o,th} = e_{th}\frac{1}{1 + \omega R_{IN}(C_C + C_{IN})}$$

The op-amp current noise source flows over the parallel combination of R_{IN} and the two capacitances and so produces a noise contribution $e_{o,i}$

$$e_{o,i} = i_n\frac{R_{IN}}{1 + (\omega R_{IN}(C_C + C_{IN}))}$$

The total output noise is the root sum of the squares of the three noise sources,

$$e_o = \sqrt{e_{th}^2\frac{1}{1 + \left(\omega R_{IN}(C_C + C_{IN})\right)^2} + i_n^2\frac{R_{IN}^2}{1 + \left(\omega R_{IN}(C_C + C_{IN})\right)^2} + e_n^2} \qquad 2.31$$

The thermal and current noise terms are effectively low-pass filtered by the total capacitance on the input node, the parallel combination of C_C and C_{IN}. It is useful to define a noise corner frequency (Spinelli and Haberman, 2010) [†], ω_N,

[†] Spinelli neglects C_{IN} since his analysis is limited to what is here termed a strongly coupled measurement, implying the assumption $C_{IN} \ll C_C$. This is not the case in weakly coupled EPS sensing.

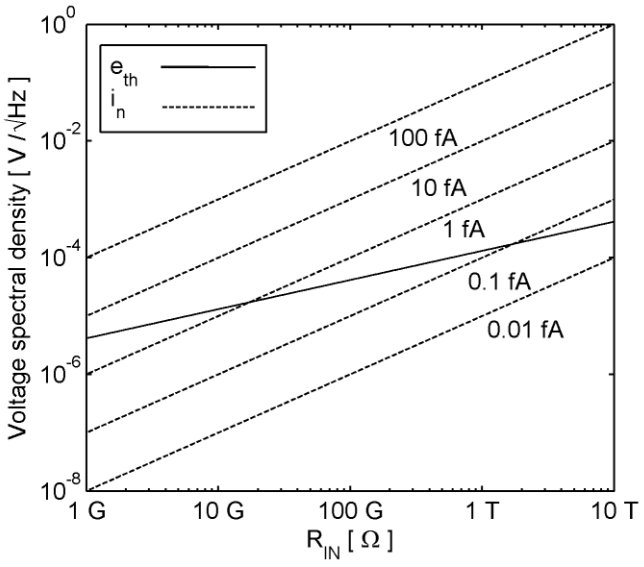


Figure 2-16: Contributions of the resistor thermal noise e_{th} (at $T = 310\ K$) and amplifier current noise for several values of i_n at a frequency $\omega \ll \omega_N$. Above ω_N each noise component is attenuated by a factor $1/(1 + \omega/\omega_N)$.

$$\omega_N = \frac{1}{R_{IN}(C_C + C_{IN})}$$

so that equation 2.31 becomes

$$e_o = \sqrt{e_{th}^2 \frac{1}{1 + (\omega/\omega_N)^2} + i_n^2 \frac{R_{IN}^2}{1 + (\omega/\omega_N)^2} + e_n^2} \qquad 2.32$$

Note that this noise corner frequency is in fact identical to the earlier given signal corner frequency. The thermal and current noise terms are dominant only at low frequencies (Figure 2-15), above which the voltage noise term dominates. Nonetheless, at low frequencies the thermal and current noise terms can be very large (in excess of $1\ \mu V/\sqrt{Hz}$), even with amplifier current noise values as low as $0.1\ fA/\sqrt{Hz}$. This large noise term tends to swamp the effects of the $1/f$ voltage noise of the amplifier.

For amplifiers with low current noise (around $0.1\ fA/\sqrt{Hz}$) then the thermal noise due to R_{IN} will usually be dominant. Only for very large values of R_{IN} (generally, greater than $1\ T\Omega$), will the current noise term dominate, as shown in Figure 2-16.

Since the spectral density of the thermal noise term is proportional to $\sqrt{R_{IN}}$, and the noise-corner frequency is inversely proportional to R_{IN}, then the generally unexpected

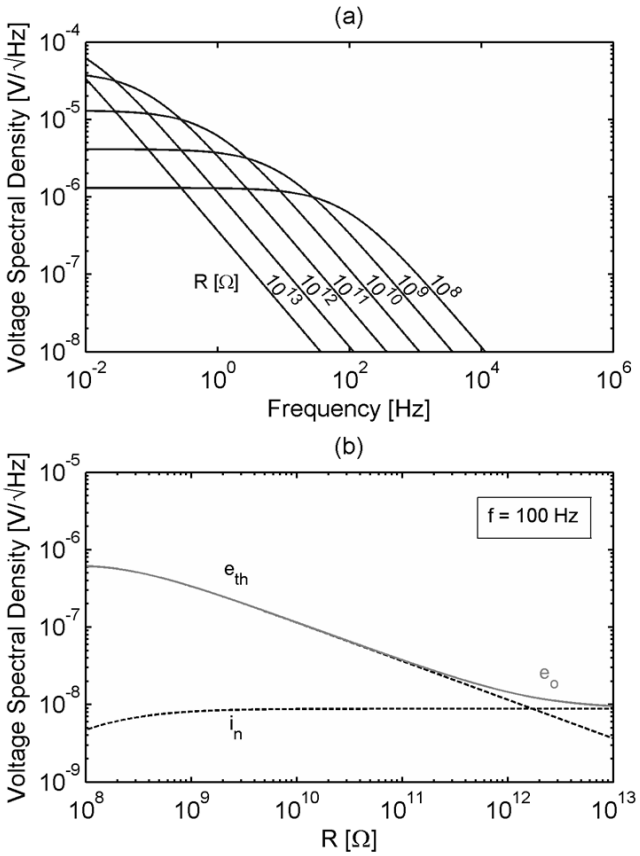


Figure 2-17: Contribution of resister thermal noise e_{th} for several values of R_{IN} on a weakly coupled typical low noise, high input impedance op-amp calculated from equation 2.32. In (a) e_{th} is plotted for several values of R_{IN}. In (b) e_{th} is plotted at a single frequency (100 Hz) in addition to the current noise contribution i_n.

result is a reduction in noise with increasing values of R_{IN}. This is true only when the signal frequency is significantly above the noise corner frequency and the current noise term is not dominant. This result has been reported previously, based on experimental data (Prance et al., 2000). As can be seen in Figure 2-17a, though a larger valued R_{IN} will of course produce an increased thermal noise term at a signal frequency ω much less than the noise corner frequency ω_N, the effect of the reducing noise corner frequency with R_{IN} is a crossing-over of the plots for the voltage noise of each value of R_{IN}.

Figure 2-17b shows how this relationship results in a reduced noise spectral density for increasing R_{IN} at a signal frequency greater than the noise corner frequency. The

relationship holds until the current noise term begins to dominate with very high valued R_{IN}.

This discussion has so far only considered noise at room temperature. As a final remark, it is worth considering the effects of decreasing temperature. In general it is not convenient in most EPS applications to operate the amplifier at reduced temperature; however, for certain laboratory applications a significant improvement in noise performance may be obtained by cooling the amplifier. Since the thermal noise term is proportional to T, some benefit is gained here. Far more significant though is the decrease in input bias current of the amplifier, which is exponentially related to temperature. The associated current noise term is thus reduced significantly, an effect which can be capitalised upon by using an input resistance in excess of $10\,T\Omega$ (see Chapter **Error! Reference source not found.**). The reduced bias current allows a large valued R_{IN}, which in turn minimizes the thermal noise term as the noise corner frequency is reduced.

2.6.2 Noise with positive feedback

When positive feedback is added, as discussed in section 2.4, in essence we are disconnecting some of the parasitic components of the EPS input circuit from ground, and instead connecting them to the output of the amplifier. In terms of the noise performance, this is entirely undesirable since the current noise and thermal noise

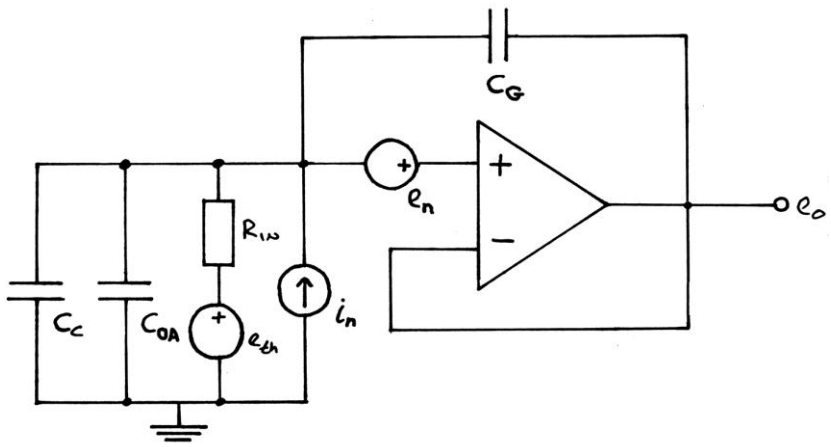


Figure 2-18: A guarded EPS input stage equivalent circuit with noise sources included.

generators are no longer shunted to ground by these (often significant) parasitic impedances. Since its effects are encountered across the entire sensor bandwidth, this discussion will begin by analysing the effects of guarding on the sensor noise.

In Figure 2-18 the noise equivalent circuit for a guarded EPS circuit is shown. Compare this circuit with that of Figure 2-14. The total input capacitance of the sensor, C_{IN}, has been split into two parts; the part which has been guarded and is now denoted C_G, and that which is not, which remains as a shunt to ground and is denoted C_{OA}, since in most cases this unguarded portion is the common-mode input capacitance of the op-amp. If the amplifiers of these two figures are identical apart from the addition of guarding, then the sum of C_G and C_{OA} must be equal to the unguarded C_{IN} of Figure 2-14. The input capacitance used to determine the signal sensitivity is $C_{OA} + C_{G,eff}$, where $C_{G,eff}$ is the effective guarded capacitance as described earlier. For the amplifier in Figure 2-18, C_G is connected directly to the voltage follower output and so $C_{G,eff}$ is equal to zero for an ideal op-amp.

Two significant modifications are required to the earlier noise calculation. First, the capacitance over which the op-amp current noise, i_n, and the resistor thermal noise, e_{th}, are shunted to ground has been reduced from C_{IN} to only a fraction of it, equal to $C_{OA} + C_{G,eff}$. The guard capacitance C_G is no longer shunting the noise signal to ground, though if it is not perfectly guarded then it will act as though it were a shunt to ground with value $C_{G,eff}$. Consequentially the noise corner frequency is increased. R_{IN}

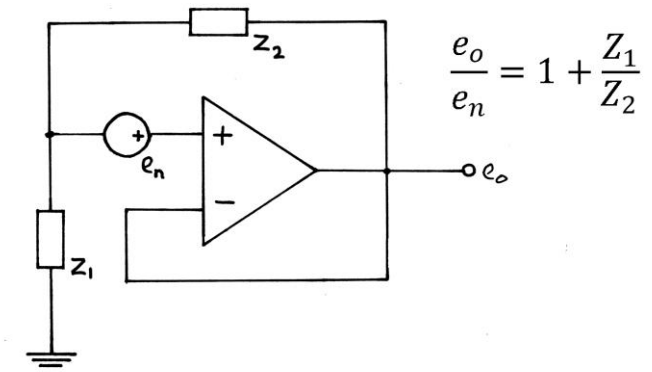


Figure 2-19: Gain applied to the voltage noise of the input op-amp by the guard capacitance C_G.

will be retained as a shunt to ground until the case of bootstrapping is addressed later. Secondly, and of more significance at higher frequencies, the noise gain of the op-amp voltage noise generator is increased. An equivalent circuit is given in Figure 2-19 which demonstrates the noise gain applied to the voltage source e_n due to the feedback capacitance C_G and the input impedance. The result of this analysis will be compared with experimental data in section 3.5.2.

The increase in the noise corner frequency is identical for the guarded amplifier as for an amplifier with no guarding which has an input capacitance equal to the effective input capacitance of the guarded amplifier. However, the amplification of voltage noise can be considered as an excess noise for the guarded amplifier.

The noise gain of the op-amp voltage noise, from Figure 2-19, is given by the following equation,

$$\frac{e_o}{e_n} = 1 + \frac{sC_G}{s(C_{OA} + C_C) + \frac{1}{R_{IN}}} \qquad 2.33$$

Note that the guard capacitance appears as C_G and not its effective value $C_{G,eff}$. Since the voltage noise will usually be swamped by the other noise terms at low frequencies, R_{IN} can be neglected[†],

$$\frac{e_o}{e_n} = 1 + \frac{C_G}{C_{OA} + C_C} \qquad 2.34$$

The thermal and current noise terms are modified to give the following;

$$e_{o,th} = e_{th}\frac{1}{1 + \omega R_{IN}(C_C + C_{OA} + C_{G,eff})}$$

[†]Since this noise voltage gain rolls-off at low frequencies due to R_{IN}, then the 1/f voltage noise contribution of the amplifier tends to remain smaller than the current and thermal noise terms, in spite of this voltage noise gain.

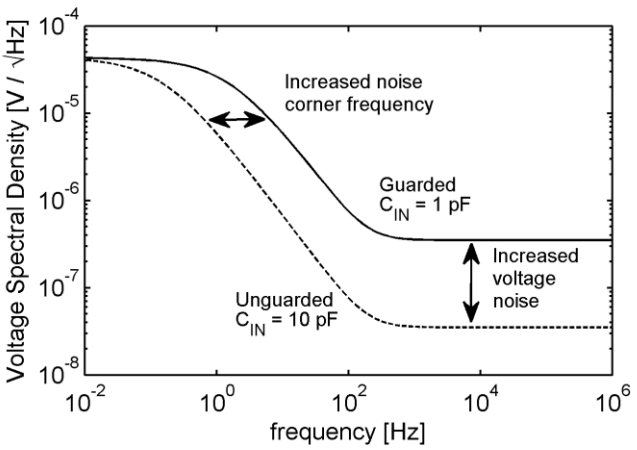


Figure 2-20: Total EPS output noise e_o for a weakly coupled, typical low noise, high input impedance op-amp at $T = 310\ K$ calculated from equation 2.32 (dashed line), and from equation 2.36 (solid line) for the same amplifier with 9 pF of the total input capacitance ideally guarded.

$$e_{o,i} = i_n \frac{R_{IN}}{1 + \left(\omega R_{IN}\left(C_C + C_{OA} + C_{G,eff}\right)\right)}$$

The noise corner frequency will be redefined as,

$$\omega_N = \frac{1}{R_{IN}\left(C_C + C_{OA} + C_{G,eff}\right)} \qquad 2.35$$

so that the total output noise, e_o, can be written as,

$$e_o = \sqrt{e_{th}^2 \frac{1}{1 + \left(\frac{\omega}{\omega_N}\right)^2} + i_n^2 \frac{R_{IN}^2}{1 + \left(\frac{\omega}{\omega_N}\right)^2} + e_n^2 \left(1 + \frac{C_G}{C_{OA} + C_C}\right)^2} \qquad 2.36$$

In Figure 2-20 the output noise for the typical amplifier used in Figure 2-15 has been repeated, along with the output noise for the same amplifier with a significant portion of the input capacitance guarded. Note the increased noise corner frequency and the effect of the voltage noise gain at higher frequencies.

At low frequencies then, the effect of the increased noise corner frequency may result in a significant increase in the thermal and current noise terms at signal frequencies. The increased gain of the voltage noise term is apparent at higher frequencies.

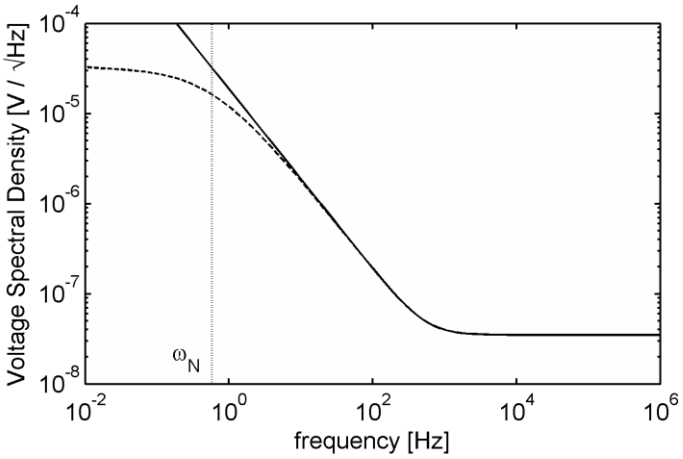


Figure 2-21: Total EPS output noise for a bootstrapped (solid line) and non-bootstrapped (dashed line) input resistance.

When $C_{G,eff}$ has a negative value so that C_{OA} is neutralized, then the same expression of equation 2.35 may be used to calculate the noise corner frequency. Since neutralization implies an overall gain of greater than unity for the amplifier, then the voltage follower circuit of Figure 2-18 must clearly be modified. As such, an expression for the voltage-noise gain must be derived for whatever amplifier is used, though it will undoubtedly retain the form of 2.36.

Bootstrapping of the input resistor causes the thermal noise generator associated with R_{IN} to be amplified. Fortunately, the relation between this noise gain and the input capacitance of the amplifier causes the thermal noise contribution at frequencies above ω_N to have exactly the same amplitude as in the non bootstrapped case, though the noise level continues to increase below the noise corner frequency, as shown in Figure 2-21. The modification to the voltage and current noise terms as a result of bootstrapping are usually negligible and are therefore not treated here. The modified thermal noise term can be approximated for frequencies above the bootstrap circuit corner frequency (set by R_{BS} and C_{BS} in Figure 2-8) as;

$$e_{o,th} \approx e_{th} \frac{1}{\omega R_{IN}(C_C + C_{IN})}$$

note that R_{IN} is used and not $R_{IN,eff}$. Bootstrapping of the input resistor does not therefore produce the reduction in noise corner frequency that is achieved by increasing the intrinsic value of R_{IN}, and so the output noise at frequencies above the noise corner

frequency remains unchanged. As such, a bootstrapped R_{IN} can be considered to have an excess noise as compared to a non-bootstrapped R_{IN}.

2.6.3 SNR: The relationship between noise and input impedance

Since the signal gain of a capacitively coupled EP sensor is directly related to the input impedance of the sensor, then determining the signal to noise ratio is really a matter of determining the ratio of input impedance to noise. The implications of positive feedback techniques on the noise of the sensor have already been discussed, as have the modification to the sensor input impedance that results from these techniques. It only remains to relate the two.

Amplifier voltage gain will usually contribute little to the signal-to-noise ratio of the sensor, since it usually quite straightforward to ensure that subsequent amplification and signal conditioning stages have lower noise than the front end of the sensor. Instead then, the sensor gain is usually considered as the signal gain at the input, which is determined exclusively by the signal coupling capacitance and the input impedance. This is the interpretation of signal gain used already in this text. As such, the sensor noise is always referred to the input. For this reason unity gain amplifiers have been used throughout the given noise analysis, so that the equations developed can be easily applied to any sensor by referring the output noise back to the input.

Positive feedback in the form of guarding and neutralization of the input capacitance has been shown to deliver the same noise performance as an unguarded sensor having the same input capacitance. This is true across much of the low frequency operating band for common sensor applications, though at higher frequencies the guarded sensor suffers from amplification of the voltage noise. This amplification factor is proportional to the guard capacitance divided by the total input capacitance (equation 2.34). This is yet another motivation for the designer to minimize the guard capacitance since, in addition to the bandwidth limiting effects, a low guard capacitance will reduce the amplification of voltage noise. The decrease in input capacitance and subsequent

increase in signal gain furnished by guarding and neutralization result in an exactly proportional increase in noise (below the voltage noise region) so that the signal-to-noise ratio is unchanged.

Bootstrapping affects only the low frequency response of the sensor. Both the signal and noise response are extended to a lower frequency than the non-bootstrapped response. Signal to noise ratio is therefore not improved nor degraded, though a tailoring of the low-end frequency response is achieved. This is in contrast to the case where the input resistor is replaced with a higher valued part. An increase in the intrinsic value of the input resistor can deliver significant improvement to the low-frequency noise response.

For low frequency sensors (near DC to 1 kHz) the dominant noise components are the thermal and current noise terms. The capacitance parameters are therefore of little concern in terms of signal-to-noise, and can be set to whatever value, using guarding and neutralization if desired, that is required to give a signal corner frequency below the lowest signal frequency of interest, but not so low that the sensor voltage noise will become dominant.

The thermal and current noise terms are both dependent on the value of R_{IN}. Recall that the contribution of these two terms is dependent on the noise corner frequency, and hence both are reduced with increasing R_{IN}. An upper limit is set on R_{IN} by the input bias current required by the amplifier. This bias current is inextricably linked to the current noise, and hence the input bias current is the chief qualifier in determining the 'best-case' noise performance with a given amplifier. This best case is achieved when the highest possible value of R_{IN} is used.

There are several factors which may limit the ability to achieve this best case performance. The first is the difficulty in obtaining or producing a resistor of the desired value, which may be in excess of 1 $T\Omega$ (see chapter **Error! Reference source not found.**). Another is that it is generally undesirable to reduce the corner frequency significantly below the lowest frequency of interest. Though this would offer the best noise performance, the benefits of signal selectivity at the sensor front end are lost. This

is particularly the case in electrophysiology measurements, where a low corner frequency would result in increased sensitivity to movement artefacts which may saturate the sensor input and hence defy filtering.

As has been seen, high impedance techniques, including positive feedback, seem to offer little in terms of signal to noise improvement over a lower impedance amplifier furnished with higher gain. So why should high impedance amplifiers be used at all? First, the impedance of the sensor should ensure that the limit set by the input voltage noise term is not met. Furthermore, high input impedance offers several important benefits in measurement applications. By setting the input impedance greater than the source impedance (usually the coupling capacitance in the case of a voltage source), then small variations in the source impedance do not affect the output of the sensor. Further, if the source potential is not a true voltage source (as in charge measurements) or it is an electric field then further benefits are encountered by reducing the source loading (Aydin et al., 2010).

3 METHODS AND TOOLS FOR SENSOR CHARACTERISATION

When producing high impedance circuits for Electric Potential Sensors (EPS) it is necessary to have a strictly defined set of performance metrics that can be obtained in a reproducible and convenient manner. A set of methodologies and tools are required that provide a controlled approximation to real world measurement situations. The key variable affecting performance in measurement of the EPS is the nature of the coupling between the sensor and the source. It is therefore necessary for the measurement toolset to include a method of reliable sensor-source coupling that electrically mimics the real world measurement for which the specific sensor is intended. The electrical performance metrics which must be obtained are sensor input impedance and noise. Knowledge of the input impedance of the sensor makes it possible to produce reliable predictions of how the sensor will perform in real world measurements. Of equal

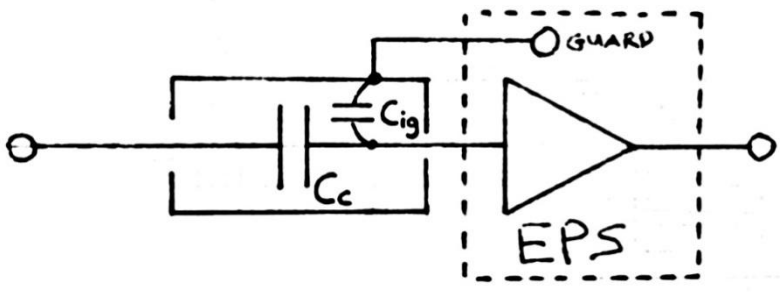


Figure 3-1:Schematic of the test capacitor circuit when connected to an EPS. C_c represents the capacitance from source to EPS input, and C_{ig} is the input-guard capacitance.

importance is the measurement of noise, since an improvement or detriment in either of these two metrics translates directly to real world performance.

The methods and tools used will be described here, and followed by a complete set of characteristic measurements obtained for a fairly typical EP sensor. This data will allow the experimental verification of some of the theory developed in the previous section.

3.1 Coupling capacitor design & construction

For characterization purposes the sensor should be capacitively coupled to a test source. The magnitude of the coupling capacitance should be matched to that expected in the real world measurement. For most EPS applications, this means the test capacitance should be very small – often in the range of several femto-Farads. In remote sensing applications an EPS sensor may be coupled to a large source of potential via a large sensing electrode over a distance of several centimetres or metres. Reproducing such a situation for characterisation proves unwieldy in a lab environment, and makes it difficult to prevent external electrical activity from affecting the measurement. Instead a small capacitance structure on the scale of several millimetres is produced so that it can be fitted into a small metal enclosure and effectively screened from external influence. The capacitance of this structure can be made equivalent to that of the large-scale remote sensing scenario by scaling the capacitor in all dimensions. This capacitor can be fitted to the input of the EPS in place of the usual electrode structure. The use of a conducting shield around the capacitor represents a significant departure from the conventional remote measurement scenario. In order to reduce the capacitive loading of this screen on the input of the EPS, it must be connected to the active guard circuit of the EPS, rather than merely grounded, as shown in Figure 3-1.

In solving one problem, another is introduced; the capacitance between the input and guard nodes of the EPS circuit, C_{ig}, may be different than the input-guard capacitance of the original sense electrode. This could alter the extent to which the guard circuit

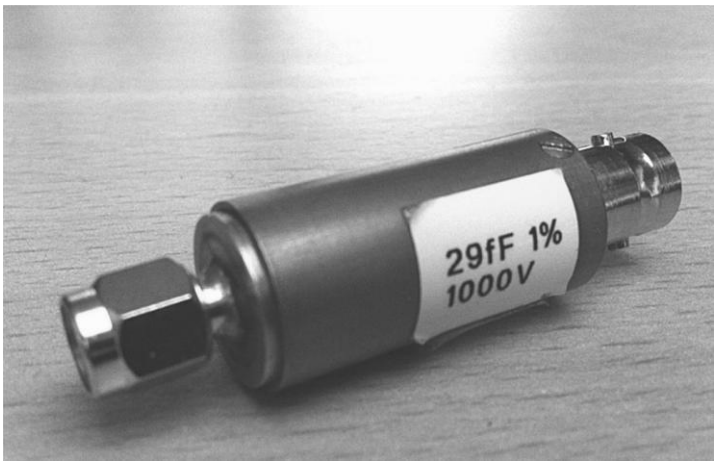


Figure 3-2: Photograph of test capacitor external structure.

neutralizes the input capacitance of the sensor. This may have the additional effect of altering the bandwidth of the sensor, as discussed in chapter 2. The variation in C_G may have further undesirable effects, and so must be considered by the experimenter when comparing performance expected from characterization data to real world measurements. In any case, a guarded, compact test capacitor provides so many benefits in terms of shielding, stability and convenience that add up to reproducibility of characteristic measurements that its shortcomings are quite acceptable.

The specifications of a coupling capacitor are therefore as follows; it should be mechanically robust and provide convenient signal connections for frequent use without risk of degradation of the fragile capacitor, it should be effectively guarded and it should be available in a range of capacitance values from the smallest values encountered in remote sensing, to larger values found in contact sensing. These specifications have been met by producing small capacitance structures on high quality PTFE substrates which are encased in a solid copper and brass case and terminated with a male SMA connector at the EPS connecting end, and a female BNC at the other end for injection of signals from a function generator or other source, as shown in Figure 3-2. The BNC connector is an insulated panel mount type so that the centre conductor provides signal connection from an appropriate source whilst isolating the BNC outer conductor from the case of the capacitor. Sufficient quantities of these capacitors have been produced to cover a range of common EPS coupling capacitances from 9 fF to 1.8 pF. A robust case has been produced by employing 25 mm cut lengths of 5/8’’

(16 mm) copper pipe. Brass end caps seal the unit and provide mechanical support for the connectors at either end. The end caps are held in place by small grub screws, allowing for straightforward assembly and disassembly. Design and fabrication was performed by the author and based upon suggestions from academic faculty, with cut copper pipe and brass caps provided by technical staff. The internal structure, shown in Figure 3-3, consists of a glass fibre reinforced epoxy (FR-4) Printed Circuit Board (PCB), devoid of copper apart from two small solder pads which allow the two connectors to be tethered together. This forms a rigid structure that allows assembly of the internal capacitor before inserting into the copper case. The capacitive element itself consists of a PTFE composite substrate with electrodes on the two parallel surfaces to produce a simple planar, parallel plate capacitor with PTFE dielectric. This capacitor is suspended in the void between the two connecters by its single core connecting wires.

The PTFE composite used to produce the capacitive element is a PCB substrate intended for radio frequency applications (Rogers Inc., n.d.). This makes it convenient for producing capacitors since the material is well characterized as a dielectric, and the metallization on top and bottom surfaces provide parallel plate electrodes. For the 0.787 mm thickness material used here, the dielectric constant is given on the manufacturer's data sheet as 2.33 +/- 0.02. Long term and thermal stability of the dielectric are very good, while high dielectric strength ensures that high potentials and

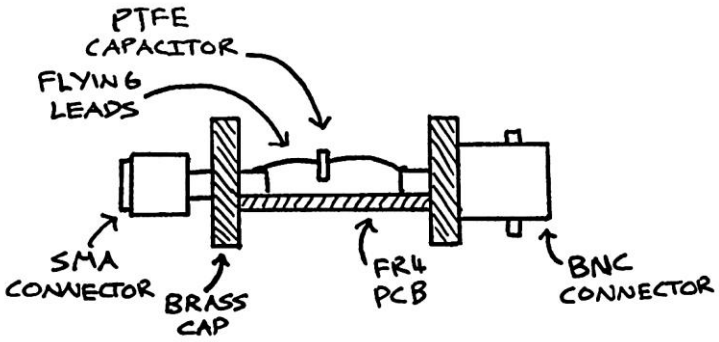


Figure 3-3: Internal structure and external connections of the test capacitor. Most mechanical and electrical connections are made by solder. The BNC is screwed into the threaded brass end cap. The BNC is of the insulated style so that no electrical connection is made between the BNC outer terminal and the case of the capacitor.

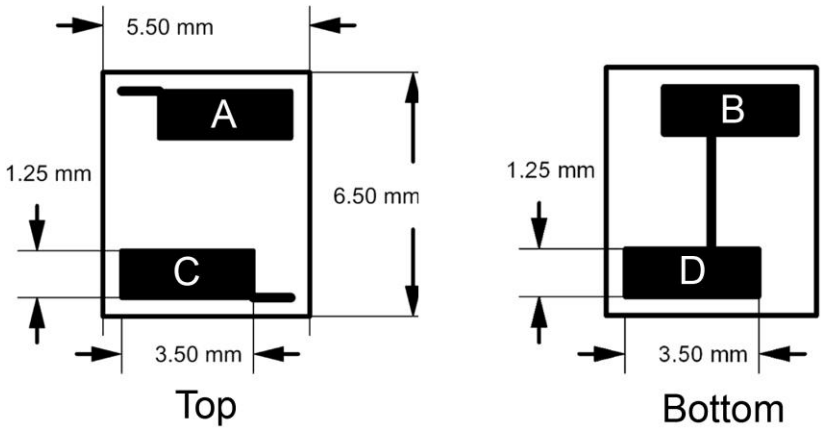


Figure 3-4: PCB layout for the capacitance structure. The dimensions shown here are intended to produce a 100 fF capacitor. Dark areas in the figure indicate the presence of copper, clear areas have the copper removed. This example consists of two separate capacitors on the same substrate, each capacitor formed between the electrode pairs A-B and C-D respectively. A copper trace connects the two capacitors on the bottom layer, and short traces provide solder pads on the top layer. The series connection is used to produce a total capacitance half of that produced by the individual capacitors.

damage due to electrostatic discharge (ESD) should not be problematic. The low value of the dielectric constant is particularly useful in producing low value capacitors. Of crucial importance is the very low leakage of the dielectric, quoted on the datasheet in the form of volume resistivity as 2×10^{13} Ohm cm. A significant DC leakage current in the capacitors would compromise their use at the very low AC frequencies often used with the EPS. The design chosen for the capacitive element consists of parallel plate electrodes with landing pads for convenient soldering of connecting wires, as shown in Figure 3-4. The electrode area is confined well within the bounds of the dielectric material to ensure as much of the electric field is retained within the dielectric material as possible. For capacitance values of 100fF or less the structure actually consists of two separate parallel plate capacitors electrically connected in series, in order to achieve a halving of capacitance value thereby allowing the capacitance structure to be built on a workable scale. The structures are produced on the bare, fully metalized PCB material by subtractive machining of the unused copper areas on a PCB prototyping mill.

The design procedure for a given capacitance value usually consists of defining the electrode area based on an approximate calculation using the standard equation for a

parallel plate capacitor, $C = \frac{\varepsilon_0 \varepsilon_r A}{d}$. This approximation tends to produce an actual capacitance value larger than intended due to edge effects (Binns, Lawrensen and Trowbridge, 1992). With the electrode area produced by the PCB mill therefore being too large, it is possible to subsequently trim the electrode area down until the desired capacitance is achieved by employing an iterative trim and measure procedure. Trimming of the electrode area is performed by hand, using a scalpel to remove portions of the copper foil. This trimming procedure makes it possible to achieve a desired capacitance value with greater accuracy than possible by design and CNC milling alone.

3.2 Measurement of the coupling capacitors

Measurement of the capacitance value for these very low valued capacitors obviously requires considerable care. A Hewlett-Packard (HP) 4275A Inductance-Capacitance-Resistance (LCR) meter has been used to measure these capacitors due to its ability to directly measure capacitance in the femto-Farad range at a convenient range of test frequencies and test signal amplitudes. The key factor in producing reliable and accurate measurements with such a device is the provisioning of a quality test fixture that interfaces with the device under test. Hewlett-Packard and several third-party companies produce several such fixtures for measurement of a variety of devices, including leaded and surface mount components. However, the measurement of these capacitors has required the construction of a custom fixture, as shown in Figure 3-5.

This fixture provides the obvious benefit of providing the correct connectivity between the 4 measurement terminals of the LCR meter and the two coaxial connectors on the test capacitor, but its true function is to provide a mechanically and electrically stable connection. Since the HP LCR meter relies on an open circuit calibration in order to provide high resolution capacitance measurement, the test fixture has to provide a geometrically stable connection to the capacitor so that the capacitor under test can be

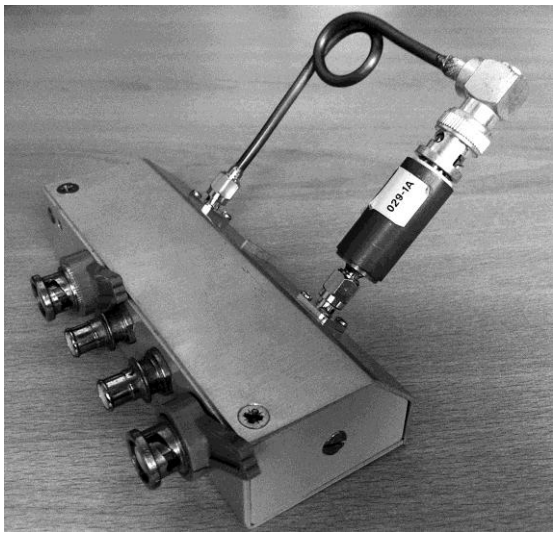


Figure 3-5: Custom fixture for measurement of test capacitors with HP-4275A LCR meter.

removed from the circuit and the open circuit calibration carried out with the test fixture in place – thus nulling out the influence of the fixture on the measurement.

To further improve the accuracy of this zero point calibration a test capacitor has been fabricated which is identical in every way to the other units, with the exception that it contains no capacitive element. By inserting this at the time of open circuit calibration the effect of the capacitance between the signal and guard sections of the enclosure and coaxial connectors of the test capacitor can be negated.

The 4 BNC connectors in the test fixture are connected to the two SMA terminals on the test fixture casing by rigid single core wires. At the SMA connector the 4 measurement terminals are joined to produce a two-terminal measurement since a 4-terminal measurement provides little benefit when measuring low-value capacitors. A semi-rigid co-axial cable provides connection between the fixture and the BNC connector on the capacitor. This rigid cable has been looped to provide strain relief. The SMA end of the capacitor is rigidly fixed directly to the test fixture SMA connector. This completely rigid construction has proved effective at providing repeatable femto-Farad capacitance measurements.

Table 3-1 lists the results of capacitance measurements on the full range of capacitors produced in the initial batch. Capacitance has been measured at 1MHz since this

PROPERTY	PART NO.					UNITS	ERROR	CONDITIONS
	1200-1A	100-1A	100-1B	053-1A	029-1A			
C*	1200	100	100	53	29	fF	2%	f = 1 MHz
$R_{LEAKAGE**}$	1×10^{12}	1×10^{14}	1×10^{14}	1×10^{15}	1×10^{16}	Ω	10%	V_{TEST}= 500 V DC
ESR*	1×10^{2}	1×10^{3}	1×10^{3}	1×10^{5}	5×10^{5}	Ω	10%	f = 1 MHz
RC product	1.2	10	10	50	290	s	-	-

Table 3-1: Results of measurements on the range of test capacitors.
***Measured on HP-4275A LCR Meter using custom bridge. DC Bias = 0v; Oscillator Level = 1.00V; High Resolution mode (averaging) on. Measurements are zeroed using an empty capacitor casing (part no. 000-1A)**
****Measured on HP-4329A High Resistance Meter, in ungrounded sample mode.**

provides the highest resolution measurement achievable with the HP-4275A. Whilst this measurement frequency does depart from the more typical audio-frequency measurement range used with most EPS sensors, performance can be expected to remain consistent at lower frequencies. This assertion is confirmed by the DC leakage measurements performed using a HP-4329A high resistance meter. The high DC leakage values measured mean that pure capacitive behaviour should be maintained to frequencies below 1 Hz.

Unique part numbers have been assigned to all the capacitors to assist tracking, particularly useful where multiple examples have been produced of the same value and when additional capacitors have been constructed at later dates. The capacitors are individually labelled with their part number, capacitance value and voltage rating. All capacitors have been rated for use at 1000V DC, based on the dielectric strength of the PTFE material and connectors. The spread in DC leakage value can be attributed to the increased dimension of the capacitor electrodes at higher capacitance values.

3.3 Determination of EPS input impedance by frequency response measurement

The calibrated test capacitors provide a simplified and consistent signal coupling situation, making it possible to perform repeatable characteristic measurements of the EP sensors. A measurement of frequency response can be used to extract several pieces of information. The input impedance of the sensor can be calculated, which can be used to recalculate the behaviour of the sensor when the coupling capacitance is different. Since the input impedance defines the sensitivity of the EPS to capacitively coupled sources of potential, it can be used as a figure of merit. Furthermore, the upper limit to the sensor bandwidth can be found.

The input impedance of the sensor can be expressed as a separate input capacitance and resistance. This is discussed in chapter 2.3. The same equivalent circuit from chapter 2.3 is used to define the input impedance of the sensor, and so the circuit is reproduced here in Figure 3-6. A calibrated test capacitor is used as C_c in this circuit. It is the well defined value of C_c that makes it possible to determine Z_{IN}. In order to find the values of C_{IN} and R_{IN} it is necessary to make two measurements; firstly the gain of the sensor at a frequency ω much greater than ω_c and secondly the value of the high-pass corner frequency ω_c. The measurement of the sensor gain must be performed within the

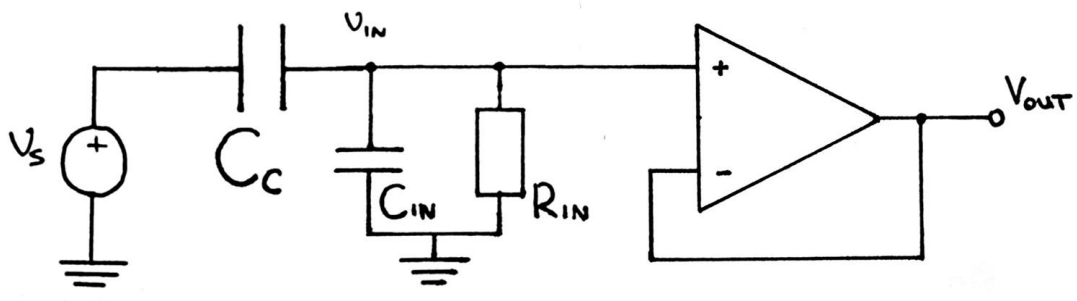


Figure 3-6: Schematic of EPS test circuit. C_{IN} and$R_{IN,}$ are the two parallel contributions to the total sensor input impedance,Z_{IN}. C_C is the input coupling capacitance, and for the test case is a calibrated test capacitor.

bandwidth of the sensor, and so is herein referred to as the mid-band gain. Of course each measurement requires, to some extent, a priori knowledge of the other. Though an experienced experimenter should quickly find these two values using a function generator and an oscilloscope, the result is discovered with ease by conducting a full frequency response measurement. A plot of gain versus frequency graphically reveals the upper frequency roll-off which defines the bandwidth of the sensor, ω_{max}, as well as the low frequency roll-off ω_c, and the mid-band gain $A_{v,mid}$.

Once these values have been measured, the input impedance of the sensor can be determined by rearranging equations 2-5 and 2-6 respectively, to give C_{IN} and R_{IN}.

$$C_{IN} = C_C\left(\frac{\mathrm{A_v}}{\mathrm{A_{v,mid}}} - 1\right) \tag{3.1}$$

and,

$$R_{IN} = \frac{1}{\omega_c(C_c+C_{in})} \quad or \quad R_{IN} = \frac{1}{2\pi f_c(C_c+C_{in})} \tag{3.2}$$

In equation 3.1 an additional term has been added, A_v, which represents the system gain. This term accounts for the gain of the amplifier at the input of the EPS and that of any subsequent amplification stages. It is completely distinct from the gain of the EPS due to the loading of the sensor input impedance, which is always unity or less. This parameter must be measured before any calculation of input impedance can be made. This may be performed by coupling a signal into the EPS via a large valued capacitor and then measuring gain at a frequency within the sensor bandwidth. This large value of C_c effectively negates any effect on the frequency response due to the input impedance of the sensor, leaving only the gain of any amplification stages. Typically, a coupling capacitor of 1 nF or greater is suitable. With such a low-impedance coupling it is not necessary to make any special considerations of guarding around the input node, so that a simple leaded component may be used with appropriate connectors added. In general, interpretation of measurements is simplified if the system gain is eliminated from measurements by dividing by A_v before continuing with analysis.

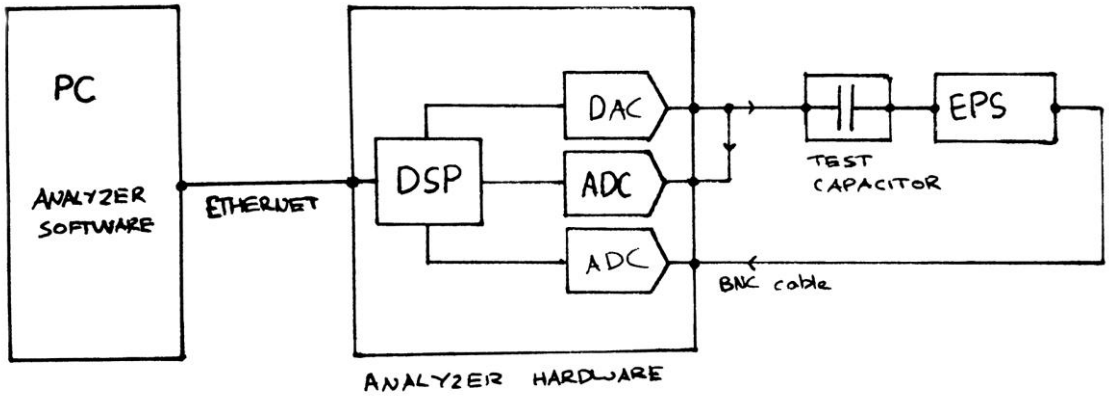


Figure 3-7: Frequency response measurement block diagram. The device under test is an EPS sensor with a test capacitor for input signal coupling. A test signal is generated by a DAC. The test signal is connected to the test capacitor and the first ADC channel. The second ADC channel samples the EPS output signal. PC software and a DSP perform an SSR measurement.

Frequency response measurements have been performed using a mixed-signal Swept Sine Response (SSR) analyzer (Bruel & Kjaer, n.d.). With this system analogue connections are made to the EPS and test-capacitor circuit via data converters, allowing a digital signal processing chain as shown in Figure 3-7. A 24-bit Digital to Analogue converter (DAC) provides a high purity sine wave stimulus signal, and a 16-bit Analogue to Digital Converter (ADC) digitizes the sensor output. PC based software operates in concert with a hardware Digital Signal Processor (DSP) to perform a phase-sensitive gain measurement across a user-defined frequency range between 125 mHz and 100 kHz.

The PC based software produces an ASCII text file containing a 2 column table of frequency versus gain measurements in units of V/V. This text file can be imported into Matlab (Mathworks, Natick, MA, USA) or a similar data processing package. A conventional Bode plot can then be produced by converting the gain values to decibels, and plotting against a log frequency scale. This plotting process has been automated by a Matlab script which takes as its input the ASCII data file and produces a formatted Bode plot and calculates the input impedance of the sensor. A definitions file allows the user to set various parameters including the coupling capacitance, system gain and the mid-band frequency (used to find the mid band gain). This script linearly interpolates

the gain data in the frequency domain in order to find a better estimate of the -3 db frequency for the determination of input resistance.

The sensor under test is placed in a shielded test enclosure (connected to system ground) with signal and power connections made through shielded BNC and DIN connections respectively. All instruments are set to 'float' shield termination so that the signal ground terminates only at the power supply, where all instruments are similarly connected to this single ground node (Morrison, 1967). This ground is connected to earth through the power supply. This configuration prevents ground loops and subsequent mains noise coupling, which is only important in low-noise measurements. A dual-rail bench Power Supply Unit (PSU) is used throughout. In exceptional cases where a very low noise measurement is required the output ripple of this power supply has been found to be excessive, and so additional smoothing has been applied to the PSU rails by a passive RC network.

3.4 EPS noise measurement using test capacitors

The separate voltage and current noise contributions of an amplifier are traditionally measured by measuring with a grounded and open-circuit input respectively. The first measurement can be reliably performed with an EPS sensor, though in the latter case the definition of open-circuit is not so useful. Instead, measurement is best performed using a test capacitor to ground the input, since then the coupling capacitance is well defined. By this method the total output noise of the sensor is measured, and so the thermal and current noise terms can only be separated by calculation of the thermal term based on a measured value of R_{IN}. The output noise should be divided by the system gain in order to find the equivalent input noise.

Measurement of the sensor noise as a spectral density requires transformation from the time domain to the frequency domain. Two methods will be described here, the first using the mixed-signal analyzer described earlier, and the second, a more protracted method using a separate digitizer and post-processing software. In both cases the sensor under test is placed in the same screened enclosure as in the frequency response measurement with identical signal, power and ground connections.

The mixed signal analyzer provides an FFT function for the measurement of voltage spectral density of an analogue input signal. An up-to 6000 point FFT can be performed, with linearly spaced data points (in the frequency domain) at a user defined centre frequency. The ADC input integrates a low noise pre-amplifier so that no further signal conditioning need be applied to the sensor output signal.

It is useful to measure the EPS noise at very low frequencies (to around 10 mHz). Whilst this information is of some value in the rare cases where an EPS is to be employed in an application requiring such low frequency response, the real value here is in the experimental observation of the noise corner frequency. This will serve as some confirmation of the earlier developed theoretical model. There are few (if any) laboratory instruments available which can perform a noise measurement at such low frequencies whilst simultaneously extending to a higher frequency of several kHz, and so a more protracted method is employed for this purpose. In essence the procedure involves digitizing the sensor output voltage over a long time period, and numerically extracting a power spectral density estimate at the post-processing stage. The measurement period must be greater than the reciprocal of the lowest frequency of interest. The Nyquist frequency (half the sampling frequency) of the digitized signal sets the upper frequency of the noise measurement. The qualifier *estimate* is applied to this power spectral density calculation in order to formally agree with the mathematics involved, though as engineers we need not be concerned with the precision of this estimate.

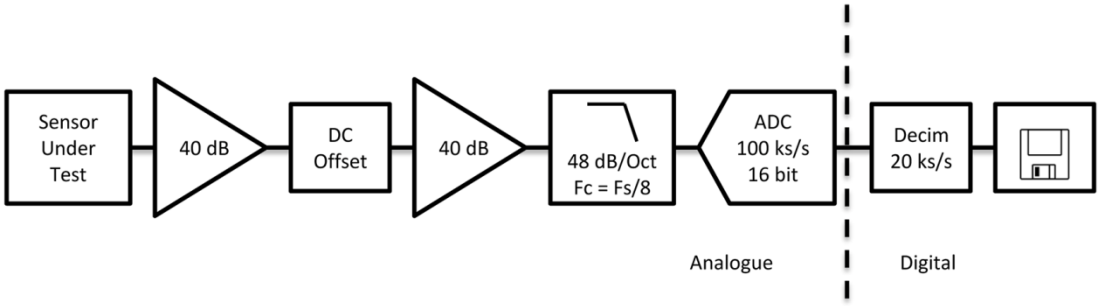


Figure 3-8: Signal conditioning chain used for low noise measurement.

The ADC used does not provide an integrated pre-amplifier or aliasing filter, and so the signal conditioning is provided externally. The signal chain is illustrated in Figure 3-8. An overall gain of 80 dB is applied to the sensor output, which is DC-coupled throughout and provides user adjustable DC offset nulling. Aliasing filtering is provided with 48 dB/octave attenuation at a corner frequency of $f_s/8$, where f_s is the sampling frequency of the digitizer, and $f_s = 100\ ks/s$. This filter provides 96 dB of attenuation at the Nyquist frequency, completely eliminating aliasing artefacts. The sampled data is decimated to a sampling rate of $20\ ks/s$ before being stored to disk in a tab-delimited text file. The ADC is a 16-bit, 1Ms/s device from National Instruments Inc. and is interfaced to a simple Labview (National Instruments, Austin, TX, USA) program which performs the decimation and recording of data to disk.

Post processing is performed on the time signal using Matlab (Mathworks, Natick, MA, USA). The periodogram spectral estimation method from the signal processing toolbox is used to compute a power spectral density (PSD) estimate. A Hamming window is used and the spectrum is computed at 1000 log-spaced frequency points, $10\ mHz \leq f \leq 10\ kHz$. Obtaining these log-spaced data points still requires computation of the full FFT for all of the samples. The square root of the PSD estimate is taken to give the voltage spectral density (VSD). In order to obtain the PSD estimate at the range of frequencies given, a record length of at least 100 seconds is required. In general a recording of 500 seconds is used, from which 5 separate PSD estimates are obtained from sequential 100 second blocks. The mean of these 5 PSD estimates is used to give the final noise data. In general some form of averaging is highly desirable for statistical

signals such as this. The 100 second data block comprises 2 M samples, and so the 2 million point FFT requires considerable computation time and memory resources (around 500 seconds on a 4-core Intel x86-64 processor with 4 GB total RAM).

The input of the sensor is grounded through the calibrated coupling capacitor. The test capacitor is used only partially to give a defined coupling capacitance to ground, but also to maintain an identical guard capacitance as in the frequency response measurement. This fixes the sensor parameters so that the measured noise can be compared with that obtained from the model given in section 2. This is particularly the case when unguarded circuits are measured, where the test capacitor contributes several pico-Farads of input capacitance in addition to the smaller coupling capacitance (which is now also terminated to ground).

3.5 Measurements on an AD549 based EPS sensor

A simplified EPS sensor has been constructed for the purposes of verifying the theoretical models discussed in chapter 2, and as such does not feature any adjustments or features that make it suitable for any other application. The sensor consists of a high

		Min	Typ	Max	Units
I_B	VCM = 0 VCM = ±10V		40 40	60 60	fA
e_n	f = 10 Hz f = 100 Hz f = 1 kHz		90 65 35		$nV/Hz^{1/2}$
i_n	f = 1 kHz		0.11		$fA/Hz^{1/2}$
A_{OL}		300	1000		V/mV
GBW	Small-signal	0.7	1		MHz
Z_{IN}	Differential		10^{13}||1		Ω||pF

Table 3-2: AD549L data sheet specifications (Analog Devices, 2008).

impedance JFET input operational amplifier, the AD549L. The L designated version offers the lowest input bias current of the AD549 range. Table 3-2 lists the specifications of this device which are most important for an EPS.

The EPS is assembled on a conventional copper clad printed circuit board (PCB) material, with standard FR-4 dielectric. The PCB is patterned by a subtractive machining process. This process is used only because of its availability to the experimenter, and is not considered to offer any benefit over a conventional wet etching process. After assembly the PCB is cleaned with compressed air and isopropyl alcohol.

The AD549 device is configured as a unity gain voltage follower. This simplifies analysis by setting $V_o = V_{IN}$, and eliminates any subsequent errors which would be introduced by gain setting resistors. The input is terminated by a co-axial SMA connector, with inner connected to the EPS input node, and the outer connected to the guard circuit node. A nominal 100 GΩ thick-film resistor in a 1206 surface-mount package is used as R_{IN}. The tolerance of this resistor is 20%. This component is not mounted to the board in a conventional surface mount land pattern, but is instead soldered to the board at one end only, whilst the other forms the 'flying lead' input node. The V+ input lead of the packaged AD549 op-amp is similarly not soldered to the PCB but instead takes a direct path through air to the centre terminal of the SMA input connector. It is along this lead that the input resistor is connected, thus forming the flying lead input. This technique eliminates any effects that might be caused by the PCB dielectric, particularly those due to the surface leakage current.

As described in section 2.5.2, the gain error for the voltage follower will be less than 4 ppm for an AD549L (from equation 2.21). By directly connecting the unity gain output to C_G, the effective guarded value of C_G will be less than 4 ppm of its intrinsic value, so $C_{G,eff} \leq 4\ aF$. Additionally, $C_{G,eff}$ is guaranteed to be non-negative. For this reason, adjustment between the unguarded and guarded mode of operation is achieved by hand soldering the guard node to either signal ground or the output node of the op-amp.

The entire input area and op-amp are surrounded by copper planes on the top and bottom PCB layers, and enclosed in a 25 x 25 x 10 mm metal can. These are all connected to the guard node. The AD549 is packaged in a TO-99 8-lead metal can, with the metal can also connected to the guard node. As mentioned, the outer 'shield' terminal of the co-axial SMA connector is also connected to the guard node, and so any external component, such as a test capacitor, which is connected to the input, will also be guarded. As a result, the majority of the sensor input capacitance will be due to this guard circuit, the capacitance of which has been denoted C_G, with only the op-amp common mode input capacitance as an additional capacitance, hence the designation of any additional unguarded capacitance as C_{OA}.

Bootstrapping of the input resistor is provided by a potentiometer so that a feedback signal of fractional gain may be derived from the unity gain op-amp output. The feedback signal is AC coupled by R_{BS} and C_{BS}, which set a corner frequency of 1.5 mHz.

The following measurements have been performed in accordance with the methods outlined previously. Due to the low front end gain of this sensor, all of the precautions

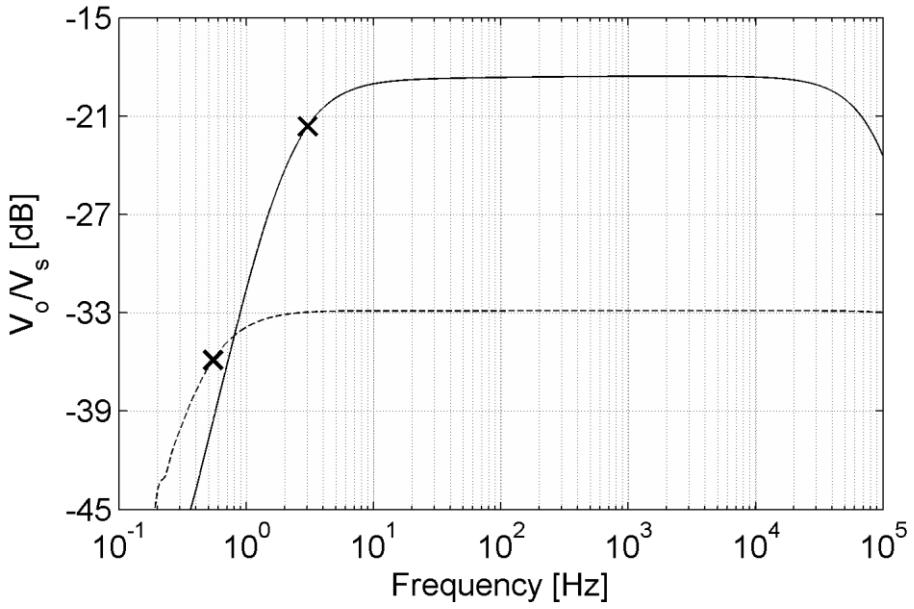


Figure 3-9: Frequency response for an EPS sensor coupled through a 100 fF test capacitor, with no guarding or bootstrapping (dashed line) and with the addition of unity guarding (solid line). An 'x' marks the lower -3db point.

described earlier are used to ensure signal integrity.

3.5.1 Frequency response and input impedance

Input impedance has been determined by measurement of frequency response under three sensor conditions; no feedback, guarding, and finally guarding and bootstrapping. In the first case where neither guarding or bootstrapping are applied C_{IN} is composed of the guard capacitance and the amplifier input capacitance, so that $C_{IN} = C_{OA} + C_G$. When guarding is applied, then with the assumption that $C_{G,eff} = 0$, the input capacitance is only composed of the amplifier input capacitance, and so $C_{IN} = C_{OA}$. These two measurements of input impedance therefore allow the amplifier input capacitance to be disentangled from the guard capacitance, which will be of use when calculating the sensor noise. In the final measurement the effect of bootstrapping of R_{IN} is observed. In this case a bootstrap signal of $0.9 \times V_o$ has been derived by careful setting of the bootstrap potentiometer whilst monitoring the feedback and output signal on an oscilloscope.

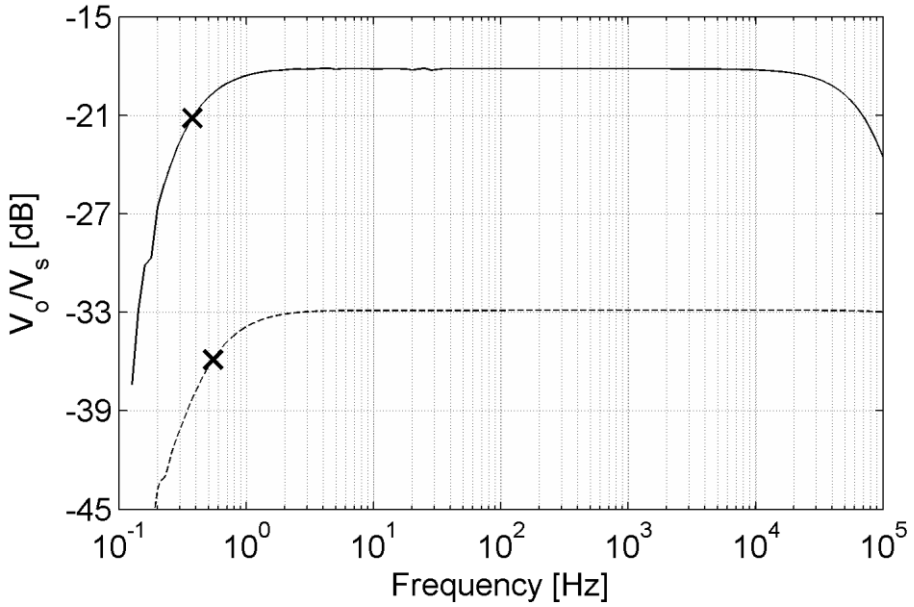


Figure 3-10: Frequency response for an EPS sensor coupled through a 100 fF test capacitor, with no guarding or bootstrapping (dashed line) and with the addition of bootstrapping and guarding(solid line). An 'x' marks the lower -3db point.

A 100 fF test capacitor has been used throughout. In Figure 3-9 the guarded and unguarded response is compared, and in Figure 3-10 the guarded and bootstrapped response is shown. From the Bode plot the two required measurements are extracted; mid frequency gain, $A_{v,mid}$, and the corner frequency, in units of Hertz, f_c. For the case of no bootstrapping or guarding, the following has been measured,

$$A_{v,mid} = -32.87\ dB = \ 0.0227\ V/V$$

$$f_c = 0.541\ Hz$$

It is now possible to use equations 3-1 and 3-2 to find C_{in} and R_{in}, with $C_c = 100\ fF$.

$$C_{IN} = C_C\left(\frac{1}{\mathrm{A_{v,mid}}} - 1\right) = 100 \times 10^{-15}\left(\frac{1}{0.0227} - 1\right) = 4.3 \times 10^{-12}$$

Guard	Bootstrap	$A_{V,mid}$ dB	f_c Hz	C_{IN} pF	R_{IN} GΩ
OFF	OFF	-32.9	0.541	4.3	66.4
ON	OFF	-18.6	3.01	0.752	62.0
ON	ON	-18.1	0.37	0.709	526

Table 3-3: Summary of experimental results for an AD549 EPS under 3 different feedback configurations

$$C_{IN} = 4.3\ pF$$

the value of C_{in} is now used to find R_{in},

$$R_{IN} = \frac{1}{2\pi f_c(C_c + C_{in})} = \frac{1}{2\pi \times 0.541 \times (4.3 \times 10^{-12} + 100 \times 10^{-15})} = 66.4\ \times 10^9$$

$$R_{IN} = 66.4\ G\Omega$$

A summary of these measurements is given in Table 3-3. Note that the addition of bootstrapping results in a minor decrease in input capacitance of around 40 fF. This is due to the guarding of the input resistors own capacitance, which as shall be confirmed later, is generally around 40 fF for a resistor in this package.

3.5.2 Noise

The noise of this sensor has been similarly measured under the 3 feedback configurations. Figure 3-11 shows the results of a measurement of voltage noise and total output noise for the sensor with no feedback. Voltage noise is measured by grounding the input, and total output noise, e_o, is measured with a 100 fF test capacitor

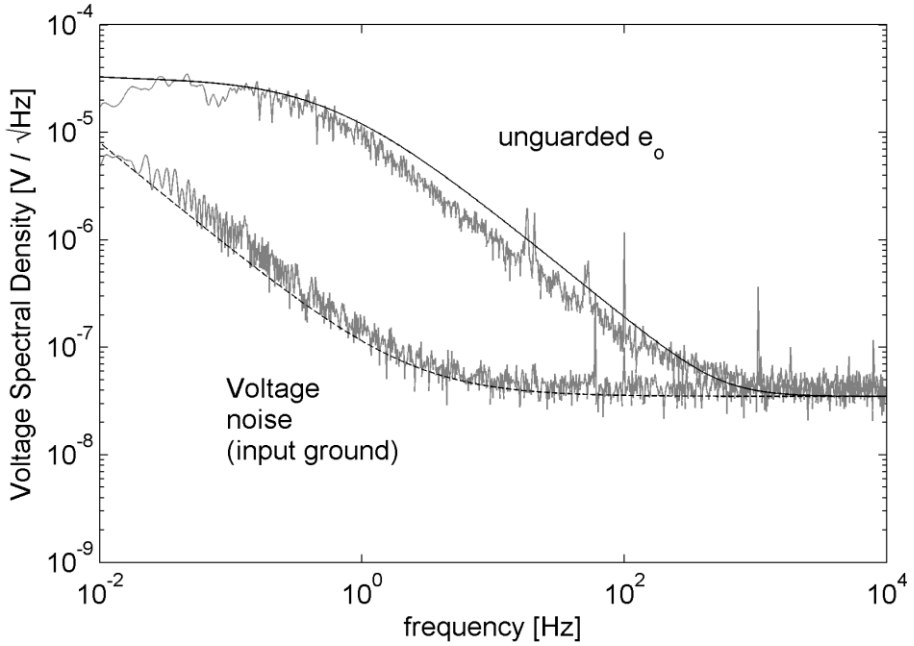


Figure 3-11: Voltage noise (input grounded) and output noise for the AD549 sensor. Grey lines are measured noise, and black lines are based on the noise model. e_n is modelled as 35 nV/√Hz with a 1/f corner at around 10 Hz.

terminated to ground. From the earlier frequency response measurements the unguarded C_{IN} is known to be 4.3 pF and R_{IN} is 66.4 GΩ. These parameters have been used to model the total output noise for this sensor, the result of which is also plotted in the figure. The current and voltage noise terms have been calculated using the data sheet values of $0.11\,fA/\sqrt{Hz}$ for the current noise and $35\,nV/\sqrt{Hz}$ for the voltage noise. Additionally the voltage noise term has been modelled with a 1/f corner at around 10 Hz, the value of which is found empirically to match the measured data. The noise corner frequency is observed clearly in the measured and modelled data, and strong agreement is found at both the low and high frequency regions. There would appear to be a small error in the noise corner frequency used in the model, which indicates the value of C_{IN} used for modelling may be less than in the measured sensor. The reason for this discrepancy is unknown.

In Figure 3-12 the total output noise for the guarded sensor is shown with the unguarded output noise for comparison. The expected increase in noise corner frequency and the feedback of voltage noise at high frequencies is evident in the measured data. Equation 2.36 has been used to find the total output noise for the guarded sensor. From the earlier

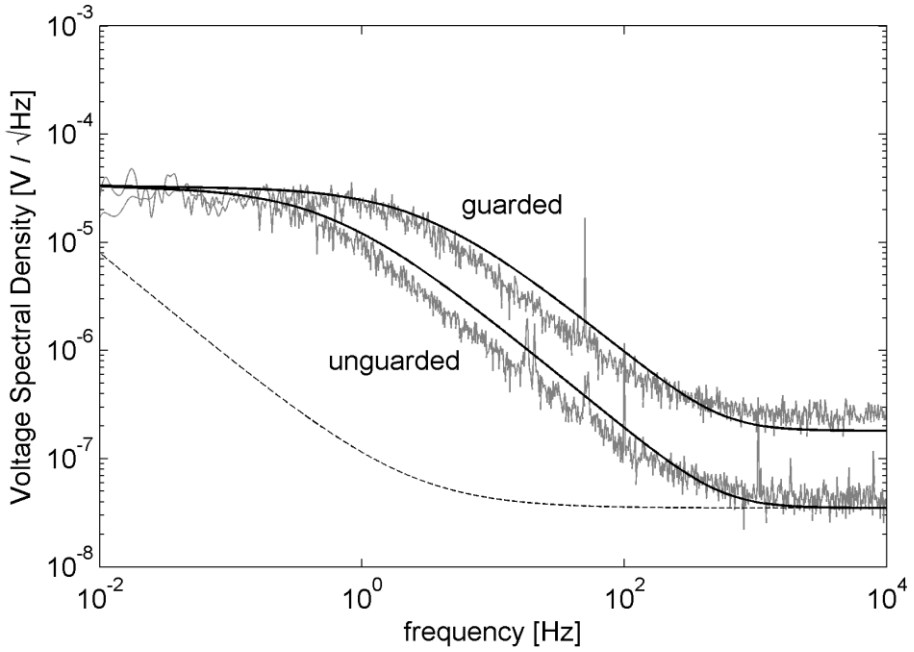


Figure 3-12: Output noise for sensor with and without guarding. Grey lines are measured, and black lines are based on the noise model. A dashed line shows the modelled voltage noise.

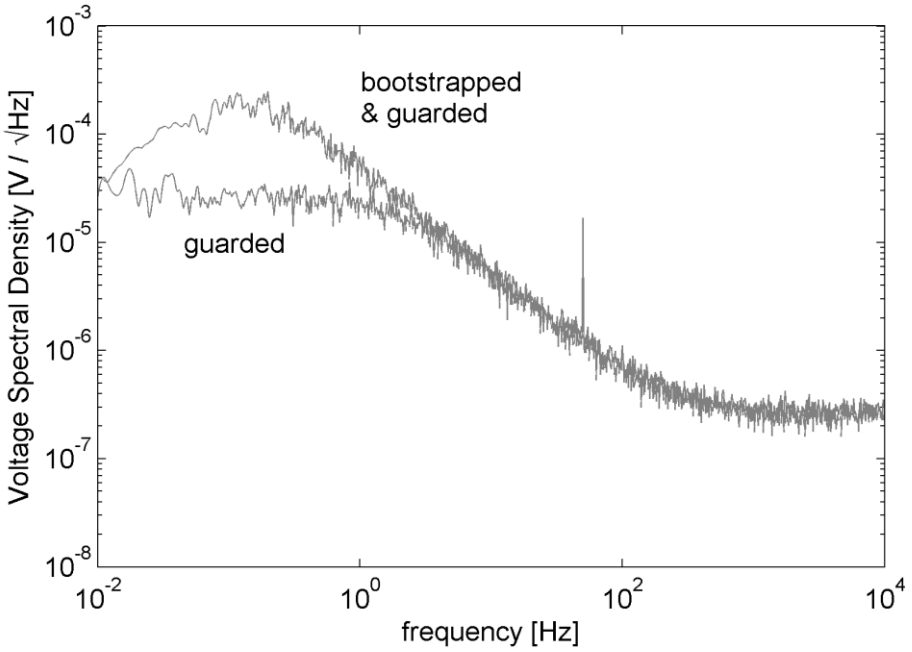


Figure 3-13: Output noise for sensor with and without bootstrapping. Guarding is applied in each case.

frequency response measurement the guard capacitance has been found to be $4.3\ pF - 0.75\ pF = 3.55\ pF$. This is determined simply by subtracting the input capacitance of the guarded and unguarded sensor. C_{OA} is simply the input capacitance of the guarded amplifier, and is therefore $0.75\ pF$. These parameters once again produce a slightly higher noise corner frequency, and slightly lower gain of the voltage noise term, than in the experimental data. This discrepancy can be addressed by increasing the value of C_G from the value experimentally determined.

Figure 3-13 shows the experimentally measured noise for a bootstrapped sensor. As expected, noise is only increased in the low frequency region, and only down to the bootstrap circuit corner frequency.

The experimental methods and results collected in this chapter form convincing support for the previous theoretical discussion of EPS performance. The data presented here on a typical op-amp based EPS provides a useful 'benchmark' when considering more complex EPS designs.

4 FET CIRCUITS FOR ULTRA LOW CAPACITANCE SENSORS

Following the generalized treatment of EP sensors, it is now possible to tailor this discussion more closely to EP sensors designed for very high input impedance, or more specifically, ultra-low input capacitance, and discuss this in the context of only those applications where such a sensor is appropriate, such as microscopic imaging. Nonetheless, the applicability to the general case will not be completely forgotten, since some of the circuits explored will offer benefits in addition to their very high impedance.

Whilst integrated operational amplifier circuits are available which are well suited to EPS applications, it could be said that an operational amplifier is sufficient, though not necessary for an EPS. As already described, the most important specification for an EPS amplifier is a very low input bias current. Operational amplifiers are available which perform well in this regard (such as the AD549) though input capacitance is often large (around the pico-Farad level). An amplifier for an EPS must have very low input bias current and it should also have low input capacitance. Voltage gain is not generally necessary at the input stage, and often unity gain is quite satisfactory.

By investigating discrete transistor circuits, a higher level of control of amplifier performance is granted to the designer. This enables the production of amplifier circuits with performance which exceeds that of general purpose, and even specialized high-impedance, operational amplifiers, whilst also minimizing extraneous components

(when compared with the transistor count of an integrated circuit) and features which are not necessary for an EPS amplifier, such as differential inputs and very large gain. In addition, by investigating these discrete circuits the transition to a specialized EPS integrated circuit is eased. This transition is one of the key motivations for this investigation, and as such, the compatibility of these circuits with typical highly integrated semiconductor fabrication processes is considered.

This chapter will discuss the use of Junction- and MOS-FET devices in EP sensors, before experimental data from a series of experiments performed on a MOSFET based EPS is given in the following chapter. A familiarity with FET devices is assumed of the reader, though the following brief introduction will serve as a reminder of the pertinent characteristics. The study of the non-ideal behaviour of FET devices is a broad field and remains an area of active research; this discussion is therefore limited to the case of linear amplifiers (that is, biased for saturated drain current) at low frequency (to be precise, below f_T of the transistor concerned).

4.1 Ideal FET Devices

The Field Effect Transistor (FET), with its low input bias current, is the basis of any high impedance amplifier. In such a device the conductance of the channel, between the source (S) and drain (D) terminals, is controlled by a voltage applied to the gate (G). The gate terminal may be a p-n junction, as in a JFET, or an insulated metal electrode, as in a MOSFET. Channel conduction may be achieved by either electron (n-type) or hole (p-type) majority carriers. In n-channel JFET devices channel conduction is controlled by a negative potential (with respect to the source) applied to the gate terminal, creating a depletion region in the channel. The gate is therefore a reverse biased p-n junction under normal operating conditions. MOSFETs are available as either depletion or enhancement devices. The transfer characteristics (the gate-source voltage vs. channel conduction) of a depletion MOSFET are similar to a junction

device, whilst an enhancement MOSFET, also known as a 'normally-off' device, allows channel conduction only when a positive gate voltage (with respect to the source) is applied. In either case the gate terminal of a MOSFET is a dielectrically insulated electrode.

The performance of a FET device is determined chiefly by the dimensional parameters, channel width W, length L, gate oxide thickness T_{OX} and channel depth, and by the material parameters which include the channel doping and the properties of the gate dielectric in MOS devices. The electrical parameters which are most important in determining the performance of an EPS amplifier are the forward transconductance g_{fs}, the gate leakage current I_G and the input capacitances C_{gs} and C_{gd}. A simple equivalent circuit for a MOS device is given in Figure 4-1. The transconductance is the ratio of drain current to gate-source voltage, $\Delta I_d/\Delta V_{GS}$, and is important in determining several amplifier parameters. The channel area is directly proportional to the forward transconductance. If a leakage current is permitted to flow between the gate and the channel, then it will be proportional to the gate area, as will the parasitic gate-drain and gate-source capacitances.

All of the above Field Effect Transistors may be suitable for use in EPS designs. Though a Junction device will usually have a larger input bias current when compared to a MOS device, the ability to produce very low gate leakage JFETs has been demonstrated by various manufacturers. Examples of such devices include those used as the input transistor in the afore-mentioned AD549 op-amp, and others such as the Burr-

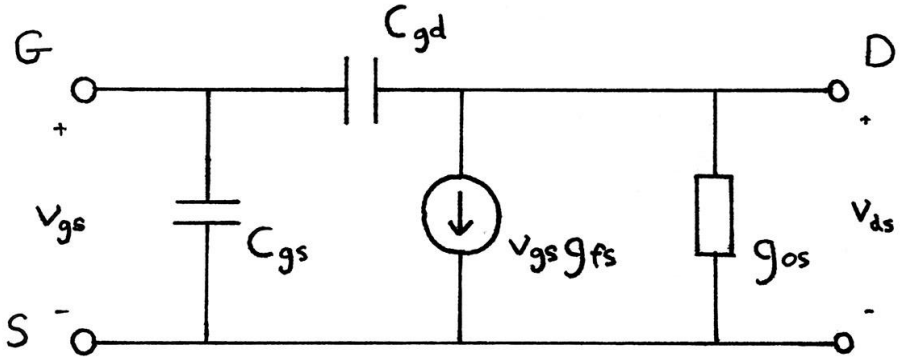


Figure 4-1: Small-signal equivalent circuit for a FET device.

Brown INA116 and Texas Instruments OPA129. These devices have input bias currents of tens to hundreds of femto-Amps; a high level of performance which has been achieved by the use of proprietary JFET fabrication techniques, the TopFET for the Analog Devices AD549 and the DiFET in Burr-Brown and Texas Instruments parts. These proprietary fabrication processes are not available to foundry customers, nor are discrete JFET devices available with performance which even approaches that of the input devices of these op-amps. MOSFET devices offer an inherently low input bias current due to the dielectric isolation of the gate terminal. This low input bias current performance is therefore readily available to the EPS designer, either as discrete devices or in common analogue CMOS fabrication processes. The selection of a MOSFET over a JFET device will usually bring with it a voltage noise penalty, largely due to the increased flicker (1/f) noise term (Christensson, Lundstrom and Svensson, 1968). This difference is largely due to the surface conduction mechanism of a MOS device, in contrast with the bulk conduction in bipolar and junction devices. The underlying processes of this 1/f noise remain a topic of debate, though several empirical models exist which fit experimental data well.

4.2 Non-Ideal FET Parameters

4.2.1 Gate leakage

Undergraduate level textbooks often describe the gate leakage current of MOS devices as negligible or close to zero (Boylestadt and Nashelsky, 2002), and in common with this interpretation a value for the gate leakage current is not generally specified on device data sheets. Several higher level texts unanimously describe the input resistance of MOS devices as 'in excess of 10^{15} Ω' (Research and Education Association, 1981). Since this parameter is of paramount importance in high impedance EPS designs, it seems worth investigating the validity of this assumption. Whilst there has recently been a wealth of research into the gate leakage current of small feature-size (<100 nm)

CMOS transistors, there has been little investigation of this parameter in larger-scale CMOS processes (e.g. $0.35\ \mu m$) commonly employed for analogue devices. This lack of research only seems to further confirm the assumption that this current is negligible for common applications in analogue CMOS and discrete devices. The aforementioned small-feature size devices which are used in digital integrated circuits can suffer from a significant gate leakage current since the thickness of the oxide between gate and channel (referred to as T_{OX}) is small enough (around 1 nm) that a significant tunnelling current exists (Lee and Hu, 2001). In a common $0.35\ \mu m$ analogue CMOS process, T_{OX} is in the range of tens to hundreds of nanometres, and so the tunnelling current, which is exponentially dependent on T_{OX}, is negligible. Though the gate leakage current, or gate to channel resistance, is not generally given in device datasheets, it is possible to estimate a value for the gate-channel resistance using common process specifications. A conventional Silicon-Dioxide gate dielectric has a volume resistivity of around $10^{13}\ \Omega\,\mathrm{m}$ (Kapoor and Shokrani, 1994), and so taking a large-area transistor with $L = 0.35\ \mu m$ and $W = 1000\ \mu m$, a value for the gate-channel resistance can be found using a typical value of T_{OX} for a $0.35\ \mu m$ analogue CMOS process of $T_{OX} = 100\ nm$. The gate-channel resistance is;

$$R_G = \frac{\rho\, T_{OX}}{W \times L} \cong 2000\ T\Omega$$

It is clear from the result of this calculation that even with large area MOS transistors, the gate leakage across the gate-oxide due to volume conductivity is indeed small. However, an additional current may flow across the gate terminal due to a variety of mechanisms which have been investigated for small-feature size devices and may be of importance when ultra-low leakage is required in large-feature devices. These mechanisms are dependent on device geometry, semiconductor processing and biasing conditions, and include the aforementioned tunnelling current, hot-carrier injection into the gate-oxide (Roy, Mukhopadhyay and Mahmoodi-Meimand, 2003), mobile-ions (impurities) in the gate-oxide (Pierret, 1983) and surface leakage across the passivation layer (Rodwell, 2005). When a gate leakage current, I_G, flows across a potential barrier

it produces a shot noise current which has a spectral density $i_n = \sqrt{2qI_G}$ (Connor, 1973). The output noise due to this current is the product of the noise current and the input resistance, and therefore may produce a significant contribution to overall noise when large input resistors are used. For EPS sensors constructed from discrete devices or on large feature size CMOS ($T_{OX} \gtrsim 10\,nm$), the conclusion is that the leakage current of MOS devices is generally small enough that the resistor thermal noise and voltage noise terms will dominate with input resistors in the range of Giga Ohms to tens of Tera Ohms.

Since the thin gate oxide is susceptible to damage by electrostatic discharge (ESD), input protection diodes must be used. Discrete devices usually integrate these diodes. ESD precautions are absolutely required for EP sensors with MOS input devices, since the gate is connected directly to an exposed electrode (the sensor input electrode) which has high impedance to ground. Figure 4-2 shows the protection diode configurations commonly used in discrete MOS devices (Siliconix Inc., 1981). Since these diodes make a direct connection between gate and source terminals, the leakage current of the protection diodes may contribute to the gate leakage of the device, and produce an associated shot noise current. It is clear then that the input protection diodes of the input transistor should be carefully designed to avoid excess noise or bias currents, whilst also providing sufficient forward conduction to prevent damage to the gate oxide.

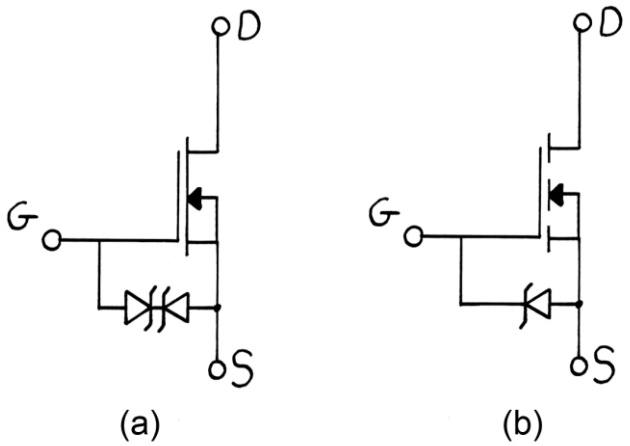


Figure 4-2: Protection diode connections for (a) Enhancement MOSFET and (b) Depletion MOSFET (Siliconix Inc., 1981)

The gate leakage current of JFET devices, as well as the current noise for which it is responsible, has already been discussed in relation to JFET input op-amps. Here this discussion can be expanded to include the effects of the JFET bias conditions on the gate leakage current. The gate of an n-channel JFET is a region of p-doped silicon, which forms p-n junctions with the drain and source terminals that are reverse biased under normal operating conditions (the polarities are simply reversed for a p-channel device). The reverse biased leakage current of a p-n junction is well understood, and like the gate leakage current in MOS devices, is a function of the geometry and the biasing condition. This current is specified as I_{GSS} on device datasheets, and is measured with $V_{DS} = 0\,V$ at a specified V_{GS}. The operating gate current I_G may not equal I_{GSS} since I_G is a function of drain current I_D, gate-source voltage V_{GS}, gate-drain voltage V_{GD} (Siliconix Inc., 1981), and an exponential function of temperature.

Gate current I_G is only weakly dependent on V_{DG} until the 'I_G breakpoint' is reached, when gate current dramatically increases at higher drain gate voltages due to impact ionization. For common discrete devices, this breakpoint is reached at drain-gate voltage of around 10 to 20 Volts, though this threshold decreases with increasing drain current. High impedance amplifiers should always operate below the I_G breakpoint, and hence low V_{DG} should always be ensured.

Below the I_G breakpoint the gate operating current is only due to the reverse biased gate-drain and gate-source diodes. This current is due to thermally generated minority carriers in the depletion region, and so is an exponential function of temperature, and is dependent on the gate area and doping level. It is this leakage current that is responsible for the shot noise generator, $i_n = \sqrt{2qI_G}$.

4.2.2 Gate capacitance

The input capacitance of a FET amplifier is formed principally of the gate to drain capacitance C_{gd}, and the gate to source capacitance C_{gs} (Figure 4-1). The contributions of these two capacitance to the total input capacitance, C_{ig}, will depend on the AC potential at the source and drain terminals. This relationship will be explored later,

when specific amplifier circuits are examined. C_{gd} is sometimes called the feedback capacitance and C_{ig} the input capacitance, corresponding to a common-source configuration.

The gate-drain capacitance C_{gd} is roughly constant with V_{GS} for a given device, though the value of the gate-source capacitance C_{gs} can vary considerably as a function of the biasing conditions. This is true for both Junction and MOS devices. C_{gd} will usually be the smaller of the two capacitances since the gate-drain depletion width will be greater than the gate-source depletion width. By the same reasoning, C_{gs} is found to be a function of V_{GS} (and by consequence I_D) - decreasing in value as the channel is further depleted with decreasing V_{GS} (for n-channel FETs). This relationship is only broken in MOS devices when V_{GS} is sufficiently negative for complete inversion of the channel (Pierret, 1983), though since this discussion is limited only to linear amplifiers this is not of interest.

For a common MOS device, the minimum capacitance C_{gs} achieved at the optimum V_{GS} may only be a half of the maximum value (NXP Semiconductors Inc., 1996). It may be possible to bias for optimal C_{ig}, though in general this is inadvisable due to the limited benefit gained, and so other considerations, such as biasing for optimal transconductance, should take precedence.

4.2.3 FET Noise

The three noise sources discussed in section 2.6 are the thermal noise due to R_{IN}, the input current noise generator i_n and the voltage noise generator e_n. The latter two sources are due to the input amplifier that is the subject of the present discussion. The current noise term has already been encountered and is generally assumed to be due to the shot noise of the input bias current. The voltage noise, though so far discussed only as an input-referred voltage source, is an output parameter of the amplifier.

The significant contributions to the voltage noise of a FET transistor originate in the channel. Though several distinct noise sources have been identified in the literature, two are predominant; the thermal noise of the resistive channel, and the 1/f, or flicker noise.

The thermal noise term e_{nt} is due to the resistive channel, the spectral density of which is given by the approximate relation;

$$e_n \cong \sqrt{4kT\frac{0.67}{g_{fs}}} \tag{4.1}$$

(Siliconix Inc., 1981) where g_{fs} is the forward transconductance of the device. The flicker noise term increases the total output noise at frequencies below the corner frequency, f_{FL}, which can be represented by the empirical relation for total output noise spectral density;

$$e_n \cong \sqrt{\left(4kT\frac{0.67}{g_{fs}}\right)\left(1+\frac{f_{FL}}{f^n}\right)} \tag{4.2}$$

where f is the measurement frequency. The exponent n is between 1 and 2 and is device and lot dependent, with f_{FL} between $100\,Hz$ and $1\,kHz$ for JFET devices (Siliconix Inc., 1981), and somewhat higher for common MOS devices.

The underlying causes of flicker noise have not been satisfactorily determined, though it is generally accepted that it is the product of both fundamental processes and manufacturing quality (Lundberg, 2002). The empirical relation given above is rightly frowned upon by some researcher since it cannot predict the flicker noise term for a given device. A full discussion of flicker noise is well beyond the scope of this text; suffice it to say that the noise corner frequency of MOS devices is generally much higher than in Junction devices (Buttler et al., 1989).

4.2.4 Device selection: optimising EPS signal to noise ratio with FET devices

The device parameter which is of principal importance in determining the input parameters of a high impedance FET amplifier is the gate area, defined by the gate dimensions W and L, so that $A = W \times L$. Excluding all second order effects, some of which have been discussed above, then the following relations can be defined;

$$I_G \propto A$$

$$C_{in} \propto A$$

$$g_{fs} \propto A$$

$$e_n \propto \frac{1}{A}$$

Low gate leakage and input capacitance, and hence high input impedance, is achieved with a small gate area. Low noise is obtained by high forward transconductance, and hence large gate area. The choice of a MOSFET device over a JFET results in further reduction of gate leakage than is possible with simple gate area scaling of JFET devices. This comes at the cost of increased voltage noise. Since the signal amplitude is a function of the source and input impedances, then the optimum signal to noise ratio is achieved for a given application (i.e. source impedance) by selecting the most appropriate compromise between input impedance and noise performance.

For MOSFET devices the relationship between the 3 noise components discussed in section 2.6 and demonstrated in section 3.5.2 for a JFET input op-amp, is almost completely overturned. Previously, it was found that the voltage noise term is only significant at high frequencies, and at low frequencies the thermal and current noise terms dominate. With a low-leakage MOS device the current noise term is negligible—a generalisation that is made safe by the fact that the low-frequency voltage noise term is much larger. With input resistance of around 1 $T\Omega$, then the voltage noise in the 1/f region of a low-leakage MOSFET is commonly in excess of the thermal noise of even this large resistance. This increased voltage noise term erodes the benefit of the very

low leakage MOS device, and so an advantage is only obtained over JFET or low-noise (large gate area) MOS devices when particularly high impedances (greater than $1\ T\Omega$) are required. At such high impedances a low-noise (high-leakage) device would suffer from excessive current noise and DC offset.

The terms 'low-leakage' and 'low-noise', as applied to FET devices, are generally used in marketing literature to indicate the intended application of a particular device. According to the 3 basic relations given above, it can generally be assumed that a low-leakage device has small gate area, and hence low gate leakage and input capacitance, at the cost of increased noise. The opposite is true of low-noise devices, where a large gate area achieves low noise at the cost of high gate leakage and input capacitance. A third category of MOS devices are marketed as suitable for radio frequency (RF) applications. These are designed to offer low input, feedback and output capacitances, and as such these parameters are well defined in the device datasheets. This performance is once again typically achieved with small gate area and/or a thicker gate oxide. Such a device therefore performs similarly to a low-leakage device. Amplifiers built with low-leakage or RF devices therefore tend to offer very high input impedance, though with relatively high noise. The end result is a quite acceptable signal to noise ratio when the source impedance is very large. Such an amplifier is therefore suitable for ultra-low capacitance applications.

For applications where the source impedance is lower ($100\ G\Omega$ or less) then a larger input leakage current and input capacitance can be tolerated. When this is the case then a more general purpose or low-noise device can be used, with the benefit of improved forward transconductance and lower noise. This benefit is only valid when the input bias current is not so large that its associated current noise dominates over the thermal noise term.

4.3 Several FET input stage designs

With some of the relations between FET input performance and the biasing and circuit conditions defined above, a selection of circuits which maximise the input impedance of the sensor can be discussed. These circuits have been developed by the author as part of the investigation into high impedance amplifiers, and in response to the theoretical understanding of EP sensors that was developed and is described in earlier chapters.

A high impedance amplifier is an inherently noisy device when compared to low impedance, low-noise amplifiers, and so by removing the requirement of high gain from the input stage the design goals can be focused on high impedance with relatively low noise with little detriment to overall system noise. If high gain is required it can be provided by a following gain stage, since the additional noise of this gain stage can be expected to be negligible compared to that of the high impedance input stage.

4.3.1 Source follower circuits

A source-follower, or common drain, circuit offers gain of close to unity with high input impedance—defined by the input (gate) parameters of the FET device—and low output impedance. The basic source-follower amplifier is shown in Figure 4-3. The FET is biased by the source resistor R_S, which develops a voltage drop according to I_D and so sets the quiescent gate-source voltage V_{GS}. The dual supplies allows the signal to swing between *approximately* $-V_{SS}$ and V_{DD}. With appropriate selection of R_S the device operates in saturation and $v_o \approx v_i$ (note that there is no phase inversion). For an AC coupled amplifier, the quiescent output voltage V_o is equal to V_{GS} assuming that the product $I_G R_{IN}$ is negligible.

This circuit serves as a replacement to the op-amp included in the EPS equivalent circuits given earlier, such as that in Figure 2-8. The input resistor R_{IN} is identical to the input resistor R_{IN} of the EPS circuit. The input resistance will therefore be defined by this component, and it may be bootstrapped as before. The value of R_{IN} must be chosen so that the product $I_G R_{IN}$ results in a tolerable DC offset - strictly this offset must be

less than V_{DD} or $-V_{SS}$, though in practice it is often desirable to have a much smaller offset.

By considering the small-signal equivalent circuit the input capacitance can be obtained in terms of the device capacitances C_{gs} and C_{gd}. Since the drain terminal is at small-signal ground, and $v_s \approx v_g$, then $C_{in} \approx C_{gd}$. In order to refine this approximate expression, it is necessary to examine the transfer characteristics of this circuit. If the output conductance is assumed to have negligible effect and there is no output load, then the voltage gain can be expressed as

$$A_v = \frac{v_o}{v_i} \approx \frac{R_S}{\frac{1}{g_{fs}} + R_S} \tag{4.3}$$

where g_{fs} is the forward transconductance of the device. Voltage gain is therefore always somewhat less than 1. The gain error can be written as $1 - A_v$, giving

$$1 - A_v \approx \frac{1}{g_{fs}R_S + 1} \tag{4.4}$$

The expression for input capacitance therefore becomes

$$C_{in} \approx C_{gd} + \frac{C_{gs}}{g_{fs}R_S + 1} \tag{4.5}$$

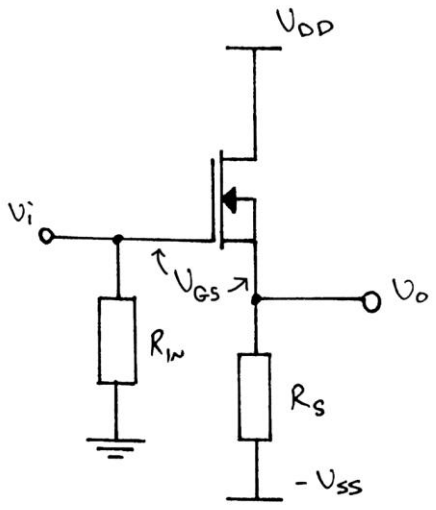


Figure 4-3: Source follower circuit with resistor biasing and n-channel depletion MOS as the input FET.

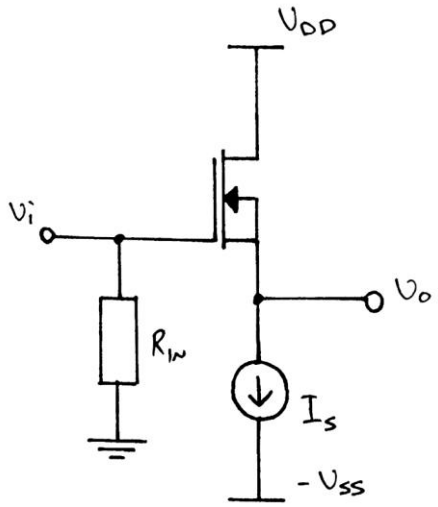


Figure 4-4: Source follower circuit biased by the ideal current source I_S.

and it is seen that the input capacitance retains a contribution from C_{gs} that is proportional to the gain error of the source follower. For a fairly typical RF MOS device with $C_{gs} = 10pf, C_{gd} = 5pf$ and $g_{fs} = 10\ mS$, then with a $1k\Omega$ source resistance the gain is;

$$A_v = 0.909 = -0.82\ dB$$

and the input capacitance is;

$$C_{in} = 5\ pF + (0.09 \times 10\ pF)$$

$$C_{in} = 5.9\ pF$$

4.3.2 Current source biasing

In Figure 4-4 the source biasing resistor has been replaced by the ideal current source I_S. The load impedance of this current source is infinite, and therefore the gain error of equation 4.4 is reduced to zero. Consequently the contribution of C_{gs} to the input capacitance is removed, and so this circuit achieves an improved input impedance as compared to the resistor biased source-follower.

Constructing real current source circuits which approximate the behaviour of the ideal circuit element I_S brings its own set of compromises and complications. In Figure 4-5

the JFET Q2 is used as a current source to bias the input MOS Q1. An equivalent MOS device could be used in place of Q2. The gate of Q2 is connected to its source, so that $I_D = I_{DSS2}$. A variety of circuits can be used to set the biasing current for Q1, including this simple FET, a FET with an additional source resistance to set I_D, or a bipolar or CMOS current mirror. The current source Q2 must be operated in saturation in order to approximate an ideal current source. This sets a limit on v_o of the circuit, since v_o is equal to the drain-source voltage of Q2, V_{DS2}. Since V_{GS2} is equal to zero for the circuit shown, then the condition for saturation is simply;

$$v_o > -V_{SS} - V_{t2} \tag{4.6}$$

where V_{t2} is the threshold, or turn-on voltage of Q2. Below this output voltage, the circuit no longer functions as a linear amplifier. The output resistance of this current source, R_O is finite, and is a function of Q2's output conductance g_{oss2}.

$$R_O = r_{o2} = \frac{1}{g_{oss2}} \tag{4.7}$$

An expression for the voltage gain error can now be written by replacing R_S of equation 4.4 with the output resistance of Q2

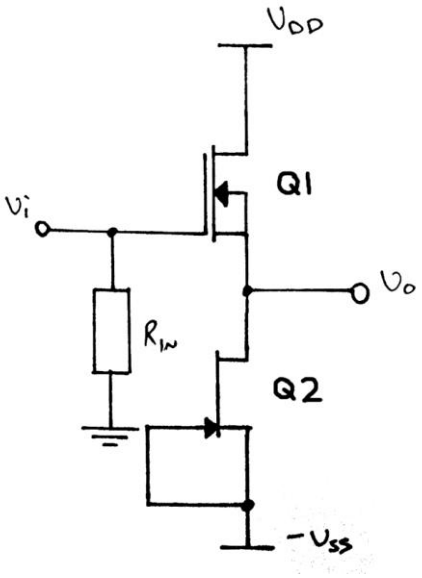


Figure 4-5: Source follower circuit biased by the JFET current source Q2.

$$1 - A_v \approx \frac{1}{\frac{g_{fs1}}{g_{oss2}} + 1} \tag{4.8}$$

The expression for C_{in} is now

$$C_{in} \approx C_{gd} + \frac{C_{gs}}{\frac{g_{fs1}}{g_{oss2}} + 1} \tag{4.9}$$

Revisiting the example circuit given earlier, and replacing the 1 $k\Omega$ source resistance with a FET current source with output conductance $g_{oss} = 10\ \mu S$, then the voltage gain is,

$$A_v = 0.9990$$

which corresponds to a gain error of around 0.1%. The total input capacitance is then;

$$C_{in} = 5\ pF + (.001\ \times 10\ pF)$$

$$C_{in} = 5.01\ pF$$

The example value of g_{oss} chosen here corresponds to a long-channel transistor which is well suited to serve as a current source. The output conductance of a FET is a function of the device geometry and operating point. g_{oss} reduces approximately linearly with drain current I_D (Vishay Siliconix Inc, 1997). For best output conductance then, I_D should be less than I_{DSS}. Long-channel devices should be chosen to prevent the short channel effects which reduce output conductance (Sedra and Smith, 2004).

The reduced loading of the output of the source-follower amplifier has been shown to reduce the contribution of the gate-source capacitance to the total C_{ig} of the FET to near zero. In order to retain this benefit, then the external load to the amplifier, which in most cases will be the next stage of amplification, should present a high impedance to the amplifier. The contribution of any external load to the gain of the source-follower circuit can be calculated by adding a load resistor R_L in parallel with the output resistance of Q2.

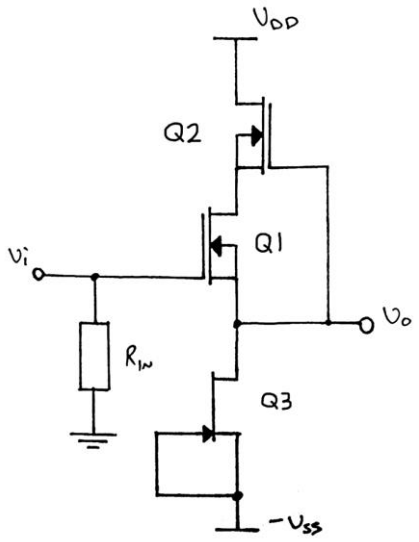


Figure 4-6: Cascode common-source amplifier

4.3.3 Cascode circuits

The cascode configuration (a contraction of the vacuum tube terms cascade and cathode) has been used in a variety of embodiments to produce high performance amplifier stages. The cascoded common-source circuit is well known to circuit designers and is described in several standard texts (Sedra and Smith, 2004). Here, the cascoded source follower circuit will be described since it has been found to produce high performance EPS circuits.

In Figure 4-6 a cascoded source follower circuit is shown, where the input FET Q1 is cascoded by Q2, with the quiescent drain current I_D set by the low output conductance JFET, Q3. This circuit is only suitable for either N-channel depletion MOS or N-channel JFET devices which allow channel conduction at negative gate-source voltages; however, variations of this circuit may be appropriate for other device types.

The common-gate amplifier Q2 effectively bootstraps the drain of Q1 to its source terminal. In section 4.3.2 it was shown that the contribution of C_{gs} to the total input capacitance C_{in} can be reduced to almost zero by ensuring that v_s is equal to v_g. By cascoding the input FET Q1, then its drain terminal is also at an AC potential v_d that is close to v_g, ensuring the contribution of the gate-drain capacitance C_{gd} to the total input

capacitance C_{in} is also reduced. The contribution of C_{gd} and C_{gs} are now both reduced so that the expression for input capacitance becomes;

$$C_{in} \approx \left(C_{gd} + C_{gs}\right) \times \frac{1}{\frac{g_{fs1}}{g_{oss3}} + 1} \qquad 4.10$$

where C_{gd} and C_{gs} are values for the input device Q1. The input capacitance of the FET device used in the earlier example is now reduced to 15 fF, so that its input capacitance is likely to be negligible compared to the capacitance due to the circuit board and other parasitics. As with guarding, the intrinsic values of C_{gd} and C_{gs} do however remain present in the noise model of the FET, and so when configured as a cascode these capacitances have the undesirable property of providing feedback of voltage noise to the input. As such, some of the benefits of the extremely low input capacitance are eroded by the increase in voltage noise.

In addition to reducing input capacitance, the cascode configuration also reduces V_{DS} of the input FET. This has the desirable property of reducing I_G, particularly for JFET devices where a large V_{DS} can result in excessive input current when V_{DS} exceeds the gate-current breakpoint. When Q1 and Q2 are matched devices, then

$$V_{DS1} \cong -2V_{GS1}$$

so that Q1 is always operating in drain-current saturation. Large signal behaviour is limited since there are now 2 devices in series with the positive power rail. When Q1 and Q2 are matched devices, the maximum gate voltage permitted for linear amplification is

$$V_{G(\max)} = V_{SS} - 2V_{th}$$

where V_{th} is the threshold voltage of the MOS device ($V_{GS(off)}$ can be substituted for V_{th} in this expression when JFET devices are used). This is twice the value as that for the single stage source follower circuit.

The low V_{DS} of Q1 has the additional undesirable effect of reducing the forward transconductance g_{fs}, which will serve to reduce the gain and hence increase input

capacitance, as well as increasing the channel voltage noise. As such, V_{GS} should be chosen to ensure sufficient V_{DS} for a satisfactory transconductance, and also the need for high load impedance is reinforced.

Dual-gate MOSFET devices integrate two separate gate electrodes on a single channel, so that a single dual-gate device can replace the FETs Q1 and Q2. These devices are typically employed in RF applications where the upper gate is used to provide automatic gain control. Such RF devices are particularly suitable for cascoded ultra-low capacitance EPS circuits with the dual-gate structure principally delivering a benefit in terms of packaging and component count, whilst the intended RF application generally indicates that the device will have low input capacitance.

4.3.4 Differential high gain input stage

Where gain is desired in the input stage, then a differential long-tailed pair (LTP) configuration is an attractive option since it provides conveniently configurable closed-loop gain and increased linearity through the use of negative feedback. When constructing such a circuit from discrete devices, it is convenient to use an IC op-amp as the second differential stage after the discrete LTP input. This configuration, referred to as the composite op-amp by some (Jung, 2002), combines the benefits of the discrete input stage with the high gain and low output impedance of the IC op-amp. The circuit of Figure 4-7 uses a discrete cascoded LTP amplifier with dual-gate MOS input devices biased by a JFET current source. This circuit retains several of the benefits of the previous cascoded source-follower, though with a somewhat degraded input capacitance, and voltage noise term increased by a factor $\sqrt{2}$. Since input performance is defined by the discrete FET stage, the op-amp used can be a low cost general purpose device.

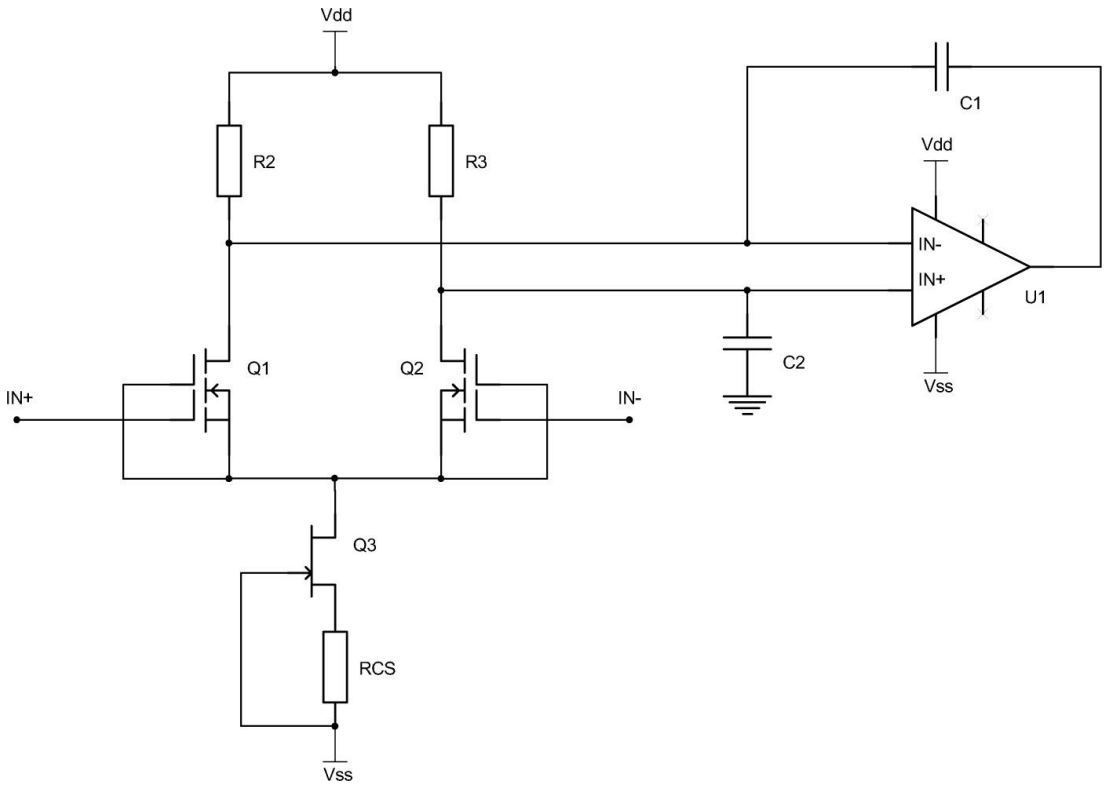


Figure 4-7: Simplified schematic for a differential-input composite op-amp with ultra high input impedance provided by the input FETs Q1 and Q2.

The non-inverting half of the differential input stage can be analysed as a common-source amplifier. If the dual-gate MOS is considered as two separate devices, then the drain of the lower gate FET, gate 1, is shared with the source terminal of the upper gate FET, gate 2. The contribution of C_{gs} to C_{in} of the input FET is reduced by a factor equal to the gain error between gate and drain terminal, though the gate-drain capacitance C_{gd} is not reduced since the AC potential at the drain terminal seen by gate 1 is approximately zero. As a result C_{in} is approximately equal to C_{gd} of the input FET. The benefit of the cascode connection in this common-source amplifier seems reduced compared to the earlier analysis of the source-follower, however, in this case the cascode FET has the important benefit of reducing the large miller capacitance that would be seen by the input FET if it were not cascoded. This miller capacitance is the result of the inverting gain between gate and drain terminals in a common-source amplifier. Without the cascode this miller capacitance results in a contribution to C_{in} of the gate-drain capacitance C_{gd} multiplied by the amplifier gain.

The input gain provided by this circuit ensures that the noise contribution of subsequent amplification stages is negligible compared to the input stage noise. Since ultra-high input impedance input stages are inherently noisy, the high-gain input stage is only necessary when low noise input devices of moderate input impedance are used. An example of such an amplifier would be a low-noise JFET input stage designed for an input impedance of tens to hundreds of Giga-Ohms and with pico-Farad input capacitance, for contact EPS applications. Since this level of performance can be achieved with a low-leakage op-amp device alone, then the benefit of the composite design may only be in cost saving since low-leakage discrete JFET devices are generally less costly than a low-leakage IC op-amp. Nonetheless, the differential input stage developed here may be of use in integrated sensor designs.

Global negative feedback removes the DC offset due to the input FETs V_{GS} that causes an output offset in single ended devices. Additional offsets due to input device mismatch and input bias current can be removed be balancing the input stage current across each half of the LTP.

4.3.5 Conclusions

The circuits presented here have been ordered in a logical fashion to aid the readers understanding, though this indeed approximately matches the chronology of the development work undertaken by the author. The circuit presented in Figure 4-6 represents the ultimate development of a single-ended discrete EPS input stage design that was reached during this work, and so is the design employed in the vast majority of experimental work described later in this thesis. This design is generally more applicable than the differential input stage described above since only a single-ended high-impedance input is generally required and the single-ended stage offers lower noise by design. These later chapters will provide experimental evidence that shows this design to be superior in delivering ultra-low input capacitance with low noise than previous EPS designs.

4.4 Design of proceeding stages for cascoded source follower circuits

The single ended source follower circuits described earlier have a DC offset at the output that is equal to the quiescent gate source voltage V_{GS} (assuming no additional offset due to the input bias current flowing across the input impedance). This offset will generally have to be removed before subsequent analogue amplification or signal processing. The qualifier analogue is added since the problem is not so severe when the input stage is followed almost directly by a high-resolution data converter, since the offset can simply be removed in software. When this offset must be removed two approaches may be taken; a DC level shift may be applied, or the output may be AC coupled to subsequent stages. Each approach has its own advantages and disadvantages.

Level shifting retains true DC sensitivity and is simple to implement. However, the tolerance of the input stage FETs, including the biasing current source, means that DC level at V_{OUT} can be expected to vary dramatically from device to device. As such the DC level shift requires trimming after manufacture. Additionally, full DC coupling has

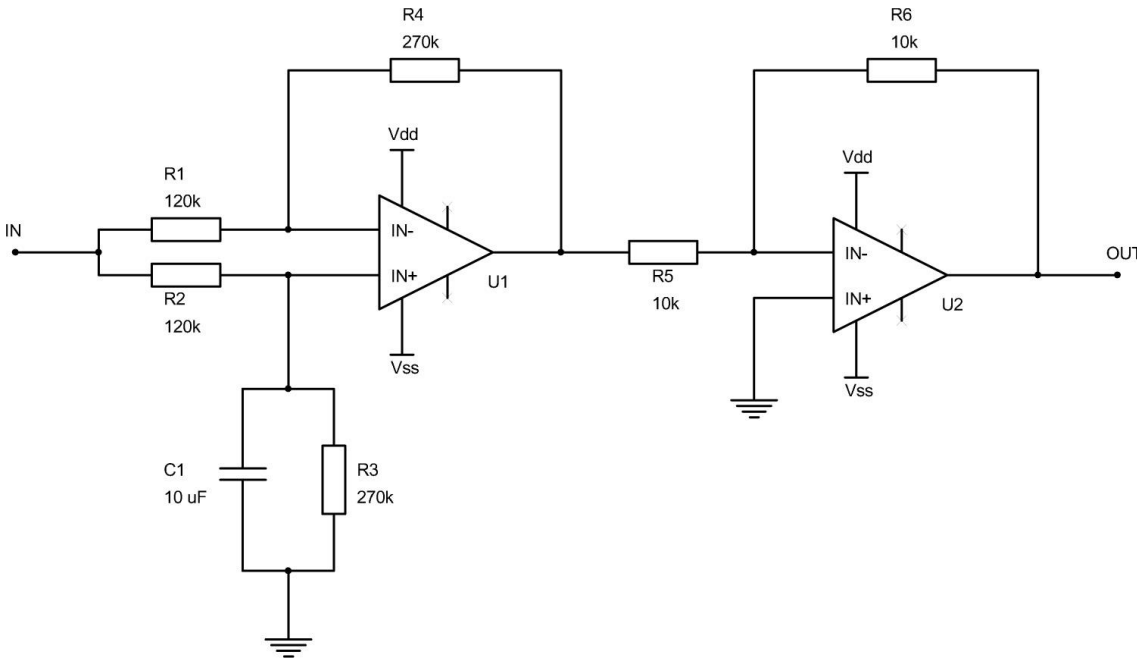


Figure 4-8: An AC-coupled signal conditioning circuit for a source-follower EPS input stage.

its own disadvantages; the large 1/f noise component at low frequencies that is produced by MOS devices is not attenuated, which due to the very low frequencies involved will simply appear as poor DC stability. AC coupling of the input stage guarantees low output offset regardless of input device variation, and also attenuates the low frequency noise. In addition, the AC coupled output provides a convenient signal for the bootstrapping of R_{IN}, should it be required. The downside of AC coupling is in the implementation; where low frequency response is desired then capacitor values quickly become very large—especially when the requirement of very long time constants for effective bootstrapping is included. The large valued capacitors required for sub-Hz response are at best costly and space-hungry in PCB designs, and completely impractical for CMOS designs. Nonetheless, an AC-coupled circuit remains the best compromise for PCB based discrete designs, an example of which is presented in Figure 4-8.

The AC-coupled circuit presented here provides an overall non-inverting gain of around 7 dB, with the AC coupling time constant set by $C1 \times (R2 \,||\, R3)$. The small amount of inverting gain provided by the op-amp U1 is sufficient to allow the limited large-signal swing of the cascoded source follower circuit to saturate the output stage of U1, so that the large-signal performance of U1 becomes the limiting factor. U2 provides a simple inversion of U1's output so that the overall gain is non-inverting. Additionally, U2 can be reconfigured to provide additional gain or include a low-pass filter.

The source follower circuits described earlier require a high load impedance in order to guarantee close-to-unity gain and hence low input capacitance. The value of this load impedance should be chosen so that it is not significantly less than the load set by the current source. The load impedance of this current source is $1/g_{oss}$ where g_{oss} is the output conductance of the current source FET device. For the typical values explored earlier, this current source has an impedance of $100\ k\Omega$, and so the input impedance of the subsequent stage should be greater than or equal to this value. The circuit of Figure 4-8 has an input impedance (above the high-pass corner frequency) set by the parallel combination $R1 \,||\, R2$. The value of these resistors must be balanced against their

thermal noise contribution. Where a higher load impedance is required than can be easily achieved through scaling R1 and R2, then an additional buffer stage should be added after the input stage, either as an op-amp voltage follower or a source- or emitter-follower stage.

4.5 Power Supply Modulation: a method for increasing dynamic range

In remote sensing applications external noise potentials can be orders of magnitude larger in amplitude than the desired signal. This is the case in remote cardiology measurements (chapter 5.2), where a large electric field at the local power line frequency (which is usually 50 or 60 Hz) is found in domestic and industrial environments, and is generally much large in magnitude than the signal due to cardiological activity. Such noise signals can be effectively filtered from the sensor output signal, as long as the noise signal does not cause the sensor to saturate. Saturation of the sensor can be avoided by reducing the overall sensitivity. However, this reduction of sensitivity may not result in an associated reduction in the electrical noise of the sensor, and so the signal to noise ratio is reduced. A proposed solution then is to increase the large signal swing of the sensor without affecting the sensor noise, so that large environmental noise signal can be accommodated at the original sensitivity, and without saturating the sensor output.

The signal swing of an amplifier can be improved by increasing the power supply rails to a higher voltage. Typical EPS circuits operate on symmetric supplies that are in the range of $\pm 2.5\,V$ to $\pm 15\,V$. Simply increasing the value of these rails is not possible - both IC op-amps and small-signal discrete transistor devices that deliver high impedance performance are not high voltage tolerant. Instead, power supply modulation

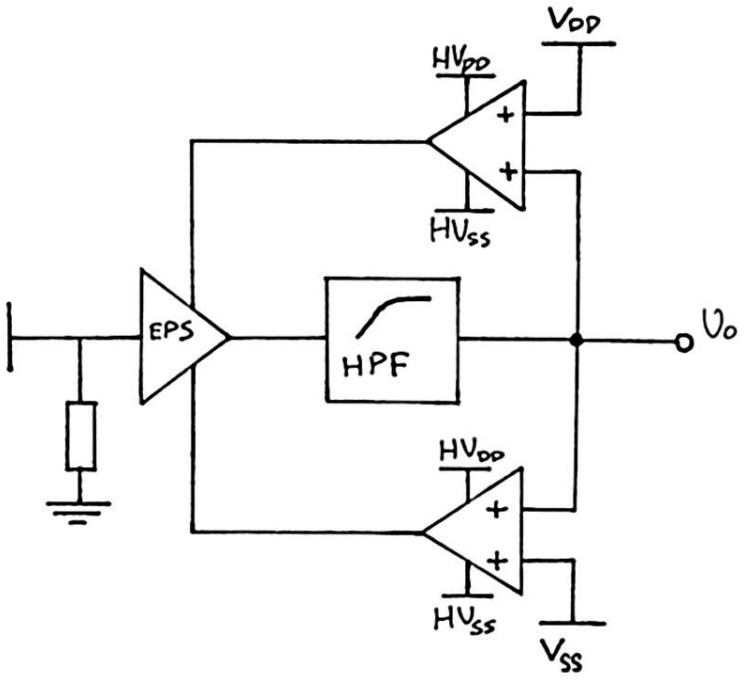


Figure 4-9: Block diagram of a power-supply modulated EPS sensor.

is presented here as a technique for increasing the large-signal swing of low voltage EPS devices.

In Figure 4-9 the conventional low voltage, unity-gain EPS is powered by the output of the two high-voltage summing amplifiers. The two amplifiers produce an output voltage that is the sum of the low voltage supply rail, V_{DD} and V_{SS} respectively, and the high pass filtered sensor output voltage. Large signal excursions are therefore accommodated by the low-voltage EPS since its power supply voltage follows its output. The ground reference of the circuit is maintained by the input resistor and the high pass filter. High impedance performance is therefore defined by the EPS input stage, as before, with large swing capability provided by the high voltage amplifiers.

A prototype EPS sensor was produced which consists of a low-voltage FET-based EPS input stage, and a high voltage amplification stage for derivation of power supply rails. This latter stage consists of a discrete op-amp style amplifier with differential input stage, voltage amplification stage, and dual output stages for generating each power supply rail. Schematics for this circuit are given in Appendix A.

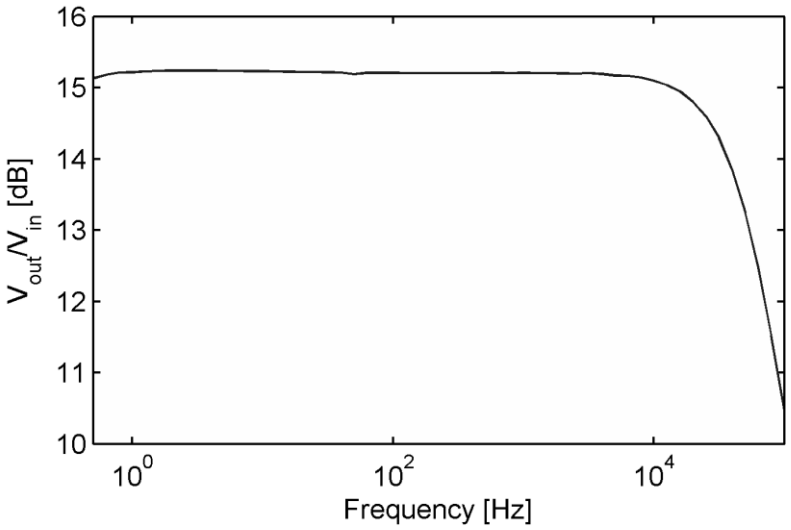


Figure 4-10: Measured frequency response of PSM power driver stage at an output voltage of 60 V_{pp}

The high voltage amplification stage has ±45 V power supply rails. Figure 4-10 shows the large-signal frequency response for this stage with a $60\,V_{pp}$ signal swing on the positive rail output. The power supply modulation action allows the input EPS to achieve identical large signal performance. In Figure 4-11 the frequency response of the whole system through a 100 fF test capacitor is shown.

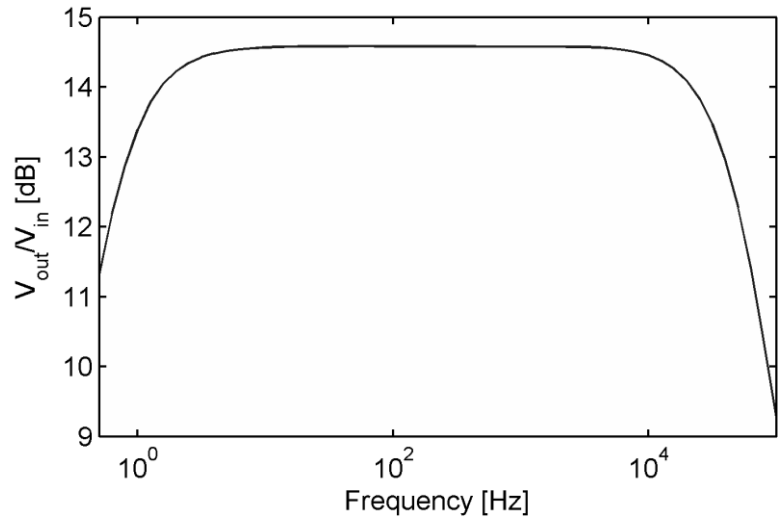


Figure 4-11: Measured frequency response of PSM EPS with a 100 fF test capacitor

5 ULTRA LOW CAPACITANCE SENSORS; CHARACTERISATION AND RESULTS

5.1 Characteristic measurements on a FET based EPS

The procedures detailed in chapter 3 have been used to characterise a MOSFET cascode EPS input stage based on the circuit of Figure 4-6. This prototype sensor is assembled on an FR-4 PCB, with a 'flying-lead' input construction similar to the AD549 based

		Min	Typ	Max	Units
V_{DS}				20	V
I_D				20	mA
g_{fs}	f = 1 kHz, I_D = 10 mA, V_{DS} = 10 V V_{G2-S} = 4 V		14		mS
C_{ig1-s}	f = 1 MHz, I_D = 10 mA, V_{DS} = 10 V V_{G2-S} = 4 V		2.1		pF

Table 5-1: BF981 data sheet specifications (Philips/NXP semiconductors, 1990)

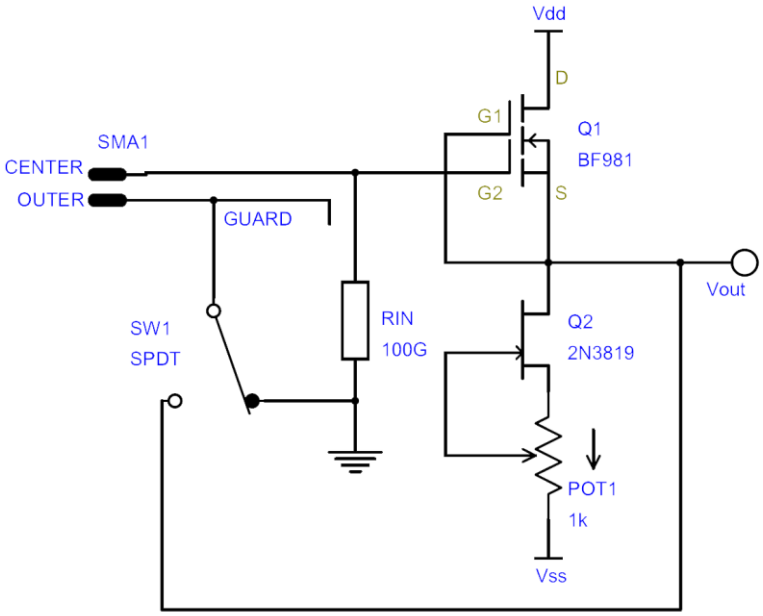


Figure 5-1: MOSFET EPS test circuit

sensor described earlier. The input is again terminated with a coaxial SMA so that calibrated test capacitors and other signals may be connected. The input device is a dual-gate MOS from NXP semiconductors (formerly Philips), the BF981. This device is supplied in a discrete 4 lead package, and though now discontinued the similar BF998 is currently available in a 4-lead SOT143 package. These are N-channel depletion mode devices with high g_{fs}/C ratio and integrated ESD protection diodes, and so are well suited to EPS applications. A subset of the device specifications are given in Table 5-1 for the BF981 device.

The schematic for the prototype sensor is given in Figure 5-1. A 100 $G\Omega$ surface mount resistor has been used as R_{IN}. Q2 is a 2N3819 JFET device, with adjustment of the drain current provided by a 1 $k\Omega$ potentiometer. Guarding is provided by direct connection to the output of Q1. A switch allows the guard circuit to be shorted to ground. Experiments have been performed with $V_{DD} = -V_{SS} = 10V$. V_{GS} has been set at approximately $-0.2\,V$ for a large drain current close to I_{DSS}, and where good transconductance is offered according to the curves given on the datasheet.

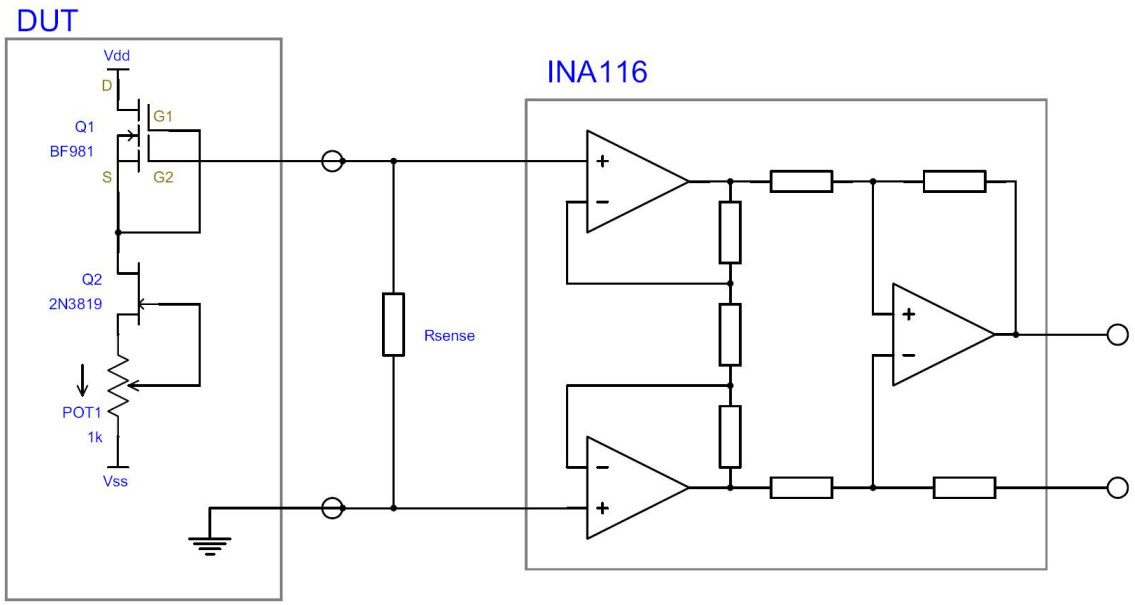


Figure 5-2: Input bias current measurement circuit.

5.1.1 Input bias current

Input bias current can be easily measured for any EPS circuit by simply comparing the output offset voltage when the input is respectively shorted to ground, and left open circuit. The change in offset voltage is related to the input bias current by the value of the input resistor R_{IN}. In some cases this technique is not appropriate, particularly for high accuracy measurements. First, the value of R_{IN} must be known precisely. Second, a DC coupled, preferably high gain, output from the EPS must be available. In the present case, measurement of small offset currents using this method is particularly difficult since the amplifier is a low gain device, and has a significant DC offset which complicates the addition of high DC gain to the output. A 1 fA input bias current would require the ability to measure a DC offset with better than 0.1 mV resolution. Instead, highly sensitive current measurements can be achieved with the circuit of Figure 5-2. This circuit has two significant benefits: first it has high DC gain; and second it is more convenient as a reusable measurement circuit since it does not require recalibration (of R_{SENSE}).

An ultra-low input bias current instrumentation amplifier (in-amp), INA116, is used with a 1 $T\Omega$ resistor for R_{SENSE} to measure currents with better than 0.01 fA resolution.

V_{GS}	V_{OPEN}[mV]	V_{MEAS} [mV]	ΔV [mV]	I_{MEAS} [fA]
+0.20	-150	-7450	-7300	**-73.0**
+0.10	-150	-1800	-1650	**-16.5**
+0.05	-150	-580	-430	**-4.30**
0.00	-150	-230	-80	**-0.80**
-0.10	-150	-135	+15	**+0.15**
-0.20	-150	-115	+35	**+0.35**

Table 5-2: Input bias current results. V_{OPEN} is the open circuit output voltage from the measurement circuit.

The INA116 is configured with a DC voltage gain of +100 V/V to give an output scaling of $10\ fA/V$ with the $1\ T\Omega$ sense resistor. The Device Under Test (DUT) is the MOSFET EPS test circuit with R_{IN} removed. If R_{IN} is not removed then it is in parallel with R_{SENSE} and changes the scaling factor. Using the full EPS test circuit allows the MOS device to be tested under the intended power supply and biasing conditions. The DC output of the in-amp is first measured with the DUT removed from the circuit so that the DC output due to the in-amps own input offset voltage and input bias current can be measured. The additional offset, ΔV, measured with the DUT added gives the input bias current by applying the scaling factor $10\ fA/V$. The in-amp provides high impedance differential inputs so that currents can be measured when neither of the measurement terminals are grounded. Even in this single ended measurement, the differential input provides high common mode rejection of noise. The $1\ T\Omega$ resistor used here, a ±20% tolerance part, has been measured on a HP model 4329A high impedance resistance meter as $1.0\ T\Omega\ \pm 5\%$ at a 10V test voltage.

Some care is necessary when measuring currents in the femto-amp range. First, a screened enclosure is used and short, rigid connections are made between the DUT and test circuit. The entire input area of both the INA116 test circuit and the DUT is cleaned with isopropyl alcohol. A warm-up time of around 10 minutes is allowed after applying power to the test circuit to allow the bias currents of both the DUT and measurement circuit to settle. Though it should not vary too greatly, the open-circuit offset voltage of the test circuit should be periodically checked.

Input bias current has been measured for the MOSFET EPS circuit at several values of quiescent gate source voltage V_{GS}. The results are presented in Table 5-2, and the I-V characteristic plot is given in Figure 5-3. A positive input bias current is defined here as one which flows *out of* the gate terminal.

Under depletion biasing (negative V_{GS}) very low input bias currents are obtained. At a small negative V_{GS} the forward and reverse leakage currents balance so that the input bias current is zero. The precise value of V_{GS} at which I_B is zero can be expected to vary between devices and also as a function of device temperature and drain voltage. Biasing for zero I_B is therefore not recommended, and instead a negative gate-source voltage of a few tenth's of a volt should be chosen to give a low bias current across a wide range of circuit conditions.

From this measurement alone, of a single device with integrated protection diodes, it is impossible to draw any conclusions about the underlying cause of input bias current. It is also impossible to determine if the leakage current path is resistive or due to a reverse biased diode; knowledge of which would allow an estimate of current noise.

It is possible though to conclude that under normal depletion biasing conditions, i.e. with negative V_{GS}, that the gate leakage current of this BF981 MOS device is very low indeed, much lower than the best JFET input op-amps which are marketed as ultra-low input bias current parts. This is most important in EPS applications since it implies low current noise. In addition, whilst it has not been possible to discriminate between

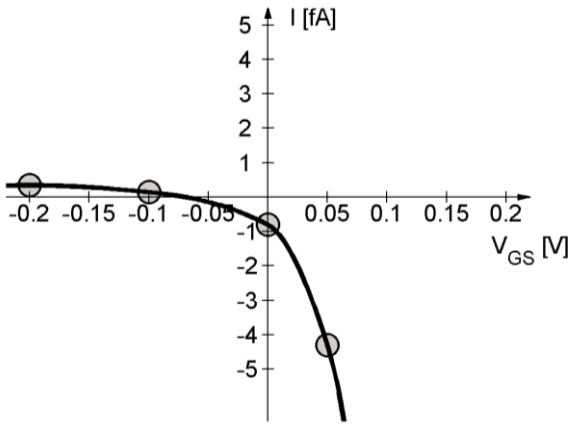


Figure 5-3: I-V plot for BF981 input bias current versus gate-source voltage. The data points are connected by a best-fit line.

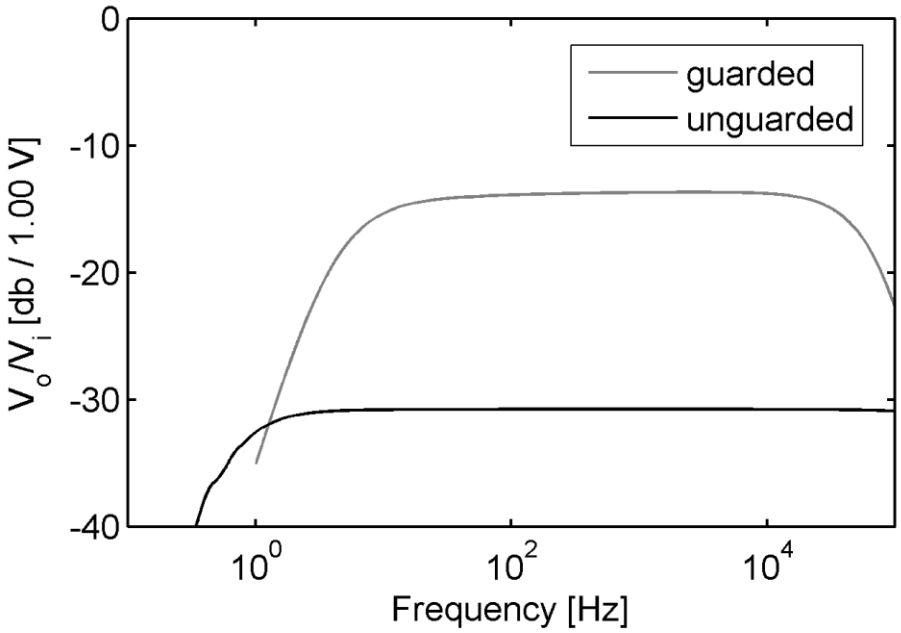


Figure 5-4: Frequency response through $C_C = 0.1\,pF$ for both guarded and unguarded configurations

protection diode leakage and true gate-channel leakage, the conclusion that this current is low is nonetheless encouraging for future integrated EPS IC designs, especially since the BF981 device is not ultimately intended for ultra low leakage applications. This last comment of course implies the dangerous assumption that the results for a BF981 discrete MOS device may be extended to all MOS devices, be they discrete devices, integrated on CMOS or another process, enhancement or depletion mode, and whether they include protection diodes or not.

5.1.2 Frequency response and input impedance

Frequency response has been measured in accordance with the methods outlined in chapter 3. A 0.1 pF test capacitor has been used for C_C. The MOS EPS circuit has been tested under the guarded and unguarded configurations under the control of the switch

	$A_{V,mid}$ dB	f_c Hz	C_{IN} pF	R_{IN} GΩ
Unguarded	-30.75	0.73	3.35	62.7
Guarded	-13.68	6.42	0.38	51.2

Table 5-3: Input impedance derived from Figure 5-4

SW1. The frequency response plot is given in Figure 5-4, with the derived input impedance in Table 5-3.

With guarding disabled, and the area around the input (including the test capacitor case) connected to ground, input capacitance is low at $3.35\,pF$. It immediately seems likely that the majority of this capacitance is due to the SMA connections, which are known to have a capacitance between inner and outer of several pF. Indeed, this hypothesis is proved correct when guarding is applied to the outer of the SMA and test capacitor case, as input capacitance drops significantly to $0.38\,pF$. This guarded input capacitance reveals the true input capacitance of the MOSFET cascode, though it may also include a small contribution from additional parasitic capacitances outside of the MOS device. Nonetheless, this value will be used in further modelling of noise performance.

The measured value of R_{IN} is lower than expected from the ±20% tolerance $100\,G\Omega$ part. Worthy of note is the slope across the mid band gain of the guarded circuit. This is due to the slight frequency dependence in the gain of the source-follower circuit. This non-linearity might not be apparent in conventional amplifier circuits, but the small gain error results in a more significant effect on the closed loop guard circuit. The input capacitance given in Table 5-3 is measured at 1 kHz, though at lower frequencies the input capacitance of the guarded circuit is slightly higher. This also explains the mismatch in R_{IN} between guarded and unguarded sensors, where it should be the same. The guarded sensor result for R_{IN} is incorrect since the capacitance value at 1 kHz has been used to calculate R_{IN} at the corner frequency, where in fact the capacitance here is somewhat larger.

High frequency performance is good for a low input capacitance sensor, with a -3db upper roll-off of 50 kHz for the guarded sensor with $0.38\,pF$ input capacitance. This limit is most likely set by the output drive capability of the source follower circuit. An output buffer would be required in order to test the bandwidth limits of the input section.

5.1.3 Noise

The noise measurement protocol has been followed as described in chapter 3. In summary, noise is measured at the output of the MOS circuit with a high-gain, low noise pre-amplifier and a power spectral density computed from a digitized time-domain recording. Voltage noise is measured with the input shorted to ground, and total output noise is measured for the guarded and unguarded configurations with a test capacitor terminating the input to ground. The noise model of section 2.6 has been used to calculate expected noise curves for comparison with the measurement.

In Figure 5-5 the measured voltage noise e_n (light grey) is shown along with a fitted voltage noise curve (blue dashes). This fitted curve is based upon the empirical equation for FET voltage noise given in section 4.2.3 as equation 4.2. The fitted curve is based upon a thermal channel noise of $20\,nV/\sqrt{Hz}$ (verified by a noise measurement extending to 100 kHz), with a flicker noise term described by the flicker corner frequency f_{FL} of 4 kHz with the exponent n equal to 1.05.

Total output noise is measured with the $0.1\,pF$ input capacitor in place, and therefore

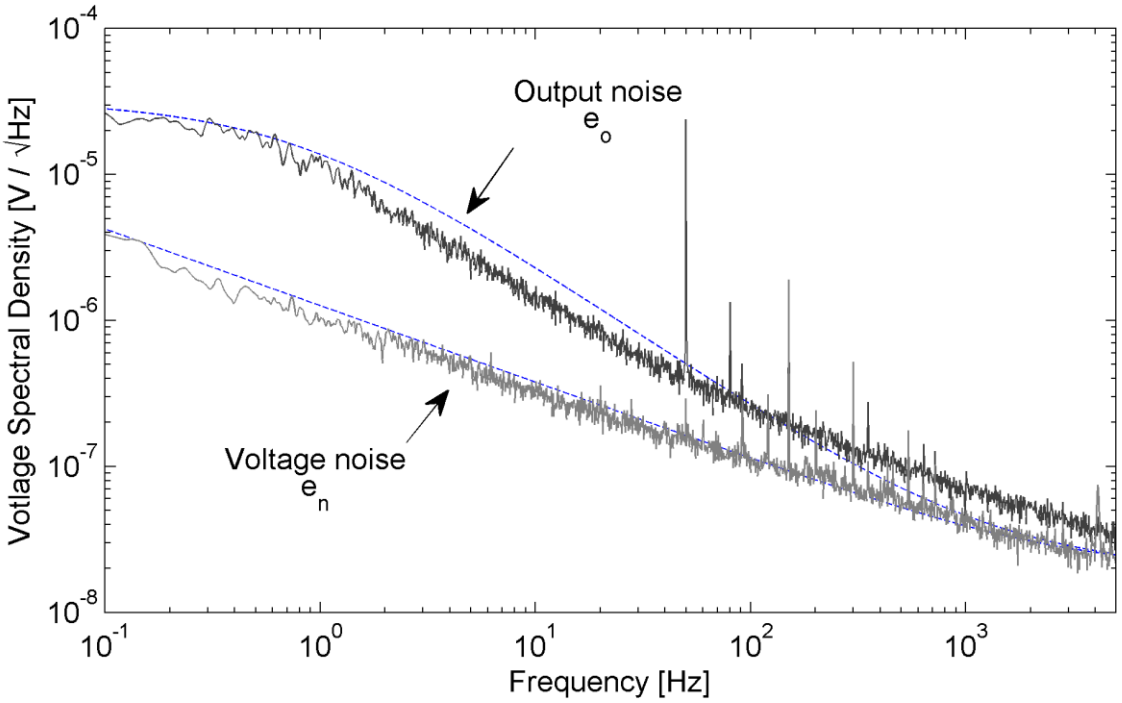


Figure 5-5: Noise for unguarded MOSFET EPS circuit. Measured (solid lines) and modelled data (dashes)

includes the thermal and current noise over the input and source (input capacitor) impedance. The measured output noise e_o is shown (dark grey) and closely matches the calculated output noise e_o (dashes). This output noise is almost entirely due to the thermal noise term, which has been calculated using the measured impedance values found earlier, $R_{IN} \cong 60\ G\Omega$ and $C_{IN} = 3.35\ pF$.

The slight discrepancy between the measured and calculated output noise at lower frequencies can be attributed to inaccuracies in the measurement, though the discrepancy at higher frequencies, above 1 kHz, shows a more interesting phenomena. At this higher frequency, where the thermal noise term is no longer dominant, then—according to the earlier developed noise model—the total output noise for the unguarded sensor should be equal to the voltage noise. Instead the output noise appears to be a mildly amplified version of the voltage noise. This can be attributed to the increased noise gain of the cascode circuit; the cascode transistor neutralizes the gate-drain capacitance by positive feedback in a manner analogous to guarding and so a similar, though in this case mild, voltage noise amplification is observed.

Current noise is not shown in Figure 5-5. The total measured output noise can be attributed entirely to the thermal noise term, and so the current noise cannot be experimentally determined at this impedance level. All that can be said is that the current noise term must be less than the thermal noise of the $60\ G\Omega$ input resistor, which when expressed as a current is $0.5\ fA/\sqrt{Hz}$. If the earlier measurement of input bias current is translated to either a shot or thermal noise current, then the current noise of this MOS transistor can be expected to be at least an order of magnitude less than $0.5\ fA/\sqrt{Hz}$.

The noise for the guarded sensor is shown in Figure 5-6. The measured voltage noise is plotted again for comparison (light grey). A calculated voltage noise is shown both without (blue dashes, e_n) and with the noise gain due to guarding included (grey dashes e_{nG}). This noise gain is proportional to the guard capacitance and the active device input capacitance (section 2.6.2). The combination of the calculated thermal noise and amplified voltage noise largely matches the measured total output noise e_o (dark grey).

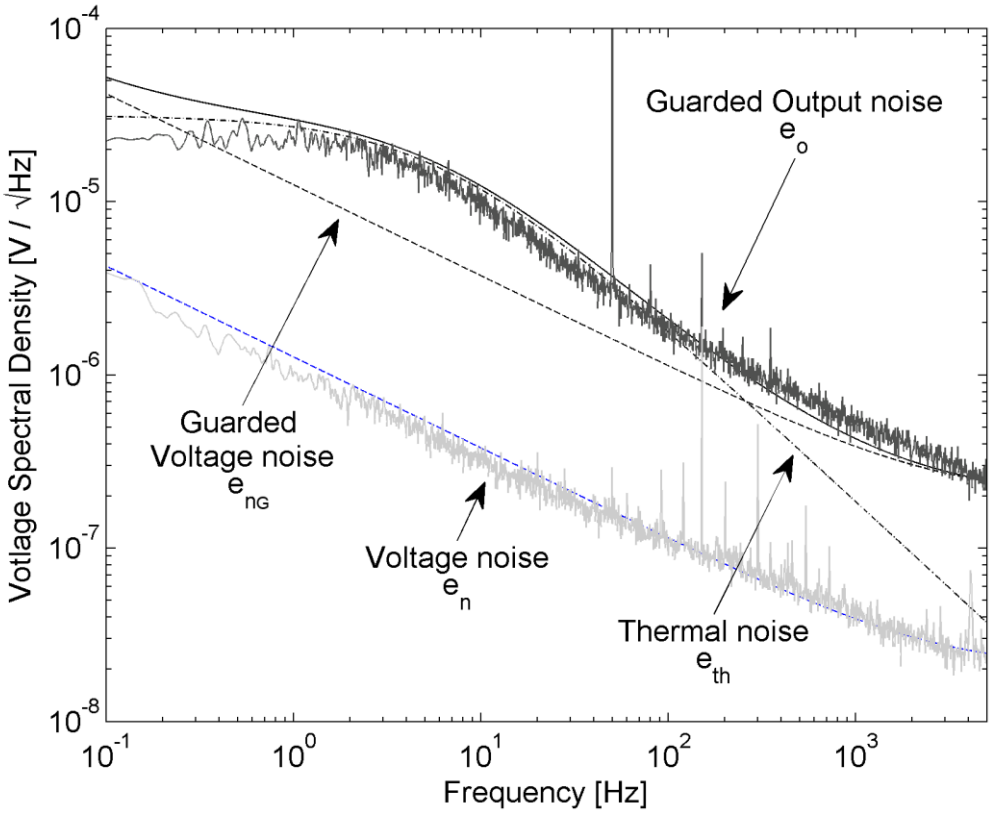


Figure 5-6: Noise for Guarded MOSFET EPS circuit.

A slight increase in the apparent voltage noise is visible in the total output noise, which may be the same voltage noise gain phenomena observed in the unguarded sensor.

At low frequencies, the total output noise of the guarded sensor is close to the ideal achievable for this high impedance. This ideal limit is set by the thermal noise term. The negligible current noise of this amplifier ensures that this ideal limit is not exceeded at low frequencies. At higher frequencies, of only 100 Hz, output noise exceeds the ideal because of the large flicker noise of the MOS device.

Integrating the output noise plot for the guarded sensor across a bandwidth of 0.1 Hz to 1 kHz gives an RMS noise voltage of 83 μV_{rms}. Considering the input of the EPS circuit can linearly amplify a large-signal swing of approximately 4 V_{rms} with 10V supplies, then the dynamic range in this bandwidth, with a 0.1 pF coupling capacitance, is 93 dB.

5.2 Remote cardiology measurement

The remote, or non-contact, measurement of cardiological activity has previously been demonstrated with EP Sensors, as well as several other techniques. Harland and colleagues have shown that when an EP sensor is placed at a spacing of several centimetres off-body, then a heartbeat signal is observed which is time aligned with the arterial pulse (Harland, Clark and Prance, 2002a) . This is distinct from the electrocardiogram (ECG) signal acquired when in contact with the skin (Harland, Clark and Prance, 2003).

The non-contact detection of heart rate has great value in a number of applications where the physical constraints of either active or passive skin electrodes make the measurement either inconvenient or impossible. Useful information about the subject can be inferred from the heart rate alone. In clinical situations a non-contact heart rate measurement allows monitoring of a patient's condition without the constraints of skin electrodes, and without the skin irritation experienced when passive Ag-AgCl electrodes are used over long periods of time. Heart rate detection has value in non-clinical situations, such as in automotive driver monitoring. Heart rate information can be used for heart rate variability (HRV) analysis, in which the subject's state of arousal can be inferred (Riener, Ferscha and Aly, 2009).

In suggesting an explanation for the observed time alignment of the remote heartbeat signal, Harland ascribes the origin of this signal to "the electric potential which may originate in the multi-polar dynamical fields generated by the cardiac system". Indeed it is reasonable to suppose that due to the complex polarisation of the cardiological electrical system that any remotely detected electrical activity should be quite different from the conventional I Lead ECG. However, the time alignment of the remote signal to the arterial pulse might also be explained if the signal sensed by an EPS originates instead in the movement of the chest wall. Completely distinct methods of remote cardiology sensing have been demonstrated which are sensitive to movement only, these are based on optical (Morbiducci et al., 2007) or Radar techniques (Matsui et al.,

2005). Since the amplitude of the electro-cardiological signal at the surface of the skin is known, then it may be possible to determine whether this electrical signal is indeed the originator of the signal detected by a remotely coupled EPS. If the signal acquired is larger than can be attributed to the surface ECG potential alone then an alternative explanation must be found, and the movement of the body is surely the prime candidate.

5.2.1 Environmental noise

The alternating current mains supply consistently presents problems to remote electric potential measurements. Mains wiring is present in almost every modern environment that a sensor might be asked to operate in. The potential is typically 110 V to 250 V at the source, and operates at either 50 or 60 Hz depending on the local electrical grid. When a sensor is weakly coupled to a source of low-voltage electric potential, it is quite likely that the much higher voltage mains wiring will couple to the sensor input so that the mains noise voltage at the sensor input is much larger than the voltage created by the weakly coupled signal source. Though the well defined frequency range over which mains wiring emits can be used to provide effective bandstop, or notch, filtering to the sensor output voltage this is often not possible due to sensor saturation. When a sensor is configured for the optimum signal to noise ratio for measurement of a low-voltage, remotely coupled electric potential, then it is quite likely that the 50/60 Hz mains potential will result in saturation of the sensor, either at the input stage or in subsequent amplifier stages. This makes it impossible to apply effective post-filtering of the noise signal.

In earlier work at Sussex, the ability to acquire cardiological signals at distances up to 1 m has been demonstrated, though only inside of a Faraday cage which removes the mains generated noise. In order to perform similar measurements outside of a Faraday cage, in an open environment with mains powered equipment, then the mains noise issue must be addressed. Two solutions exist; either the dynamic range of the sensor should be increased in order to prevent saturation, or some mechanism can be provided to produce a sensor which has a frequency dependent input sensitivity. The latter

solution has been explored extensively in an experiment conducted by Beardsmore-Rust and lead by Prance (Prance et al., 2008), and has been shown to be effective in retaining a sufficient signal-to-noise ratio in an unshielded environment. This work involved producing a sensor which effectively had a precisely controlled frequency-dependent input impedance. This was achieved by applying filtering within the sensor feedback loop so that only the desired frequency bands are guarded at the sensor input. The former solution requires that the sensor provide a wide dynamic range, which is equivalent to saying the sensor should have either very low noise or allow a very high signal swing. This allows the sensor to accommodate both the high amplitude noise and the smaller signal. Post filtering can then be applied to remove the noise components in order to restore a sufficient signal-to-noise ratio.

A wide dynamic range sensor, which accommodates both signal and large amplitude noise potentials without saturation, can be produced by providing either large signal swing, low electrical noise, or some combination of the two. Sensors with both of these characteristics have been investigated and described in chapter 4.

With attention paid to the electrical noise of the sensor, it has been possible to reduce the signal gain so that environmental noise does not cause saturation, whilst the small amplitude ECG signal remains above the noise floor of the sensor and thus retains sufficient signal to noise ratio.

5.2.2 Laboratory experiment

The simplest sensor configuration has been employed here; a single sensor placed at a separation of around 10cm from the back of the subject. It is likely that more complex spatial configurations of multiple sensor may be used to provide differential rejection of movement artefacts or enhancement of the heart rate signal, though this has not been investigated here.

The subject is seated on a wooden chair with the single sensor supported on a wooden bench immediately behind the subject (Figure 5-8). This configuration produces good

results and further demonstrates the ability to sense from the back of the subject, in contrast to the previously mentioned optical and Radar based techniques.

The sensor is mounted at a height just below the shoulders. In this experiment a wooden chair is used which leaves only an air gap between subject and sensor. The subject to sensor spacing is not tightly controlled, though it is maintained at approximately 10 cm. The experiment is conducted in an open lab environment with mains operated (UK 230V 50 Hz) equipment in close proximity. Absolutely no special precautions have been taken to reduce the mains noise in the proximity of the measurement. No conductive contact is made to the subject, either for the purposes of signal acquisition or grounding. The subject is therefore fully floating in an electrical sense, with only a high impedance connection to ground potential through the surroundings.

The sensor is based upon the single ended cascoded source follower circuit of section 4.3.3. The discrete input stage is followed by the AC coupled amplification stage given in section 4.4. The circuit is assembled as a modular system, with separate PCBs for the input and following stages. The input stage connects to the main board through stacking board to board connectors. This modularisation has been used to allow rapid prototyping of the two stages separately. This sensor is shown in Figure 5-8, fitted with

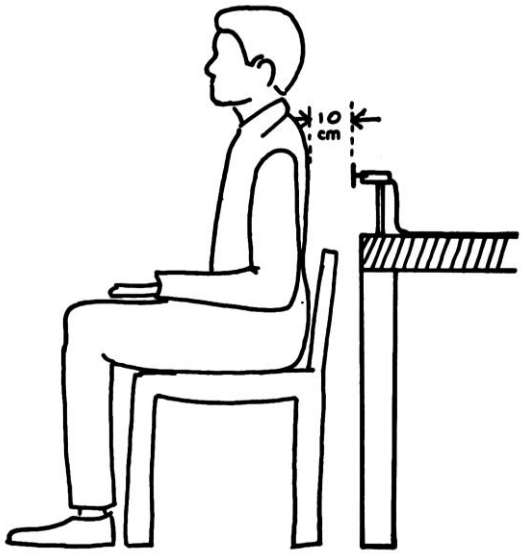


Figure 5-7: Experimental setup. A single EPS sensor is placed behind the seated subject. An air gap of approximately 10cm is maintained between the subject and the input electrode of the sensor.

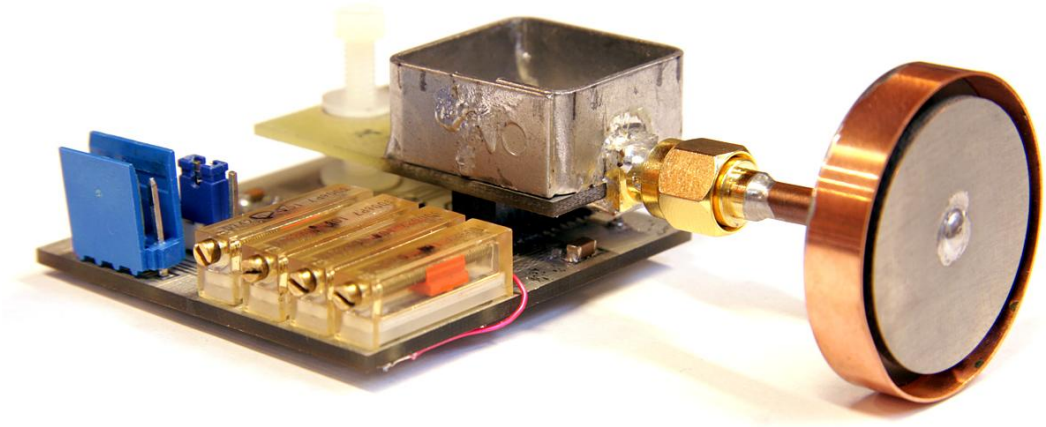


Figure 5-8: Photograph of the modular sensor.

a co-axial electrode structure. The electrode has a 20 mm diameter input electrode, and is surrounded on its back and sides by a screen which is connected to the guard of the sensor. Low capacitance between the input electrode and its guarded screen has been ensured by using a short length of semi-rigid, low capacitance, coaxial cable and by leaving an air gap between the electrode and back-side screen. This reduced input-guard capacitance contributes to low noise and increased bandwidth.

Symmetrical 10V power supplies allow the sensor to produce a ground referenced undistorted large signal swing of approximately $18\ V_{pk-pk}$. Unity guarding and a $1\ T\Omega$ input resistor gives an input impedance of $0.3\ pF\ ||\ 1\ T\Omega$. A low voltage gain of $2.00\times$ ensures that input dynamic range is maximised. The input impedance corresponds to a 0.5 Hz high-pass corner for weakly coupled signals.

The sensor output is digitized by a NI-6251 (National Instruments, Austin, TX, USA) high speed, high resolution digitizer (16-bit at 1 MSPS) after aliasing filtering at 1 kHz. Signal processing is then performed in real time on the digitized signal by a LabView (National Instruments, Austin, TX, USA) virtual instrument.

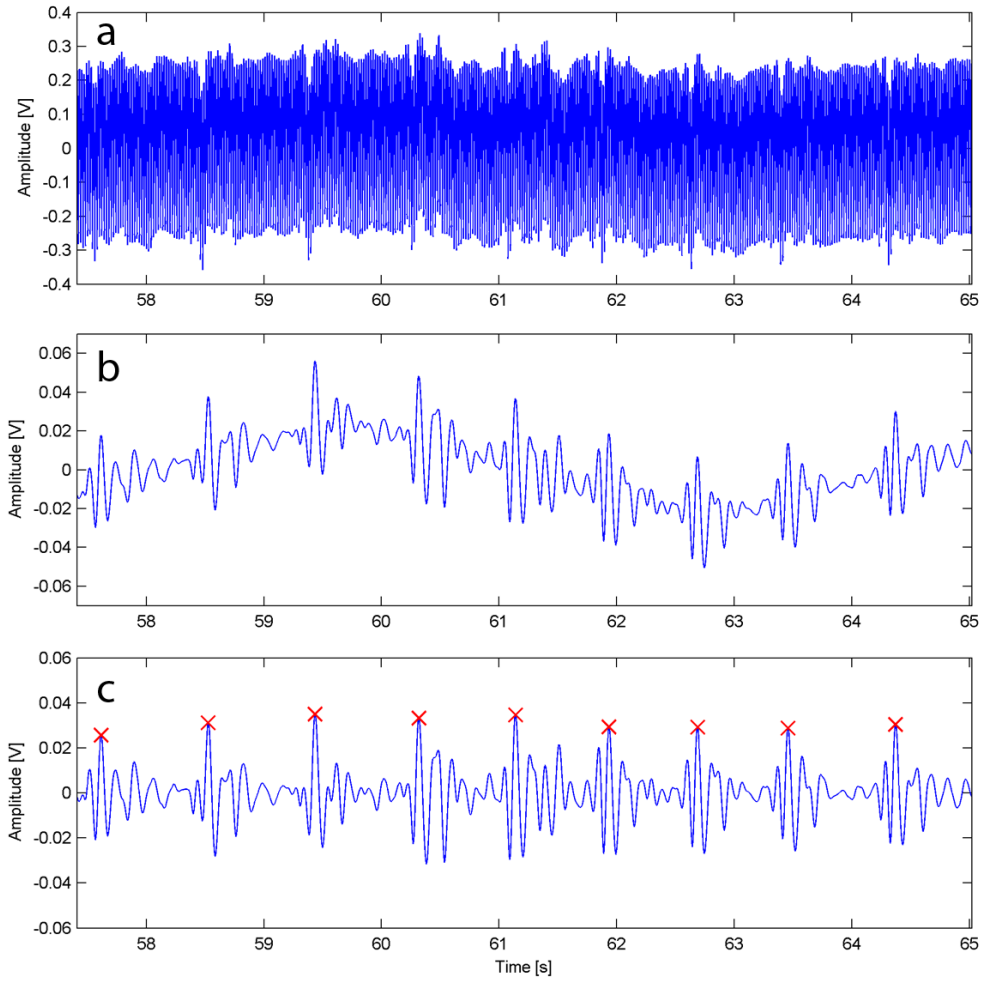


Figure 5-9: 7.5 second segment of: a) raw sensor output b) low-pass filtered c) low & high pass filtered. In c a simple peak detection algorithm has been used in post-processing to identify the pulse, indicated by a cross.

5.2.3 Signal Processing and heart rate extraction

The raw unprocessed sensor output, in Figure 5-9**a,** shows a cardiological signal which is obscured by approximately 0.6 V_{pk-pk} of 50 Hz and its harmonics arising from the mains wiring and nearby mains powered equipment. In Figure 5-9**b** a 2nd Order Butterworth low-pass IIR (infinite impulse response) filter with a corner frequency of 15 Hz has been applied, in addition to an IIR band-stop (notch) filter centred at 50 Hz. This combination of filters reduces the 50 Hz component to below the noise floor of the sensor and reveals the underlying signal. The remaining very low frequency component, with a period of approximately 8 seconds, is synchronized with the subjects breathing.

This breathing signal originates in the large amplitude chest expansion of the subject during inhalation and exhalation.

In Figure 5-9**c** the breathing signal has been removed by applying a 3 Hz 1st Order Butterworth high-pass IIR filter. Exchanging this filter for a low-pass type would instead reject the heart rate signal, thus enhancing the breathing.

5.2.4 Discussion

The signal in Figure 5-9**c** has a sufficient signal-to-noise ratio for extraction of heart rate information. The extraction of this heart rate has been demonstrated by applying a simple peak detection algorithm to identify the pulse, and is indicated in the figure by a cross.

It is clear, as concluded by Harland et al., that the waveform obtained by remote electric field sensing is not representative of a true ECG; it does not contain a clear QRS impulse or additional features, and as such can only be used to derive a heart rate. The amplitude of the heart rate signal, when referred to the input of the sensor, has a peak amplitude of around 15 mV. This is far in excess of the potential at the skin typically obtained in contact ECG measurements, which is around 1 mV. The skin potential can only be expected to be attenuated when sensed remotely. This leads to the conclusion that the observed heart rate signal at this separation of 10 cm is predominantly due to the movement of the subjects body as a result of the arterial pulse and the ventricular contraction of the heart.

The very narrow bandwidth filtering required to produce a good signal to noise ratio, as in Figure 5-9**c**, produces undesirable ringing artefacts and phase distortion. It is conceivable that these distortions may be disadvantageous in HRV analysis and so more sophisticated signal processing may be required. In particular, linear phase FIR (finite impulse response) filtering may be more suited to such analysis.

Shown in Figure 5-10**a** is the frequency spectrum of the unprocessed sensor data. Aside from the 50 Hz noise, there is a large amount of signal power from ~20 Hz extending down to below 1 Hz. The spectrum of the bandpassed heart rate signal is given in Figure 5-10**b.** The predominant features of the 'pulse' (here this term has a dual meaning in both the biological sense, and the signal sense) occupy this bandwidth from 5 Hz to 15 Hz. It has been shown that the breathing signal can be extracted by passing the lower frequency bandwidth of 0.5 Hz to 3 Hz. Whilst this approach has been successful here, as illustrated in Figure 5-9**b**, the simple discrimination of breathing and heart rate from the EPS signal by frequency filtering alone is not so successful when movement artefacts are included. The subject in this experiment was instructed to remain as still as possible during the measurement, ensuring a minimum amount of movement artefacts in the data. With either small or large movements of the subject, the sensor records large amplitude excursions which generally exceed the amplitude of the heart rate signal. This movement noise occupies a frequency band equal to that of the desired signal. Frequency domain filtering therefore has limited success. Most of the movement noise power is however restricted to lower frequencies, so that high pass filtering at around 3 Hz is moderately successful at isolating the heart rate signal from smaller movement artefacts. Extracting the breathing signal is less successful when it is superimposed on a background of movement noise.

This movement noise is predominately due to the relative movement between the subject and sensor, so that mechanically coupling subject and sensor may improve

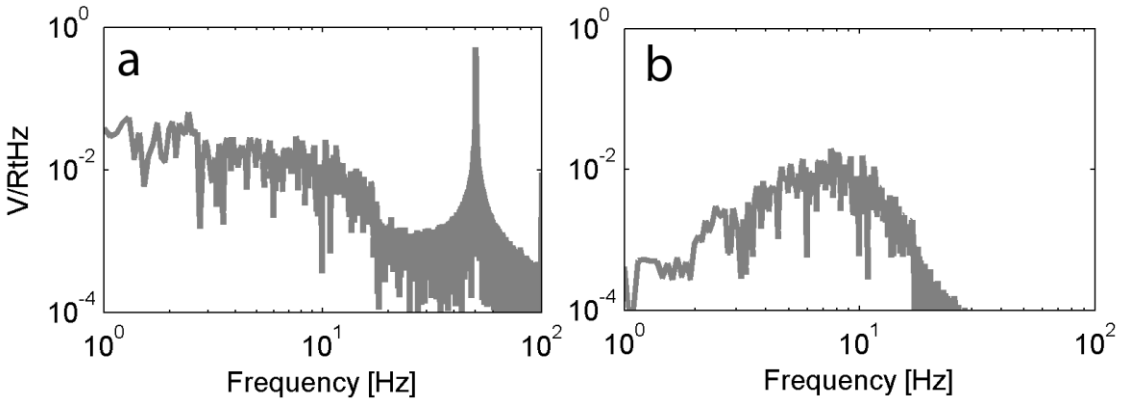


Figure 5-10: Frequency spectrum derived from Figure 5-9 parts a and c respectively.

movement rejection. Additionally, it may be possible to use differential pairs of sensors that are spatially configured so that the movement signal is common to both sensors and is thus rejected, whilst the heart rate and/or breathing signal is retained, or indeed enhanced.

Since a remote measure of cardiological activity can only supply heart-rate data then it is sensible to present the data as a simple heart rate, or peak-peak interval (the so-called R-R interval) rather than a full waveform, which is often difficult to interpret for the untrained user. In order to determine this rate, then some form of peak detection must be provided in order to identify the signal peaks due to each heartbeat. The application of conventional peak detection algorithms to these remotely detected signals is complicated by the variability of the peak amplitude. An algorithm which seeks to overcome the fixed-threshold of conventional algorithms is described in Appendix B.

5.3 Surface EMG and Micro-MUAP

5.3.1 Surface Electromyography

The measurement of muscle activity by observation of the electrical potential at the surface of the skin is the surface electromyogram (SEMG). This technique has wide ranging clinical applications (Pullman et al., 2000), including the diagnosis of disorders of motor action control, as well as in fundamental biological and clinical research.

The surface EMG signal is a result of the individual motor unit action potentials (MUAP) which stimulate muscle contraction. The force of muscle contraction is proportional to both the number of active motor units, and the firing rate (frequency) of the individual motor units. This firing rate varies from only a few Hz during minimum voluntary contraction, to 50 Hz (Sandbrink, 2010). In conventional surface EMG this underlying process—the firing of individual motor units—cannot be observed. Instead the integrated response of several motor units is recorded. The most commonly used

quantitative analysis technique used in surface EMG studies is based upon the measurement of the RMS level of the integrated signal. The surface EMG signal acquired by conventional electrodes is mostly constrained in the 50 Hz to 150 Hz bandwidth, and has an amplitude in the range $0-10\,mV_{pk-pk}$ or $0-1.5\,mV_{rms}$ (De Luca, 2002). The conversion between peak to peak and RMS amplitude uses the scaling factor of 6.6 since the EMG signal is Gaussian. Invasive intramuscular EMG must be used for individual MUAP analysis. Invasive techniques have several limitations, in addition to the discomfort caused to the patient. In the past decade, attempts have been made to observe individual MUAPs from surface EMG studies, either by signal processing techniques of the conventional surface EMG, or by modifying the acquisition method (Zhou and Rymer, 2004). Here the use of an EP sensor with a very small electrode area (of the order $25\,\mu m$) is investigated, which exploits the exponential decay of the MUAP amplitude through the tissue in order to observe individual MUAPs.

5.3.2 Electrode technologies

In the vast majority of conventional SEMG measurements gelled silver-silver chloride electrodes (Ag-AgCl) are used to form a low impedance ($< 10\,k\Omega$) connection to the skin (Duchene and Gouble, 1993). As in the measurement of ECG, EP sensors can be used as a replacement for Ag-AgCl electrodes by using the EPS as an active electrode which senses skin potential through a thin dielectric interface. The high impedance EP sensor is capable of making low noise measurements across this dielectric interface without electrically loading the source potential. The dry electrode-skin interface avoids the skin irritation and inconvenience experienced with wet gel electrodes.

In order to demonstrate the ability of the EP sensor to mimic the operation of conventional Ag-AgCl electrodes, a macro-scale sensor with a circular electrode diameter of 12mm is used. A further experiment involves the use of an ultra-low capacitance sensor, based upon the single ended cascoded source follower circuit of section 4.3.3. This sensor is supplemented with a micro- scale electrode structure with

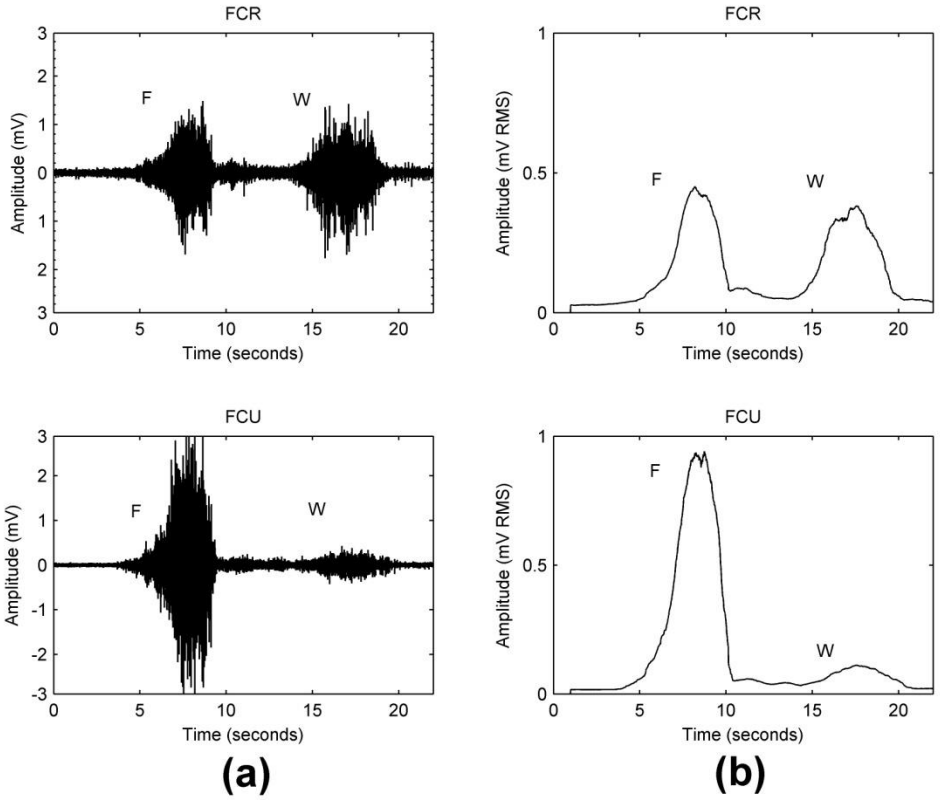


Figure 5-11: (a) SEMG from the FCR and FCU muscles (b) RMS values.

an input electrode diameter of $25\,\mu m$. The construction of this high spatial resolution electrode will be the subject of a complete discussion in the following chapter.

5.3.3 Surface EMG results

12 mm circular electrodes were used to study the surface EMG of the flexor carpi ulnarius (FCU) and flexor carpi radius (FCR) muscles. A sensor was placed on the upper and lower forearm in the approximate positions of the FCR and FCU muscles respectively. The SEMG signal from each sensor is measured differentially against a reference sensor placed on the wrist. These differential signals are digitised at $10\,kSs^{-1}$, with an analogue bandwidth of 30 Hz to 1 kHz. Additionally, a bandstop (notch) filter centred at 50 Hz was applied to the digitized signal.

In Figure 5-11 (Prance and Watson, 2009) the simultaneous SEMGs of the FCR and FCU muscles are given. The subject was instructed to sequentially perform the actions

of relaxing the arm, clenching the fist (F) and relaxing again before flexing the wrist (W). These actions are indicated in the SEMG traces. In Figure 5-11**a** the SEMG signal is derived directly from the filtered sensor output and referred to the input voltage by dividing by the total system voltage gain. In Figure 5-11**b** the RMS amplitude is shown, determined numerically from the voltage waveform with a time-constant of 0.5 seconds. The discrimination between the F and W actions by the two sensors demonstrates the good spatial selectivity of the high impedance sensors.

5.3.4 Surface micro-MUAP results

In Figure 5-12 the SEMGs from a 12 mm diameter electrode (left column) and the 25 μm diameter electrode (right column) are shown. These measurements have been recorded consecutively from the FCR when clenching a fist. A resting period of 5

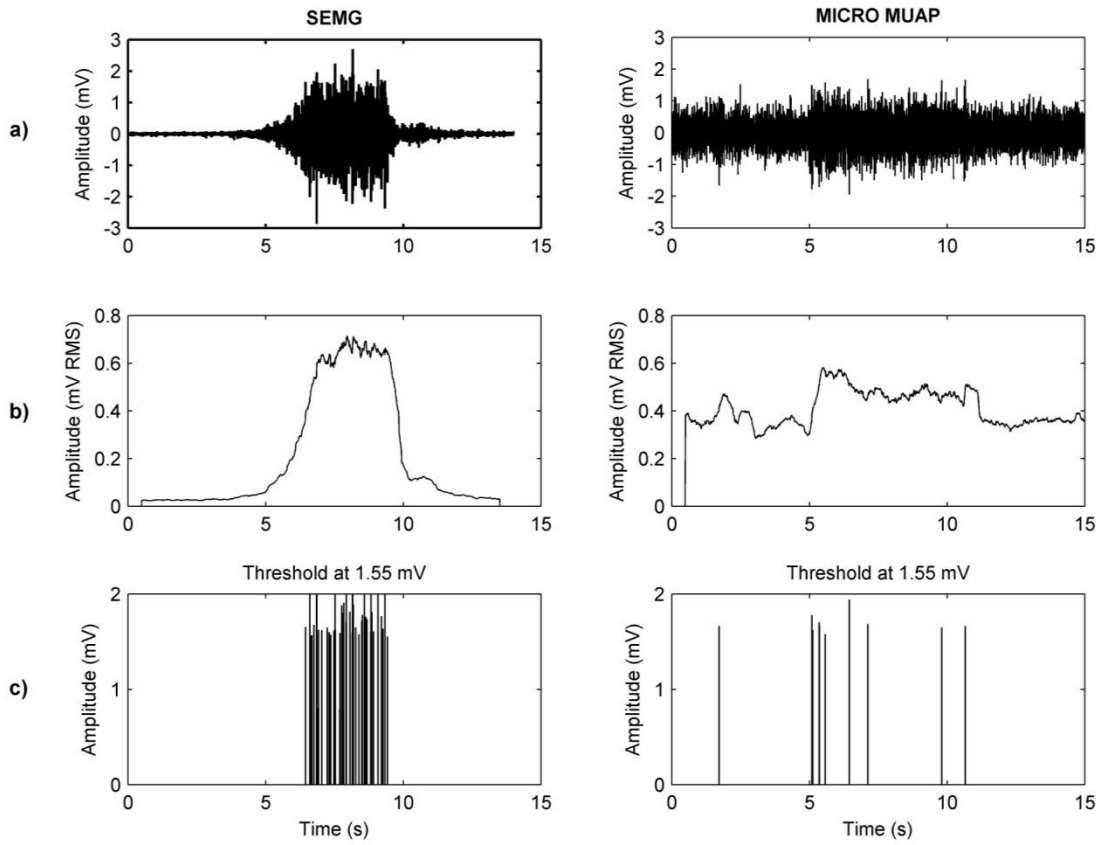


Figure 5-12: (a) SEMG and micro-SEMG from the FCR muscle (b) RMS values (c) rectified SEMG with 1.55 mV threshold applied.

seconds is performed before and after 5 seconds of the clenching action.

Each sensor has a sufficient input impedance such that the signal is a true representation of the skin potential at the electrode-skin interface—there is no attenuation. As such the amplitude of the two EMG traces may be compared directly. Immediately obvious is the increased noise level of the micro-scale sensor. This is due to the increased sensor-skin impedance and the ultra-high input impedance required to ensure no input attenuation. However, an EMG signal is visible against the background noise, most clearly shown in the plot of RMS voltage.

In traditional surface EMG studies electrode diameters of several millimetres are used, as is also the case in the SEMG data of Figure 5-12. As a result a large population of motor units are responsible for the observed EMG. The tissue has a low-pass effect on the MUAP and the peak potential is exponentially dependent on the separation between the motor unit and the EMG electrode. The SEMG shown in Figure 5-12 therefore consists of many high amplitude peaks arising in motor units which are very close to the electrode. With the $25\ \mu m$ diameter electrode, only a small number of motor units can be in proximity to the electrode so that individual action potentials are observed. This is shown in Figure 5-12**c** where a threshold has been applied at 1.55 mV to reveal only the highest amplitude peaks. The micro sensor signal is sparse compared to the macro scale sensor, indicating fewer motor units in immediate proximity to the sensor.

5.3.5 Discussion

The signal to noise ratio shown here is insufficient for studying the waveform of the motor unit action potential, though with the basic threshold technique shown here it may be possible to detect motor unit firing for the purpose of measuring the firing rate.

Due to the high spatial sensitivity the exact placement of the sensor in relation to individual motor units is critical. In order to derive a firing rate for a single motor unit it will be necessary to position the sensor so that it is much closer to one motor unit than any other. If, for example, the sensor is approximately equidistant between two motor units then a false double rate might be observed. A proposed high density two-

dimensional array of electric potential sensors might make it possible to perform simultaneous high resolution sEMGs over a relatively large skin surface area so that individual MUAP firing rates may be observed with relatively simple signal processing.

6 ELECTRIC FIELD IMAGING

6.1 Introduction

Scanning electric potential microscopy (SEPM) involves the direct measurement of spatial electric potential by a high impedance EP sensor. Multiple spatial measurements of potential can be used to form an image. A series of techniques allow images of microscopic resolution to be formed which may be used to study the surface topography of a sample, or its electrical parameters, such as dielectric constant, electrical impedance or static charge density.

These separate measurements will be presented, classified according to the principal mode of operation. Each mode requires a slightly differing sample and acquisition configuration, though it must be emphasized that these different modes are all achieved using a common set of apparatus (with the exception of the array charge scanner). The versatility of the apparatus across a variety of measurements can be considered a major advantage of this SEPM system.

The bulk of the experimental work described in this chapter has been conducted on a microscopic scanned probe apparatus. This apparatus will be described in detail, and the experiments employing the 3 main imaging modes will be described.

The first of these modes is the imaging of AC potentials, which allows surface imaging of conducting and dielectric samples. In the case of dielectric samples, this technique reveals additional bulk material, or buried, features. This closely follows the work of

previous experiments with scanned EPS systems carried out at the University of Sussex. This new work represents a refinement of the methods and apparatus of SEPM, with the results of experiments used to derive a more complete understanding of the SEPM instruments. The closely related method of imaging AC currents also represents a furthering of the earlier work of previous Sussex experiments, with an experiment showing a new application in the analysis of geological samples. Finally, the technique of imaging DC, or static, potentials is described. This represents an entirely novel method, in the context of both previous SEPM experiments, and also in the wider field of microscopy. The techniques discussed here have been developed in partnership with Sam Beardsmore-Rust during a set of earlier experiments conducted on a macroscopic resolution (~1 cm) array scanning apparatus. This apparatus and the results of these earlier experiments will be reviewed briefly. This apparatus is of interest not only because of its DC imaging capability, but also since it demonstrates the operation of a 1-D array of EP sensors. This experiment will then act as a useful introduction to the imaging of DC potentials on the microscopic scale with the scanned probe apparatus. A series of such experiments will be described which were conducted on the present high resolution SEPM instrument, with a full discussion of a particular application of this instrument to the imaging of forensic fingerprints.

6.1.1 Scanning probe microscopy

The ability to image electric potentials has applications in a wide variety of traditional, and novel, microscopy applications. When a single electric potential probe is used to form the image, then this microscope belongs to the broad class of scanning probe microscopes. These include the scanning tunnelling (STM) (Binnig et al., 1982) and atomic force (AFM) (Quate, Gerber and Binnig, 1986) microscopes. Each of these techniques offer excellent, often atomic-scale, resolution and a wide variety of measurement modes that can be used to reveal myriad surface and material properties. As a result, they have been widely adopted in a variety of industrial and research roles. However, both these techniques rely on forces which exist between a fine probe and a surface when they are separated on an atomic length scale. This enforces atomic scale

(sub-nanometre) control of the probe position, and therefore limits the speed of image formation as well as requiring costly translation stages.

In SEPM a micro-scale electrode structure is used so that spatial electric potential can be measured with a resolution commensurate with the electrode dimension. SEPM has previously been demonstrated in earlier work at the University of Sussex with a maximum spatial resolution of $1\ \mu m$ (Clippingdale et al., 1994a). Whilst this resolution is significantly lower than in AFM or STM, it covers a 'middle ground' of length scales where AFM or STM are too slow, or optical methods are not adequate since they cannot measure electrical and bulk material properties. Scanning electron microscopes (SEM) can compete on resolution, offer high imaging speed and in some cases can be used to determine advanced sample properties such as electrical parameters. However, not only is the apparatus large and costly, the measurement cannot be considered non-invasive since the e-beam can result in either sample charging or, more significantly, damage to the sample. In contrast, the scanning electric potential microscope uses an ultra high impedance sensor with a non-contact probe. The sensor draws no real current from the sample so that samples are subjected neither to high current densities as in STM, or exposed to energetic particles, making the SEPM truly non-invasive in both an electrical and a mechanical sense.

In the context of the EP sensor developed at the University of Sussex, the origin of the SEPM can be traced to the work of Clippingdale (Clippingdale, 1993) and Prance. In this early work a single scanned probe was used to image the potential distribution above a sample of dielectric material in order to determine its properties. Later, the application of this microscope was extended to the imaging of active VLSI circuits (Prance et al., 1998). In both experiments a $1\ \mu m$ spatial resolution was achieved through the use of a probe having an exposed electrode of approximately $1\ \mu m$ diameter, and by having the probe and sample separated by approximately $1\ \mu m$. The excellent spatial resolution shown in these experiments was achieved by tolerating a probe design that was both fragile and difficult to construct. In addition, the high input

impedance necessitated by the high resolution probe could only be achieved with a narrow 'tuned' frequency response, and with generally poor electrical stability.

Later work at Sussex, principally during the studentship of W. Gebriel (Gebrial, 2002b), continued the development of the SEPM techniques and apparatus, with new applications in the non destructive testing of composite materials (Gebrial et al., 2006b), circuit imaging(Gebrial et al., 2002a) and the examination of electrical signals in nerve fibres (Gebrial et al., 2007). In the present work (Watson et al., 2010a), the applications of the SEPM have been extended to several new areas, and two major advances have been made over the previous systems. First, significant improvements to the EPS have negated the need to tune the sensor for a narrow frequency band, enabling broadband AC measurements with lower noise and higher sensitivity than previously achieved. Second, the sensor has been paired with a more robust electrode structure that can withstand significant mechanical and environmental stress.

6.1.2 High resolution electric field sensing

SEPM is based upon the direct measurement of electric potential with high spatial resolution. In order to spatially resolve electric potentials an EPS must be fitted with an

Figure 6-1: (left) photograph of EPS probe on the scanning apparatus and (right) several micro electrodes.

input electrode which has an exposed area commensurate with the desired spatial resolution. This spatial sensitivity relies on the fact that an EP sensor is a high impedance device, and so the presence of the probe itself has little effect on the spatial potential which it is to measure.

The spatial sensitivity of an electrode can be confined to only its tip by surrounding it with a shield, so that the electrode is in fact a co-axial structure. This shield connection is not grounded, but is connected to the guard of the EPS. This maintains both the high input impedance of the EPS, and also avoids presenting the spatial electric potential with a short to ground.

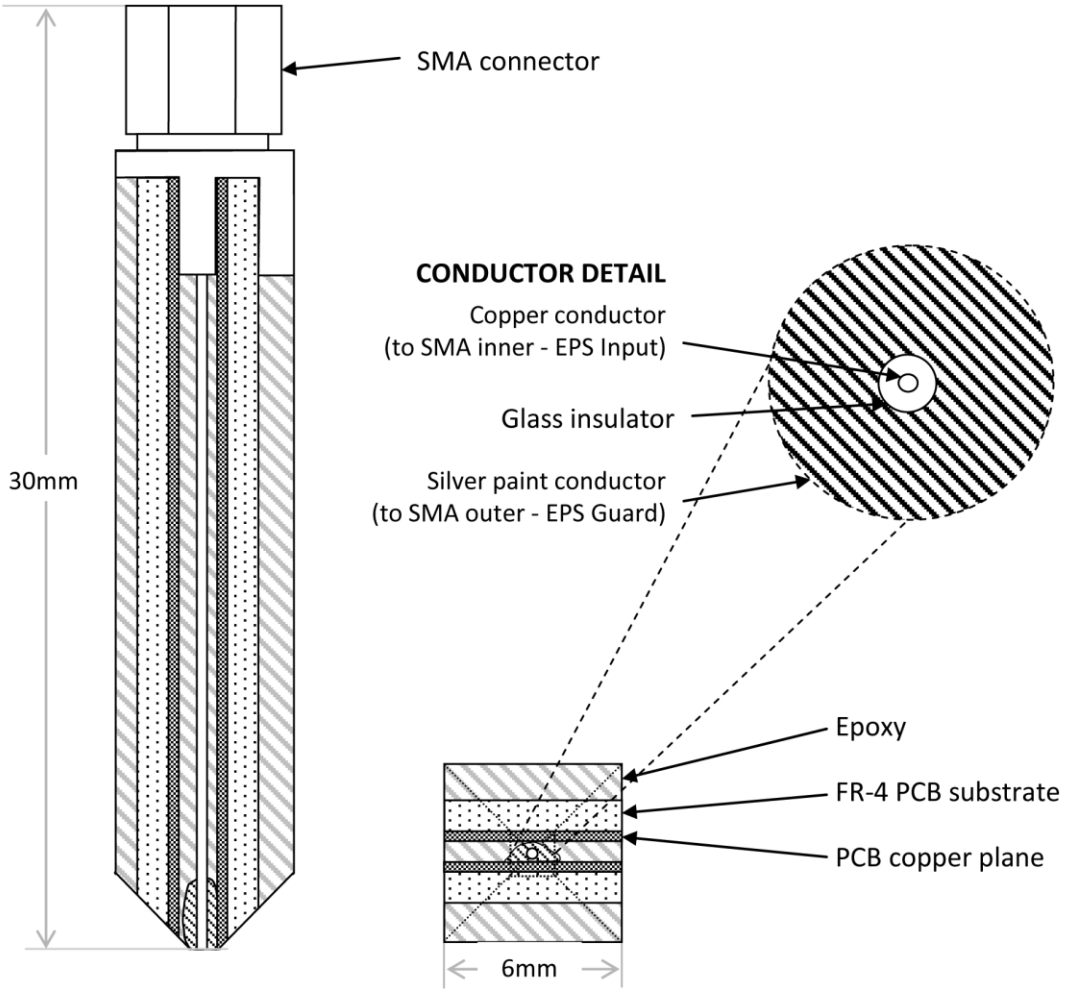


Figure 6-2: Drawing of micro-probe structure. A section through the probe (left) shows the laminations of copper-clad FR-4 PCB substrate and epoxy resin, shown also in end profile (bottom). An expanded view of the central conductor area (right) shows the central copper conductor with glass insulator and coaxial silver-paint outer.

Several electrode structures of various electrode diameters have been produced. When paired with an EP sensor these form an EPS probe, illustrated in Figure 6-1, which is mounted to a translation stage to be used as a scanned probe microscope.

The scanned EPS probe is used to make many point measurements in order to construct an image. Each measurement is therefore referred to as a pixel. The probe's response to the pixel beneath it and the additional contribution to the measured potential due to those pixels adjacent to it can be described by a spatial sensitivity function. A step sensitivity function is assumed and therefore contributions from adjacent pixels are neglected. It may be possible to account for this inaccuracy by using a measured or calculated spatial sensitivity function and inversion methods, as has been demonstrated in related scanned probe microscopies (Faircloth and Allen, 2003).

A co-axial electrode structure has been designed to minimize the influence of adjacent pixels on the probe. The electrode consists of a 5 µm diameter glass-insulated micro-wire coated in silver paint and set in epoxy resin, shown in Figure 6-2. The electrode is terminated by an SMA connector in order to exchange electrodes on the EPS. Silver paint forms a conducting coaxial guard around the sense electrode, spaced by no more than 1 µm, in order to confine the spatial sensitivity of the electrode.

The diameter of the guard electrode is of supreme importance in defining the spatial sensitivity of the probe. When this 5 µm probe is spaced from a sample by 5 µm, the resolution of the imaging system is also 5 µm. When the sample-probe spacing is increased resolution drops off approximately linearly with spacing. As such the system allows flexibility in spatial resolution, allowing scanning to be performed at higher speed over larger areas with reduced resolution.

In addition to the probe with a 5 µm diameter, larger diameter probes have been constructed, including 60 µm and 120 µm probes. Though the highest resolution probe can be used to image at lower resolutions by increasing spacing, a larger area probe has the benefit of increased electrical sensitivity by having increased coupling capacitance.

6.1.3 Scanning probe apparatus

The SEPM apparatus consists of: a single electric potential probe; a translation stage; and a combined controller and data acquisition unit. The translation stage (Figure 6-3 & Figure 6-4) is a two-axis gantry table with linear slide bearings. Stepper motor driven ball screws allow 6 µm positional resolution over a large 300 mm x 300 mm scan area. The integrated controller/acquisition unit provides positioning control and digitisation of sensor signals through a USB interface to a LabView (National Instruments, Austin, TX, USA) virtual (software) instrument on a PC. This part of the hardware has been described in detail by Beardsmore-Rust (Beardsmore-Rust, 2010).

The PC control software allows programmatic generation of raster scan patterns with flexible scan area and step size. Simultaneous control and sensor data acquisition allows real-time generation of images. The PC based system offers flexibility in the image acquisition so that a variety of measurement modes can be used.

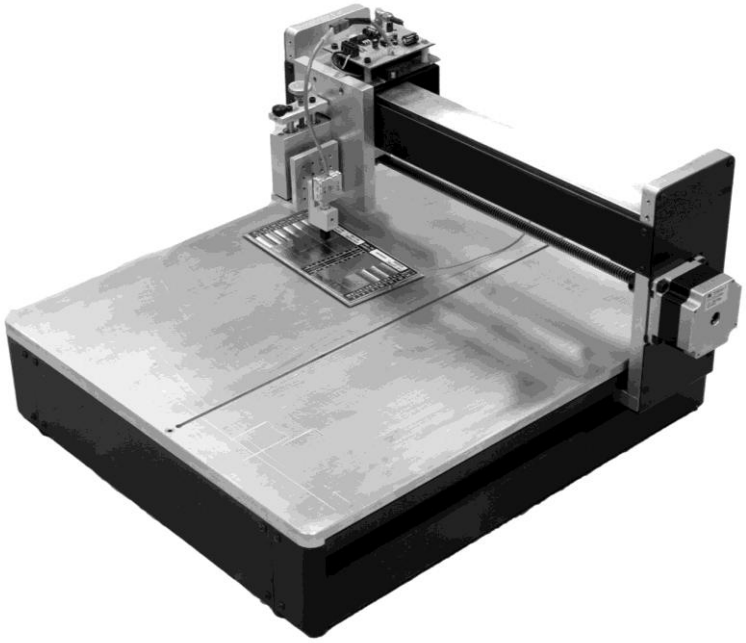


Figure 6-3:SEPM translation stage with probe.

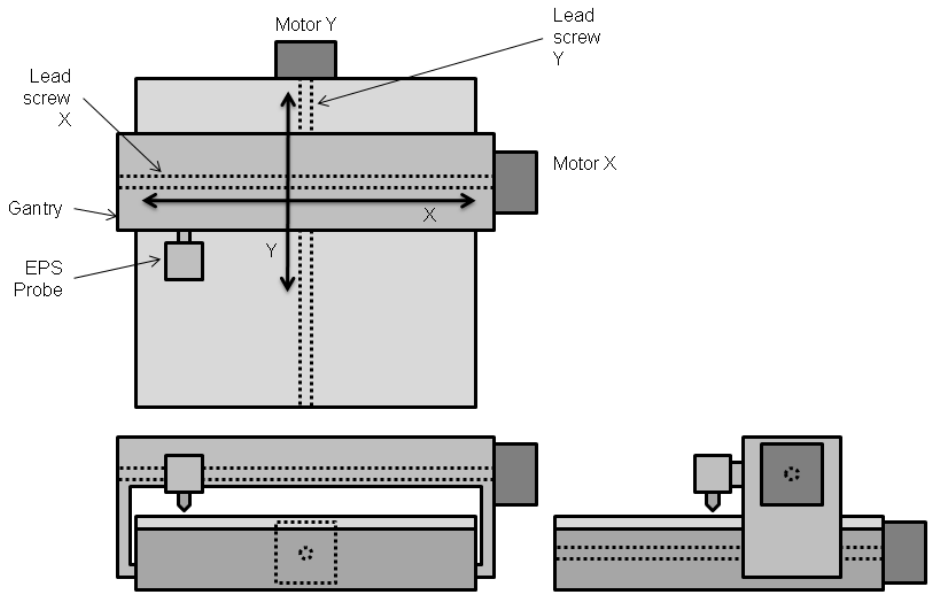


Figure 6-4:SEPM translation stage

A commercial USB data acquisition and digital interface board forms the core of the hardware controller unit. The digital interface lines of this board are used to form a simple bit-banged interface to a microcontroller which generates stepper motor drive signals and monitors hardware limit switches (Figure 6-5).

The hardware systems, as well as the initial versions of the software which controls it, were developed by Beardsmore-Rust. Early results using this apparatus, as a joint effort

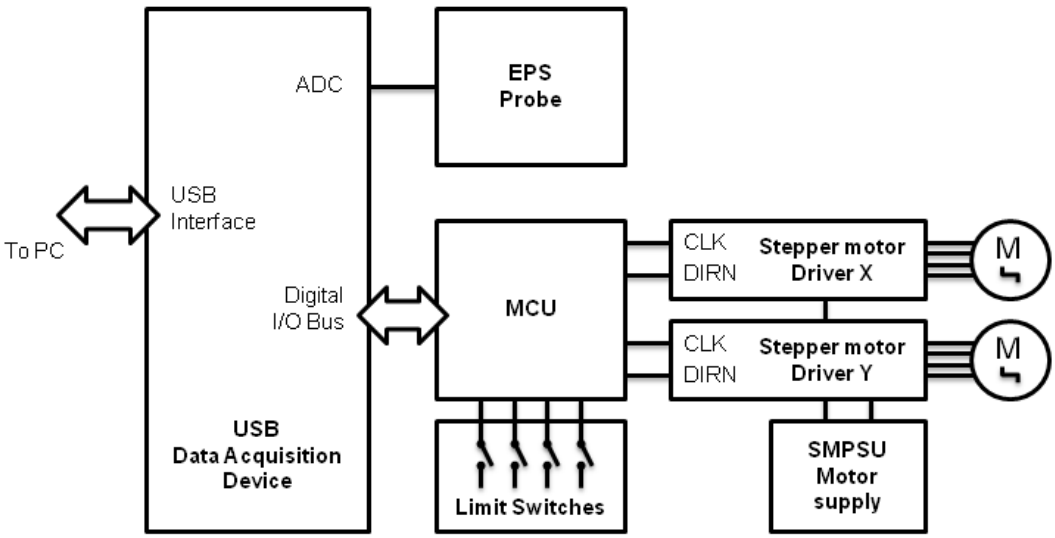


Figure 6-5: Block diagram illustrating major components of the hardware controller unit

between Beardsmore-Rust and the author, have been described by Beardsmore-Rust already. Following this early work, all additional results have been conducted by the author.

The EPS probe is mounted on a carriage with coarse and fine adjustment of the probe height. Initially a thumbscrew was used for manual setting of probe height, though this has since been supplemented with a stepper motor driven screw for programmatic

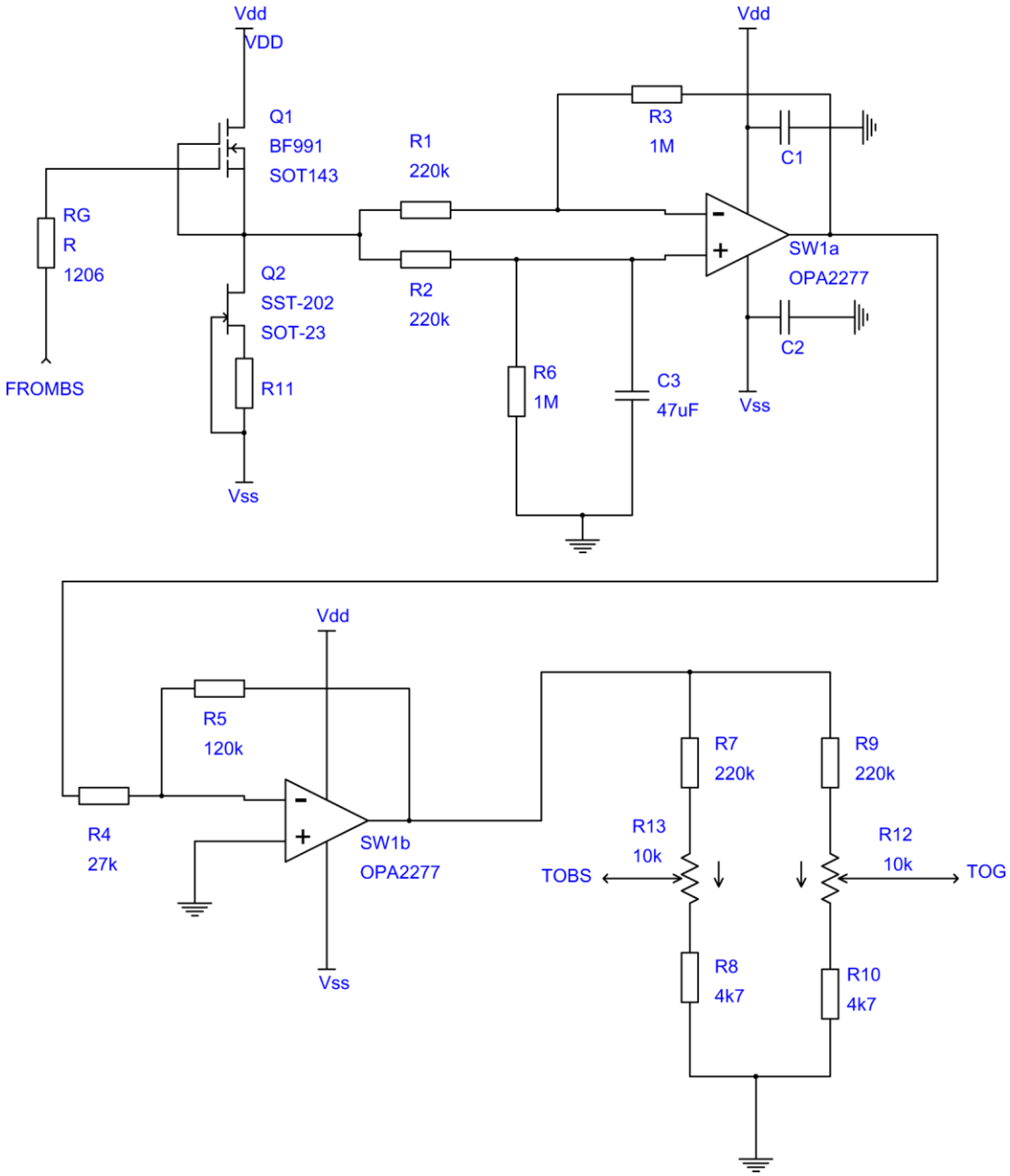


Figure 6-6:EPS sensor schematic.

setting of probe height (Appendix C).

In addition to the sensor digitization provided by the controller (and subsequent software signal processing available on the PC), a separate lock-in amplifier is provided for use in some measurement modes. This instrument measures the amplitude and phase of the signal detected by the probe with respect to a reference signal. A commercial instrument with the requisite amplitude and phase resolution in the audio frequency bandwidth was not available, and so an instrument has been constructed (Appendix 7Appendix E). This instrument interfaces to the LabView virtual instrument over an RS-232 interface.

The EPS sensor is a discrete MOSFET input ultra-low capacitance design. This sensor is similar to previously discussed discrete MOSFET designs, as is clear in the schematic of Figure 6-6. The significant difference is in the construction; the entire active sensor is packaged in a 20 x 20 mm metal can. The PCB design is shown in Figure 6-7. This compact design allows the sensor to be mounted directly to the probe. The input is

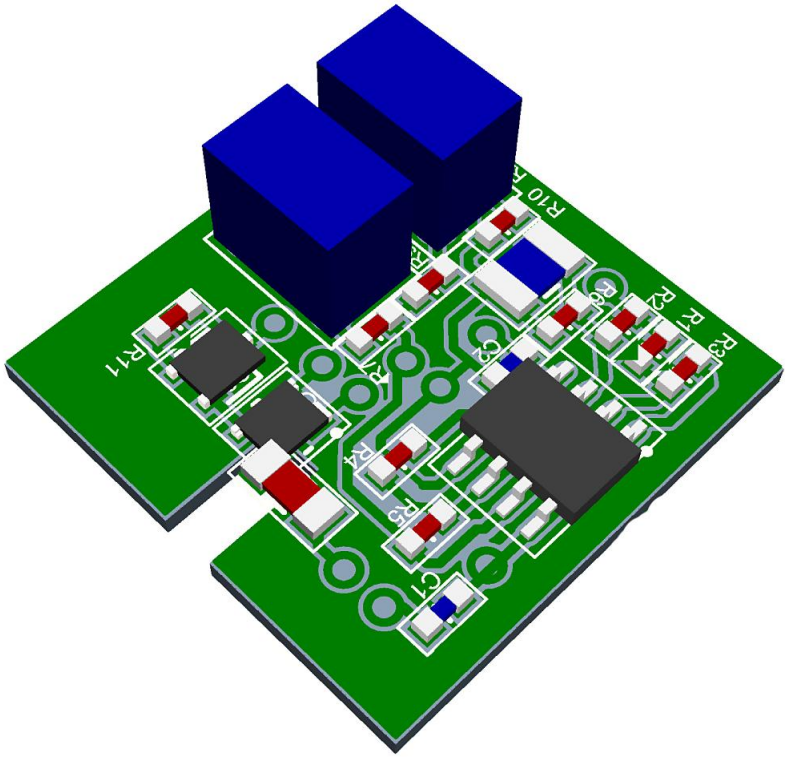


Figure 6-7: 3D render of EPS Sensor PCB (excluding enclosure).

terminated by a coaxial SMA connector for straightforward probe and sensor exchange.

Power and signal connections are made between the sensor and the translation stage carriage by a 6 pin in-line cable connector, to a power supply (PSU) board mounted close to the sensor on the translation stage carriage. This PSU board derives low-noise symmetric supplies for the sensor from the translation stages' main power supply rail. The sensor signal is passed through this board to another SMA connector so that a screened connection can be made back to the control unit, separate from the noisy motor control signals on the main umbilical cable connection between the translation stage and control unit.

Several variant sensors have been produced, each having different input impedance and gain settings to provide optimal operation across different measurements. One such example has been configured for ultra low input capacitance. The frequency response for this sensor is shown in Figure 6-8. The response shows that the sensor has an input capacitance of $6\,fF$ and an input resistance of$4.5\,T\Omega$. This sets a lower corner frequency of 0.5 Hz and an upper bandwidth of 3 kHz.

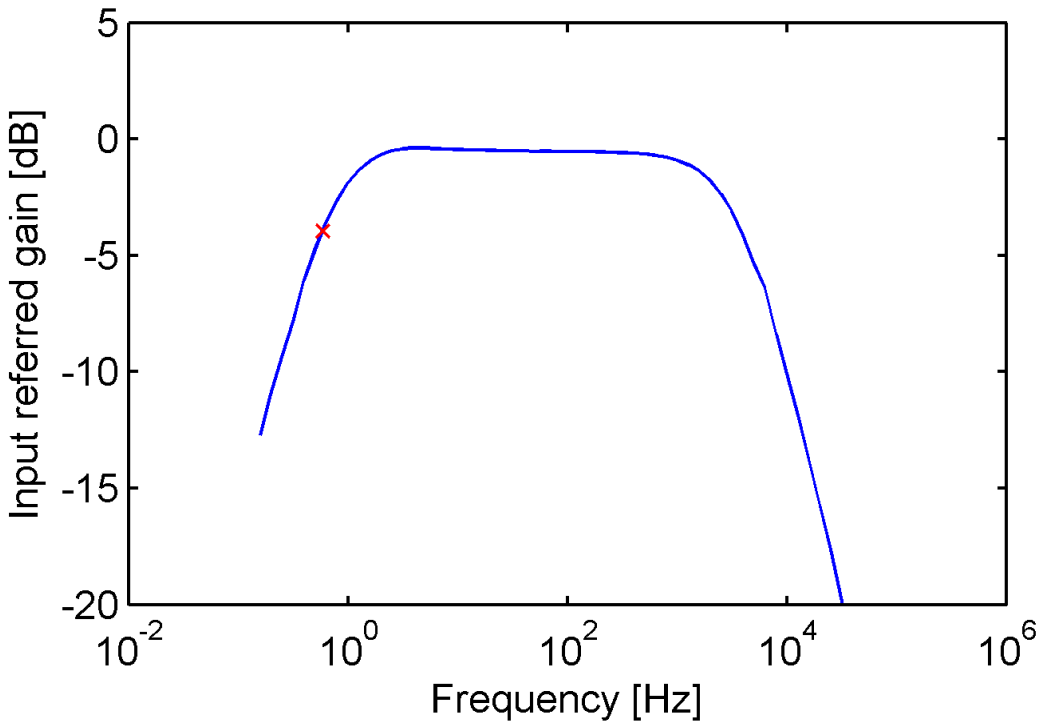


Figure 6-8: Input referred frequency response for an ultra-low input capacitance EP sensors coupled through a 53 fF test capacitor.

6.1.4 Arrays of sensors

Whilst the focus of this chapter, and the experimental results given, relate to the scanned probe microscope, the majority of the methods presented here are equally applicable to 1 dimensional and 2 dimensional arrays of EP sensors. The use of sensor arrays has been demonstrated in several previous works. One of these previous experiments was the previously mentioned array charge scanner, conducted by Beardsmore-Rust and the author (Beardsmore-Rust et al., 2009a), and shall be discussed here. Array measurements have been performed previously at Sussex, most notably (in the present context) in the microscopic imaging work of Gebrial (Gebrial et al., 2006a), but also in other experiments at the macroscopic scale (Clippingdale et al., 1994b) (Beardsmore-Rust et al., 2009d).

The important property of an EPS that lends itself to array applications is the ultra high input impedance. Because the EPS measures electric fields non-invasively, then multiple adjacent sensors can perform simultaneous measurement of electric potential without having any significant influence on one another (Beardsmore-Rust et al., 2009a), or the field which is to be measured (Aydin et al., 2010). The major benefit of using arrays of sensors is the reduction in time required to acquire high pixel count images of electric potential. It is quite simple to demonstrate the potential time saved by array sensing. If one EPS measurement takes some fixed amount of time t, then in order to acquire a square image of $N \times N$ pixels with a single scanned probe will take $t \times N^2$. By instead using an N pixel wide 1-D array of sensors, the time requirement is dramatically reduced to only $t \times N$. Extending the array in both dimension, an $N \times N$ 2-D array of sensors only requires a single measurement time, t, and this time can be on the order of milliseconds. This saving not only represents an improvement in terms of convenience, but also in the ability to monitor dynamical processes.

The scanned probe instrument nonetheless remains a worthwhile endeavour, since it currently is the only method which can offer microscopic resolution. It has not so far been possible to produce arrays of sensor on a micron-scale sensor pitch, though as realisations of individual sensors in highly integrated semiconductor processes proceed

at the time of writing, the ultimate goal of micron-scale 2 dimensional sensor arrays seems to be a near-term possibility. It is however presently possible to produce 1 dimensional sensor arrays on the 1 cm scale using existing conventional PCB fabrication techniques. Such an instrument has been produced, and will be described briefly here so that the methods developed on this instrument can be described later.

6.1.5 1-D Array scanning apparatus

A conventional (optical) office flatbed scanner has been repurposed as a 1 dimensional translation stage for a linear 1-D array of EP sensors, shown in Figure 6-9. The mechanical hardware has been reused, with a microcontroller and USB interface added for interface to a PC running LabView. This hardware has been described by Beardsmore-Rust elsewhere (Beardsmore-Rust et al., 2009a). An array of 16 EP sensors have been designed and constructed by the author. This array fits on the sliding carriage in place of the conventional optical array, so that it can be displaced linearly along the length of an A4 sample mounted above the array of sensors.

An array of 16 electrodes are constructed on a PCB, shown in Figure 6-10. Each electrode is individually guarded around its perimeter. Two separate PCB's of 8 active EPS circuits each are mounted perpendicularly to the board edge. Each electrode has a

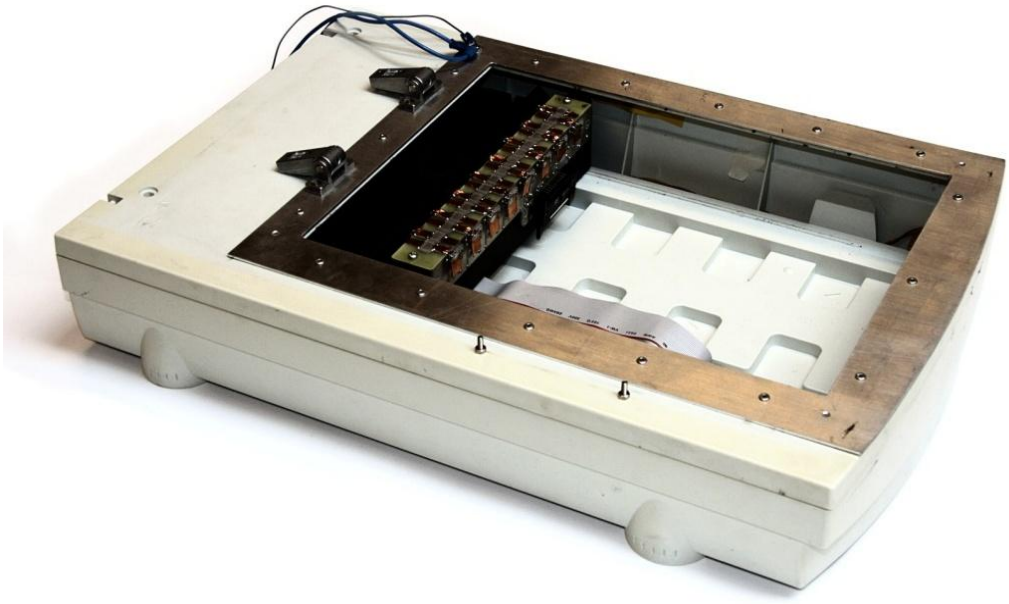


Figure 6-9: 1-dimensional array EPS scanner

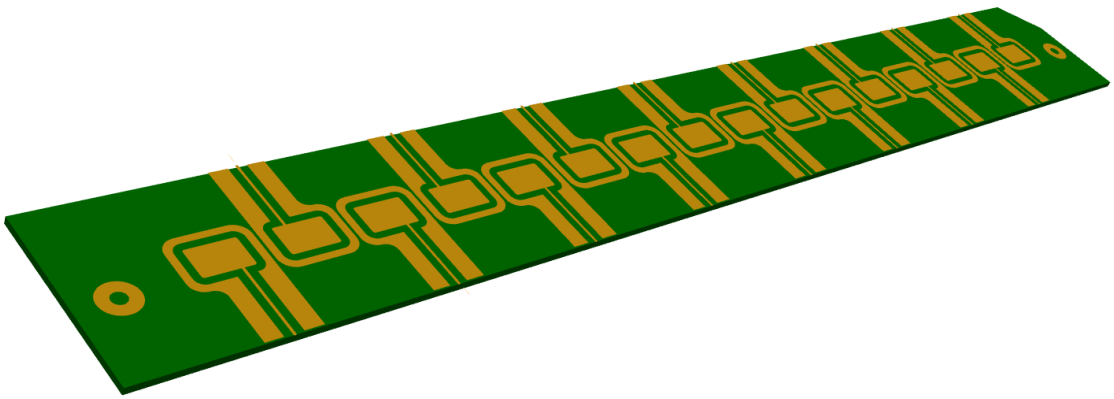


Figure 6-10: A 3D render of a 1-dimensional electrode array printed circuit board.

sensitive area of approximately 1 cm^2 and the centres of each electrode are aligned on a 1 cm pitch. In the same manner as the scanned probe apparatus, this arrangements achieves spatial resolution of approximately 1 cm when the sample is spaced by approximately 1 cm from the electrode.

Each sensor is based on an LMP7721 low input bias current op-amp, and has an un-bootstrapped input impedance of 50 $G\Omega$. The sensor output signals are routed to the USB data acquisition device in the scanner chassis via a multiplexer and a ribbon cable.

6.2 Imaging AC Potentials

When an EPS probe is brought close to a source of electric potential, a capacitor is formed between the electrode and the sample. A capacitive divider is therefore formed between the electrode-source capacitance, C_{es}, and the input capacitance (capacitance to ground) of the EPS, C_{IN}, as shown in Figure 6-11. This divider ratio sets the sensitivity of the microscope. Since the guarding of the input electrode confines the effective area to the diameter of the centre sense electrode, we can use this diameter to approximate C_{es} as a parallel plate capacitor. This approximation has been found to provide the most accurate agreement with experiment, versus more complicated geometries such as the sphere-plane model (Sarid, 2007). This capacitance is then given by Equation 6.1

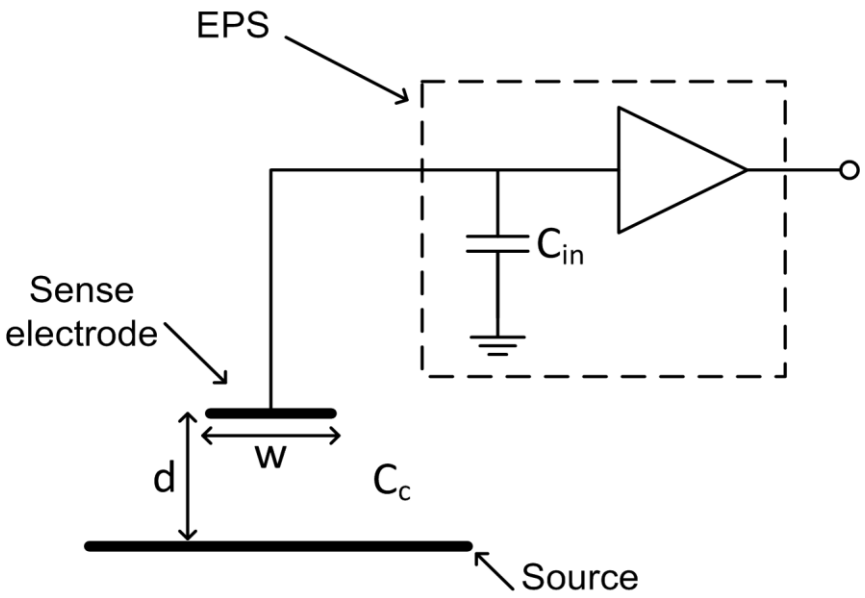


Figure 6-11: Sensor and electrode geometry. C_{es} is the capacitance formed between the sense electrode and the source, C_{in} is the total input capacitance of the EPS sensor and electrode structure

$$C_{es} = \frac{\varepsilon_0 \, \varepsilon_r \, \pi \, r^2}{d} \tag{6.1}$$

Where r is the effective electrode radius and d is the electrode-source separation. The ratio of source potential to EPS output potential is given by

$$\frac{V_{out}}{V_{in}} = \frac{C_{es}}{C_{es} + C_{in}}$$

$$\frac{V_{out}}{V_{in}} = \frac{\alpha}{\alpha + d} \;\; where \; \alpha = \frac{\varepsilon_0 \, \varepsilon_r \, \pi r^2}{C_{in}} \tag{6.2}$$

Using the 5 µm diameter electrode and an electrode-source separation of 5 µm, where resolution is maximized, this ratio is found to be 0.7 for an EPS input capacitance of 0.1 fF, assuming $\varepsilon_r = 1$ in air. The EPS input capacitance is found by measuring the EPS response through a calibrated test capacitor.

With the EPS input referred noise voltage of 10 µV/√Hz, surface potentials of a few tens of millivolts may be detected in a broadband measurement, with scope to significantly improve this sensitivity using narrow band or lock-in measurements. Performing this calculation illustrates the importance of extremely low input capacitance when performing high spatial resolution measurements.

From Equation 6.2 it is clear that the sensor output voltage is proportional to electrode-source separation, d. This then forms the basis of a surface topography measurement. For small deviations about the nominal working distance, the AC output voltage of the sensor can be translated to a measure of electrode-source separation, and therefore the surface topography of the source electrode. The ratio of output to source amplitude is plotted in Figure 6-12 for the 5 µm diameter electrode, calculated using Equation 2.34. For conducting samples this measurement is performed by applying an AC potential to the sample and measuring the sensor output amplitude using a lock-in amplifier. The scanning hardware/software system supplies the necessary AC signal and performs a lock-in amplitude measurement. The error evident in the measured data of Figure 6-12 can be attributed to the mechanical error in the probe height setting of the translation stage since the electrical noise of the sensor is significantly lower than this error.

Thin dielectric samples may also be measured using an identical technique by applying the source AC potential to a conducting plane beneath the sample. For a material of uniform dielectric constant the image produced from amplitude information is purely topographical. Where variations in dielectric constant exist, the according variation in

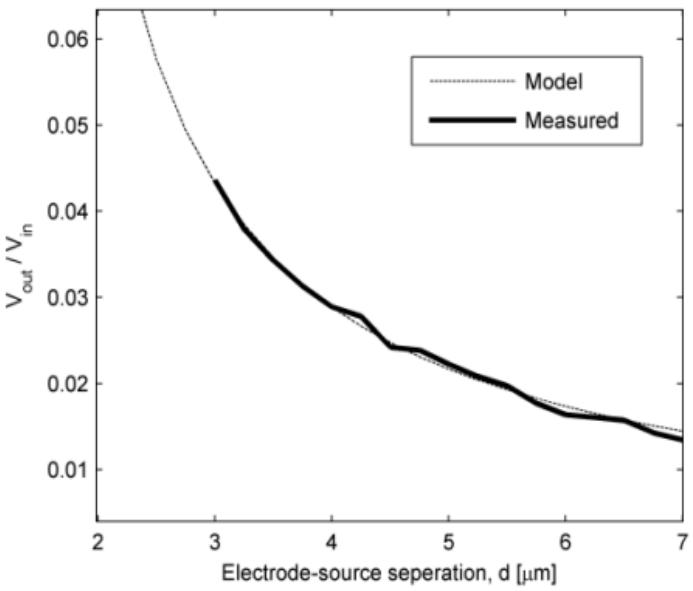


Figure 6-12: Vout/Vin (from Equation 2) for a sense electrode with r = 2.5 µm and a probe input capacitance of 1 fF, as a function of source-electrode separation, d.

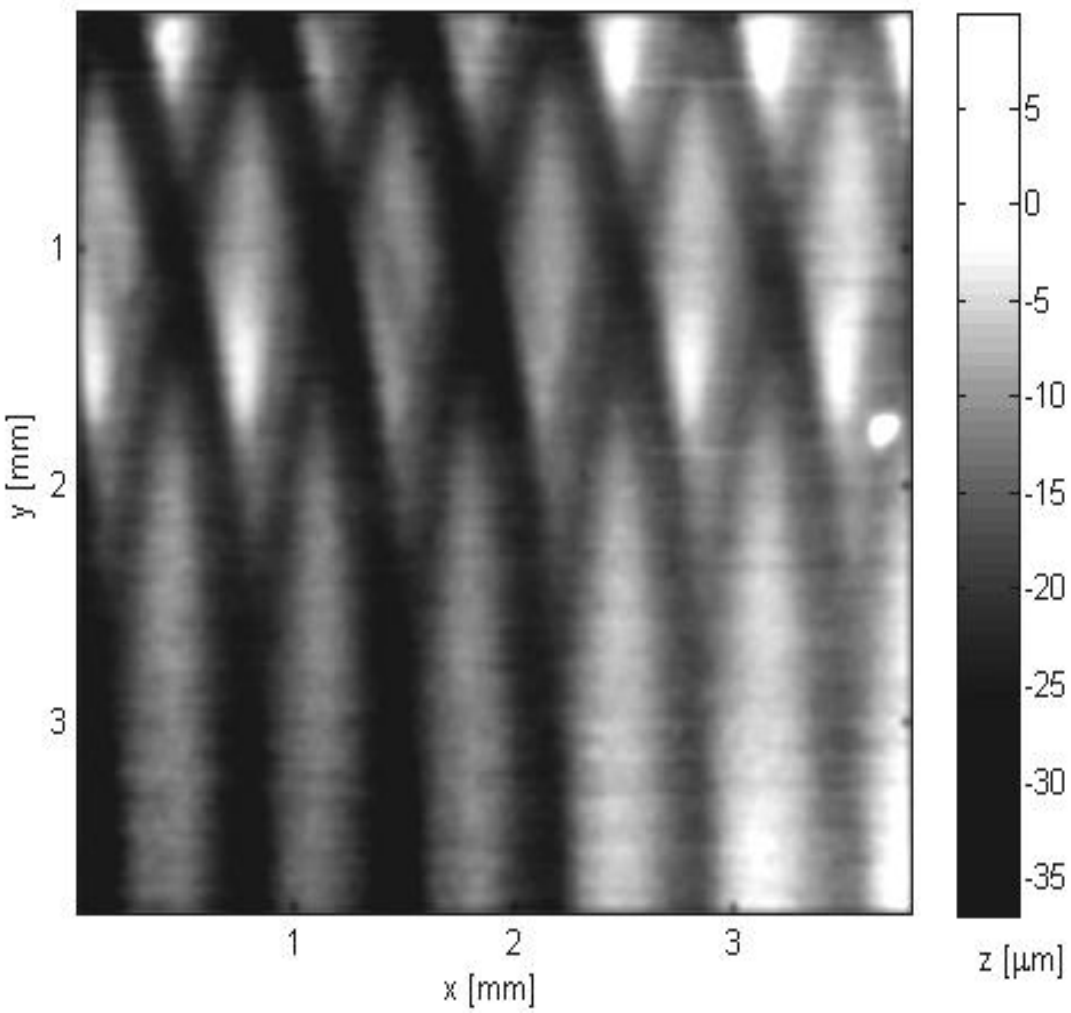


Figure 6-13: Topographical image of a conducting sample.

electrode-source capacitance produces amplitude variations apparent in the final image. In this manner buried defects and discontinuities may be revealed, a property which is of particular use for imaging faults in composite materials. The present system operates at frequencies in the range 10 Hz to 100 kHz, although it is possible to extend this range through the use of specialized high-frequency EPS sensors (Mukherjee, Watson and Prance, 2011).

6.2.1 Results: Conducting samples

The image created by the amplitude of the sensor output, as a function of position, can be translated directly to a surface topography map (Figure 6-13). Electrode-sample separation may be found by solving 6.2 for *d*. This gives;

$$d = \alpha\left(\frac{1}{V} - 1\right) \qquad 6.3$$

This separation value is then subtracted from the nominal working distance (defined at pixel 0, bottom right of image) to give *z*, the height at each pixel, where positive values indicate a high area on the sample.

Figure 6-13 is formed from 90 k-pixels on a 300 by 300 grid. The sample is energised by a 350 Hz sine wave of 7 V_{rms} amplitude. Each pixel is spaced by 12.6 µm, producing a 3.8mm x 3.8mm image. The time required to produce an image is limited by the positioning system velocity and the probe output amplitude measurement time. The maximum speed with the current apparatus is 50 ms per pixel, so that a large image as shown in Figure 6-13 takes 75 minutes to produce. The sample shown here is a surface

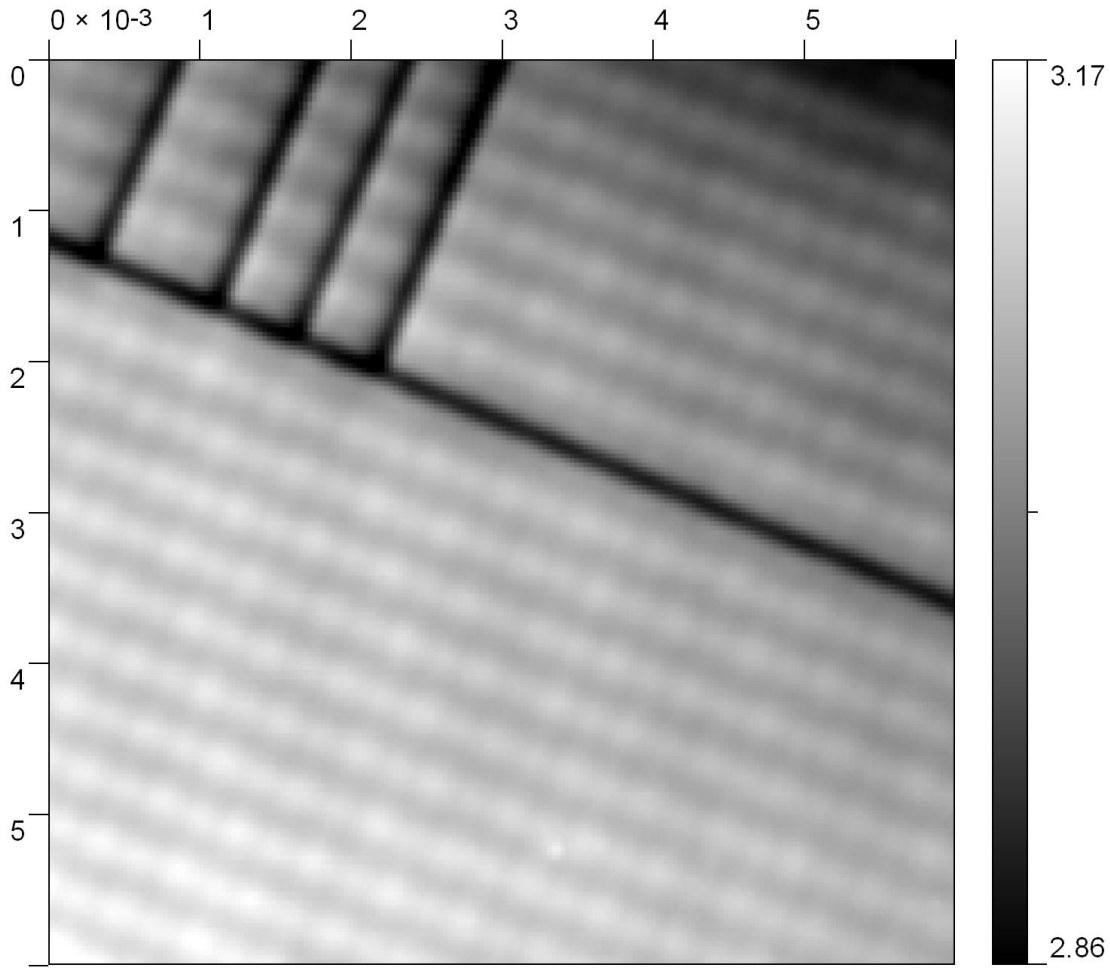


Figure 6-14: Composite fiberglass FR-4 PCB material imaged using a 350 Hz AC signal.

roughness reference, with the image centred over an area having a peak to peak height variation of approximately 30 μm.

6.2.2 Results: Dielectric Samples

In Figure 6-14 an image has been produced by plotting the sensor output amplitude when scanned over a dielectric sample. An AC signal is applied to a source electrode underneath the sample, and the resulting potential above the sample is measured by the probe. This sample has had lines machined (approximate depth 100 µm) into the otherwise flat surface to demonstrate the visibility of surface topography variations in a dielectric sample. Furthermore, the parallel lines across the entire image are due to the underlying glass fibre mat structure, which produces a variation in output amplitude as a result of the slightly different dielectric constants of the glass mat and resin. This dielectric contrast should make it possible to detect buried defects in dielectric materials such as voids or water ingress.. The Z axis scale is output voltage in units of V rms, and the source voltage is 7 V rms. The image consists of 400 x 400 pixels at 15 µm pitch.

6.2.3 Conclusions

The AC imaging mode forms the base imaging mode of the SEPM. The images produced provide a quantitative measurement of surface topography over a useful microscopic length scale. The sample type is not strictly limited to conductors, as in STM, and no costly optics are required as in 3D optical microscopy. The measure of surface topography may be used as a surface reference in conjunction with the other imaging modes of SEPM which rely on a known surface topography.

6.3 Imaging AC Currents

When a sample is driven by a current source, then a potential distribution can be created across the sample. This is achieved by applying an AC current at one point, and

terminating the current into a load or short to ground at another point. The direction of current can be chosen in order to produce the potential distribution in the plane of interest, in SEPM this will usually be chosen so that the gradient exists along the surface to be scanned. From the potential distribution, some knowledge of the local impedance of the sample may be inferred.

Such potential distributions are utilised in numerous applications as a method for imaging the spatial distribution of impedance, such as in electrical impedance tomography (EIT) (Chesney, Isaacson and Newell, 1999), where the computed potential distribution is used to non-invasively image tissues in medical subjects. Related techniques are applied over larger length scales; in petrophysics Electrical Resistance Tomography (ERT) is applied to large geological structures such as earth banks (Chambers et al., 2008) in order to assess moisture content and hence geological stability.

By measuring a potential distribution across a surface, SEPM can be used to non-invasively detect faults and discontinuities in structures which have an otherwise uniform impedance. Using this method, it has previously been shown that faults in carbon composites materials can be detected non-invasively (Gebrial et al., 2006b).

In SEPM the probe output potential is principally a function of two variables; the surface potential and the coupling capacitance between sample and probe. This latter capacitance is dependent on the sample-probe distance, and so forms the basis of the topography measurement. In order to determine the surface potential from the probe potential alone, then either the sample-probe distance must be constant (the sample must be flat), or the sample-probe distance must be known. It is possible to determine the sample topography by AC voltage measurement, so that an AC current measurement can be performed and surface potential subsequently calculated. However, it would be far more convenient if both topography and surface potential could be measured simultaneously. By modifying the probe so that its input impedance is dominated by a resistance at the measurement frequency, then a measurement of phase can be used in order to determine the sample-probe capacitance, and hence separation. This phase shift

is due to the resistor-capacitor circuit formed between the sample-probe capacitance and the input resistance of the probe. The probe output amplitude remains a function of both the sample-probe capacitance and the surface potential.

6.3.1 Core sample potential distribution imaging

In this experiment, the fine scale potential distribution across a geological core sample is imaged. It is proposed that this potential distribution can be used to derive the rock resistivity, and hence porosity. Porosity is one of several metrics used in characterisation of core samples that provide important information on geological history and environmental change(Rothwell and Rack, 2006). A multitude of related geological resistivity imaging methods exist, across a broad range of length scales. This result demonstrates an extension towards high resolution with a non-contact probe.

An EP sensor with a reduced input resistance of 1 $G\Omega$ has been constructed so that the input impedance is resistive at low-audio frequencies of several hundred Hertz. The probe output amplitude is shown to be dependent on probe-sample separation and surface potential, whilst the output phase is shown to be a function of probe-sample separation only.

A Penrith sandstone core sample has been obtained (Figure 6-15). The sample dimensions are 230 x 70 x 10 mm. A current is driven across the longest dimension of the sample by two stainless steel plate electrodes. These electrodes are embedded into a

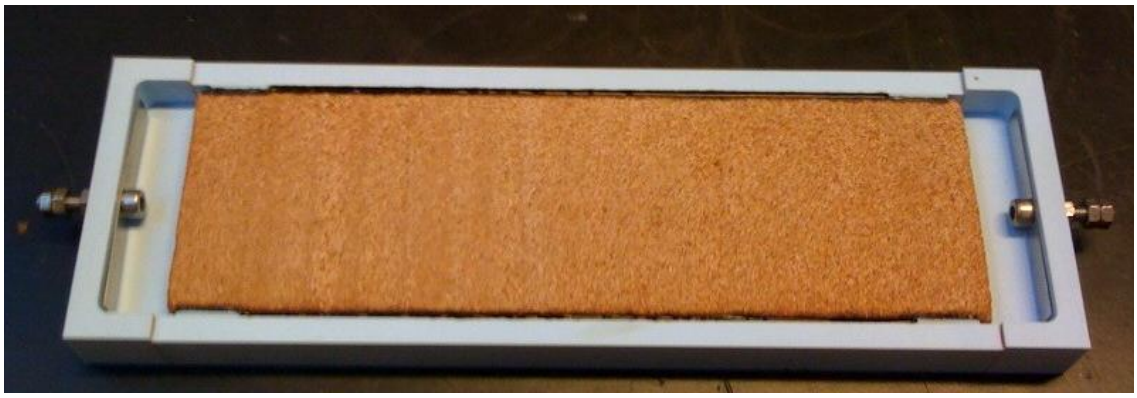
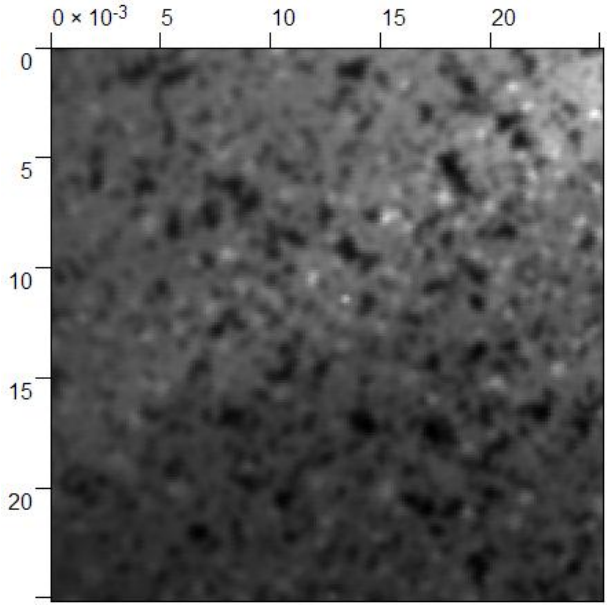
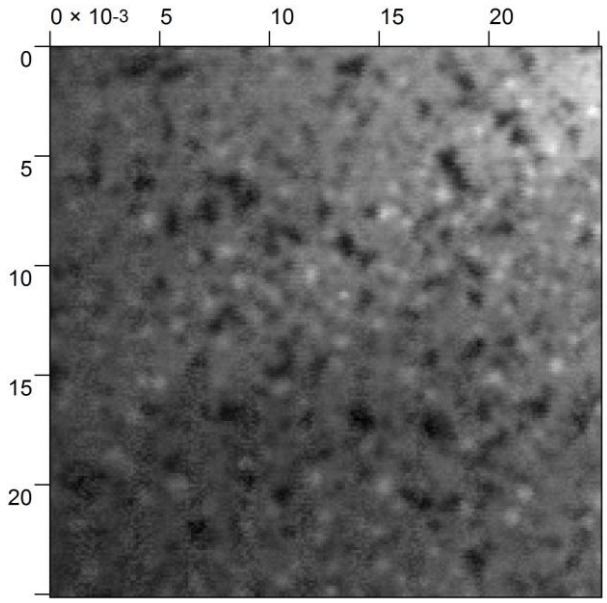


Figure 6-15: Sandstone core sample mounted in a saline bath with stainless steel electrodes.

bath into which the sandstone sample has been mounted. The bath allows saturation of the sandstone sample with brine. The brine is a conductive solution that is the predominant current conduction medium. The sandstone itself is mostly insulative, so it is in fact the potential distribution of the brine that is imaged. The observed potential distribution indicates the brine concentration and hence rock porosity.



(a)



(b)

Figure 6-16: (a) Amplitude and (b) phase images of a 25 x 25 mm section of a Penrith sandstone sample, composed of 200 x 200 pixels of 12.6 µm pixel pitch.

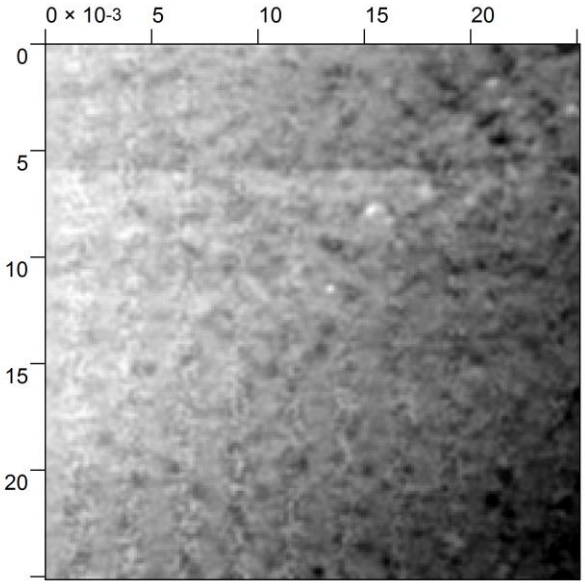


Figure 6-17: Subtraction of normalized phase data from normalized amplitude enhances potential gradient.

In the following results, the modified EPS sensor has been used with a $5\ \mu m$ probe. A $7\ V_{rms}$ voltage source with a $120\ \Omega$ series resistance is used to current drive the sample. The sample is prepared by overnight soaking in a brine solution prepared from distilled water with NaCl added at a 40 g/L concentration.

In Figure 6-16 a set of amplitude and phase images, acquired simultaneously, are shown. The potential slope (which according to the direction of current flow should descend from left to right) is not immediately evident across this small area. As such the two images appear identical on first inspection. Though in this experiment the analytical extraction of surface potential and topography from these images has not been attempted, it is possible to demonstrate the separation of surface topography and potential by performing a simple subtraction of the normalized amplitude and phase data. Though this naive scaling does not correctly cancel topography variations from the amplitude data, it does provide a certain (imperfect) amount of topography rejection from the image, thereby enhancing the visibility of the potential gradient. The result of this calculation is shown in Figure 6-17.

In order to measure the large-scale structure of the sandstone sample, a 1-dimensional line scan has been performed, shown in Figure 6-18. This scan was performed with a

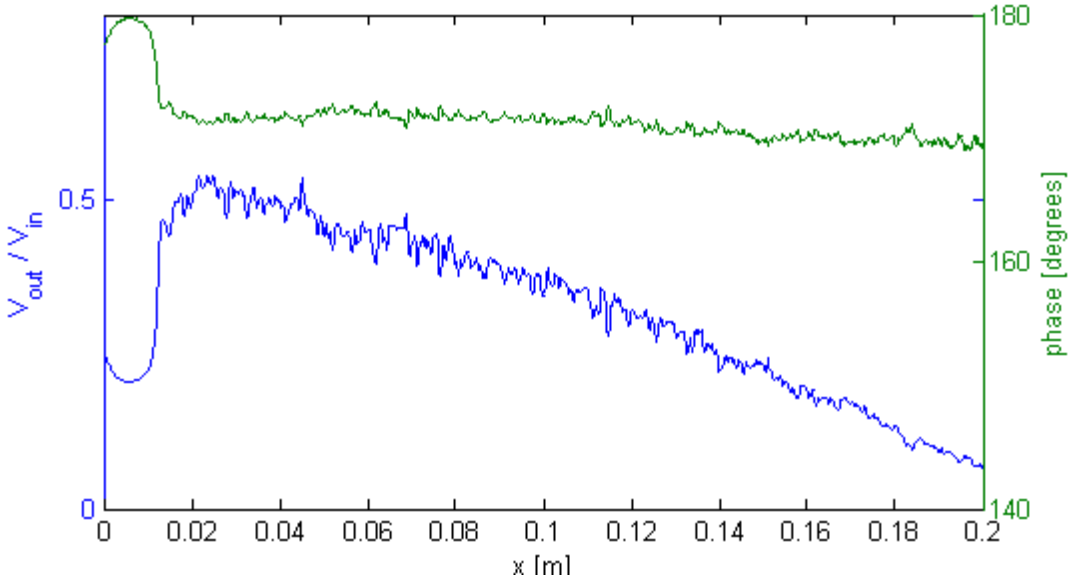


Figure 6-18: Sandstone core sample mounted in a saline bath with stainless steel electrodes. The phase response (upper trace) is shown along with the amplitude response (lower trace).

low resolution, 0.2 mm diameter electrode and consists of 2000 data points spaced by 120 μm. Across the full length of the sample it is clear that the output amplitude is dependent on the source potential, whilst the phase angle is not.

6.3.2 Conclusions

Current mode measurements can be used to image potential distributions, and hence local resistivity variations. Using a modified probe, and by measuring both amplitude and phase, it is possible to simultaneously and independently measure surface potential and surface topography.

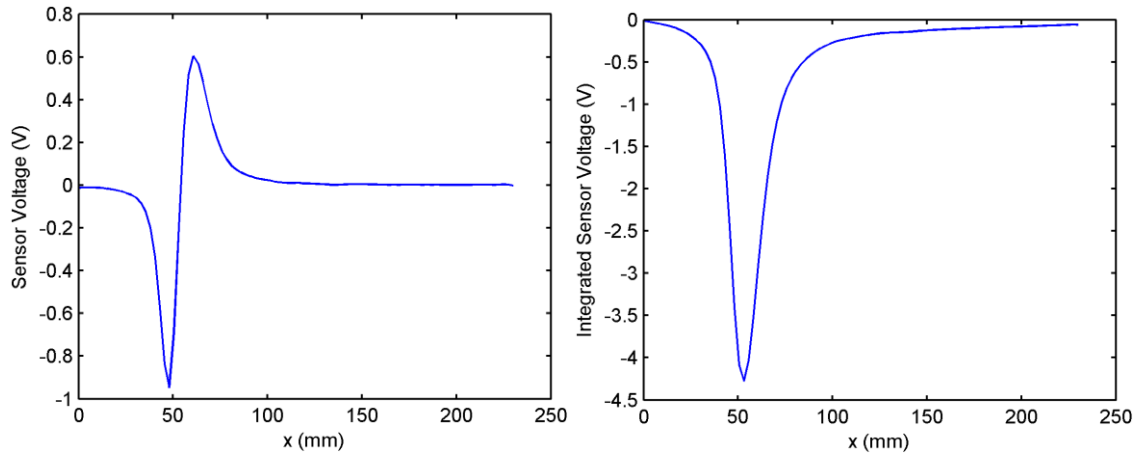
6.4 Imaging DC Potentials

The imaging modes discussed so far have all been restricted to AC potential measurement only. This limitation is imposed by the non-contact capacitive coupling used with the scanned probe. This limitation could of course be overcome by using a

contacting probe so that DC potentials can be measured. However, such a probe requires careful design of the probe such that it is robust enough to make contact with a sample. To make contacting measurements at very high resolution, as in 'tapping-mode' AFM (Quate, Gerber and Binnig, 1986), careful control of probe position is required so that tip or sample damage does not result. Such careful probe control usually rules out the translation stages used in the present scanned probe stage, and therefore limits scan-area and speed.

Instead, DC potentials may be measured by a capacitive probe with little added complexity over, and with fewer of the disadvantages of, a contacting probe. Electrical potentials may be measured on conductors, or on dielectrics due to static charges.

A novel method has been developed for the non-contact measurement of surface charge and DC potentials (Beardsmore-Rust et al., 2009a). Surface charge measurement is achieved in a method similar to the capacitive probe (Davies, 1967), in which surface charge is measured by the voltage induced on an electrode when it is brought in proximity with a charged surface. When the probe approaches the charged surface a voltage is induced on it, governed by the equation $\sigma = kCV$. Where σ is the surface charge density, C is the probe input capacitance and V the probe output voltage. The constant k has been introduced to account for the probe amplification and probe geometry. Though it may be possible to determine the constant k analytically, in all the experiments presented here k has been found (respectively for each measurement geometry and probe configuration) by using a known test charge and observing the probe output voltage(Beardsmore-Rust et al., 2009a). In conventional capacitive probe measurements the resistive part of the input impedance of the amplifier is neglected (it is assumed to be infinity) so that the probe output voltage due to a static charge remains constant over time. This simplification is quite justified over normal measurement time scales since the electrometer amplifiers used in such measurements generally have an input resistance which is very large, and an input capacitance of several tens or hundreds of pico-Farads so that the decay time constant is long. These conventional measurements therefore rely on the DC accuracy of the electrometer used, and as such



(a) **(b)**

Figure 6-19: (a) probe output pulse amplitude for a line scan over a small charged region on a PTFE sheet is proportional to surface charge gradient. The integrated output (b) is proportional to absolute surface charge.

suffer from issues of long-term drift. The long-time constant enforces periodic zeroing of the amplifier (Faircloth and Allen, 2003).

In contrast to conventional capacitive electrometer probes, the EPS has excellent DC stability with zero input bias current, and a much lower input capacitance than traditional capacitive probes, of as little as $10^{-16}\,F$. Due to the ultra-low input capacitance, in combination with an input resistance which is generally $1\,T\Omega$ or less, the input time constant is short (of the order milliseconds). As a result any induced probe potential quickly decays and the probe settles back to zero-volts output. This decay means that it is impossible to measure DC potentials in the conventional manner. Instead, a dynamical measurement method is used. In this method, the probe movement required for scanning probe microscopy is exploited to produce a time-dependent probe output. In moving from one measurement position to another, a voltage is induced on the probe that is proportional to the change in the surface charge from the initial position to the final. This induced voltage is observed at the probe output as a pulse waveform. The pulse height is used as a measure of the spatial charge gradient.

To illustrate the method, in Figure 6-19 the probe output pulse amplitude is shown for a single sensor scanned linearly across a PTFE plastic sample. This pulse amplitude is proportional to the surface charge gradient between each measurement location, so that

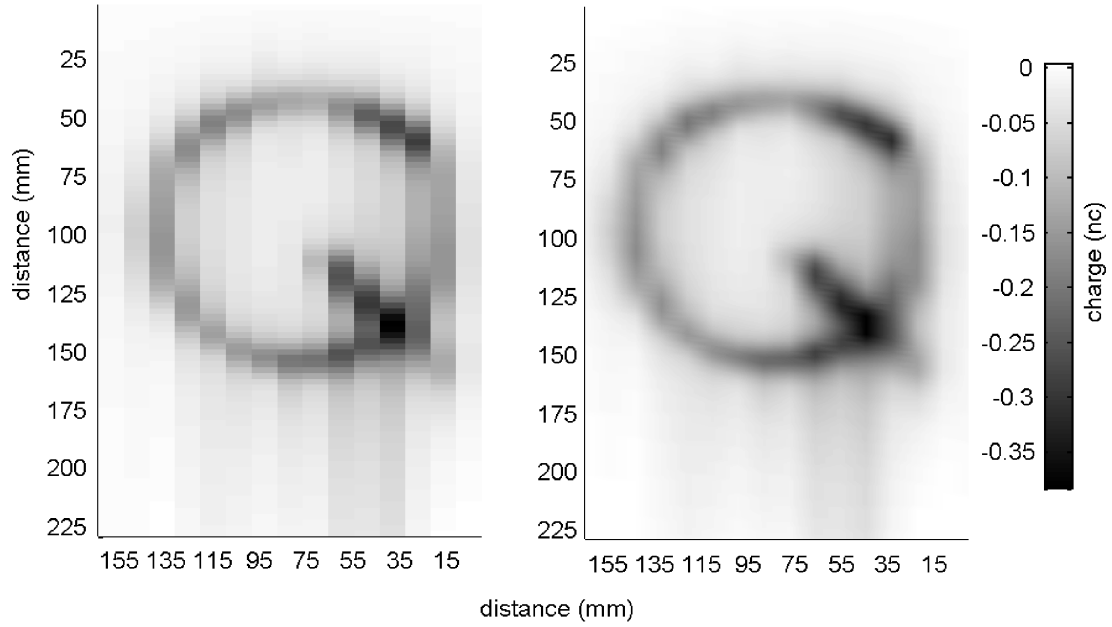


Figure 6-20: Charge distribution due to tribocharging on a 230 x 160 mm polythene sheet. (left) raw data consists of 16 x 92 pixels and (right) interpolated data.

numerically integrating along the path of the sensor gives the absolute surface charge density.

This method eliminates DC errors due to the probe amplifier and requires no periodic zeroing. This technique has enabled the measurement of surface charge density with high sensitivity and low noise (Beardsmore-Rust et al., 2009a). The very low input capacitance of the EPS overcomes the attenuation of signals when using very small electrode areas to enable high spatial resolution surface charge measurements of up to 5000 dots per inch (dpi) (Watson et al., 2010a).

The measurement of DC potentials, rather than surface charge density, is identical except that the probe output voltage is no longer governed by the equation $Q = CV$, but is a simple function of the capacitive divider formed between the probe-sample capacitance and the input capacitance of the probe.

6.4.1 Macroscopic 1-D array charge imaging

Initial experiments employing the static charge measurement method described here were conducted on a 1-D array scanning apparatus (Beardsmore-Rust et al., 2009a).

This apparatus was described earlier (Section 6.1.3). Due to the ease with which an image can be formed on a thin sheet of plastic by triboelectric charging, this has been the basis of these early charge imaging experiments. Triboelectric charging, or contact electrification (Fuhrmann, 1978), is the process of charge transfer by contact or rubbing. Using nothing more than a finger, it is possible to create a charge distribution on a thin ($\sim 50\ \mu m$) sheets of plastic. The finger may be used to draw any pattern. The relatively low level of charge deposited in this process is nonetheless easily measured by the array scanning apparatus. In Figure 6-20 an image of the charge distribution on a polythene sheet is shown, where the character Q has been drawn out by a finger.

These initial works were conducted in partnership with Beardsmore-Rust, who performed additional experiments and used the device to form a quantitative tribo-electric series (Beardsmore-Rust et al., 2009b).

6.4.2 Imaging electrostatic fingerprints

Despite the rapid development of forensic science techniques, classic fingerprint evidence is of increasing importance particularly for biometric identification purposes (Ratha, Connell and Bolle, 2001)(Jain, 2007). It remains a primary forensic method of identification in many criminal cases and has stimulated recent work aimed at quantifying the error rate in matching fingerprints (Saks and Koehler, 2005) and also at a deeper understanding of the mechanism of pattern formation (Kucken, 2007). While many techniques exist for enhancing fingerprints on a variety of materials (Thomas, 1978), they all rely on either visible deposits (Worley et al., 2006) or hidden (latent) fingerprints resulting from the transfer of residues from the finger to the surface (Scruton, Robins and Blott, 1975). However, it is extremely difficult to establish even an approximate timeline of events from fingerprint evidence alone. Simple classification as either recent or old represents the state of the art (Thomas and Reynoldson, 1975) and is unsuitable for evidential purposes. Results are presented here for an alternative, new technique which images the electrical charge deposited when a finger contacts an electrically insulating surface (Watson et al., 2010b)(Watson et al., 2011). The images

have a spatial resolution appropriate for identification purposes, and are of comparable quality to conventional fingerprint images. Furthermore, the decay of the charge image with time can be observed and has two major implications. First, this method does not suffer from the background noise caused by a history of old fingerprints and second, it has the potential to determine the time sequence of recent fingerprints. An additional benefit over conventional latent fingerprint development techniques is its non-destructive nature, allowing subsequent measurement of the fingermark after charge imaging. The method is applicable to insulating sheets, such as most modern plastics, and has been tested on PVC, PTFE, and Acetate sheets.

The mechanism which produces an invisible surface charge fingerprint on a plastic is known as triboelectric charging. This is the familiar but poorly understood process by which insulating materials acquire charge as a result of contact or rubbing (Fuhrmann, 1978). When an object, conductive or insulating, is brought into contact with such a material and subsequently removed a small amount of charge is deposited on the insulating material. The exact quantity of charge produced is largely material dependent and is related qualitatively to the triboelectric series, which ranks materials according to their tendency to charge upon contact (Diaz and Felix-Navarro, 2004). The surface charge distribution produced during tribocharging is confined to the points of contact, and therefore serves as an impression of the contacting object. For common plastics this spatial charge distribution decays below measurable levels over a period of days or weeks (Beardsmore-Rust et al., 2009b). During this slow charge decay process the spatial definition of the charge distribution remains intact with the absolute level of the charge being reduced, rather than spreading spatially.

Here results are presented which were obtained using a coaxial probe with a 25 μm diameter sense electrode, capable of resolving features with 100 μm spatial resolution (250 dpi) and minimum detectable surface charge density of 5 pCcm-2.

Samples of 50 μm thick clear PTFE sheet were used. No sample preparations were necessary before surface charge imaging, nor were the materials discharged by ionizing air after removing from packaging. Natural fingerprints were applied to the plastics by a

single donor, after washing the hands with soap and water before air drying. The donor finger was brought gently into firm contact with the PTFE sheet and removed again, the whole process taking approximately 1 second.

Comparison fingerprint images were obtained by a commercial fingerprint sensor and from an ink impression respectively. The fingerprint sensor is a solid-state active capacitance device (model MBF200, Fujitsu Inc.) of the single touch variety (not sweep type) which records a 500-dpi fingerprint image. The ink impression was produced on paper and scanned by a standard flat bed scanner at 500 dpi.

The image obtained from the scan of absolute surface charge density is shown in Figure 6-21. Because the PTFE material is not discharged by ionizing air, this is likely to leave a large magnitude but spatially uniform surface charge on the plastic. Creases in the plastic are highly visible in the surface charge scans partially due to the charge produced on the surface during the crease formation, and from the tendency of the crease to produce a large charge gradient. The high spatial and charge resolution of the EPS

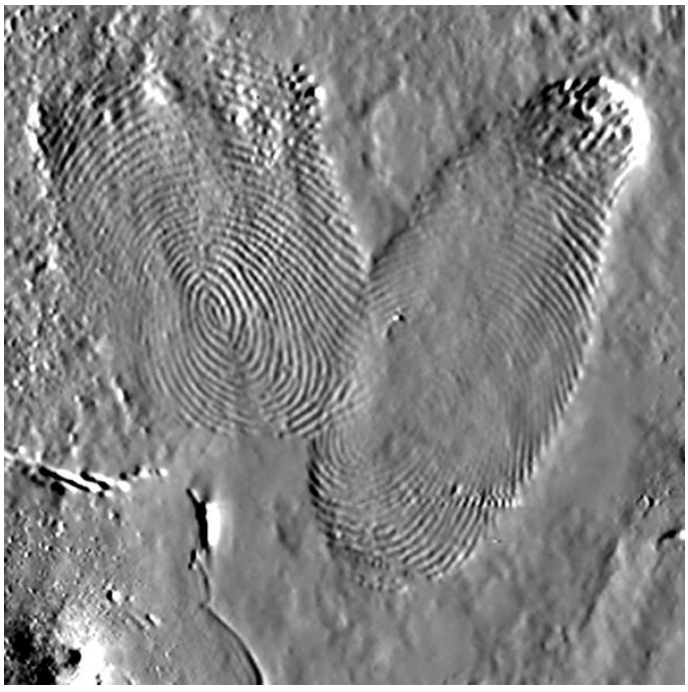


Figure 6-21: Two fingerprints produced by momentary contact of the index and middle fingers respectively on an 50 µm thick PTFE sample. Image size is 36 mm x 36 mm and pixel pitch is 120 µm. The colour range from black to white corresponds to 1 to -1 nC cm ^{2} respectively.

scanning probe reveals a latent electrostatic fingerprint. A single contact by a finger leaves a charge impression on the insulating plastic surface, which may be partially confined within the surface of the plastic itself, and also within the deposits left behind by the finger contact. No special preparations or development processes are required before imaging and the measurement is completely non-destructive. This means that, if necessary, the measurement may be repeated, since the charge distribution is undisturbed. Furthermore, the latent fingerprint is left intact so that subsequent forensic techniques may be applied to the sample, such as conventional latent fingerprint imaging or DNA material collection. This method therefore complements the non-contact Scanning Kelvin Probe method (Williams and McMurray, 2007) for latent fingerprint imaging which also preserves DNA material but is applicable to conducting surfaces only.

The latent fingerprint charge images obtained by EPS charge scanning are of sufficient resolution for forensic identification. Figure 6-22 compares a latent fingerprint charge image with images of the fingerprint obtained directly from the finger by passive capacitance and optical methods respectively. Standard identification features in the ridge pattern such as bifurcations and ridge endings are observed in the image obtained

Figure 6-22: Images of a fingerprint obtained by; (a) charge scan of the latent print on a 50 µm thick PTFE sample cropped from Fig. 1; (b) directly from the finger by a commercial capacitive fingerprint sensor IC (Fujitsu MBF200); and (c) optically scanned from an ink fingerprint impression. All images have been adjusted for best contrast. Comparison of the 4 circled features reveals a high degree of correlation between all 3 methods.

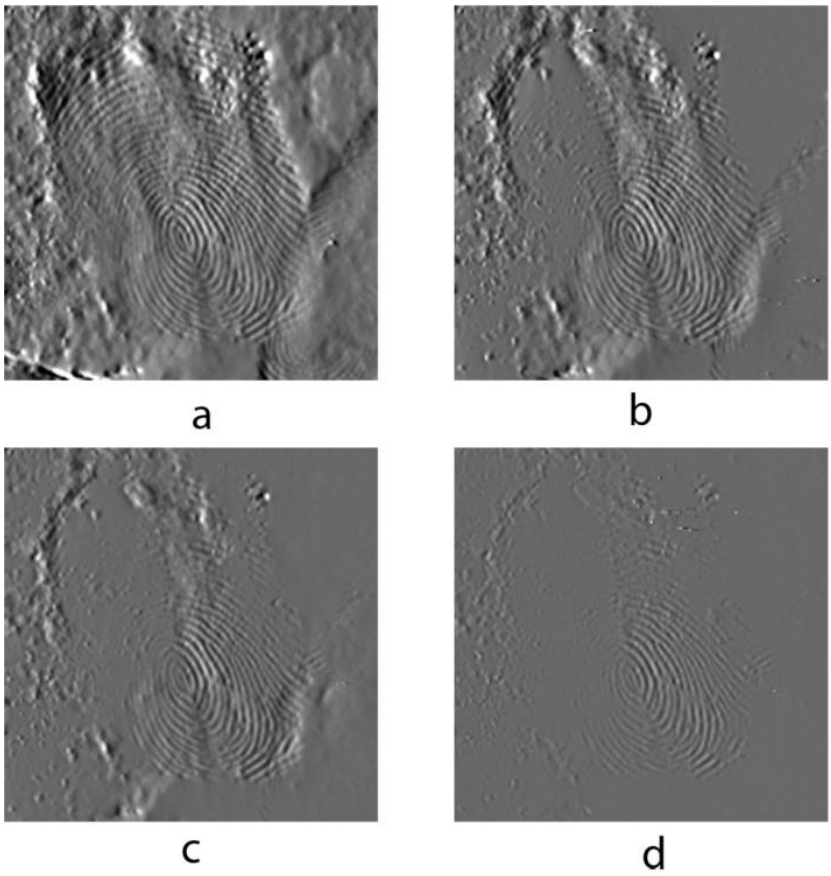


Figure 6-23: Measurements of surface charge density on an 50 µm thick PTFE sheet; (a) immediately after application, (b) 5 days after application, (c) 14 days after application and (d) after exposure to ionized air.

by charge scanning. Conventional fingerprint analysis techniques may therefore be applied to latent fingerprint charge images (Maio et al., 2009). Whilst it is undoubtedly useful that a single apparatus could be used for both latent fingerprint imaging and surface charge measurement, it may be more convenient to utilize the surface charge measurement for timeline estimation only and utilize a conventional imaging technique for fingerprint imaging.

Figure 6-23 shows the decay of a charge image over a period of 14 days. The definition of the latent image remains intact throughout, although the overall level of charge is seen to diminish. Figure 6-23 shows the image when the sample has been discharged by ionizing air. A weak fingerprint image remains visible. This can be attributed to several effects; the inability of ionized air to completely remove any surface charge, and differential discharging between the bare PTFE material and the areas where fingermark residue is present. The decay of charge over time gives latent fingerprint charge images

the property, unique in fingerprint imaging, of strong time dependence. This property has two clear benefits; very old fingerprints are not visible in charge imaging; and it may be possible to date or time-sequence recent prints. The amount of charge deposited by a finger contact on a given insulating material is dependent on the material and nature of the contact, and largely independent of the charge being carried on the finger. It may therefore be possible to make an estimate of the initial charge.

The charge decay versus time for a single pixel of a fingerprint image on a PTFE substrate is shown in Figure 6-24. Such a curve is easily obtained for any given material using the present charge imaging method. A clear exponential decay is observed, with additional variations synchronized with the diurnal cycle. At certain points the graph indicates an apparent increase in surface charge. This is caused by environmental conditions affecting the relation between actual surface charge and sensor output voltage, and is therefore erroneous.

An exponential curve is fitted which gives charge Q at time t as, $Q(t) = Q_0\, e^{-t/\tau}$ where τ is chosen for the best fit to the graph, and Q_0 the charge at time $t = 0$. The charge decay rate, τ, is material dependent and is easily determined experimentally using the present technique. It has been previously shown that repeated measurements

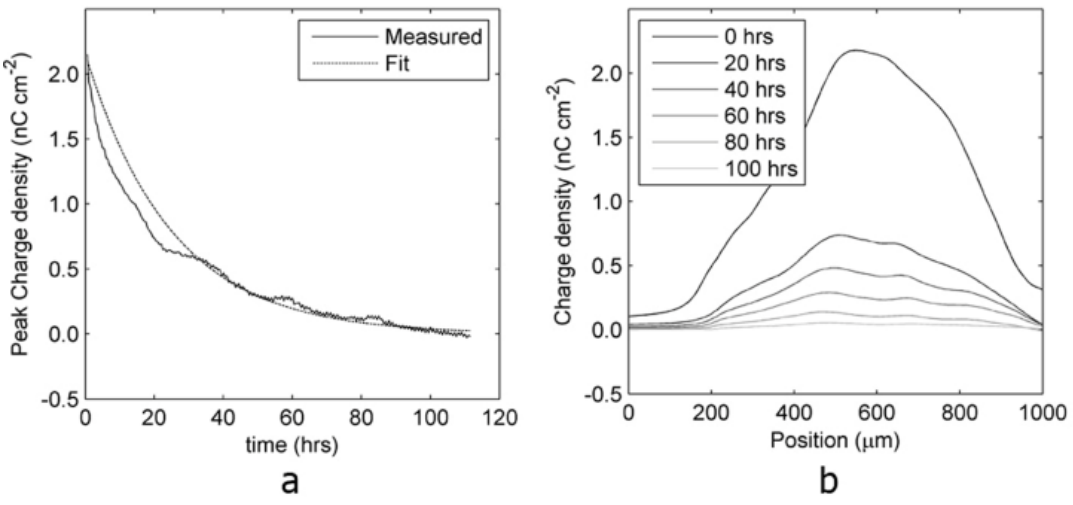


Figure 6-24: (a) Plot of the peak surface charge density of a single latent charge fingerprint ridge deposited by a momentary finger contact on an 50 μm thick PTFE sheet. Measurements are repeated at 30 minute intervals for 110 hours. An exponential decay curve is fitted (see main text) with τ = 25 hrs. (b) Profile of the latent fingerprint ridge used in a.

made using this technique have no effect on the charge decay rate (Beardsmore-Rust et al., 2009a), demonstrating the non-destructive nature of the measurement. Not only is the surface charge distribution undisturbed, but any surface deposits from the fingerprint also remain intact. Whilst attempts have been made to quantify the triboelectric charge for a given material, variations in composition and surface treatment make producing a universal data set difficult (Lowell and Akande, 1988). Instead it is more useful to have the ability to make triboelectric charging and decay-time measurements in the lab for a given sample. This is easily achieved for any material using the EPS scanning system.

Whilst the probe responds only to surface charge (and not also to surface topography variations in the absence of any surface charge) it is not clear from the present results whether the majority of the surface charge is confined to the plastic sheet itself or is predominantly present in the fingerprint deposits on the surface. Evidently, if a surface charge is on a ridge on the plastic surface, it shall produce a larger probe output voltage than if it were further away, on the surface of the plastic. Experiments with different donor finger preparations (solvent cleaning, or unclean fingers with significant sebaceous material) would resolve the independent contribution of the triboelectric charging effect of the plastic surface and the contribution of charge retained in the fingerprint deposits.

500 dots per inch (dpi) is defined as the standard for forensic fingerprint images (ANSI/NIST-ITL, 2007). In order to demonstrate the resolution achievable by the scanning probe we have imaged the DC potentials on a ‘comb’ structured electrode sample. This planar, etched sample consists of 2 interspersed conductive ‘comb’ electrodes on a glass substrate. By providing separate connections to electrical ground and a DC voltage source, a regular pattern of DC and ground surface potentials is produced. Such a sample is necessary to demonstrate the resolution of scanning probe microscopes, since it would otherwise be possible to produce apparently high resolution scans by using a very small pixel size, without considering the actual spatial sensitivity of the probe itself.

Figure 6-25 demonstrates the ability of the EPS scanning probe to resolve a patterned comb electrode with 12.5 line-pairs per mm with good acuity. This corresponds to a true 635 dpi resolution, in excess of the 500 dpi standard. Imaging of voltage source potentials cannot however be expected to give a true indication of the spatial resolution when measuring surface charge due to the additional affects of neighbouring charges on the probe. However, with the presence of a ground plane underneath the sample, and the restriction that the sample thickness be comparable to that of the spatial resolution of the measurement, surface charges behave more like voltage sources and couple with the probe in much the same way as a true voltage source.

6.4.3 Conclusions

The measure of the charge decay rate and the quantitative measure of charge obtained by the scanning EPS system facilitates an estimate of the age of a fingerprint. The unique ability to obtain this information could be of profound use in forensic

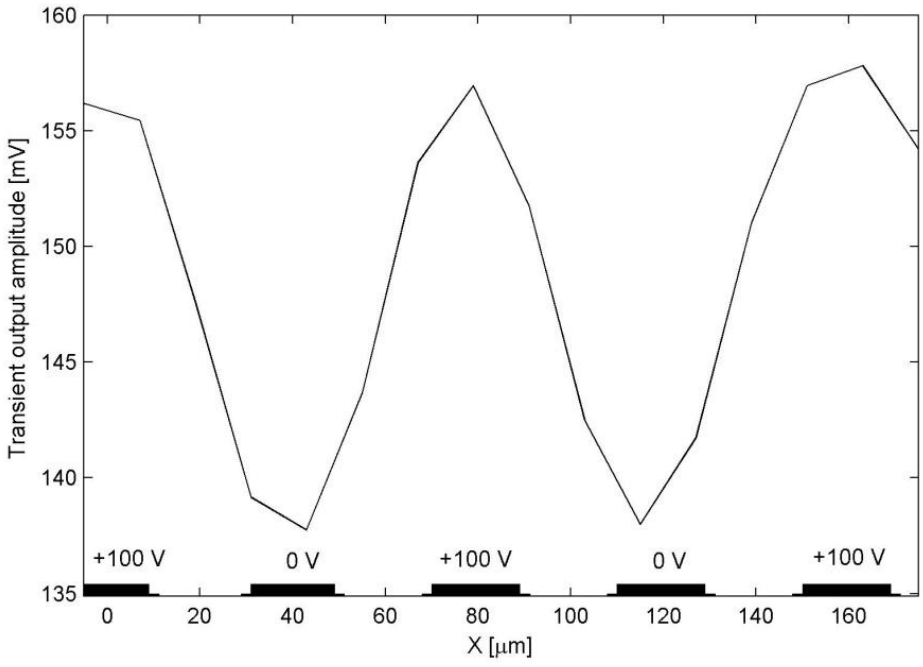


Figure 6-25: Comb electrode sample scanned with 12 µm pixel size using the 5 µm probe at a fixed probe-sample separation of 5 µm. The comb electrode structure is indicated along the bottom of the plot; 20 µm wide strip electrodes are separated by a 20µm gap. +V is applied from a DC power supply at 100V.

investigations. We have shown that the images obtained resolve common fingerprint features used for identification, and that the quantity of charge in the latent fingerprint is strongly time dependent. The scanning EPS as a surface charge imaging system has further applications in materials testing and fundamental research into charge migration processes, with current research effort being directed toward improvement of spatial resolution. At present, images with 5 µm spatial resolution have been acquired with the scanning EPS system. The present measurements have all been conducted on thin sheets of insulating materials (~50 um thick). High resolution measurement of significantly thicker samples presents additional difficulty, since the measurement probe is influenced by space charge within the bulk material. This problem has received significant attention in published research and has been partially addressed by inverse matrix techniques (Faircloth and Allen, 2003)(Okabe and Kumada, 2007). The development of high density arrays of Electric Potential Sensors is a long term goal of the ongoing sensor development work. Such an instrument would bring about a dramatic improvement in measurement time for surface charge imaging.

6.5 Conclusions

In this chapter several measurements have been described which can be performed at spatial resolutions of up to $5\ \mu m$. In addition to this high resolution lower resolutions are readily achieved by simple adjustment of the probe-sample separation, with the additional facility to utilise large diameter electrodes for increased electrical sensitivity at these lower resolutions.

This selection of measurements broaden the usefulness of the scanning probe apparatus by providing several complementary techniques that may be applied to both conducting and dielectric samples.

A 1-D array apparatus has also been described. This instrument suggests an additional extension to 2-dimensional array sensors. Since the compatibility of the EPS sensing

technology with array configurations has been shown, and several useful applications identified, there is considerable motivation for the development of high resolution 2 dimensional array sensors, a goal which may be achieved through the use of highly integrated circuits.

7 CONCLUSIONS

The relationship between the feedback techniques of guarding, neutralization and bootstrapping to noise and bandwidth has been examined analytically and experimentally. A complete noise model of the sensor input has been described and verified in experiments on two separate sensors. in sections 3.5 and 5.1 respectively.

It has been shown that these feedback techniques do indeed result in a genuine and useful increase to input impedance, though this benefit is often balanced by a commensurate increase in noise. A signal to noise advantage is only experienced when the signal sensitivity is increased over and above the amount by which noise increases. In a great many other cases, it remains desirable to increase input impedance even though signal to noise is unchanged (and dynamic range reduced), since this either results in more useful output signal scaling (just as gain would) or, more usefully, it removes the effect of loading upon the source impedance. This latter benefit is useful in a variety of ways: it removes the effect of a varying source (coupling) capacitance on the output amplitude by setting the input capacitance to be negligible in comparison; it provides accurate measurement of electric potential (as demonstrated by Aydin el al 2010); it allows a degree of tailoring the low-frequency response by adjustment of the input resistance; and it enables the use of arrays of independent sensors.

Some of this understanding has been applied in the development of discrete transistor circuits for EP sensing. This development was driven by several motivations, not least of which was a furthering of the performance realised in EP sensors, but also to explore such circuits so that they may be implemented in highly integrated semiconductor processes. At the time of writing, a major semiconductor company is proceeding with

production of such a device, and so some of the knowledge developed here has already been applied.

These discrete transistor circuits have been shown to deliver ultra-low input capacitance without the need for excessive neutralization. The applicability of these sensors has been demonstrated in chapter 5 in two experiments. The remote measurement of cardiological activity has demonstrated that such a sensor may be used to acquire such signals in open unshielded environments where in several previous experiments screening from electrical mains supplies was required. In this experiment the increased dynamic range of this low-noise, low-gain sensor allowed post-filtering of mains borne noise, demonstrating an alternative method to the signal specific EP sensors previously described by Beardsmore-Rust et al.

In a second ultra-low capacitance experiment the surface electromyogram was measures as it has been previously by other experimenters. Additionally, a high spatial resolution surface EMG was acquired, which may provide a means of non-invasively monitoring individual motor unit action potentials. This latter measurement employed the high resolution probes described later in this thesis, and was made possible by the ultra low capacitance sensors' ability to operate with microscopic electrode diameters whilst retaining sufficient signal sensitivity.

An investigation into the frequency dependent behaviour of the high ohmic resistors used in nearly all EP sensors was carried out. As a result of this study the resistor's contribution to the sensor input capacitance has been quantified. The value found in these experiments tallies with the measured reduction in input capacitance that is found when a sensor has its input resistor bootstrapped - as noted in chapter 3. In addition, it has been found that surface mount parts are to be preferred over glass encapsulated types due to the former's lower parasitic capacitance.

The earlier work of other Sussex experimenters on high resolution electric field imaging has been continued, with refinements to existing methods realised through the use of the more robust probes and the ultra-low capacitance sensors described earlier. A new method for the imaging of static charge and DC potentials has been demonstrated at

high spatial resolution, with applications in fundamental materials and surface research, and also in forensics. This forensic application is of particular interest since this method has the unique property in latent fingerprint imaging of time dependence.

As already mentioned, the study of the electric potential sensor in the most fundamental electronic sense, as has been undertaken as part of this study, is already proving worthwhile as the EP sensor is rapidly being translated to a commercially produced integrated circuit. As this work continues the applications identified here and in the works of others at the University of Sussex must continue to be refined and expanded with the detail and thorough understanding that is required for the EPS to become a reliable and widely beneficial sensor technology.

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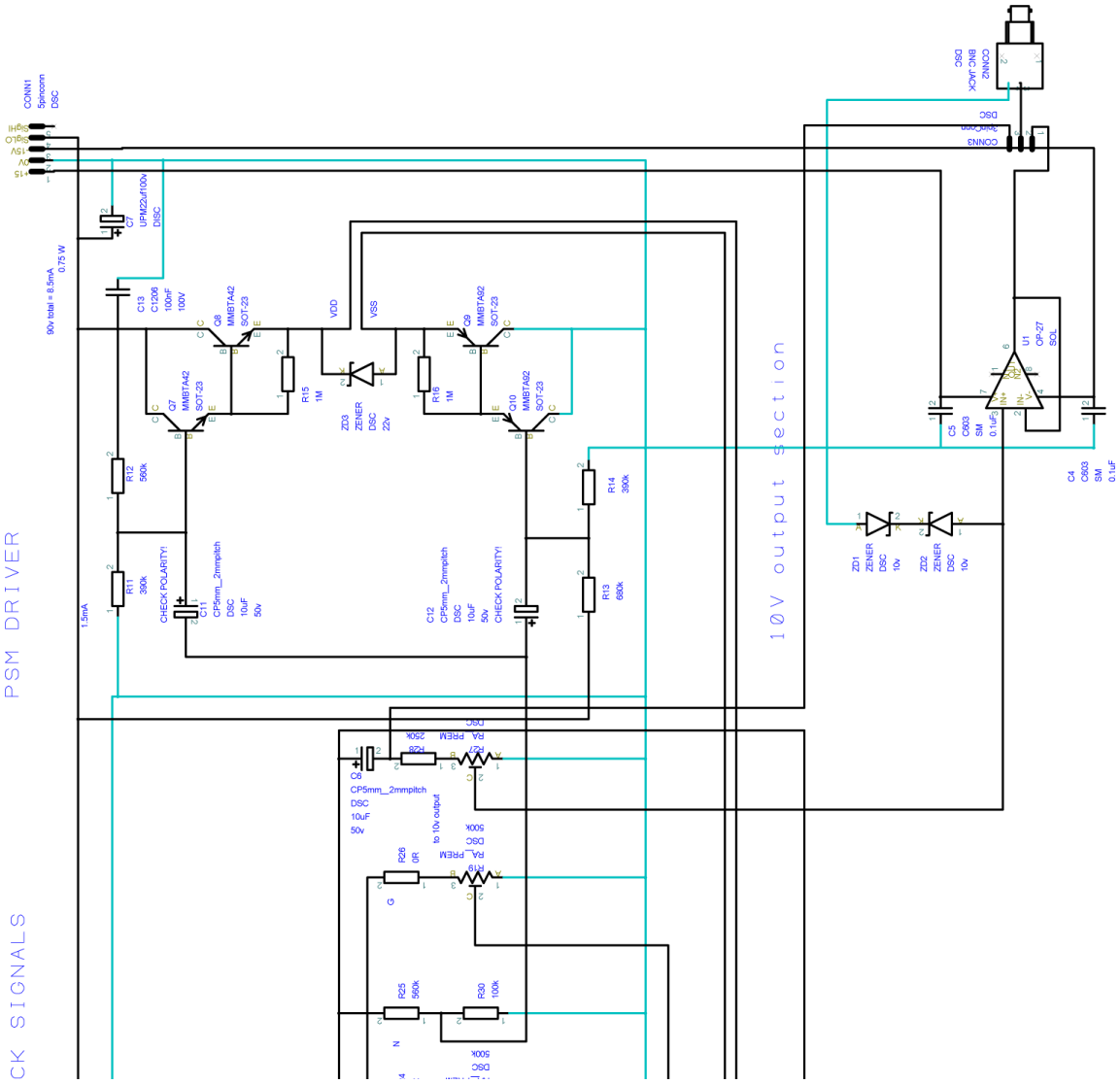
Appendix A Power Supply Modulation Schematic



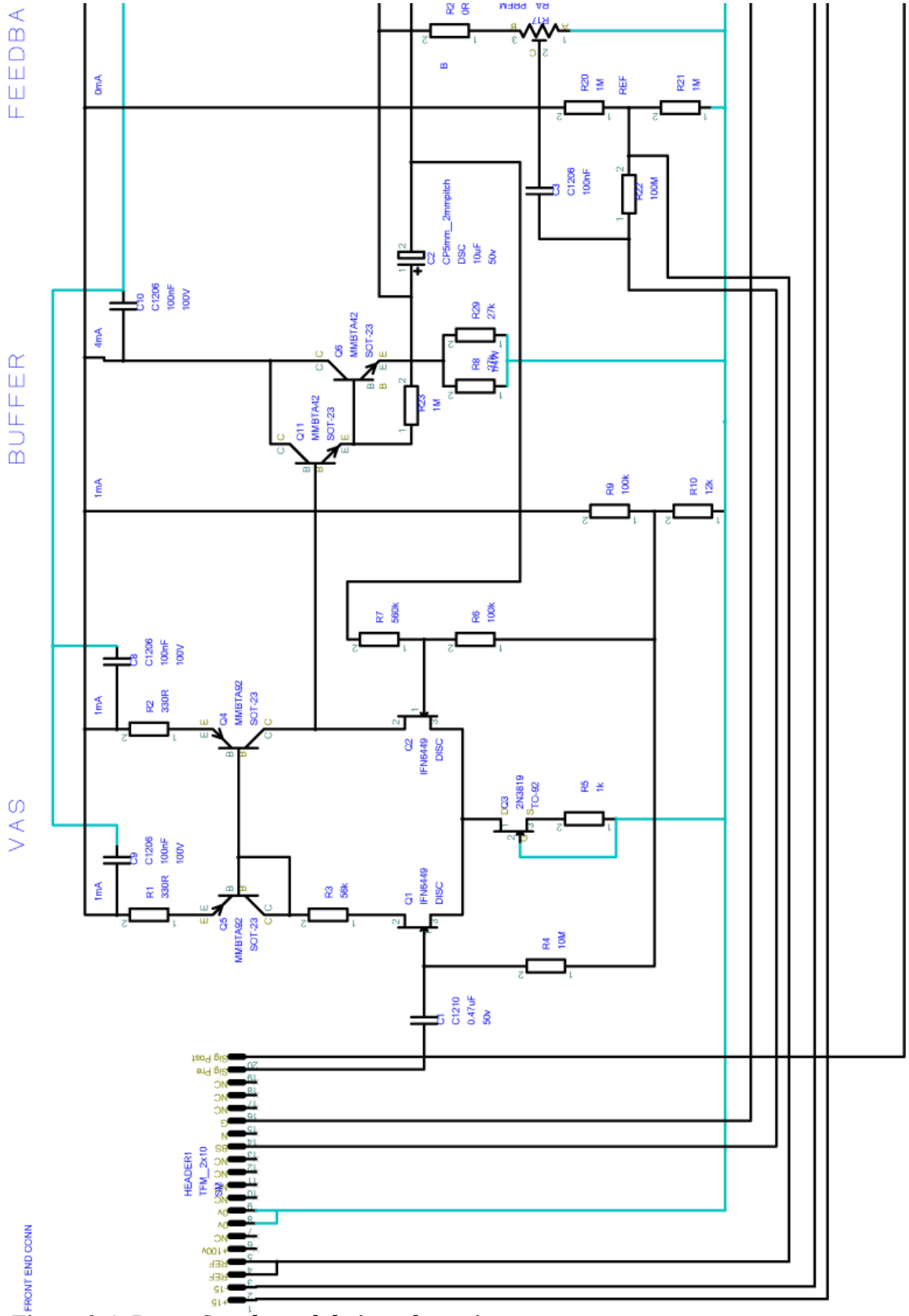


Figure A-1: Power Supply modulation schematic

Appendix B Frequency dependent behaviour of high resistance glass encapsulated and surface mount resistors

Resistors in the range of Giga-Ohms to tens of Tera-Ohms are by no means a 'standard' catalogue part. Such resistor values are however produced by several specialist manufacturers and have wide availability. These devices are also available in conventional surface mount packages. Due to the high value, and perhaps also the limited marketplace, such devices tend to have either poor tolerances, high cost, or in some cases both.

In addition to the commercial options, some experimenters have found success in producing high-Ohmic resistors from more widely available materials. One oft-cited method exploits the insulation leakage of annealed copper wire. By twisting together a pair of wires, resistances in the Tera-Ohm range are produced which can then easily be adjusted by trimming the length of the twisted wire.

One important parameter of high-ohmic resistors of any type is the parasitic capacitance which appears in parallel with the resistance. This capacitance produces a frequency dependent resistor. This parameter is not generally specified on data sheets, though it can have important implications for high impedance electric potential sensors — particularly when bootstrapping is applied to the resistor. In this experiment the value of this parasitic capacitance is measured for several resistors of different packaging and resistance values.

Thick film resistors are now available in standard surface mount (SM) packages in the range 10 $M\Omega$ to 10 $T\Omega$ with 20% precision available off the shelf, and low temperature coefficients of resistance of 50 to 1000 $ppm/°K$ (dependent on packaging and value) (SRT Resistor Technology, Cadolzburg, Germany, 2009). Several vendors produce similar high ohmic parts. These devices are designed to replace traditional leaded, glass-encapsulated resistors. The traditional devices consist of a resistive film deposited onto

a ceramic cylinder, with a helical cut along the length of the rod. The resistive element is hermitically sealed in a glass tube and terminated with wire leads.

While it is common place to consider the effects of stray capacitance when working at high frequencies, with high value resistors the effects of stray capacitance can impact on performance at very low frequencies. The frequency dependence of glass encapsulated resistors has been measured previously (Price, 2002), here we conduct a series of experiments to compare glass encapsulated and SM resistors, and determine the frequency dependent behaviour and associated stray capacitance of each.

B.1 Method

Glass-encapsulated and surface mount resistors of $100\,G\Omega$ and $1\,T\Omega$ nominal value have been measured in a bandwidth of $0.2\,Hz$ to $2\,kHz$, for comparison with previous measurements (Price, 2002). The glass encapsulated devices used here are in the 3811 package (Welwyn Components Ltd, Northumberland, UK, 2006), and the surface mount resistors are in the standard 1206 size SM package (SRT Resistor Technology, Cadolzburg, Germany, 2009).

In contrast with the method employed in previous measurements, a resistor divider network is used to perform the impedance measurements as shown in Figure B-1. This

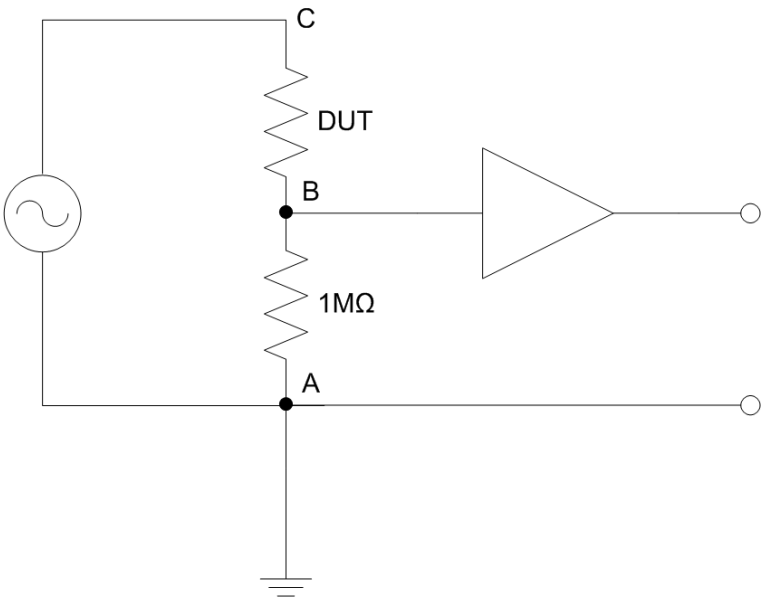


Figure B-1: Test fixture schematic

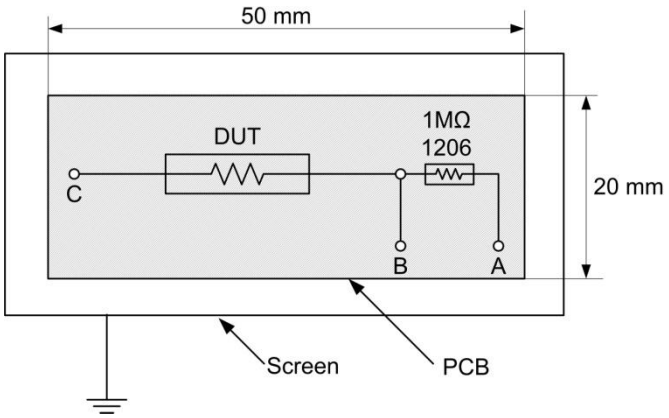


Figure B-2: Test fixture layout

method simplifies analysis and allows an open circuit calibration to be performed, which compensates for the losses in the test fixture. The output voltage of the circuit is proportional to the impedance of the device under test Z_{DUT}, the measurement resistor R_{meas}, and the voltage gain of the preamplifier A_v, and is given as;

$$\frac{v_{out}}{v_{in}} = A_v\left(\frac{R_{meas}}{R_{meas} + Z_{DUT}}\right) \qquad \text{B.1}$$

A 1 $M\Omega$ SM resistor is used for R_{meas}. The voltage at node B is buffered by a pre-amplifier with $Z_{IN} = 100\ M\Omega\ ||\ 33\ pF$, which forms the input to a swept-sine response (SSR) analyzer. The analyzer generates a $5\ V\ rms$ sine output at node C and records the amplitude present at the input. The input capacitance of the preamplifier in parallel with R_{meas} sets an upper frequency limit to the measurement of around $5\ kHz$. Low frequency resolution is limited by 1/f noise in the pre-amplifier. When calculating Z_{DUT} in equation B.1, R_{meas} is replaced with the impedance of the parallel combination of R_{meas} and Z_{in} of the pre-amplifier to compensate for the phase shift introduced by the reactive part of Z_{in}. The test fixture layout is shown in Figure B-2. A low leakage PCB material (Park Electromechanical corp, Melville, NY, 2011) provides solder terminals for leaded resistors and landing pads for the SM resistors. The landing pads can be isolated during measurements of leaded devices. The test fixture connects directly to the preamplifier input via a coaxial connector to minimise stray capacitance at node B. A large metal screen encloses the fixture, spaced at least 5 cm from the PCB at all points. The open circuit impedance of the test fixture has been measured by removing

Package	$Nominal\ R\ [G\Omega]$	$Tolerance\ \pm\ \%$	$R_0\ [G\Omega]$	C_s [pF]
Leaded	100	20	120	0.12
Leaded	1000	20	1200	0.12
1206 SM	100	20	100	0.04
1206 SM	1000	20	800	0.04

Table B-1: Set of resistors studied. R_0 is the measured DC resistance in each case

the device under test. It has been found that this impedance is an order of magnitude higher than that of the highest impedance resistor measured, at all frequencies. The contribution of this stray impedance to the measurement of Z_{DUT} is removed by treating the open circuit impedance as a parallel contribution to Z_{DUT}.

DC resistance is also measured independently using a high resistance meter and a test signal of 10 V, the results of which are given as R_0 in table B-1.

B.2 Results

Figure B-3 shows the results of the impedance measurements for the 4 resistors described in Table B-1. All show a significant reduction of impedance as frequency increases. A 20 dB per decade frequency dependence is observed above a few tens of Hertz, characteristic of a single lumped capacitance shunting the resistance. With the 1 TΩ resistors in particular, an additional dependence at frequencies below 10 Hz of 10 dB per decade is seen, characteristic of distributed capacitance in the resistive film (Lin and Chaing, 1988). This affects the impedance of the 1 TΩ 1206 SM resistor even at 0.2 Hz, where the impedance is significantly less than the DC resistance R_0.

By plotting the impedance responses for each package type on the same axes, as in Figure B-3, a near identical response in the 20 db per decade roll off region is seen for the two 1206 SM devices and the two glass encapsulated devices respectively. This indicates that the single lumped capacitance responsible for this steeper roll off is specific to the geometry of the package and independent of resistance. It is therefore possible to assign a single value for the stray capacitance of a given package, using the equivalent circuit of a parallel RC network. Two dashed-line traces are overlaid on

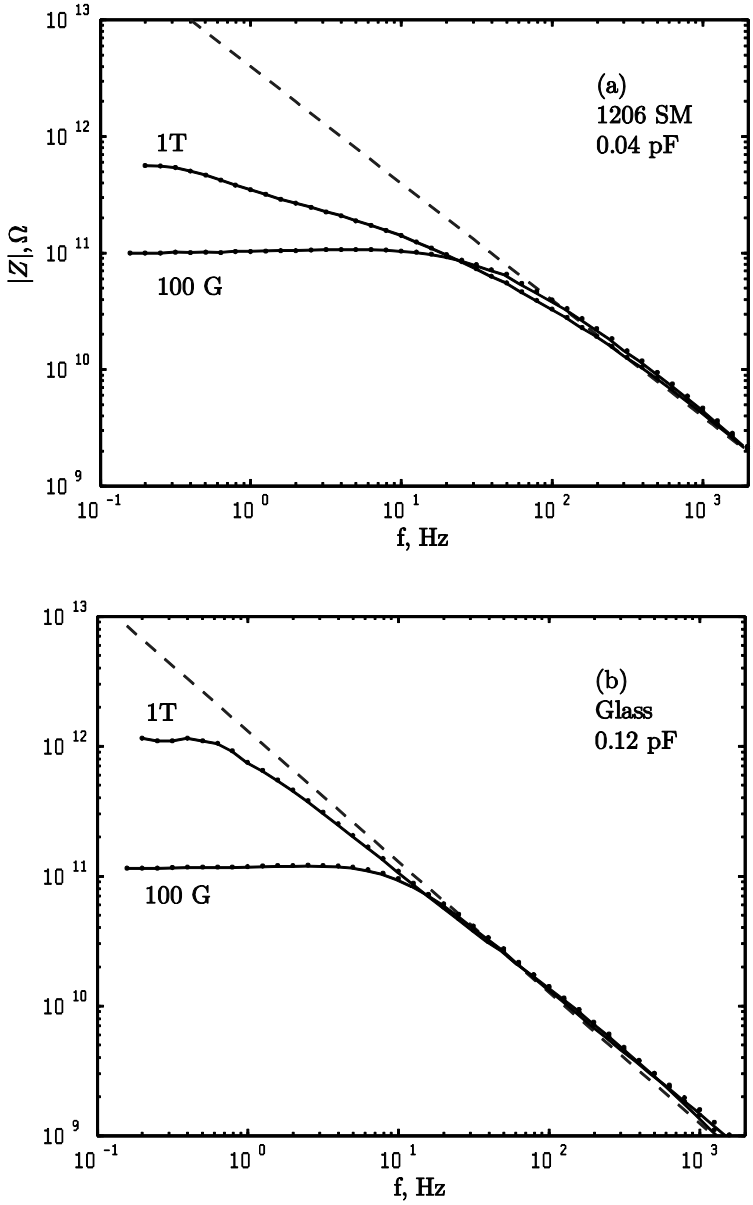


Figure B-3: Magnitude of electrical impedance versus frequency. (a) 1206 SM devices, (b) glass encapsulated devices. Dashed lines correspond to the calculated impedance of the respective capacitance value

Figure B-3 representing the impedance of the calculated values of the stray capacitance C_S for the two package types; 0.04 pF for the 1206 SM package and 0.12 pF for the glass encapsulated package. The overall impedance of the resistor is given as:

$$Z_{DUT} = R_{DUT} + \frac{1}{sC_s} \qquad \text{B.2}$$

Although this simple equivalent circuit does not take into account distributed capacitance and therefore does not accurately predict response in the region below 10 Hz for higher valued resistors (1 TΩ), this treatment is found to be sufficient for predicting performance in most AC circuits.

B.3 Conclusions

The impedance of high resistance glass encapsulated and surface mount resistors has been measured. It has been shown that at frequencies above a few Hertz resistors greater than 100GΩ show a rapid decrease in impedance. A value for the stray capacitance of these resistors can be assigned which is determined by the package only, and used to predict AC performance. Resistors in the 1206 surface mount package have lower overall stray capacitance than glass encapsulated types, corresponding to improved AC performance. The significance of the stray capacitance with very high resistance also has implications for DC measurements, where precautions must be taken to ensure a settling time of at least several RC time constants is allowed before taking measurements. In the case of the 1 $T\Omega$ resistor this will be at least 10 seconds.

Appendix C A heart rate detection method for remote cardiology measurements

In order to programmatically measure heart rate, and hence heart-rate variability, it is necessary to perform some form of peak-detection. Strictly, peaks are defined as local maxima. The corresponding local minima are termed valleys. In traditional ECG measurements heart rate is traditionally determined by using a threshold peak detection algorithm to detect the R peak of the QRS complex. Heart rate is henceforth calculated from the so-called R-R interval.

A threshold peak detector qualifies any signal level above a predetermined threshold value as a peak. Such an algorithm would produce multiple peak values, and so the local maxima of the thresholded signal is determined by one of several methods. A simple detector searches for the zero-crossing point of the first time-derivative of the thresholded signal. Regardless of the method used to determine local maxima, most algorithms nonetheless require a threshold value in order to qualify valid peaks.

The necessity for a predetermined threshold value makes conventional peak detection algorithms unsuitable for use on cardiological signals acquired by remote EPS sensing since the signal amplitude, and hence threshold value required, can vary greatly. Indeed, this requirement is also disadvantageous in conventional ECG measurement where amplitude variation is smaller though still significant. Methods have been proposed for automatically determining the threshold value (Jacobson, 2002) for conventional ECG data. Jacobson's method uses an unsupervised learning algorithm to determine the threshold value to be used on a given ECG trace. This method is therefore unsuitable for either real-time processing of signals, or for processing of signals where the peak-amplitude varies considerably from peak to peak. This second point is a requirement for a peak-detection system for remote EPS sensing of cardiological signals, and the first is highly desirable.

A peak detection algorithm which is capable of processing real-time signals and requires no predetermined threshold value has been developed in Matlab (Mathworks,

Natick, MA, USA) and subsequently implemented in LabView (National Instruments, Austin, TX, USA) to demonstrate real-time signal processing. The algorithm operates sequentially on individual samples of data, and determines if the current sample should be considered a peak by comparison with the previously determined peak.

The algorithm is best described by splitting it into 3 stages. A sample is defined as the current peak candidate if its amplitude is greater than the previous peak candidate. This is illustrated in Code Listing C-1.

```
%Initialize peak candidate values
x_peak = 0;
y_peak = 0;
if x > x_peak
       x_peak = x;
       y_peak = y;
end
```

Code Listing C-1: An incoming data sample, consisting of amplitude data x, and time stamp t, becomes the new peak candidate if its amplitude is greater than the amplitude of the previous peak candidate, x_peak.

The operation of this code is illustrated by plotting all peak candidates encountered when processing a simple test waveform, as shown in Figure C-1.

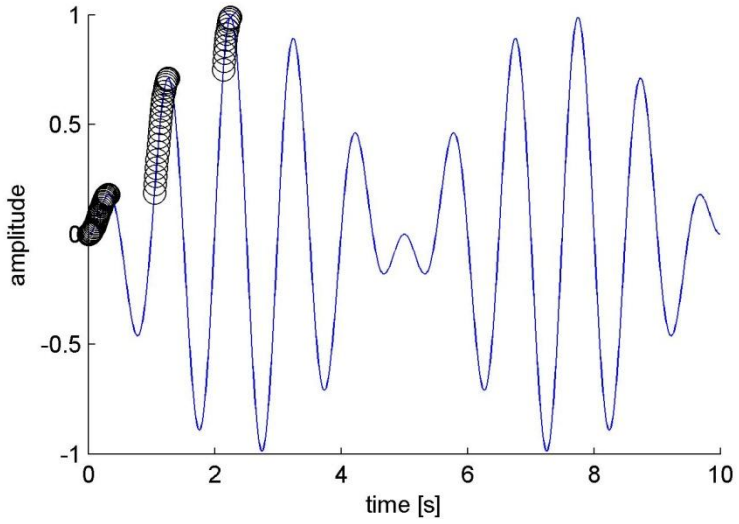


Figure C-1: A test signal composed of the sum of 3 sine waves of fixed frequency but varying amplitude is used to demonstrate the operation of the code of listing C-1. Each peak candidate is plotted as a black circle.

The output of this algorithm is not useful since it only finds the largest incoming peak. A weighting function is applied to the previous peak candidate so that its amplitude is scaled according to its age, that is, the delta of the current sample time stamp and the previous peak candidate time stamp. In this manner a sample is qualified as a candidate peak by its relationship to both the amplitude of previous peaks, and the periodicity of those peaks. The weighting function used has an inverse square decay, and is defined in as

$$f_w(t) = 1 - \left(\frac{1}{k^2}\Delta t^2\right), where\ \Delta t = t_s - t_{peak}$$

where t_s is the current sample time stamp, t_{peak} the time stamp of the previous peak candidate, and k is a constant and has units of seconds. The value of the time constant k corresponds to the value of t when the function is zero.

This enhancement to the algorithm is given in code-listing C-2 and illustrated in figure C-2.

```
x_peak = 0;
y_peak = 0;
delta_t = t - t_peak;
x_peak_weighted = x_peak * weight_fnc(delta_t);
if x > x_peak_weighted
       x_peak = x;
       y_peak = y;
end
```

Code Listing C-2: The amplitude of the previous peak candidate is multiplied by a function of the time difference between the incoming sample and the previous peak candidate, before comparison with the incoming comparison sample amplitude.

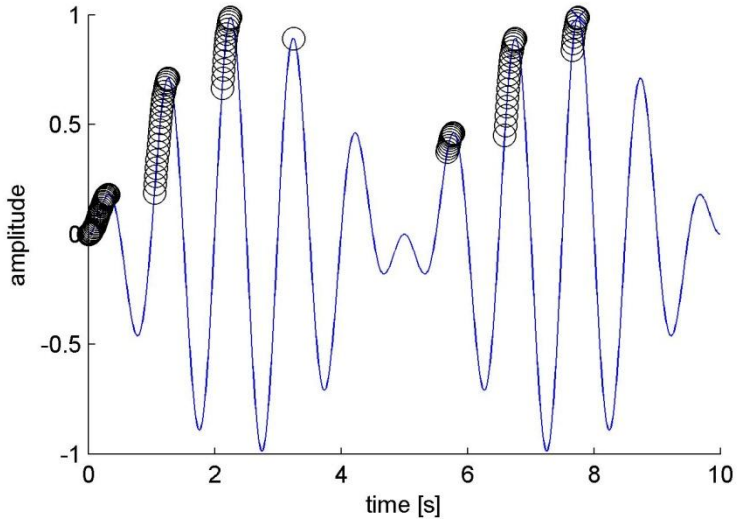


Figure C-2: The code of listing C-2 now detects peaks whenever their value exceeds that of the weighted previous peak. A time constant of 3 seconds has been used for the weighting function. Note that the 5th peak is not detected since it represents a large change in amplitude from the 4th peak. The 6th peak is successfully detected since its amplitude is now similar to previous peaks.

The final stage in the algorithm involves determining actual peaks from the peak candidates. A true peak could be defined as any peak candidate which is not immediately replaced by a new peak candidate on the next iteration of the algorithm. From figure C-2 it is clear that this approach would be successful since it would correctly identify the local maxima. When candidate peaks are surrounded by noisy false peaks, as in remote cardiological measurements, more sophisticated strategies may be employed. One is to qualify a valid peak as a candidate which survives for some extended lifetime. This strategy will tend to select the last in a group of peaks, and so is generally quite effective if the target is to identify the heart rate. A more advanced strategy might attempt to recognise a group of peaks and find the centre of the peaks by some weighted mean.

The final implementation of this algorithm has been performed in LabView , the graphical code can be found at the end of this appendix in Figure C-3. This sub-VI takes as its input a cluster of samples, though it internally operates sample-by-sample. It returns a cluster of the time and amplitude coordinates of the detected peaks.

The function of the algorithm is operationally equivalent to a conventional threshold peak detector where the threshold value is derived from some time averaged (i.e. low-passed in the frequency domain) value of the signal. However, this algorithm reduces the computational and memory requirements of such an approach significantly.

The weighting function can be interpreted as the allowable rate of change of peak amplitude; if the weight function decay is too fast then noise signals which occur after valid peaks will be detected, if it is too slow then valid peaks of slightly reduced amplitude will not be detected. The lifetime defines the periodicity of valid peaks, and should be set to reflect the minimum peak interval expected. If the lifetime is set to an excessively short value, the result will be detection of noise peaks that are close in amplitude to the desired peak. For high-quality conventional ECG signals, a lifetime of only 1 sample period is usually sufficient, since no noise peaks with amplitude close to the R-peak exist. In remote EPS measurements of cardiological activity, a correctly set lifetime ensures' ringing' artefacts in the signal, such as those in figure C-2 are not detected as peaks and only the maximum peak of the ring waveform is detected.

This algorithm is suitable for implementation in small embedded systems since memory requirements are low; only a single sample buffer is required.

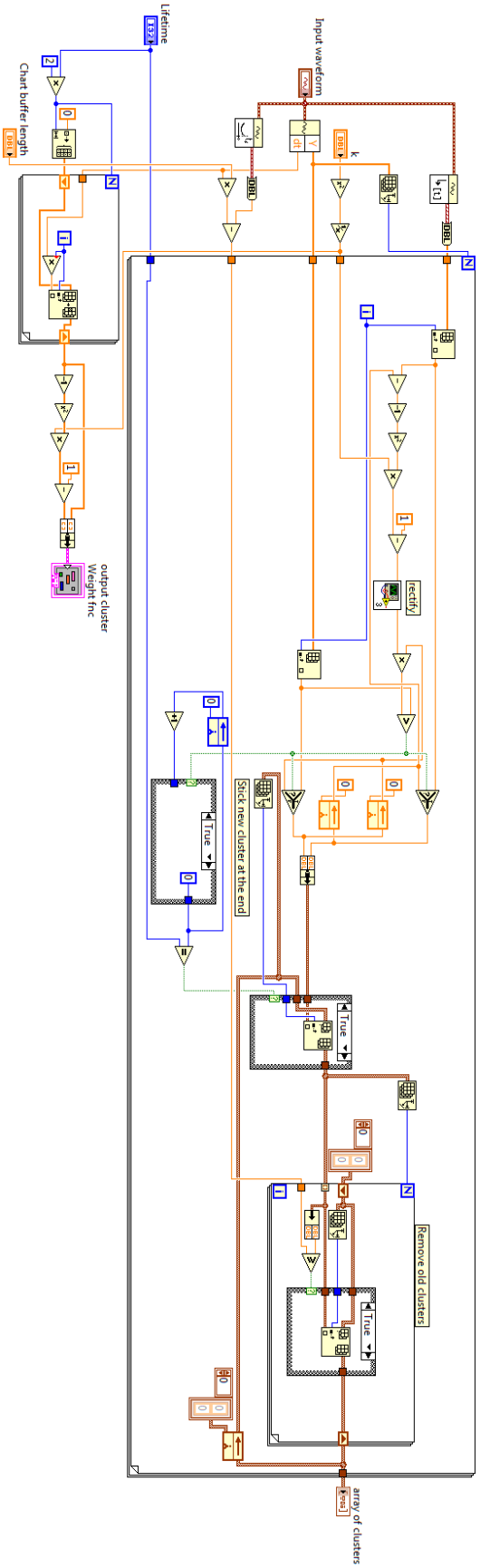


Figure C-3: LabView Graphical code

Appendix D Z-Axis Stepper motor driver

A stepper motor drive controller has been added, separate to the X & Y motor controllers, for control of the Z-axis stepper motor. This consists of an MCU, an ST Microelectronics L297 stepper controller, and an L298 H-bridge driver. The MCU interfaces to the control unit USB interface via additional digital I/O lines used as a bit-banged interface. In addition, push button switches on the control board provide direct up & down control of the z-stepper by the user. Schematics and a printed circuit board layout are given below.

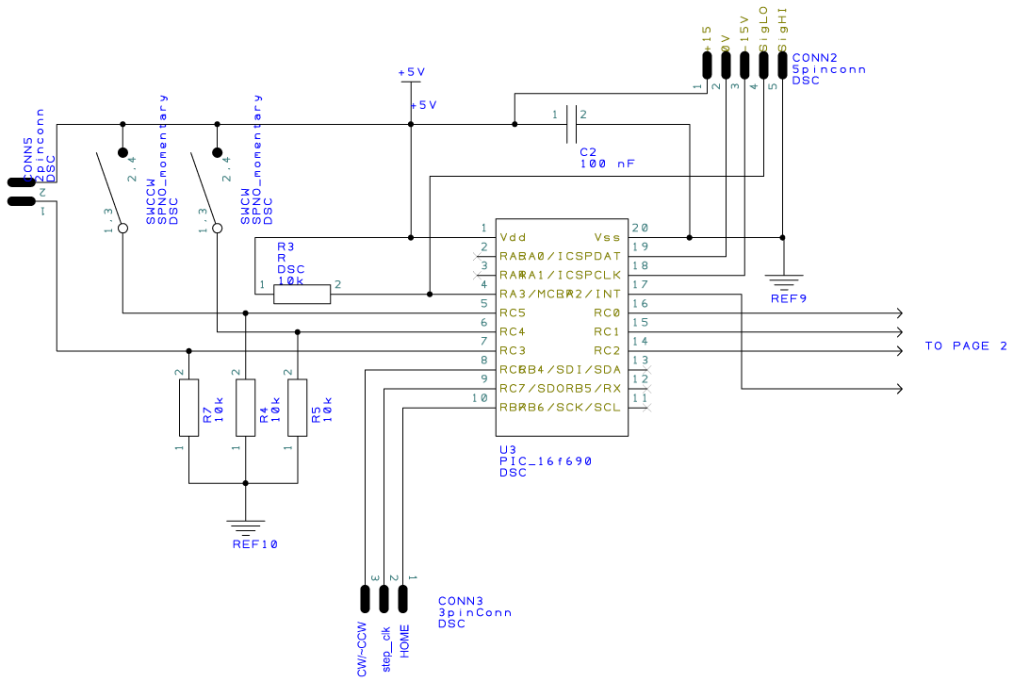


Figure D-1: Z-Axis stepper motor driver Schematic Page 1

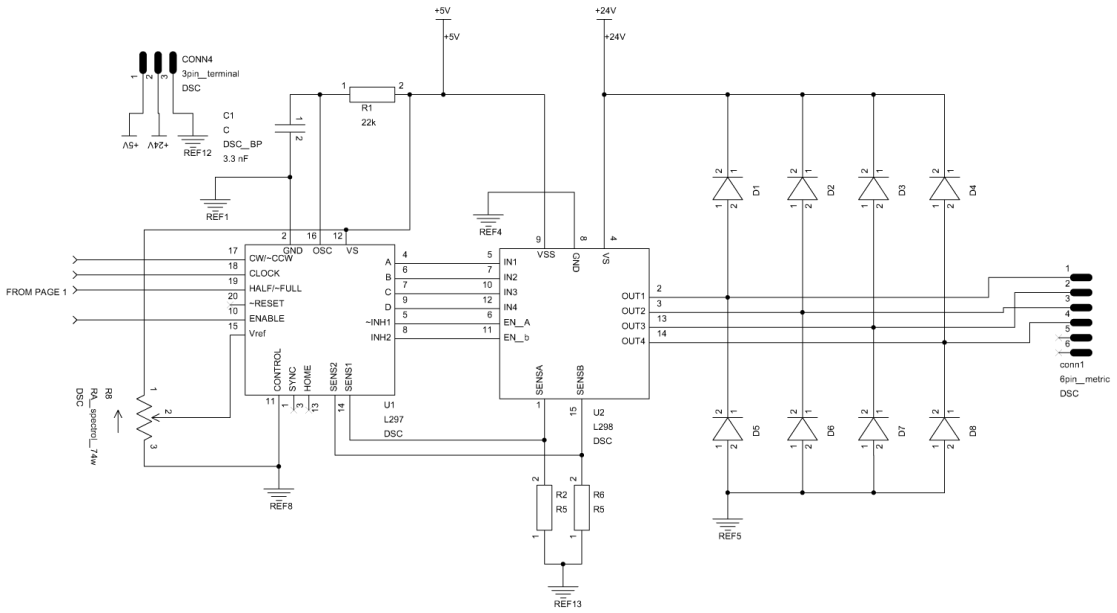


Figure D-2: Z-Axis stepper motor driver Schematic Page 2

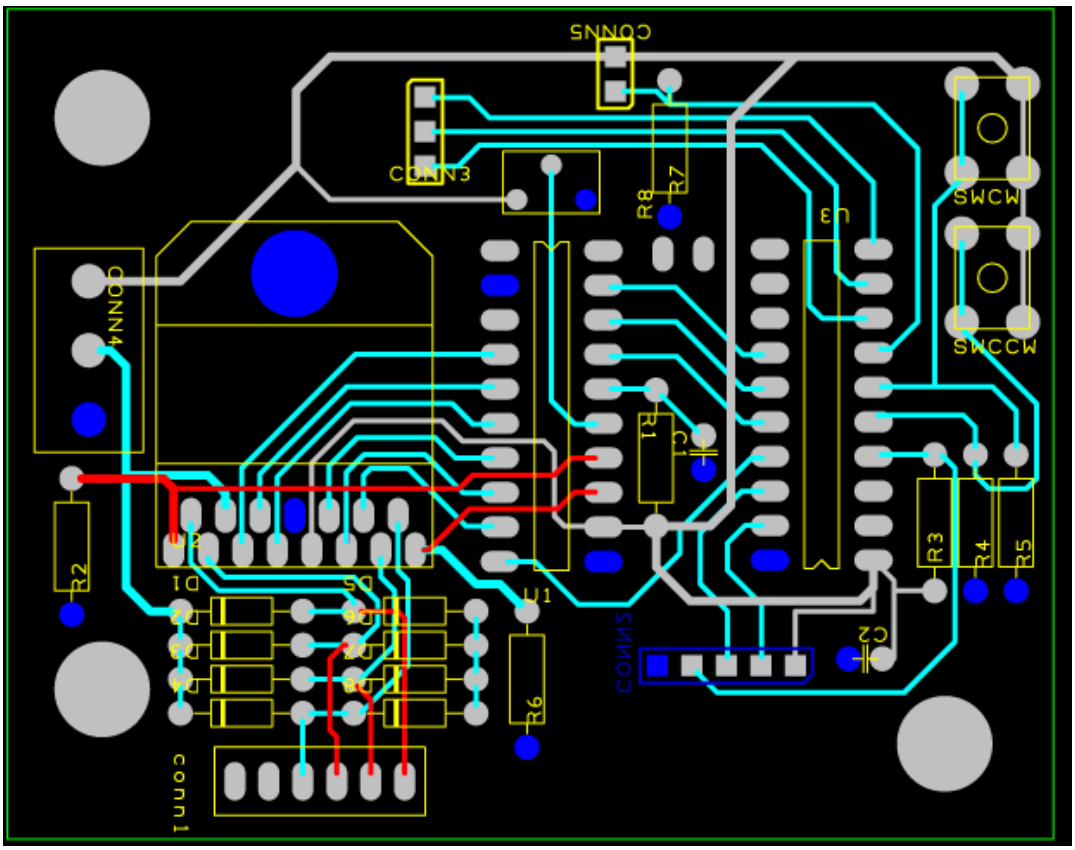


Figure D-3: Z-Axis stepper motor driver PCB layout

Appendix E Lock-in amplifier

A lock-in amplifier provides high resolution amplitude and phase measurements of a sinusoidal signal even with poor signal to noise ratios. The noisy signal is compared with a reference set at the same frequency, and the difference in amplitude and phase between the two is found. This phase sensitive detection is particularly applicable in situations where the reference sinusoid is being generated locally and detected by a noisy sensor, as is the case in the AC electric field imaging mode described earlier.

The elementary two-channel lock-in amplifier consists of 2-inputs, the signal and reference, and two outputs, shown Figure E-1. The reference input is fed into a phase-locked loop (PLL) which generates high purity quadrature sine and cosine waves.

The input signal can be written as $s(t) = A\cos(\omega t + \varphi) + n$, (National Instruments Inc, 2008) where A is amplitude, φ is phase, and n is some additional uncorrelated noise. If the PLL produces a reference cosine output of $r(t) = 2\cos(\omega t)$, then the mixer output will be;

$$y(t) = s(t) \times \mathrm{r(t)} = A\cos\varphi + A\cos(2\omega t + \varphi) + 2n\cos(\omega t)$$

The mixer output has a DC component $A\cos\varphi$, which can be recovered by the low-pass filter (LPF). The quadrature sine wave produced by the PLL gives the second output a DC component, $A\sin\varphi$. From these two outputs the amplitude and phase can be determined.

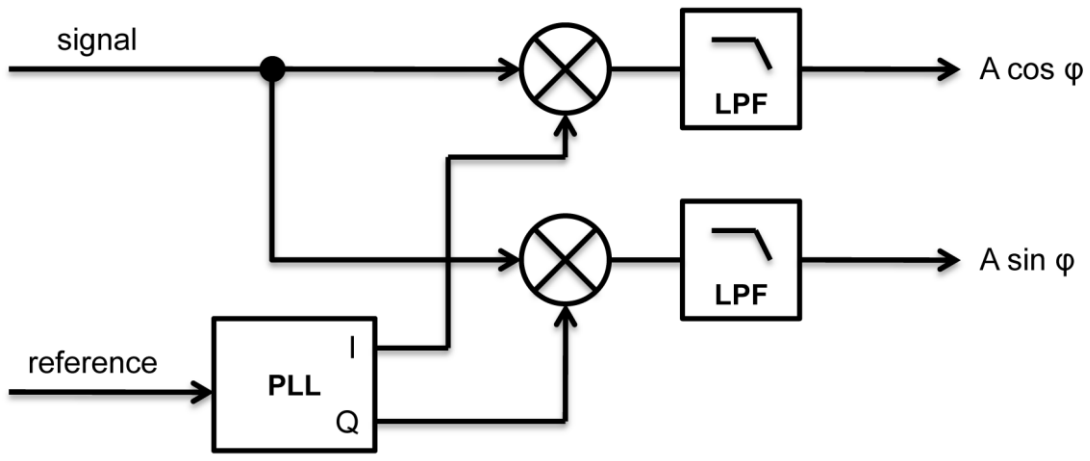


Figure E-1: A 2-channel lock-in amplifier

A lock-in amplifier is well suited to digital implementation since idealized multipliers, filters and PLL's can be implemented (Rocholeau, 2008). Further, an FPGA allows the full signal path to be implemented as discrete digital elements capable of operating at speeds far in excess of those achievable using a software or DSP based approach.

Here a standalone, FPGA based all-digital lock-in amplifier is described with very high temporal, and hence phase, resolution. The overall topology of this implementation has been inspired by the online-published work of Rocholeau. Rocholeau has shown a working device based on an Altera Cyclone-II FPGA with the hardware description written in Verilog, and with a complete video output for display of results to the user. Here a Xilinx Spartan 3E based device is used. The hardware description is written in VHDL. A full analogue front end has been constructed, providing high speed signal input as well as auxiliary analogue output. Measurement output can therefore be provided as analogue levels, or alternately via an RS-232 PC interface. The FPGA device is on a 'Spartan 3-E Starter kit' development board.

E.1 Signal path

The major signal path components are illustrated in Figure E-2. The digital signal processing is performed using signed fixed point math throughout, with various scaling and sign-extension operations between stages (not shown). A single channel 14-bit 50 MSPS Analogue to Digital Converter (ADC) digitizes the input signal in signed two's compliment notation. The 14b parallel output from the DAC is immediately registered (not-shown) at the FPGA input by a 14b wide register clocked at the 50 MHz FPGA system clock. A linear phase low-pass FIR filter removes high frequency noise. The linear phase shift added by this filter is easily corrected. This filter is an IP core generated by the Xilinx CORE generator. Two separate 14b X 14b multipliers are used to mix the digitized signal with the quadrature I and Q reference sines from the all-digital PLL (ADPLL). Up to this point, each signal chain element operates at the full 50 MHz sample rate. The multipliers utilise the Spartan-3's onboard hardware multipliers for high speed operation.

A two-stage low pass filter approach is used to extract the DC component from the (50 MHz) mixer outputs. The first stage, an FIR based decimate algorithm reduces the sample rate to 1 kSPS. To use conventional lock-in terminology, where the LPF is described by its low-pass time constant, this decimation procedure sets a minimum time constant of 2 ms. The FIR filter provides stop-band attenuation which is matched to the dynamic range of 14b input; in other words, frequencies above the Nyquist rate of the output signal (500 Hz) are completely rejected. The output has 20b resolution in order to retain the resolution added as a consequence of the low-pass filter. Xilinx CORE generator has been used to implement this IP core. The second stage is the simplest

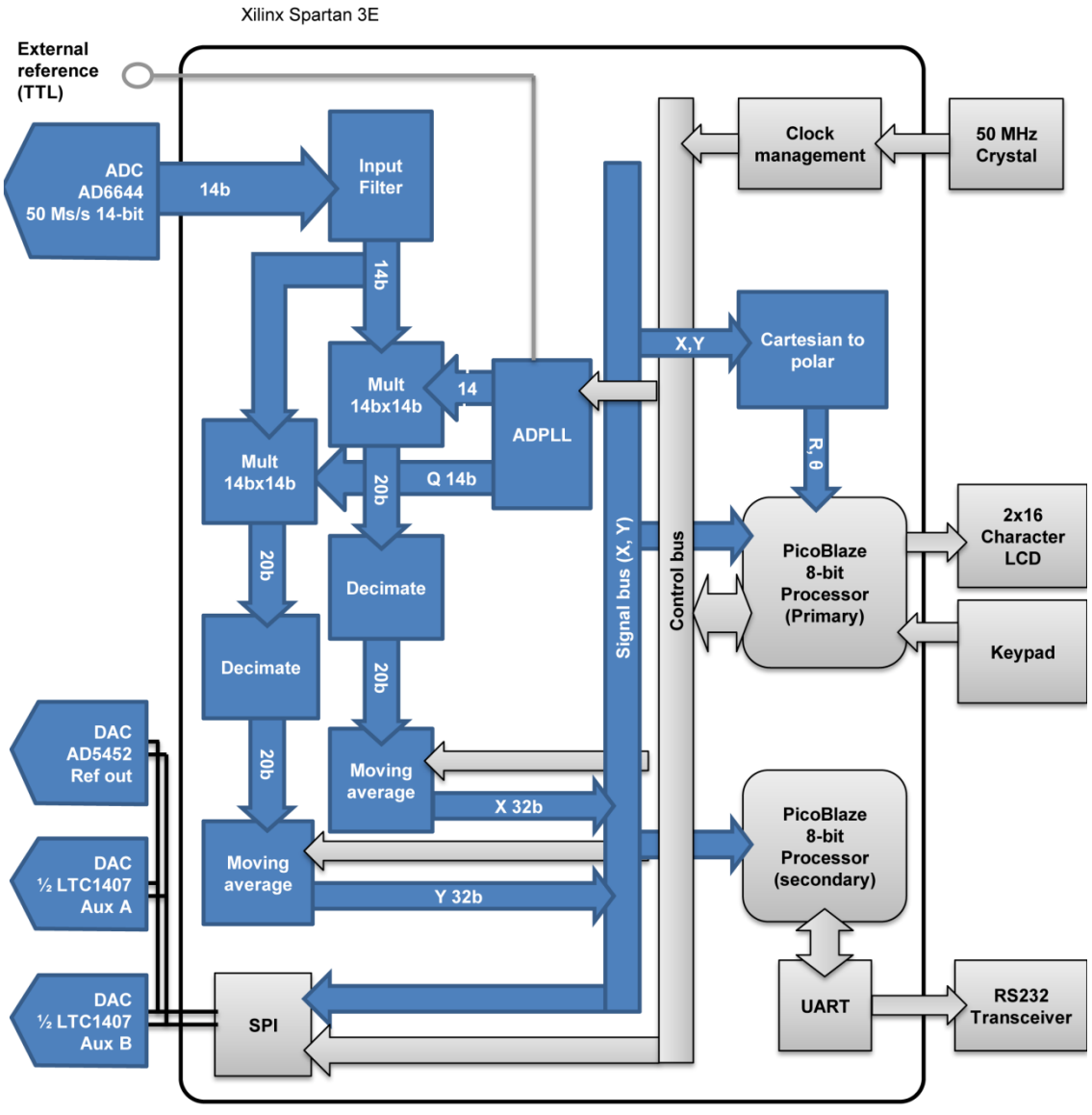


Figure E-2: A reduced block diagram of the signal path (dark grey/blue) and control elements (light grey).

implementation of an FIR filter; a moving average filter. This filter uses a hardware state machine (written in VHDL) and block-RAM primitives to produce a 32b x 1024 sample buffer. The filter has run-time switching of buffer length to enable time-constant switching from 2 ms up to 1.024 s. Time constants must be a power of 2, a restriction which allows the filter to dispose of any multipliers and achieve proper input and coefficient scaling through simple bit-shift operations. The only math operation remaining is a multiply accumulate (MAC), achieved by a 42b MAC operation.

It would be impossible to document all the VHDL code for this large project here, so instead of giving none of the underlying code, a short extract is presented in the form of mavfilt.vhd – the moving average filter.

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.numeric_std.all;

entity mavfilt is          --define input/output
    port (
        clk : in std_logic;
        en : in std_logic;
        reset_in : in std_logic;
        fdin : in std_logic_vector(31 downto 0);
        fdout : out std_logic_vector(31 downto 0);
        flength : in std_logic_vector (10 downto 0)          --filter length
        );
end mavfilt;

architecture Behavioral of mavfilt is      --internal signals
signal we : std_logic_vector (0 downto 0):= (others => '0');
signal addr : std_logic_vector (10 downto 0):= (others => '0');
signal dout : std_logic_vector (31 downto 0):= (others => '0');
signal accum : signed (41 downto 0):= (others => '0');
signal inreg : std_logic_vector (31 downto 0):= (others => '0');
signal flength_reg : std_logic_vector (10 downto 0):= (others => '0');
signal fdout_int : std_logic_vector (41 downto 0):= (others => '0');
signal reset_reg : std_logic;

    type stateType is (           --states
        reset,
        input,
        store,
        disable_we,
        inc_addr,
        wait_ram,
        acc,
        store_acc,
        scale
    );
    signal state               : stateType := input;

begin
bram_a_16_1024 : bram_16_1024      --connect two BRAMS into a 32x1024 RAM
        port map (
            clka => clk,
            wea => we,
            addra => addr,
```

```
            dina => inreg(31 downto 16),
            douta => dout(31 downto 16));

bram_b_16_1024 : bram_16_1024
        port map (
            clka => clk,
            wea => we,
            addra => addr,
            dina => inreg(15 downto 0),
            douta => dout(15 downto 0));


    process (clk)         --begin the real code here
    begin
    if clk'event and clk = '1' then
        if reset_in = '1' then
            reset_reg <= '1';
        end if;
        case state is       --here's the state machine
            when reset =>
                if addr = "10000000000" then
                    we <= "0";
                    state <= input;
                    addr <= (others => '0');
                    reset_reg <= '0';
                else
                    addr<=std_logic_vector(unsigned(addr) + "1");
                    state <= reset;
                end if;
            when input =>
                if reset_reg = '1' then
                    inreg <= (others => '0');
                    addr <= (others => '0');
                    accum <= (others => '0');
                    we <= "1";
                    state <= reset;
                elsif flength = "00000000000" then
                    state <= input;
                elsif en = '1' then
                    inreg <= fdin;
                    state <= store;
                else
                    state <= input;
                end if;
            when store =>
                    we <= "1";
                    flength_reg <= flength;
                    state <= disable_we;
            when disable_we =>
                we <= "0";
                state <= inc_addr;
            when inc_addr =>
                if (addr = flength_reg) then
                    addr <= "00000000000";
                else
                    addr <= std_logic_vector(unsigned(addr)+"1");
                end if;
                state <= wait_ram;
            when wait_ram =>
                state <= acc;
            when acc =>
                accum <= accum - signed(dout) + signed(inreg);
                state <= store_acc;
            when store_acc =>
                fdout_int <= std_logic_vector(accum);
                state <= scale;
            when scale =>
                if flength_reg(10) = '1' then
```

```
                    fdout <= fdout_int(41 downto 10);
                    state <= input;
                else
                    flength_reg <= flength_reg(9 downto 0) & '0';
                    fdout_int <= fdout_int(41)
& fdout_int(39 downto 0) & '0';
                    state <= scale;
                end if;
```

The final component in the signal path, and perhaps the most important, is the all-digital phase-locked loop (ADPLL). This implementation is based upon the block diagram given by Rocholeau. The three major components of any PLL are a phase comparator, a loop filter and an oscillator. In this all digital implementation the phase comparator is a pair of flip-flops, the loop filter a simple Proportional-Integral filter, and the 'oscillator' is a direct-digital synthesis module. As Rocholeau himself has noted, tuning the loop filter is the most critical and difficult part of the ADPLL implementation. Through extended simulation and testing an unconditionally stable ADPLL has been achieved. Since very high phase resolution is a goal of this lock-in design the loop filter has been configured to give low jitter, though this has come at the expense of a long lock time. The PLL achieves a lock within a few seconds for input frequencies in the range 50 Hz to 1 MHz. The DDS simultaneously generates quadrature Sine and Cosine waves at the 50 MHz rate with 14b resolution.

E.2 Control and external interfacing

Two PicoBlaze 8-bit microprocessors provide overall control of the various signal chain elements, as well as providing a front panel display and user interface, and controlling both analogue and digital external interfaces. The primary processor controls the configuration of the major signal processing blocks and external signal routing, providing user interaction through a character LCD display and a set of front panel keys. The user may configure the moving average filter time constant, and also control various parameters of the ADPLL. The PLL can be configured to take input from a rear panel connector which should provide a TTL level reference clock. Alternatively, the PLL function can be bypassed and instead the DDS portion used to internally generate the reference sine directly, according to a user set frequency.

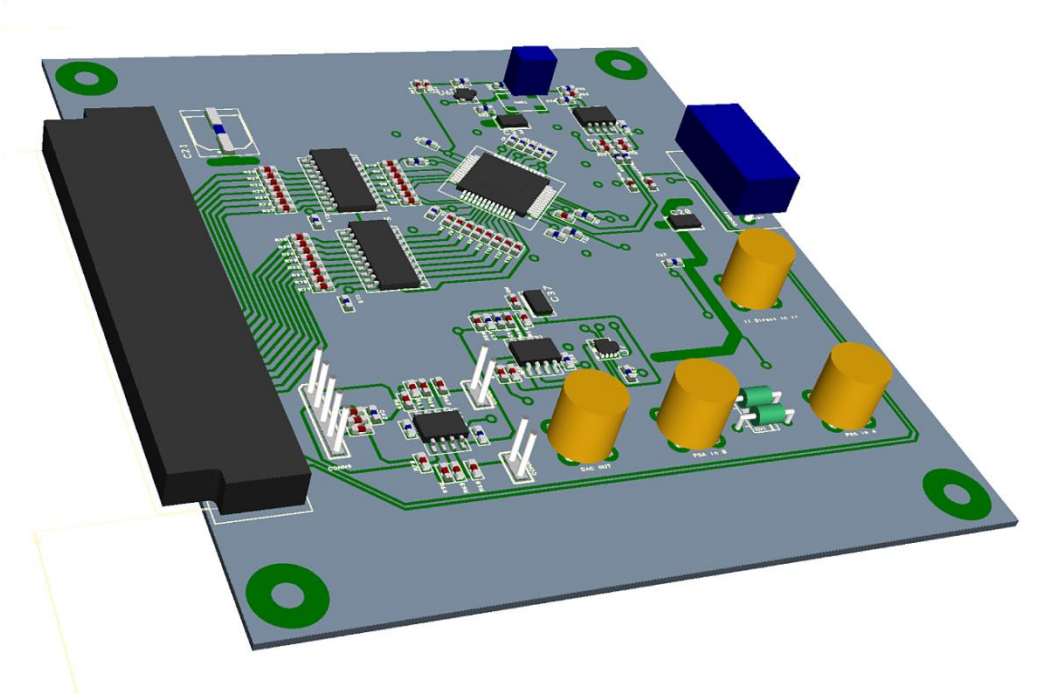
The secondary processor takes on the sole task of relaying the low passed output signals, denoted X and Y, over an RS232 serial communications link. This allows direct interfacing of the digital data with a PC. In addition to this digital output, a set of 3 analogue outputs can also be used to output data. As such, the all digital lock-in can actually be used as a stand-alone instrument. Two outputs are individually user configurable to provide either; X, Y, amplitude, phase, ADPLL sine output, or the raw

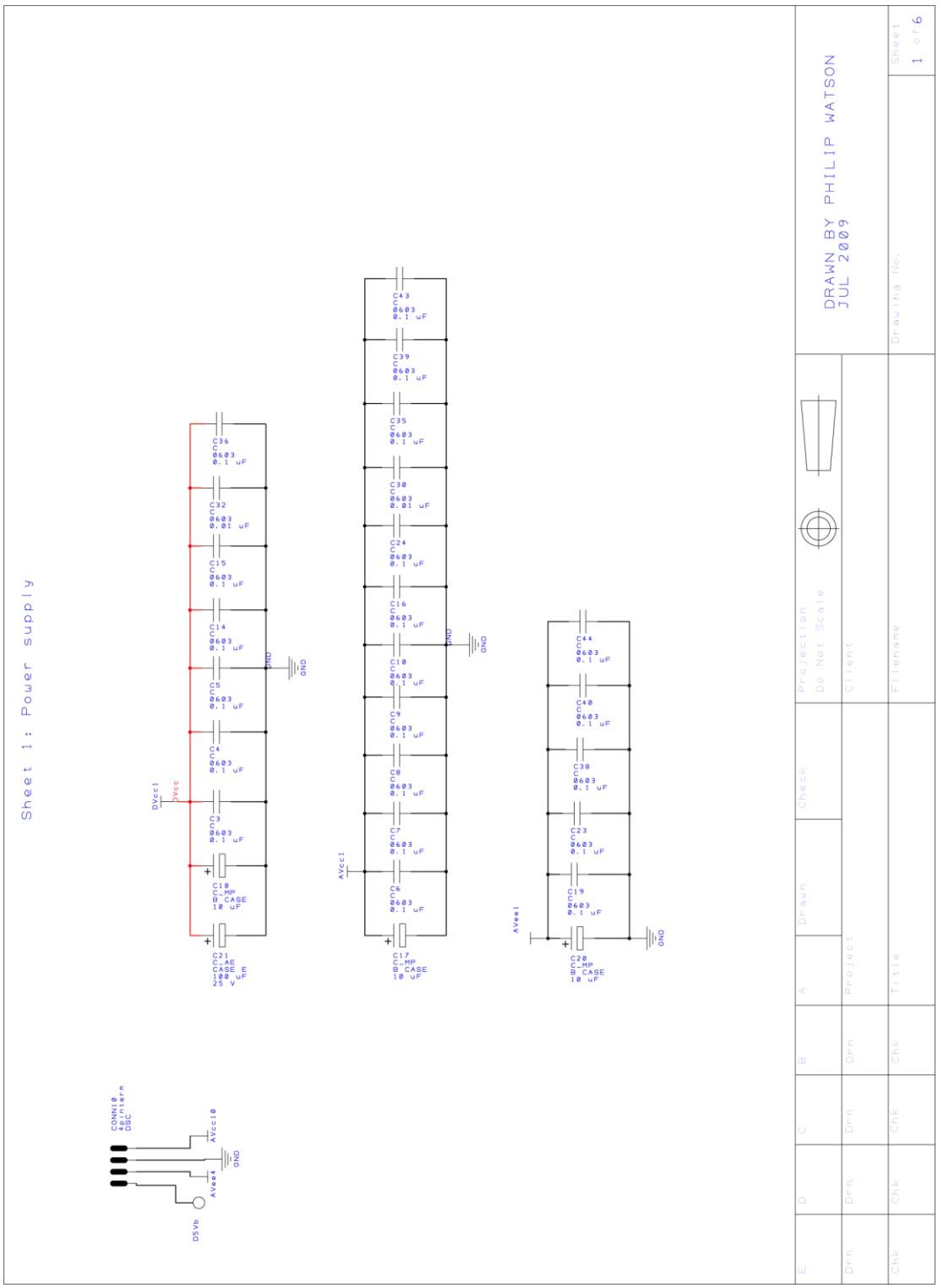
Figure E-3 Front, rear, and internal photographs of lockin.

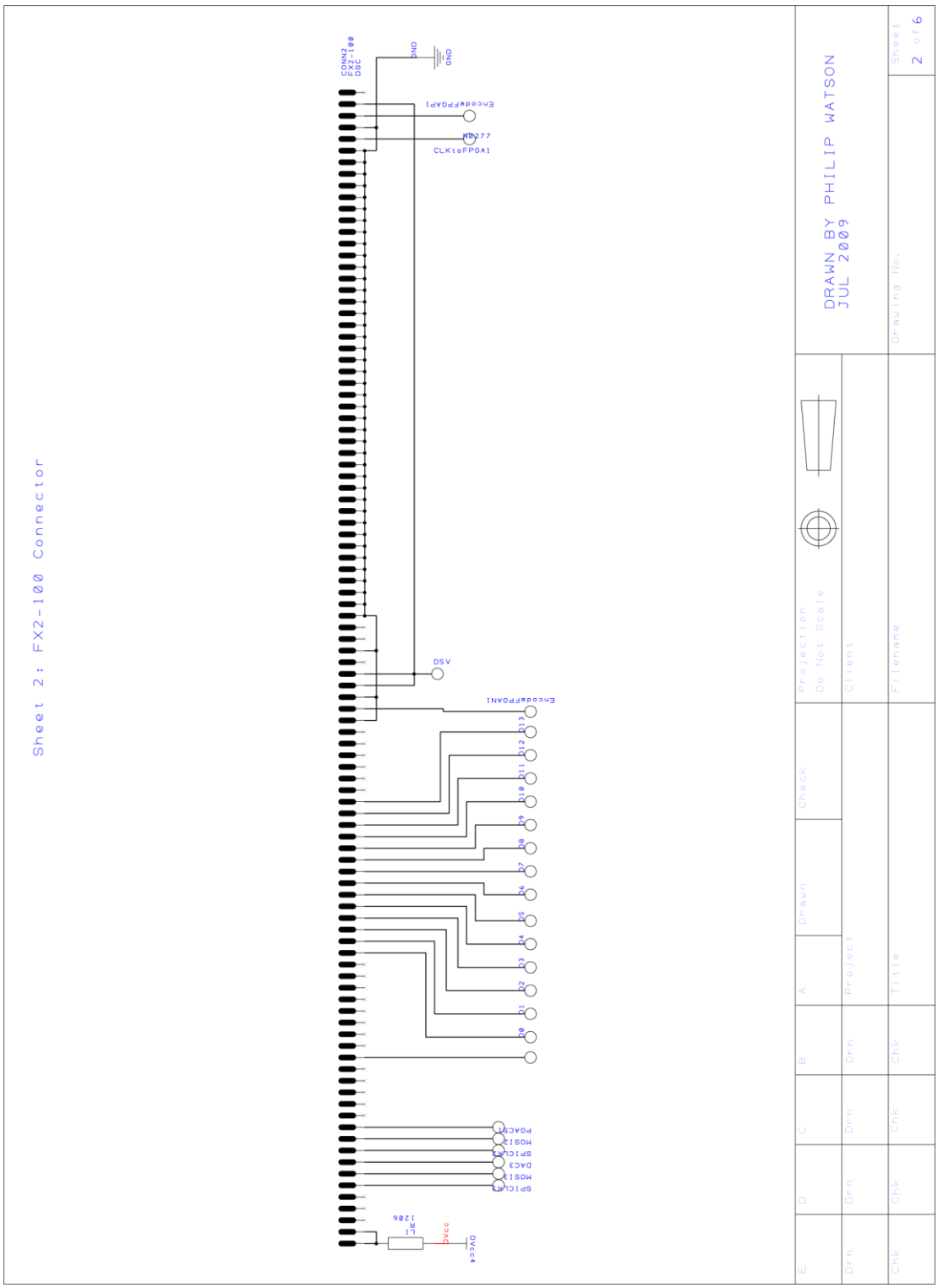
digitized input. The third output is dedicated to outputting a high resolution version of the ADPLL sine output. This final output is particularly useful when the ADPLL is configured to internally generate a user defined reference, so that the sine can be used as the stimulus signal for a sensor.

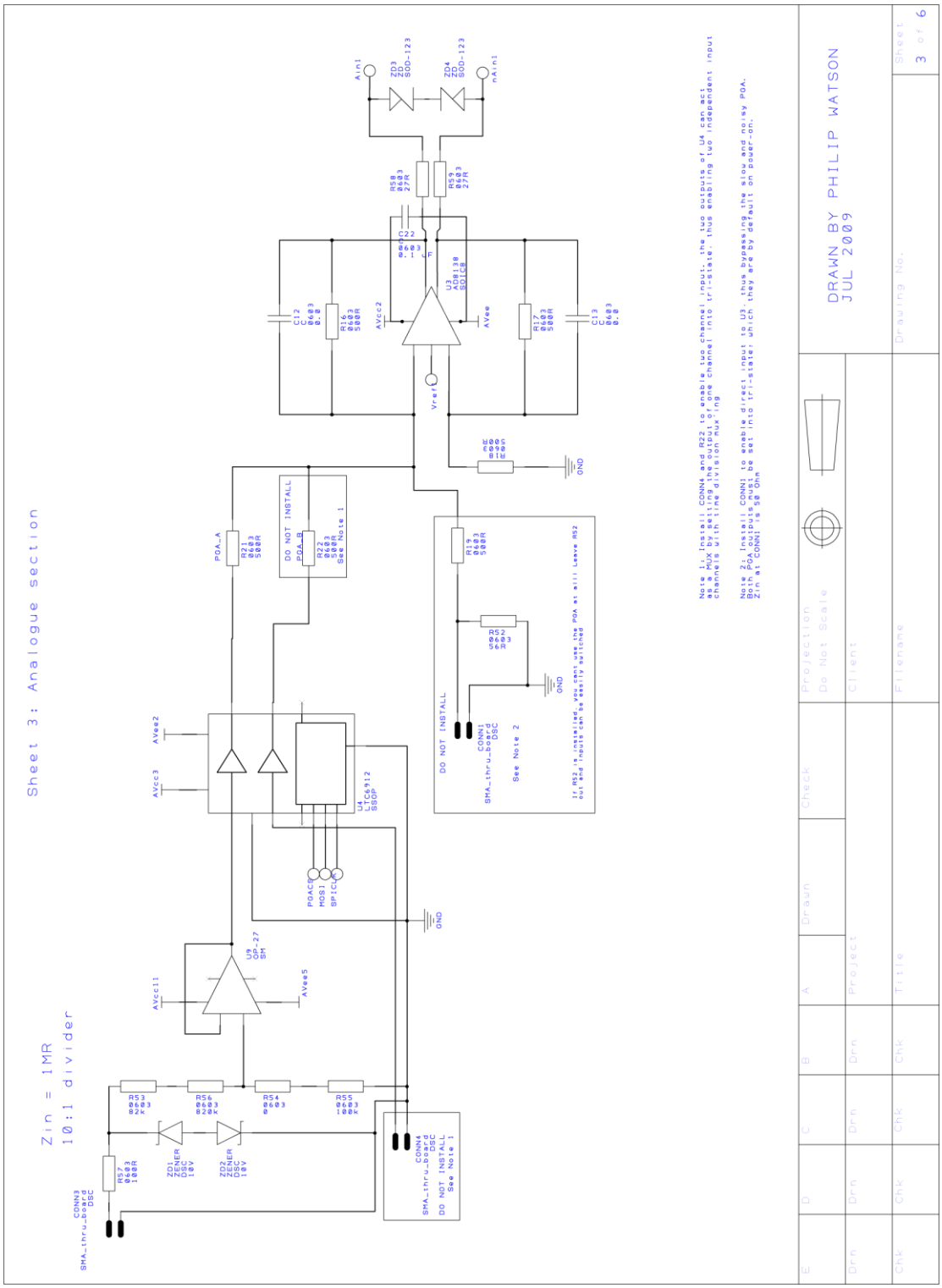
The complete instrument is packaged in a 19" 2U rack enclosure (Figure E-3). Three power rails for digital logic, analogue V_{dd} and V_{ss} are provided by a linear power supply. The front panel includes the LCD display, controls keys and rotary encoder, and power and PLL lock indicators.

Included at the end of this appendix are a full set of schematics for the analogue-digital interface board which connects to the FPGA development kit via its 100-pin expansion connector. This board supplements the FPGA with the high speed ADC and several other analogue input and output channels. A 3D render of this board is also included.




Sheet 1: Power supply
DRAWN BY PHILIP WATSON
JUL 2009
Sheet 1 of 6
Drawing No.
Filename
Title
Project
Client
Check
Drawn
Projection
Do Not Scale
DVcc1
DVcc
GND
AVcc1
AVee1
AVcc10
AVee4
DSVb
C36 0603 0.1 uF
C32 0603 0.01 uF
C15 0603 0.1 uF
C14 0603 0.1 uF
C5 0603 0.1 uF
C4 0603 0.1 uF
C3 0603 0.1 uF
C18 SMD_MP B_CASE 10 uF
C21 SMD_AE CASE 100_um 25 V
C43 0603 0.1 uF
C39 0603 0.1 uF
C35 0603 0.1 uF
C30 0603 0.01 uF
C24 0603 0.1 uF
C16 0603 0.1 uF
C10 0603 0.1 uF
C9 0603 0.1 uF
C8 0603 0.1 uF
C7 0603 0.1 uF
C6 0603 0.1 uF
C17 SMD_MP B_CASE 10 uF
C44 0603 0.1 uF
C40 0603 0.1 uF
C38 0603 0.1 uF
C23 0603 0.1 uF
C19 0603 0.1 uF
C20 SMD_MP B_CASE 10 uF
CONN10 4pin1mm DSC


Sheet 2: FX2-100 Connector
CONN2
FX2-100
GND
GND
EncodeFPGAP1
CLKtoFPGA1
5V
EncodeFPGAN1
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
FDACS1
MOSI2
SPICLK
DAC3
MOSI3
SPICLK
1206
3V3
DRAWN BY PHILIP WATSON
JUL 2009
Sheet
2 of 6
Drawing No.
Projection
Do Not Scale
Client
Filename
Check
Draun
Project
Title
A
B
C
D
E
Drn
Chk


Sheet 3: Analogue section
Zin = 1MR
10:1 divider
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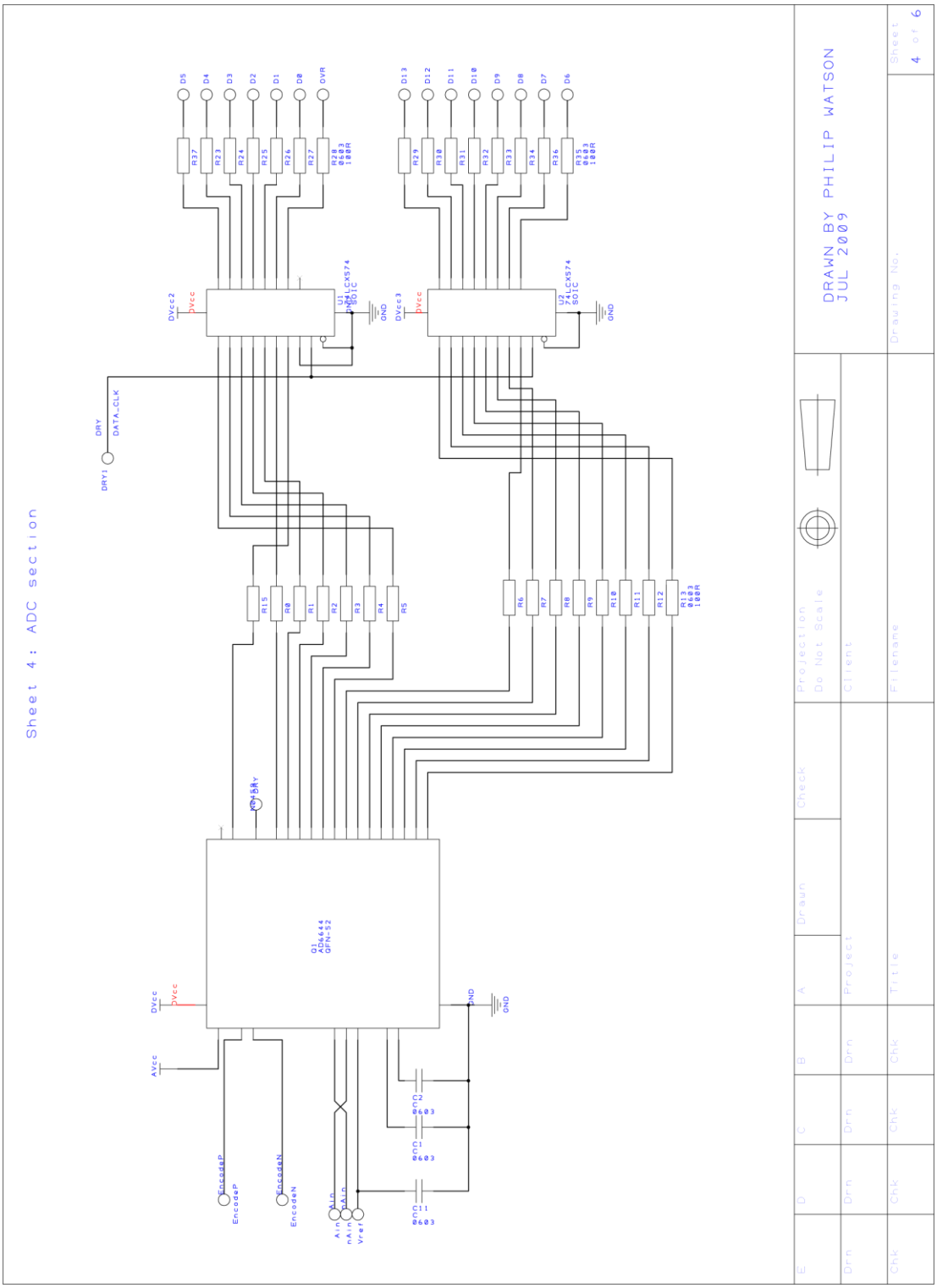
Sheet 3 of 6
Drawing No.
Filename
Client
Projection
Do Not Scale
Check
Drawn
Project
Title
Note 1: Install CONN4 and R22 to enable two channel input. the two outputs of U4 can act
as one by setting the output to one channel into tri-state. thus enabling two independent input
channels with the given mux'ing
Note 2: Install CONN1 to enable direct input to U3. thus bypassing the slew and noisy PGA.
Both PGA outputs must be set into tri-state: which they are by default on power-on.
Zin at CONN1 is 50 Ohm
Ain1
nAin1
ZD3
ZD4
SOD-123
R58
R59
27R
C22
0603
0.1 u
U3
AD8138
SOIC8
AVcc2
AVee
Vref1
C12
C13
R16
R17
500R
GND
PGA_A
PGA_B
R21
R23
DO NOT INSTALL
See Note 1
R19
R52
CONN1
SMA_thru_board
DSC
See Note 2
If R52 is installed, you cant use the PGA as will Leave R52
out and inputs can be easily switched
AVee2
AVcc3
U4
LTC6912
SSOP
PGACS
MOSI
SPICLK
AVcc11
AVee5
U9
LT1027
SM
R53
820k
R56
820k
R54
R55
100k
R57
100R
ZD1
ZENER
DSC
10V
ZD2
ZENER
DSC
10V
CONN3
SMA_thru_board
DSC
CONN4
SMA_thru_board
DSC
DO NOT INSTALL
See Note 1


Sheet 4 : ADC section
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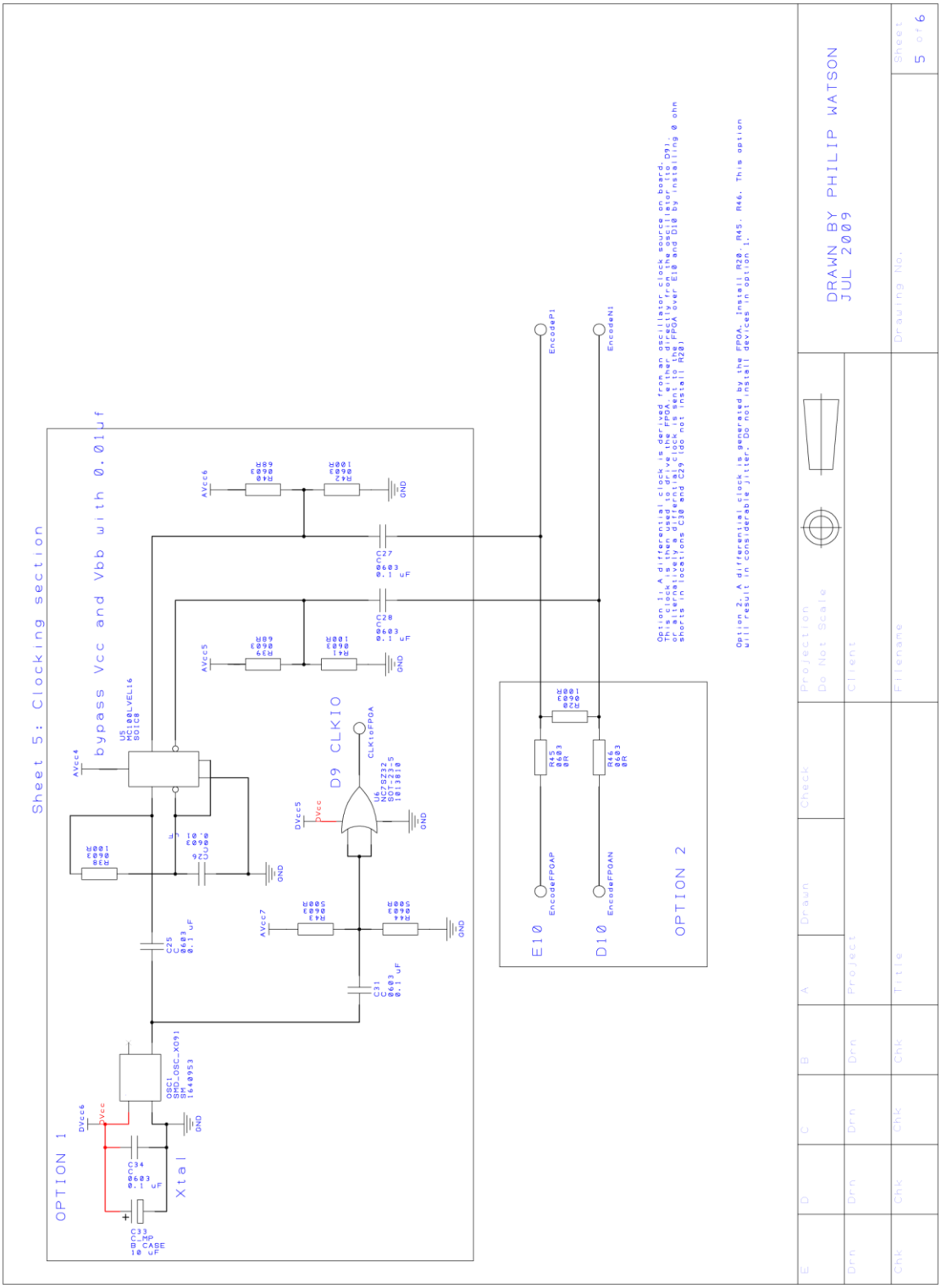
JUL 2009
Sheet 4 of 6
Drawing No.
Projection
Do Not Scale
Client
Filename
Check
Drawn
Project
Title
U1 74LCX574 SOIC
U2 74LCX574 SOIC
U3 AD6644 QFN-52
DVcc
AVcc
GND
DRY
DATA_CLK
EncodeP
EncodeN
Ain
nAin
Vref


Sheet 5: Clocking section
bypass Vcc and Vbb with 0.01uf
OPTION 1
Xtal
D9 CLKIO
OPTION 2
E10
D10
DRAWN BY PHILIP WATSON
JUL 2009

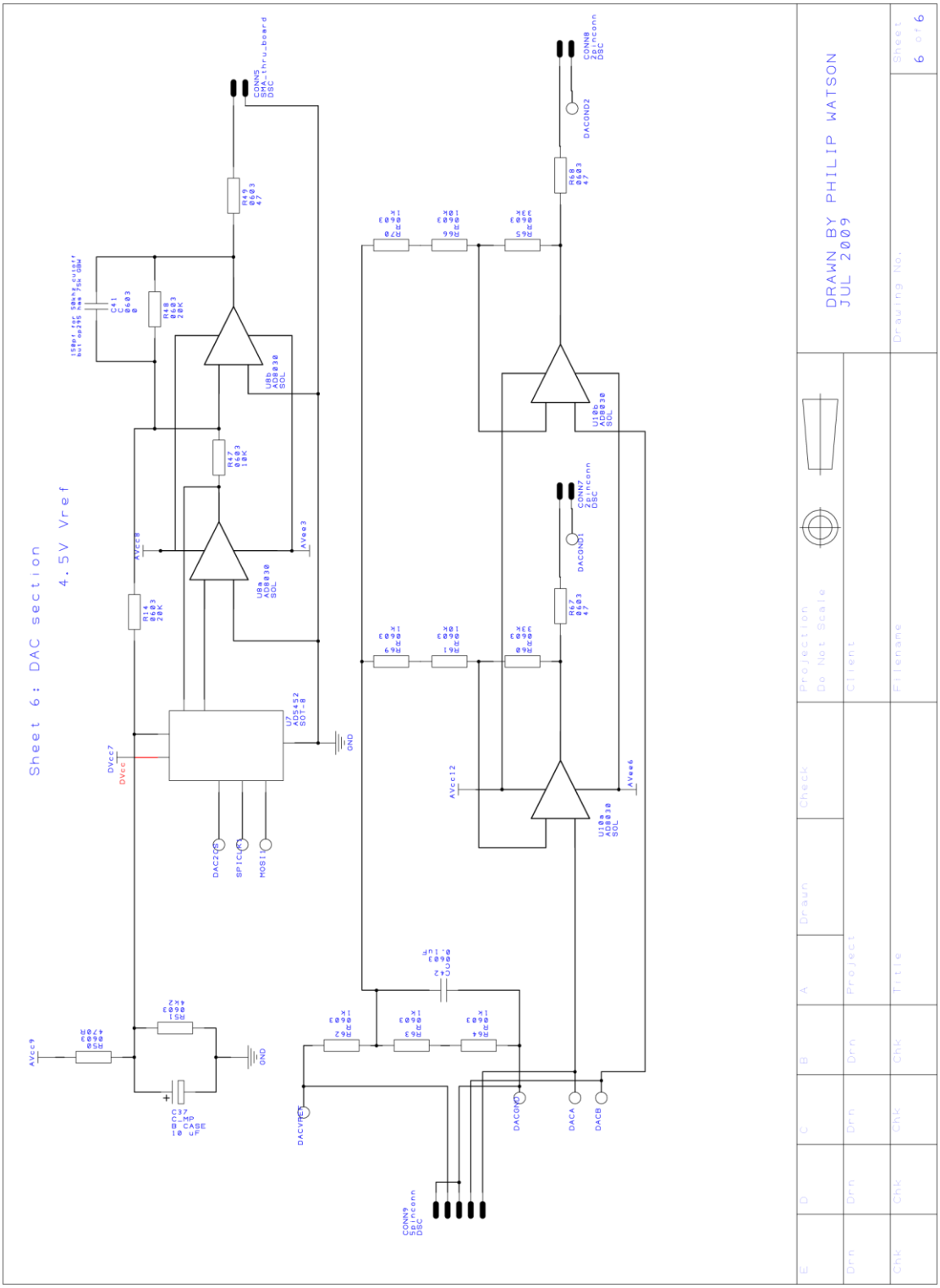


Figure E-4: Lockin amplifier schematics and 3-D render