DEVELOPMENT OF A REAL-TIME CELLULAR IMPEDANCE ANALYSIS SYSTEM

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ABSTRACT

The cell impedance analysis technique is a label-free, non-invasive method, which simplifies sample preparation and allows applications requiring unmodified cell retrieval. However, traditional impedance measurement methods suffer from various problems (speed, bandwidth, accuracy) for extracting the cellular impedance information. This thesis proposes an improved system for extracting precise cellular impedance in real-time, with a wide bandwidth and satisfactory accuracy.

The system hardware consists of five main parts: a microelectrode array (MEA), a stimulation circuit, a sensing circuit, a multi-function card and a computer. The development of system hardware is explored. Accordingly, a novel bioimpedance measurement method coined digital auto balancing bridge method, which is improved from the traditional analogue auto balancing bridge circuitry, is realized for real-time cellular impedance measurement.

Two different digital bridge balancing algorithms are proposed and realized, which are based on least mean squares (LMS) algorithm and fast block LMS (FBLMS) algorithm for single- and multi-frequency measurements respectively. Details on their implementation in FPGA are discussed. The test results prove that the LMS-based algorithm is suitable for accelerating the measurement speed in single-frequency situation, whilst the FBLMS-based algorithm has advantages in stable convergence in multi-frequency applications.

A novel algorithm, called the All Phase Fast Fourier Transform (APFFT), is applied for post-processing of bioimpedance measurement results. Compared with

the classical FFT algorithm, the APFFT significantly reduces spectral leakage caused by truncation error. Compared to the traditional FFT and Digital Quadrature Demodulation (DQD) methods, the APFFT shows excellent performance for extracting accurate phase and amplitude in the frequency spectrum.

Additionally, testing and evaluation of the realized system has been performed. The results show that our system achieved a satisfactory accuracy within a wide bandwidth, a fast measurement speed and a good repeatability. Furthermore, our system is compared with a commercial impedance analyzer (Agilent 4294A) in biological experiments. The results reveal that our system achieved a comparable accuracy to the commercial instrument in the biological experiments.

Finally, conclusions are given and the future work is proposed.

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LIST OF ACRONYMS

MEA:	Microelectrode Array
LMS:	Least Mean Squares
FBLMS:	Fast Block Least Mean Squares
FPGA:	Field Programmable Gate Array
FFT:	Fast Fourier Transform
APFFT:	All Phase Fast Fourier Transform
DQD:	Digital Quadrature Demodulation
AC:	Alternating Current
DC:	Direct Current
ECIS:	Electric Cell-substrate Impedance Sensing
IDEs:	interdigitated electrodes
UV:	Ultraviolet
DNA:	Deoxyribonucleic Acid
2D:	Two-Dimensional
SII:	Scanning Electrical Impedance Imaging\
HCC:	hepatocellular carcinoma
ATP:	Adenosine triphosphate
NRU:	neutral red uptake
CFE:	colony forming efficiency
NK:	natural killer
EIT :	Electrical Impedance Tomography
PXI-E:	Peripheral Component Interconnect Express Extensions for Instrumentation
SNR:	Signal-to-noise ratio
THD:	Total harmonic distortion

SINAD : Signal-to-noise and distortion ratio

SFDR: Spurious-Free Dynamic Range

Na: Sodium

K: Potassium

Ca: Calcium

Cl: Chloride

HCO3: Bicarbonate

Na: Nanoampere

RMS: Root Mean Square

VCCS: Voltage-To-Current Converters

DAC: Digital-To-Analog Converter

I-V: Current Injection And Voltage Measurement

ADC: Analog-To-Digital Converter

PSRR: Power Supply Rejection Ratio ()

CMRR: Common Mode Rejection Ratio (),

IT: Impedance Tomography

DABB: Digital Auto Balancing Bridge

I2C: Inter-Integrated Circuit Bus

INA : Instrument Amplifier Circuit

CMP: An Analog Comparator

REF: Voltage Reference

PGA : Programmable Gain Amplifier

CMOS: Complementary Metal–Oxide–Semiconductor

JFET : Junction Gate Field-Effect Transistor

I/O: Input/Output

LVDS: Low-Voltage Differential Signaling

QFN:	Quad Flat No-Leads Package
SiGe:	Silicon-Germanium
DDS:	Direct Digital Synthesis
RAM:	Random-Access Memory
DSP：	Digital Signal Processor
FIFO：	First In First Out
DCM：	Digital Clock Managers
PLL：	Phase Locked Loop
DDR2：	Double Data Rate
SDRAM :	Synchronous Dynamic Random Access Memory
IIR：	Infinite Impulse Response Filter
FIR：	Finite Impulse Response
CORDIC：	Coordinate Rotation Digital Computer
VHDL：	Very-High-Speed Integrated Circuit Hardware Description Language
XST ：	Xilinx Synthesis Tool
IP：	Intellectual Property
DFT：	Discrete Fourier Transform
MFEIT:	Multi-Frequency Electrical Impedance Tomography
DTFT:	Discrete Time Fourier Transform
LTI:	Linear Time Invariant
DPSD :	Digital Phase-Sensitive Demodulator

LIST OF SYMBOLS

I_r: reference current

Z_X: unknown impedance

V_o: output voltage

A_{ri}: the amplitude of the reference current

A_o: the amplitude of the resulting voltage

ω_r: the frequency of the reference current

θ: the phase difference

V_f: feedback voltage

R_f: feedback resisitance

D: the electric displacement field

B: the magnetic induction

E: electric field

H: magnetic field

ε : the electrical permittivity

μ : the magnetic permeability

σ: electric conductivity

J: current density

ϕ: the electric potential

t_{clk}: the period of FPGA's counting clock

Chapter 1. INTRODUCTION

1.1 GENERAL BACKGROUNDS

A cell is the basic unit of life. It plays an important role in recognizing the function and dysfunction of tissues, organs and organisms. For the last 30 years, great efforts were made for developing faster, more compact, and more accurate approaches for cell analysis in life sciences and biological applications. In the field of cell analysis, optical techniques have been commonly used and subject to a significant development in recent decades due to the application of lasers and fluorescence markers and the invention of the fluorescence-activated cell sorter. The optical approaches, or fluorescent-based approaches, are more sensitive and accurate in morphology (Leischner *et al.*, 2010; Bernell *et al.*, 1996; Nassberger *et al.*, 1991). However, cell tagging techniques modify cells and require more sophisticated preparations (Gardsvoll *et al.*, 2007; Abati *et al.*, 1995).

Impedance-based cell sensing technique is label-free which simplifies sample preparation and allows applications requiring unmodified cell retrieval. Compared to the traditional approaches that use radioisotope, fluorescence, luminescence, or light absorption, impedance-based methods measure the cell function without labeling (Solly et al., 2004; Yu et al., 2006). It is used to monitor various cellular functions such as cell motion, cell attachment and spreading, cell wounding assay, cell morphology, cell toxicology and cell signal transduction, by measuring the bio-impedance properties of cells in the frequency domain (Giaever and Keese, 1986; Tiruppathi *et al.*, 1992; Mahmood *et al.*, 2013; Wegener *et al.*, 2000; Hug, 2003; Betzen *et al.*, 2009; Huang *et al.*, 2008). The non-invasive nature of this method makes it suitable when further analysis to the target sample is needed, and simplify the overall analysis process.

Many publications on cell impedance analysis have appeared in the last few years. Different approaches, for example, bridges, lock-in, impedance analyzers, etc. are developed for cell impedance sensing (Linderholm *et al.*, 2008; Susloparova *et al.*, 2013; Park *et al.*, 1983). All these approaches presented both comparative advantages and drawbacks, which made them suitable for specific applications (Sun *et al.*, 2010; Wang *et al.*, 2010a; Liu *et al.*, 2009a).

Challenges, however, still remain when using impedance approaches to investigate living cells. The main objective of my work is looking for a suitable measurement approach, which fulfils the requirements of cell-scale impedance analysis and imaging: fast, accurate and convenient. With these advantages, the proposed method can be applied in broader fields such as high-throughput drug screening, large-scale cell culturing, long-term cell monitoring, cell-based biosensors and so on.

1.2 IMPEDANCE MEASUREMENTS OF CELLS

The first reported study on cell impedance measurement was made by Hober, who measured the electric conductibility in the center of cells (Hober, 1910). In 1928, Christie described a method for measuring the relative impedance of living cells to diathermy currents. The results show that the addition of saponin produces a noticeable increase in the conductivity of an electrolyte (Christie, 1928). Before 1980s, impedance-based cell researches developed slowly due to the limit of measurement and micro-manufacturing technologies. In 1984, Giaver and Keese applied electric fields to detect cell spreading and motion. In their experiment, human lung fibroblasts cells were cultured on the modified dish which included a large electrode and 4 small electrodes. An AC voltage was applied on cells for impedance measurement. It was the first demonstration of a system capable of

monitoring the proliferation and motion of an ensemble of cells in vitro, which established a foundation of cell impedance measurement technologies (Giaever and Keese, 1984). Giaever and Keese continued their research afterwards, including investigating cell behaviors, cellular shape change assessment and cell spreading (De Blasio *et al.*, 2004; Wegener *et al.*, 2000; Lo *et al.*, 1999, 1995; Tiruppathi *et al.*, 1992; Giaever and Keese, 1986). There are various systems developed for cell impedance analysis, Electric Cell-substrate Impedance Sensing (ECIS) and interdigitated electrodes (IDEs) based methods are most commonly applied for cell-scale measurements.

1.2.1 INTORDUCTION OF ECIS TECHNOLOGY

Electric Cell-substrate Impedance Sensing (ECIS) technique is one of the cellular impedance measurement techniques developed rapidly in the last 30 years. It can reveal the dynamics of morphological changes and movements of the cell in response to cell adhesion, spreading and motility, by culturing cells on electrodes contacts (Giaever and Keese, 1993). By using standard culture medium as electrolyte, the first ECIS instrumentation applied an AC signal of 1V at 4,000 Hz through a resistor of 1M Ohm in series with two gold electrodes. Voltage and phase data from the electrode systems were measured with a lock-in amplifier, and the data were processed by a computer which also controlled the applied AC signal and recorded the measurement results on different electrodes.

Figure 1.1 shows a schematic of a commercial ECIS system (8W1E, Applied Biophysics, USA). The sensing chip contains eight detecting electrodes integrated on the bottom of eight miniature culture wells. The diameter of each electrode is 250 μm. Each electrode is connected with a square pad at one end of the chip. These electrodes and pads are thin gold films (50 nm) sputtered on a

polycarbonate substrate. A cable connects the chip to a lock-in amplifier (Chen *et al.*, 1990).

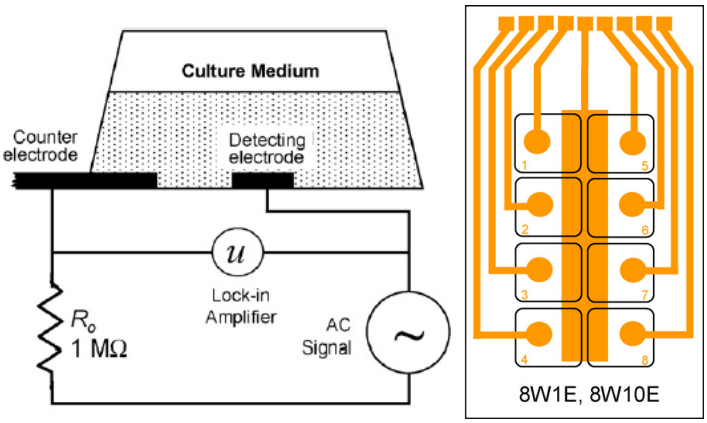

Figure 1.1 The circuit of an ECIS system and the scheme of an ECIS sensing chip (8W1E, Applied Biophysics, USA)(Rahman *et al.*, 2009).

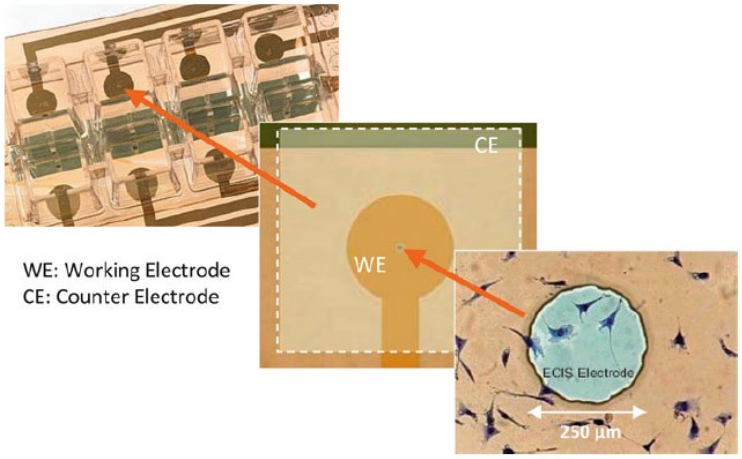

Figure 1.2 The commercial ECIS 8W1E array including 8 wells(Rahman et al., 2009).

As Figure 1.2 show, each well of 8W1E has a circular active electrode that is 250 mm in diameter (WE) and a much larger counter electrode (CE) to complete the circuit when the medium (electrolyte) is present in the well. To measure the impedance of cultured cells, a gold film is deposited on a proper substrate such as glass or silicon to fabricate specific electrode patterns. The method is based on measuring the changes in the effective electrode impedance. Cells attach and spread on the electrode when the planar electrode is immersed in the culture medium. With the increase of coverage over the electrode, the measured electrical impedance increased(Chen *et al.*, 2012; Wiertz *et al.*, 2008; Wegener *et al.*, 2000).

To assure that the ECIS measurement is non-invasive, the intensity of the applied current is kept relatively low. This AC current results in slight hyper- and hypo-polarization of the plasma membranes that has no measurable effect upon cell behaviors (Giaever and Keese, 2012). It is proved that small electrical currents for measurements have no detectable effect on living cells. Therefore ECIS method has been considered as a noninvasive method (Wegener *et al.*, 2000), which is reliable for long-term experiments.

1.2.2 INTRODUCTION OF IDES TECHNOLOGY

With the aim of improving the sensitivity, integration and analysis speed of cellular impedance measurement, a great effort has been focused on interdigitated electrodes (IDEs) technology. The application of IDEs was first reported in 1997 showing that IDEs can be used to examine more complex reactions affecting shape and morphology of the cells (Ehret *et al.*, 1997). IDEs have two main advantages compared to the traditional methods: one is that the submicron electrode widths and spacing can provide improved special sensitivity; another is that the fabrication by means of deep UV lithography allows reproducible and low cost devices (Laureyn *et al.*, 2000). Figure 1.3 illustrates the schematic diagram of the IDEs structure developed by Seoul National University, Republic of Korea. There are 50 pairs of the micro-band in their IDEs structure. (Kim *et al.*, 2012)

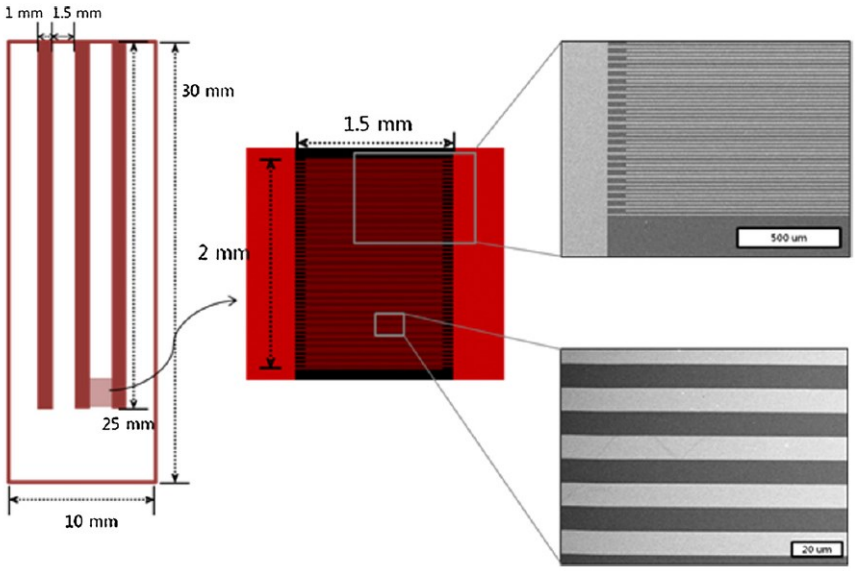

Figure 1.3 The IDEs structure developed by Seoul National University. The micro-band length and gap between the working electrode and the auxiliary electrode were 1.49 mm and 1.5 mm, respectively. The dimensions of the micro-band width and space were both 10 um (Kim et al., 2012)

Up to now, IDEs-based bio-impedance measuring techniques have been continuously developed and enhanced. It has been used to study cell proliferation and morphology (Rumenapp *et al.*, 2009), adhesion of adherent growing cell cultures (Ressler *et al.*, 2004; Ehret *et al.*, 1998), toxic potentials of chemical substances using primary neuronal cells (Buehler *et al.*, 2011), and electrochemical detection of isothermal DNA amplification (Fang *et al.*, 2012).

1.3 CELL IMPEDANCE IMAGING TECHNIQUE

The development of a cell imaging system allows that the measurement of impedance across the cell provides important information for monitoring cell activation and valuable cellular mechanisms, and enhences the understanding of the internal electrical structure of the cell (Liu *et al.*, 2006). However, compared with the cellular impedance measurements, there are fewer expriments attempting to obtain an image of the impedance distribution of cells. To our best

knowledge, the first attempt at cellular impedance imaging is reported in David A. Borkholder's doctoral degree thesis, in 1998. By using a 6 x 6 elements microelectrode array, he recorded the impedance variation of the cell population. Figure 1.4 shows both a white light image of cells cultured on the array and a 2D impedance map reconstructed by his system. The 2D impedance map was calculated by simply dividing the impedance value of cells by that of the bare electrodes (before plating cells) (Borkholder, 1998).

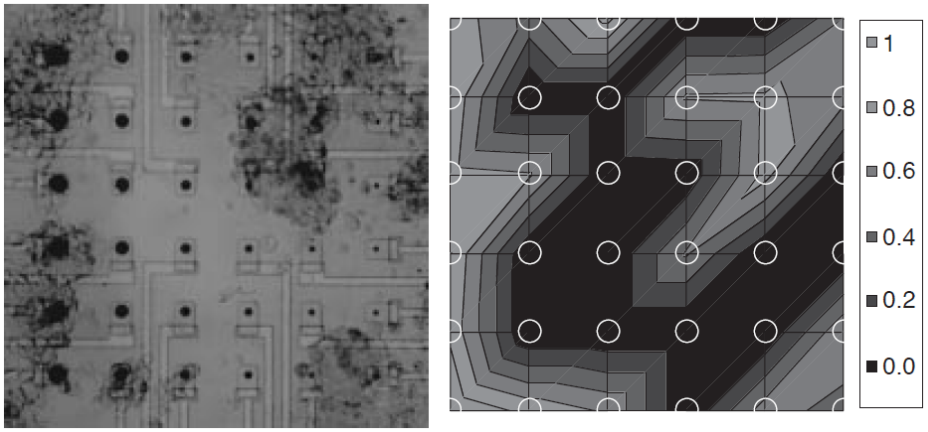

Figure 1.4 2D impedance map of the real impedance difference (with cells minus bare electrode) multiplied by the electrode area and normalized to the maximum value (Borkholder, 1998).

In 2006, Linderholm et al., presented a miniaturized impedance imaging system for 2D imaging of cell and tissue culture. The system is based on 16 microelectrodes (5 micron x 4 mm). The system used an Agilent 4294A impedance analyzer combined with a front-end amplifier for the impedance measurements. Impedance tomography images are generated at 10 kHz, which revealed Human epithelial stem cell migration, variations of epithelial thickness and changes in tissue resistivity during several days (Linderholm *et al.*, 2006). Two years later, they measured the growth human epithelial stem cells. A rapid resistivity decrease caused by permeabilized cell membranes was observed in the reconstructed impedance image, which suggesting that this technique can be used in electroporation studies (Linderholm *et al.*, 2008).

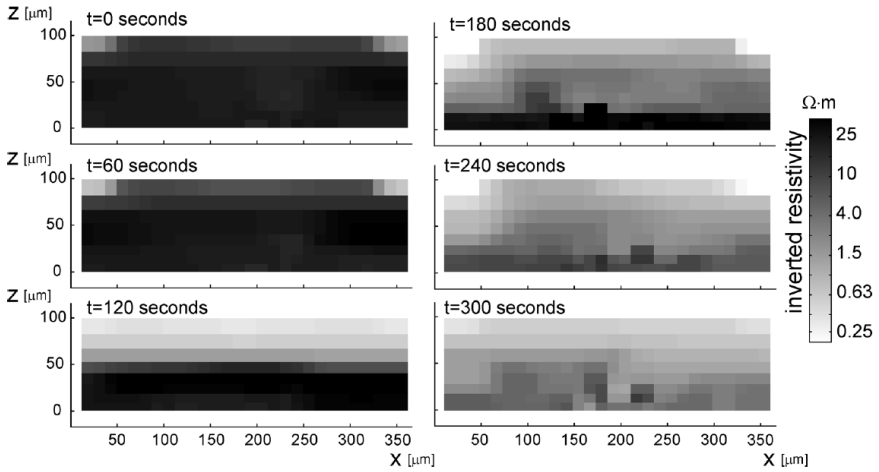

Figure 1.5 The resistivity images show the permeabilizing effects of cells (Linderholm et al., 2008).

Liu *et al*., proposed a scanning electrical impedance imaging (SII) method to view the impedance distribution of cells and tissues. By applying the reciprocity principle to the modeling of the SII system and a fast nonlinear inverse method for image reconstruction, the method can accurately show the exact distribution of conductivity from the measured current map (Liu *et al.*, 2008).

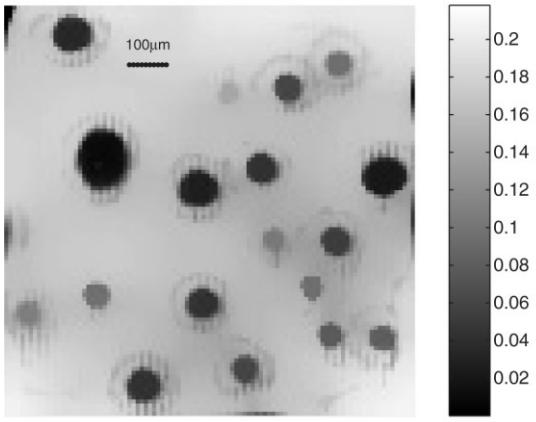

Figure 1.6 Reconstructed images from SII system developed by Liu et al., the investigated samples are breast cancer cell groups (Liu et al., 2008).

Dharia *et al*., introduced an electric impedance measurement technique to construct topographical maps of the spatial distribution of membrane capacitance of single cells. In their experiment, the electrode array was clamped in a

polycarbonate interface that allowed for cell loading and positioning. They used a lock-in amplifier system (SR830, Stanford Research, USA) and an expandable 16-bit data acquisition system (ITC 1600, InstruTECH, USA) to measure the impedance. Results show their system can effectively be applied to map cell shape and position in the recording chamber and map the endogenous spatial distribution of membrane capacitance around a single cell (Dharia *et al.*, 2009).

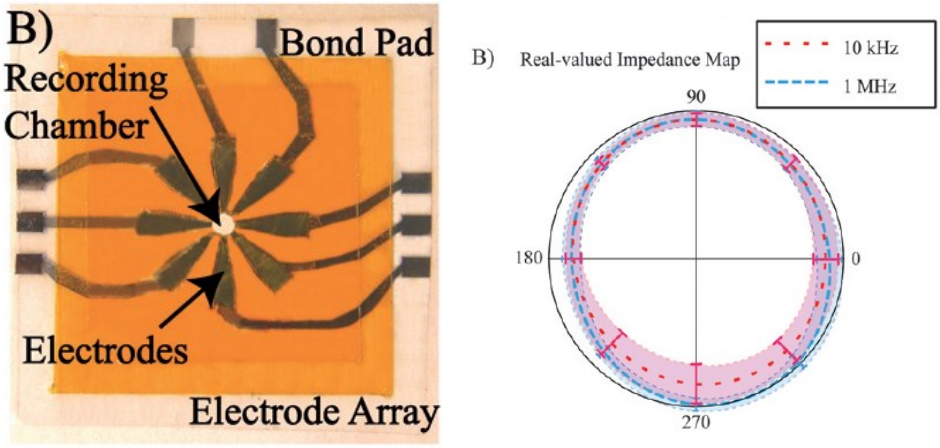

Figure 1.7 The electrode array of sceTopo system and the topography result of the real component of the cellular impedance. (Dharia et al., 2009).

Tao, *et al.*, presented a miniaturized electrical impedance tomography system that can image the 2D electrical conductivity distribution of cells. A 16-electrode circular array (the electrodes are 35um thick and the area of an individual electrode is 2.06mm^2) was fabricated and used to apply electric currents and to measure voltages across the sample. The current stimulation and voltage acquisition were performed by an impedance analyzer (Sun *et al.*, 2010). They showed reconstructed images of physarum polycephalum in Figure 1.8.

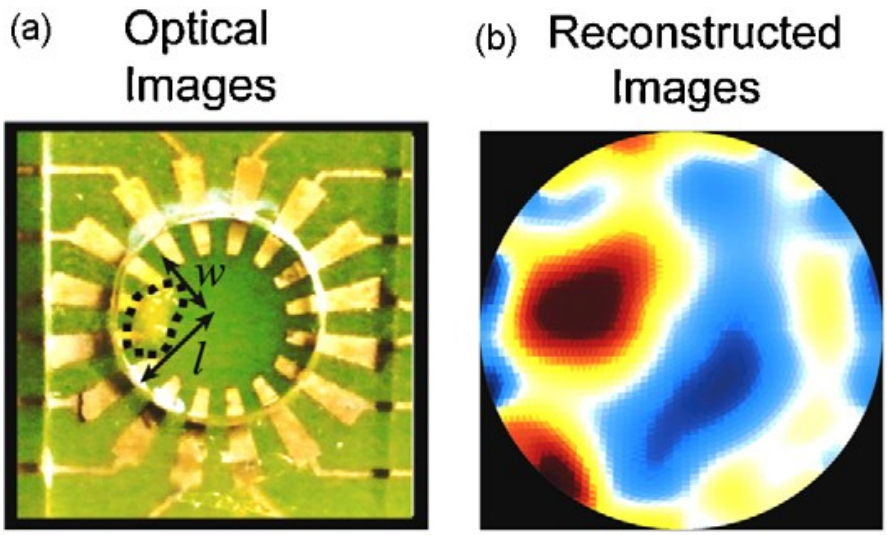

Figure 1.8 (a) Optical images of Physarum polycephalum on the agar gel in the EIT chips, (b) corresponding reconstructed images (Sun et al., 2010).

Wang *et al.* reported an electrochemical impedance microscope based on surface plasmon resonance that resolved local impedance with submicrometre spatial resolution and picoseconds time detection sensitivity. They used an electrochemical impedance microscope to monitor the dynamics of cellular processes (apoptosis and electroporation of individual cells). The high spatial and temporal resolution makes it can resolve subcellular structures and processes without labels (Wang *et al.*, 2011).

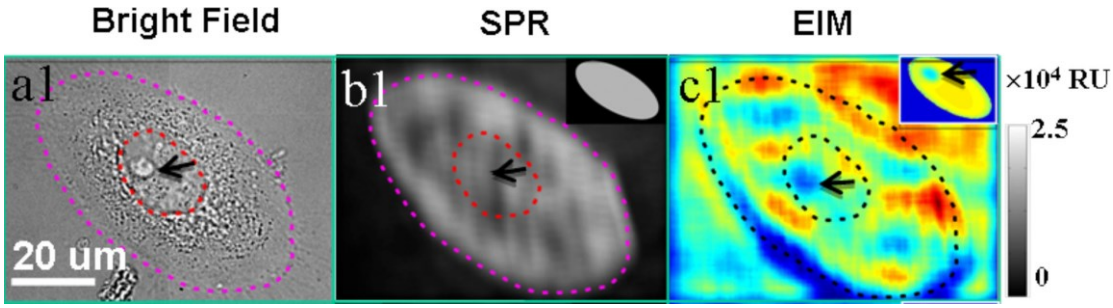

Figure 1.9 The simultaneously recorded optical transmission (a), SPR (b) and EIM (c) images of a SiHa cell at 0 (1), 30 (2) and 75 (3) min after apoptosis treatment (Wang et al., 2011).

Compared to other imaging approaches, electrical impedance based cell imaging exhibits several advantages such as relatively low cost and labeling-free operation, as well as non-invasive nature. Potential biomedical applications of a

micro impedance tomography system include monitoring of cell electroporation, wound healing investigation and cell migration. However, the current electrical impedance imaging technique is limited by its low resolution, thus not suitable for single-cell scale imaging. With the development of micro fabrication technique and measurement approaches, this obstacle will be overcome in the future.

1.4 APPLICATIONS OF CELLULAR IMPEDANCE ANALYSIS

During the past 20 years, there have been remarkable advances in technology and applications regarding cell impedance. Some publications described the applications of monitoring cellular events, such as cell adhesion and spreading on different substrates, cell micromotion, cell migration, cell morphology and cell shape change due to various factors, and cell responses to cytotoxic compounds. The most widely reported application area relates to investigating the effect of different chemicals on cells applied in pharmacology, cytotoxicity, and cell biology. Some examples of the different categories are presented as follows.

1.4.1 MONITORING OF CELL ADHESION, SPREADING, MORPHOLOGY, AND PROLIFERATION

Cell adhesion and motility strongly depend on the interactions between cells and extracellular culture substrates. When a cell reaches the substrate, it flattens and deforms by passive adhesion and spreading at first. The area of contact between the cell membrane and surface is small initially but increases continuously while the cell spreads (Wang and Liu, 2010). When the cell spreads further, the mechanisms of cell crawling such as the organization of actin cytoskeleton and formation of focal adhesions are involved (Jiang, 2012). In this process, the current flow within the adhesion area is highly dependent on the

cell-substrate interface and can be characterized by cell impedance methods. A rather limited number of experimental approaches are capable of investigating cell–substrate interactions in a quantitative way, but the impedance sensing method provides a solution to probe the kinetic aspects of this complex process (Wegener et al., 2000).

Luong, J. H. *et al*. developed an electric cell-substrate impedance sensing system to monitor the attachment and motility behavior of insect cells. They cultured adherent cells on an array of eight small gold electrodes deposited on the bottom of tissue culture wells. The experiment revealed that the impedance increased due to the attachment and spreading of cells on the gold electrode (Luong et al., 2001). Arndt, S *et al.* applied impedance method to monitor the apoptosis-induced changes in cell shape in an integral. To improve the sensitivity, they used endothelial cells derived from cerebral micro-vessels as cellular model systems. From readings of the electrical impedance of the cell-covered electrode, they found the time course of cell shape changes strongly correlates with the measured impedance (Arndt et al., 2004). Heiskanen, A. R. *et al.* studied the interaction between thiol-modified Au electrodes and Saccharomyces cerevisiae cells. The results revealed that the charge transfer resistance showed a linear relationship to the number of cells even beyond the monolayer coverage. They demonstrated that the impedance approaches feasible for real-time monitoring of saccharomyces cerevisiae proliferation (Heiskanen et al., 2008).

1.4.2 MONITORING OF CELL MIGRATION AND INVASION

Cell migration is a critical process and plays an important role in different complex processes including homeostasis, embryonic development, wound healing, immune response, and cancer metastasis (Wang and Liu, 2010). Cell migration begins with polarity and extending a protrusion in the direction of movement.

Then followed by the cell-cell adhesion. Subsequently the cell contracts and releases the attachments at the rear, resulting in moving forward to complete the cycle. The commonly used approaches for cell migration assay include Boyden chamber assay, wound-healing assay, Dunn chemotaxis chamber assay, and time-lapse microscopy, which are important tools of investigating cell migration (Jiang, 2012).

Many of impedance-based experiments on cell migration were reported. Kidney, J C *et al.* examined neutrophil transepithelial migration by resistance measurements. Resistance across each membrane of bronchial epithelial cells (16HBE) was recorded before measuring neutrophil transmigration over 2 hours. They found that 16HBE resistances were associated with neutrophil migration (Kidney and Proud, 2000). Edens *et al.* modeled polymorphonuclear leukocytes transepithelial migration across T84 monolayers and demonstrated that enhanced paracellular permeability to small solutes occurred in the absence of transepithelial migration (Edens et al., 2002). Linderholm, P. *et al.* presented a miniaturized impedance imaging system for imaging cell migration, increase of epithelial thickness and changes in tissue resistivity (Linderholm et al., 2006). Primiceri, E *et al.* developed an electrochemical impedance spectroscopy biochip to investigate the migratory ability of hepatocellular carcinoma (HCC) cells. The results revealed that the impedance approach is faster and easier than traditional transwell assays and can be suitable for high-throughput studies in drug discovery applications (Primiceri et al., 2011).

1.4.3 IN VITRO CYTOTOXICITY ASSAYS

In vitro cytotoxicity assays are the major alternative methods to animal testing for basal cytotoxicity assessment of chemicals, indicating the number of cells which are dead or alive (Zucco *et al.*, 2004). After exposure to test chemicals,

cells respond to cytoxins in the forms of loss of adhesion and cell rounding, membrane protrusions or blebbing, formation of apoptotic bodies, and ultimately engulfment of apoptotic bodies by phagocytosis (Jiang, 2012).

The traditional in vitro cell-based assays such as biochemical methods (3-(4,5-dimethylthiazol- 2-yl)-2,5-diphenyltetrazolium bromide test, MTT), ATP measurement, neutral red uptake (NRU), or growth assay like colony forming efficiency (CFE) are commonly utilized to study cytotoxic effects induced by chemicals in different cell systems (Ceriotti et al., 2007b). But these methods are based on single end points, which only detect very specific cellular changes. Also, they are time consuming, labor intensive and require complex operations at every prescheduled time point (Ceriotti et al., 2007a).

Impedance-based methods provide multiple parameters in the same assay under dynamic conditions. The cellular changes depend on cell types, compound properties and concentration, and compound exposure duration (Wang *et al.*, 2012). These apopototic responses can change cell adhesion and morphology, which induce variation of cell-substrate impedance in a fast or prolonged manner. Some useful information can be gained from real-time impedance sensing approaches, such as rate and real-time dose response of the toxins compound.

At the cellular level, impedance methods have been widely researched and used to profile compound cytotoxicity. Xiao, Caide *et al.* applied ECIS method to measure the concentration and time response function of fibroblastic V79 cells exposed to a toxicant. They proved that the chemical cytotoxicity was easily screened by observing the response function of attached cells in the presence of inhibitor (Xiao et al., 2002). They subsequently developed an on-line and continuous ECIS system for their experiment. Acute and long-term cytotoxicity effects were evaluated by resistance changing of adhesion, spreading, and proliferation of V79 fibroblastic cells (Xiao and Luong, 2003, 2005).

Glamann, Joakim et al. added natural killer (NK) cells to adherent carcinoma cells and observed the measured impedance of the RT-CES system (ACEA Biosciences, USA) declined fast dependent on the NK cell/target cell ratio. They also showed that RT-CES could be used to monitor antibody-dependent cellular cytotoxicity (Glamann and Hansen, 2006). Boyd, Jessica M *et al.* developed a cell-microelectronic sensing system to study different cytotoxic effects of the same class chemicals using nitrosamines as examples. They demonstrated that T24 cells were the most sensitive to nitrosamine exposure among the four cell lines tested (T24>CHO>A549>HepG2). The experiment suggested that T24 may serve as a new sensitive model for cytotoxicity screening, and parallel cytotoxicity profiling of nitrosamines in the four cell lines by the impedance method can be used to investigate the unique cytotoxicity of NDPhA causing cell-cycle arrest.(Male et al., 2008) Garcia, S. N. *et al.* used impedance-based cytotoxicity assay for the investigation of biocompatibility of medical devices. They performed cytotoxicity analyses using water-soluble tetrazolium salt (WST-1) and qualitatively scored cytotoxicity by examining changes in morphology at 24-h intervals. There was a clear correlation between addition of cytotoxic agents, cellular impedance, and concomitant cell layer destruction observed by microscopy (Garcia et al., 2013) .

1.5 SCOPE OF THE THESIS

The Electrical Impedance Tomography (EIT) technique has been conclusively proved to be a promising method for organ-level or tissue-level analysis in previous studies. Despite impressive advances in EIT research with reconstructed images of spatial impedance, application of EIT in monitoring cells is still very rare due to the performance of measurement systems. The speed, accuracy and

bandwidth of the traditional systems are significantly limited by the performance of measurement methods applied.

The objective of this work is to design and exploit a novel cellular impedance measurement method for real-time cell analysis and imaging. The work can be divided into two specific aims as the following.

Aim 1: Design a high performance impedance measurement method for increasing the measurement speed, accuracy and bandwidth of cell impedance measurement. It can be applied for real-time monitoring cellular impedance variation of cells and cell- scale electrical impedance tomography applications.

Aim 2: Develop a miniature prototype system and realize related algorithms to verify the proposed approach. Test the measurement performances (speed, accuracy, repeatablity, *etc.*) of the realized system to evaluate its advantage.

1.6 THESIS OUTLINE

Chapter 1. This chapter introduces the research backgrounds. General knowledge about cellular impedance, the development of cellular impedance measurements and imaging techniques, as well as recent progress, are reviewed briefly. Subsequently, the applications of cell impedance analysis are introduced. Finally, the scope of our work and the outline of the thesis are presented.

Chapter 2. The chapter focuses on measurement techniques in cell impedance analysis. Commonly used approaches for impedance measurement, including bridge, lock-in amplifier, impedance analyzer have been introduced and compared. The principle of EIT technique is introduced. The challenges in cellular impedance measurement are discussed.

Chapter 3. This chapter presents the design of system hardware. The system hardware consists of five main parts: a microelectrode array, a stimulation circuit, a sensing circuit, a multi-function card and a PXI-E based computer. Details on the design of each part are introduced.

Chapter 4. This chapter presents a novel bioimpedance measurement approach based on digital auto balancing bridge method, which developed from the traditional analogue auto balancing bridge method for impedance measurement. The methods of signal-frequency and multi-frequency DABB have been designed by using LMS-based and FBLMS-based bridge balancing algorithms repectively.

Chapter 5. This chapter describes a new algorithm-All phase Fast Fourier Transform (APFFT) for bioimpedance spectrum analysis. It provides higher precision in phase and amplitude than traditional methods in post-processing of bioimpedance spectrum. The principle, analysis and simulation results of APFFT algorithm are presented in this chapter.

Chapter.6. This chapter presented the validation and testing of the fabricated prototype system. The performances of the main circuits of our system are tested firstly, which consist SNR, THD, SINAD and SFDR. Then the performances (accuracy, speed, repeatability) of the whole system are evaluated.

Chapter 7. This chapter concludes the thesis and identifying areas of focus for future research.

Chapter 2. IMPEDANCE MEASUREMENT TECHNIQUES IN CELL ANALYSIS

In the first chapter, the background of cellular impedance analysis is introduced. In order to acquire the bioimpedance information from cells, various approaches were developed in the past decades. In this chapter, the discovered electrical properties of cells are introduced firstly. Then the basic principles of commonly used cellular impedance measurement techniques are reviewed. The methods based on lock-in amplifier and on impedance analyzer are introduced as affinity approaches. Besides, electrical impedance tomography (EIT) technique is introduced in brief. Finally, challenges in cellular impedance measurement and imaging are presented.

2.1 CELL STRUCTURE ANDITS ELECTRICAL PROPERTIES

The cell is the basic structural and functional unit of living organisms. All of the functional units of a cell are separated by membranes from the surrounding medium (Pliquett, 2008). There are two types of cells: eukaryotic and prokaryotic. They are different in both the cell structures and biological properties. Cells consist of a plasma membrane surrounding a cytoplasm containing numerous organelles, including nucleus, peroxisome, microtubule, mitochondrion, ribosomes, endoplasmic, reticulum, lysosomes and so on. Figure 2.1 demonstrates a basic structural picture of an animal cell (Alberts and Bray, 2007).

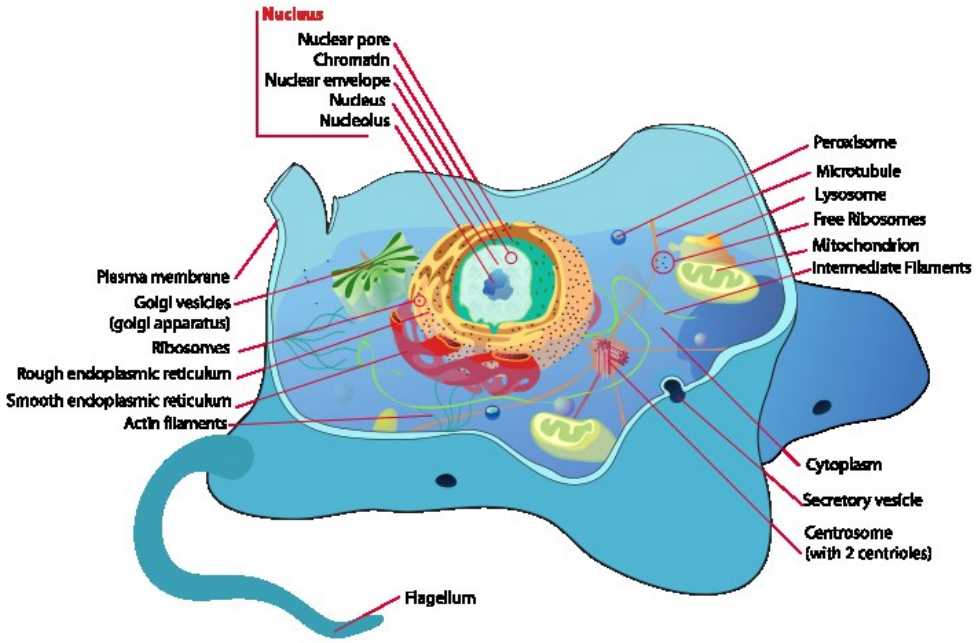

Figure 2.1 A diagram of an animal cell structure. Picture from http://en.wikipedia.org/wiki/File:Animal_cell_structure_en.svg

2.1.1 CELL MEMBRANE

Cole *et al.* measured the membrane resistance of the squid giant axon in 1939. The experimental results showed the nerve membrane has a resistance of about 1000 Ohm/cm^2 (Cole and Hodgkin, 1939). Afterwards, membranes of human muscle (Jenerick, 1953), nerve cell (Strohl, 1954), red cells (Johnson and Woodbury, 1964) have been further investigated. The cell membrane is a semipermeable lipid bilayer common to all living cells. It separates the interior of all cells from the extracellular environment. The cell membrane is selectively permeable to ions and organic molecules, which controls the movement of matter in and out of cells. It is involved in many cellular processes, such as cell adhesion, ion conductivity and cell signaling. It also functions as the attachment surface for some extracellular structures, including the cell wall, glycocalyx, and intracellular cytoskeleton (Alberts and Bray, 2007).

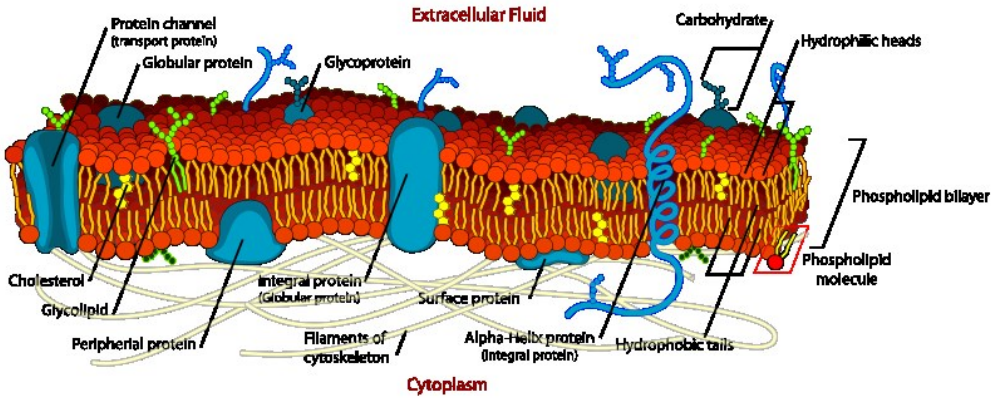

Figure 2.2 The structure of cell membrane. Picture from http://en.wikipedia.org/wiki/File:Cell_membrane_detailed_diagram_en.svg

There are three independent mechanisms for the transport of materials from extracellular space, including free diffusion, facilitated diffusion, and active transport. By these mechanisms, the cell membrane serves as a selective filter that permits only certain substances to come inside or go outside the cell. A membrane transport protein involved in the movement of ions and small molecules such as another protein across a biological membrane. They exist within and span across of the membrane. Both the lipid bi-layer and embedded proteins affect the electrical properties of the cell by transporting mechanism (Clausen et al., 1986; Taylor, 1977; Jansen et al., 1989). The intracellular plasma and extracellular fluids are composed of different ions or electrolytes. The major electrolytes include Na+ (sodium), K+ (potassium), Ca++ (calcium) and Cl− (chloride). The originally driving force of ion exchange is the difference in concentration between the inside and outside of the cell. This difference or concentration gradient is maintained mainly by Na+/K+ pumps that move Na+ out of the cell and K+ into the cell by active transport (Jeong, 2011).

Ion channels are integral membrane proteins with a pore. The specific ions in extracellular space and interior of the cell can move across the ion channel. There are four common ion channels, which include Na+ channel, K+ channel, Cl− channel, and Ca++ channel (Jeong, 2011). Ion channels allow the ion flow across a highly

isolating barrier (Pliquett, 2008). The activation of ion channels can be induced by ligand binding or a physical stimulus like pressure, temperature or a change of the electrical potential difference across the membrane (Pliquett et al., 2007; Macdonald, 1997; Gullingsrud and Schulten, 2004; Starmer, 1986). The movements of charged ions and electrons across the membrane are restricted. They can go through the membrane from the specialized ion channels and membrane spanning protein semiconductors respectively (Abrams et al., 1996).

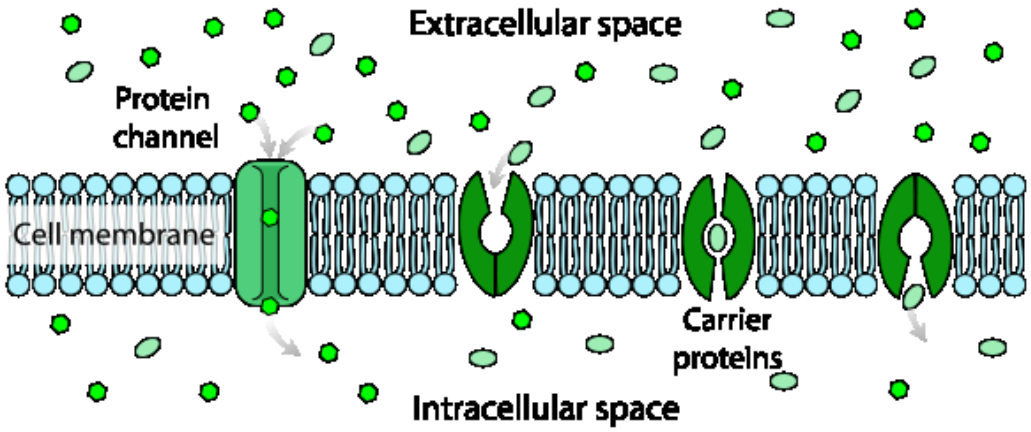

Figure 2.3 A plasma membrane with ion channels. (Jeong, 2011).

Both intra- and extracellular liquids contain ions that can be considered as electrolytes due to the free migration of charges. If a single ion channel be considered as a cylinder filled with electrolyte, the resistance of the whole cell can be estimated. The total resistance of the plasma membrane can therefore be calculated by considering the parallel combination of all the ionic channels permeating the membrane that are open for ion transport. Measurement of the membrane resistance can thus indicate how many ionic channels are open at any given time. Scharfetter *et al.* investigated the influence of ion concentration changes on the accuracy of volume measurements with bio-impedance spectroscopy. They found resistivity changes due to concentration changes of Na+, K+, Cl-, HCO3- and unspecified intracellular ions are linearly correlated (Scharfetter et al., 1997) .

Building up an equivalent circuit model of the cell membrane is useful for understanding cellular electrical properties. Since ion channels can restrict charges flowing by being open or closed, they can be characterized as resistors. Equilibrium potential for each ion represents the electrical potential difference across the channel, which is normally modeled as a voltage source. The cytoplasm and interstitial fluid are the electrical conductors and they are separated by the lipid bilayer of the membrane which has an insulating property. This characteristic can be modeled as a capacitor (Jeong, 2011). For fixed ion concentrations and fixed values of ion channel conductance, the simplified equivalent circuit of the membrane was modeled as a circuit containing a capacitance in parallel with a battery and conductance as in Figure 2.4 showed(Newman, 2008).

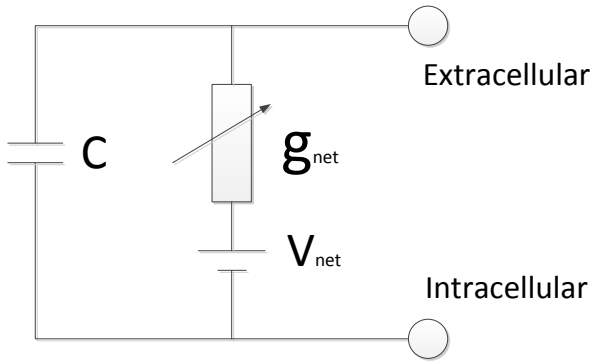

Figure 2.4 The simplified membrane model (Newman, 2008).

2.1.2 CYTOPLASM

The cytoplasm comprises cytosol and the organelles. Cytosol is the gel-like matter surrounded within the cell membrane, and organelles are the sub-structures inside cells. All of the contents of the cells of prokaryote organisms are contained within the cytoplasm. The cytoplasm consists of about 70% to 90% water and is usually colorless (Luby-Phelps, 1999).

The cytosol is a solution of many diverse types of molecules that fill most of the volume of cells. It consists generally of water, small molecules, dissolved ions,

and large water-soluble molecules (such as proteins). The concentrations of the ions in cytosol unlike those in the extracellular fluid. The cytosol also contains more charged macromolecules such as proteins and nucleic acids than the outside of the cell (Lodish, 2008). Previous studies shown that the electrical resistivity of the cytoplasm of most cells is two to three times that of the extracellular fluid (Foster *et al.*, 1976). These estimates have resulted primarily from studies on nerve axons (Cole and Hodgkin, 1939) or muscle fibers (Falk and Fatt, 1964; Fatt and Katz, 1953), or from dielectric measurements on suspensions of cells (Cole, 1968). The greater value may be due to limited ion mobility in the cytoplasm and also because the cell interior is partly occupied by low conductivity organelles. For simplicity, the resistivity of the cell interior is termed cytoplasmic resistivity, R_c, with the appreciation that this is an imperfect description (Fry et al., 2012) .

Many previous studies have focused on the electrical resistivity of the whole cells but individual aqueous cytoplasm. Forster *et al.* used single microelectrode technique measured the apparent cytoplasmic resistivity of two different giant cells in 1976. Cellular impedance is measured between 500 kHz and 5.7 MHz. They discovered that the extrapolated cytoplasmic specific resistivities of Aplysia giant neurons and muscle fibers of the giant barnacle are 40 and 74 Ω-cm respectively, (Foster et al., 1976). In 1983, Akeson, S. P. *et al.* found the Laplace solution applicable at very high electric field strengths for calculating specific cytoplasmic resistivity when membrane undergoes dielectric breakdown (Akeson and Mel, 1983). Two years later, Pilwat *et al*. verified this method to calculate the intracellular resistivity of cells from electrical membrane breakdown measurements (Pilwat and Zimmermann, 1985).

Recently, Fry, C. H. *et al.* studied the cytoplasmic resistivity in atrial myocardium. In their study, resistivity of the cytoplasm in atrial tissue was measured using two methods: a dielectrophoresis technique with isolated cells and

impedance measurements with both isolated cells and multicellular preparations. All methods yielded similar values for cytoplasmic resistance, with a mean of 138 +/- 5 Ohm/cm at 23 ℃ (Fry et al., 2012). Zhao, Yang *et al.* presented a microfluidic system allowing continuous characterization of specific membrane capacitance and cytoplasm conductivity of single cells in suspension. In their experiments, cells were aspirated continuously through a constriction channel while cell elongations and impedance at 1 kHz and 100 kHz were measured concurrently using microscopy imaging and a lock-in amplifier. 1kHz impedance data were used to evaluate cellular sealing properties with constriction channel walls and 100 kHz impedance data were translated to quantify equivalent membrane capacitance and cytoplasm resistance of single cells (Zheng et al., 2013).

In summary, cells are expected to show both reactive and resistive properties due to the composition of the cell membrane and extra- and intracellular materials. If cellular impedance is measured over a wide-ranging frequency range, such a frequency-dependent response can be detected (Stahn et al., 2012).Therefore, a wideband cellular impedance measurement method is crtical for revealing the hidden information of cells.

2.2 METHODS OF CELLULAR IMPEDANCE MEASUREMENTS

There are several impedance measurement approaches developed for testing electrical components or materials. However, applications in cell assays make stricter demands of measurement instruments. In cellular impedance measurements, low noise excitation sources, high sensitive acquisition circuits are required, as well as current limitation for keeping cellular viability, and subsequent signal processing for calculating cellular impedance from the

measured data. Lock-in amplifiers and impedance analyzers are usually applied in cell impedance measurements.

2.2.1 LOCK-IN AMPLIFIER

Lock-in amplifiers are commonly utilized for measuring the small signal from any cellular action or response. It applies phase-sensitive detection (PSD) technique, where a reference signal is used to recover a narrow-band response from broadband noise (Caplan and Stern, 1971). The technique is suitable for separating the response of a system to an applied stimulus from the noise background, which is widely applied in many scientific fields for many years (Cammann, 1972; Lue, 1977; Redondo et al., 1981; Grubic and Kemmerle, 1985). By measuring the coherent system response from an excitation AC signal, the lock-in technique can detect even minute changes in magnitude and phase, so it can be used to characterize the impedance of samples under test (Dixon and Wu, 1989).

Typically, the lock-in-amplifier based cell impedance measurements are conducted in the following procedures. A constant AC voltage is applied to cell-electrolyte-electrode system and a current limiting resistor. The resulting electric potential between the working electrode and the counter electrode is measured. In order to avoid cell damage, the amplitude of current passed through the cell has to be limited to the nanoampere (nA) range by a current-limiting resistor (Asphahani and Zhang, 2007). Therefore the cell will not be influenced by electrical stimulation during the impedance measurement.

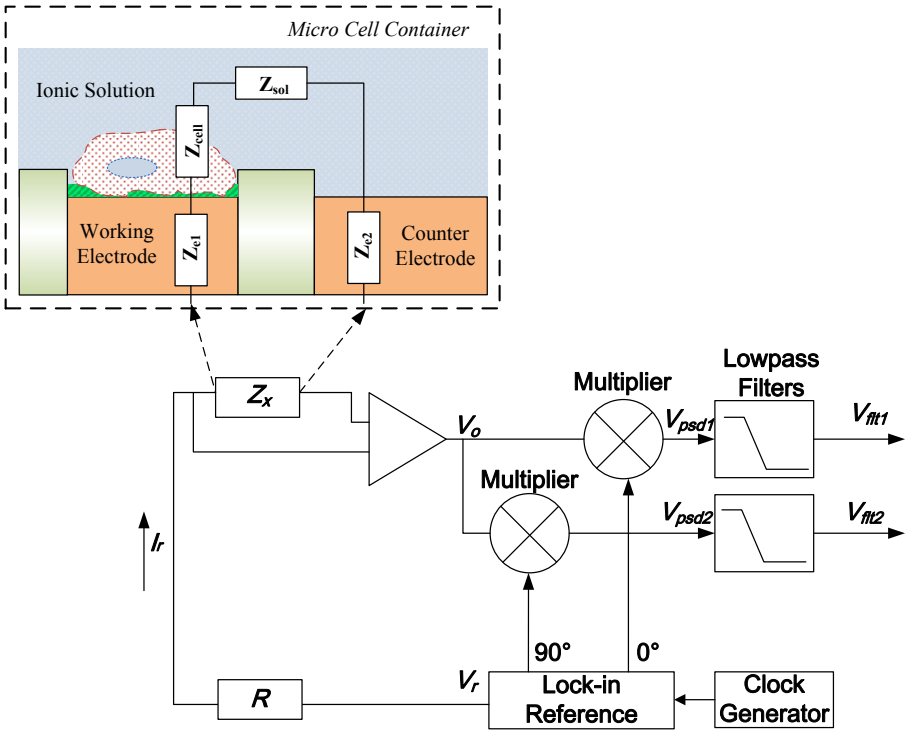

Figure 2.5 The principle diagram of lock-in-amplifier-based cell measurement.

As shown in Figure 2.5, typically, a reference current (I_r) generated from a lock-in reference is injected to an unknown impedance (Z_X) that produces a resulting voltage (V_o) with a modification of the signal phase and magnitude. The reference current and the resulting voltage (V_o) can be expressed as follows:

$$I_r = A_{ri}\sin(\omega_r t) \tag{2.1}$$

$$V_o = A_o\sin(\omega_r t + \theta) \tag{2.2}$$

where A_{ri} is the amplitude of the reference current, A_o is the amplitude of the resulting voltage, ω_r is the frequency of the reference current, θ is the phase difference between I_r and V_o. Therefore the complex impedance of Z_X at frequency ω_r can be expressed as follows:

$$\vec{Z}_x(\omega_r) = \left|\frac{A_o}{A_{ri}}\right| \angle\theta \tag{2.3}$$

In order to solve (2.3), the amplitude A_o and the phase difference θ has to be measured. The lock-in system detects the resulting voltage and multiplies it by the in-phase (0°) and the quadrature (90°) components of the lock-in reference respectively. The lock-in reference can be expressed as:

$$V_r = A_r \sin(\omega_r t) \tag{2.4}$$

Hence, the outputs of the multipliers (V_{psd1} and V_{psd2}) are simplied to the product of two sine waves:

$$\begin{aligned} V_{psd1} &= A_o A_r \sin(\omega_r t + \theta)\sin(\omega_r t) \\ &= \frac{1}{2} A_o A_r \cos(\theta) - \frac{1}{2} A_o A_r \cos(2\omega_r t + \theta) \end{aligned} \tag{2.5}$$

$$\begin{aligned} V_{psd2} &= A_o A_r \sin(\omega_r t + \theta)\sin(\omega_r t + 90°) \\ &= \frac{1}{2} A_o A_r \sin(\theta) + \frac{1}{2} A_o A_r \sin(2\omega_r t + \theta) \end{aligned} \tag{2.6}$$

The AC components of (2.5) and (2.6) are filtered by low-pass filters to estimate the DC values. Hence, two filtered DC signals are obtained as follows:

$$V_{flt1} = \frac{1}{2} A_o A_r \cos(\theta) \tag{2.7}$$

$$V_{flt2} = \frac{1}{2} A_o A_r \sin(\theta) \tag{2.8}$$

If A_r equals 2, the amplitude A_o and the phase difference θ can be calculated from (2.7) and (2.8) as follows：

$$A_o = \sqrt{V_{flt1}^2 + V_{flt2}^2} \tag{2.9}$$

$$\theta = arctg\frac{V_{flt2}}{V_{flt1}} \tag{2.10}$$

Therefore, the impedance Z_x can be calculated.

Conventionally, the lock-in technique demands sophisticated analogue circuits to realize the phase-sensitive detection and filtering (Ramani and Ganapathy, 1981; Tamiya et al., 1986). Most of the previous analog-based commercial lock-in instruments only achieved a narrow measurement bandwidth range from DC to few hundred kHz with limited dynamicrange. The major challenges of analog lock-in technique are bandwidth, output offsets, harmonic rejection and limited dynamic reservation.

With the rapid development of the digital technology, scientists have been trying to find a digital method to overcome the deficiencies of the analog lock-in technique. Modern digital lock-in technique can be used to remove large amounts of the analog circuitry by performing signal processing digitally (Dong et al., 2005; Sormaillon et al., 2008). This capability provides many additional benefits including increased reliability, accuracy and flexibility (Gaspar et al., 2004). The SNR of the lock-in amplifier is high enough to detect tiny changes of the impedance of a single cell. Therefore many lock-in instruments were applied in cellular impedance-based experiments recently (Susloparova *et al.*, 2013; Wang *et al.*, 2010b; Choi *et al.*, 2007; Barnett and Misler, 1997).

However, the major deficiency of the lock-in method is the measurement speed determined by the time constant of the low pass filters (whatever in analog parts or digital algorithm) . In order to derive the DC component from the filtered signal, the Root Mean Square(RMS) -voltage calibration has to be performed (Scofield, 1994), which takes more time to process. Hence the lock-in amplifier

cannot meet the time requirements of real-time biological impedance measurements, especially in impedance-based tomography applications.

2.2.2 *IMPEDANCE ANALYZERS*

Impedance analyzers are useful instruments for testing various components and materials in different conditions. It measures impedance at spot frequencies or within a range of frequencies. The auto balancing bridge method is commonly used in commercial impedance analyzers. The general principle diagram of the auto balancing bridge method is shown in Figure 2.6. The two arms of this bridge are formed by two symmetrical voltage generators and by the impedances to be compared.

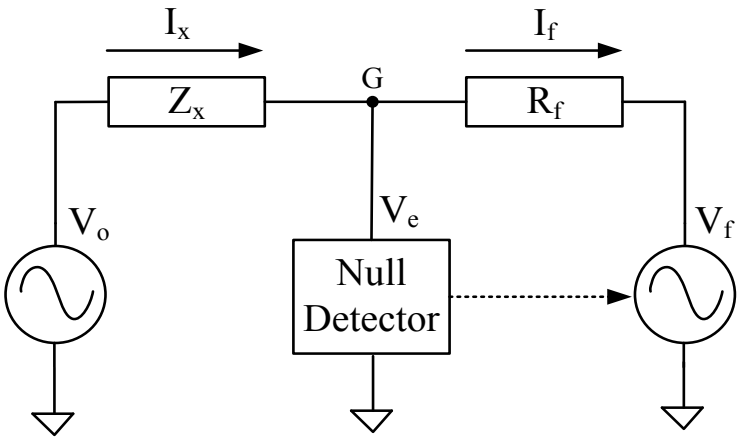

Figure 2.6 Principle diagram of auto balancing bridge.

In this bridge, V_o and V_f are two sinusoidal voltage sources with the same frequency ω_o, but with different amplitudes and phase shifts. The reference voltage source V_o has a constant amplitude A_o and zero phase shift, whereas V_f has a variable amplitude A_f and phase shift φ. The V_o and V_f can be expressed as follows:

$$V_o = A_o \sin(\omega_o t) \tag{2.11}$$

$$V_f = A_f \sin(\omega_o t + \varphi) \tag{2.12}$$

where A_f and φ can be controlled to balance the bridge. The other two elements of the bridge are the unknown impedance Z_x, and the reference impedance Z_f. For simplicity, Z_f is usually chosen to be resistive, i.e., $Z_f = R_f$. When the current flowing through the reference resistor R_f is not balanced with the one through the object under test Z_x, an imbalance current ($I_x - I_f$) will cause an imbalance voltage V_e at the terminal G. The null detector detects this voltage and adjusts both the magnitude and phase of the output voltage V_f to nullify the imbalance voltage on the terminal G. In an ideal situation, when the bridge balanced (V_e = 0), the current If will be equal to the current I_x. The following (2.13) is derived:

$$\frac{V_o}{Z_x} = \frac{V_f}{R_f} \tag{2.13}$$

The unknown impedance at the frequency ω_o is given by (4).

$$Z_x = \frac{V_o}{V_f} R_f = R_f \frac{A_o}{A_f} \angle \varphi \tag{2.14}$$

Normally, a simple negative feedback operational amplifier architecture is suitable for its I-V converter in a low frequency range typically below 100 kHz. The general circuit is shown on Figure 2.7. The current flowing through the measured sample (Z_x), due to operation amplifier's "virtual short" effect. The negative pin of the amplifier always maintains the same potential with the positive input pin.

Consequently, when the positive input pin connected to ground, the potential on the negative pin is zero volts because the current through R_f balances with the one flowing through the Z_x. The complex impedance of the Z_x can be measured with a measurement circuit consisting of two voltmeters (V_x and V_r). The voltmeter V_x measured applied voltage on the object and the voltmeter V_r measured the voltage on R_f and then calculated balance current which equals resulting current.

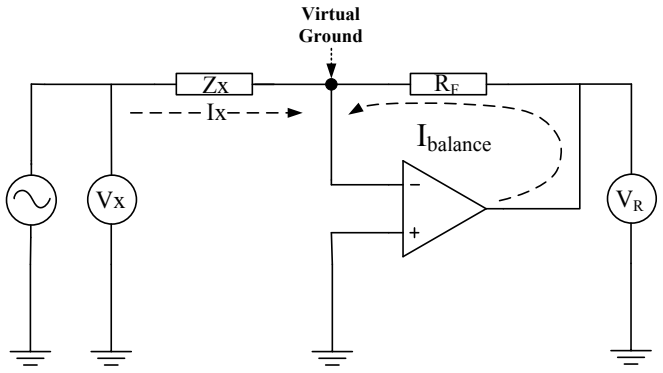

Figure 2.7 the simple negative feedback operational amplifier architecture

In practice, the performances of the operational amplifier (offset voltage, bandwidth, gain*, etc.*) will decrease versus the increasing of operating frequencies. At higher frequency, the auto-balance function normally realized by more complex circuit including null detector, phase detector, vector modulator, *etc.* as shown in Figure 2.8.

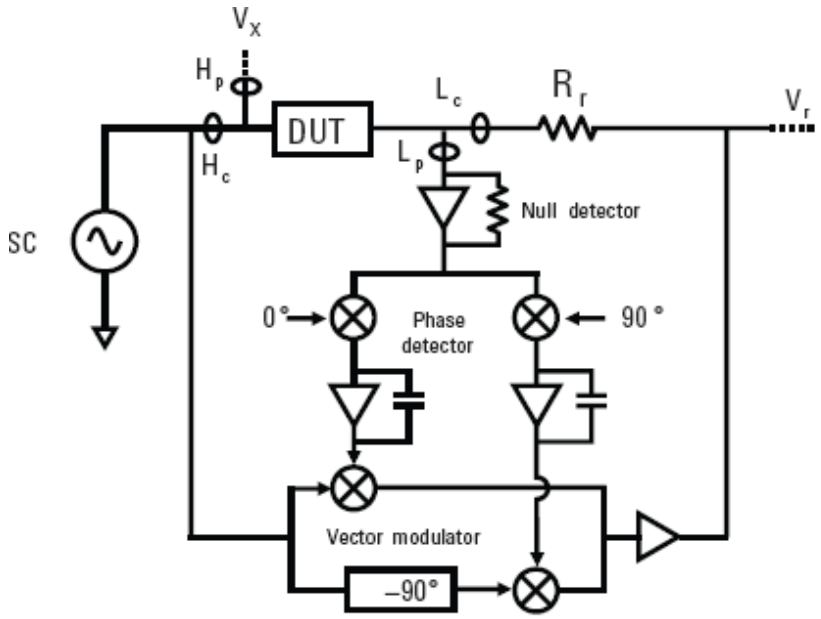

Figure 2.8 High frequency auto balancing bridge circuit. (AgilentTechnologies, 2009)

When an unbalanced current is detected by the null detector, the phase detectors in the next stage separate the current into quadrature vector components. The phase detector output signals go through loop filters and are applied to the vector modulator to drive the 0° /-90° component signals. The 0° /-90° component signals are compounded and the resultant signal is fed back through a range resistor (R_r) to cancel the current flowing through the test object. Even if the balancing control loop has phase errors, the unbalance current component, due to the phase errors, is also detected and fed back to cancel the error in the range resistor current (AgilentTechnologies, 2009).

This architecture is widely applied in most commercial impedance analyzers (eg. Solartron 1260A, Agilent 4294A, HIOKI 3532 *etc.*). It can be used in a broad frequency range (covering millihertz to hundreds of megahertz) with high measurement accuracy and a wide impedance measurement range. However, there are some deficiencies in this method:

1. It's difficult to design an analog circuit for obtaining reference quadrature signals with the rigid amplitude and phase balances. Any imbalance

between the pair of quadrature signals leads to the deviation of the decomposed signal.

2. The harmonic frequency of the reference signal will affect the detection accuracy.
3. The analog circuit should feature high linearity to maintain the accuracy in a wide frequency range.
4. The performance of analog circuit will be degraded by temperature drift and device degradation.

In high frequency applications (beyond 1MHz), this method shows better bandwidth performance than other solutions. However, as a tradeoff for its high accuracy, the slow measurement speed, sophisticated analog parts, bulky volume and high cost restrict its convenience in some cellular applications such like cell-based biosensor, multi-channel drug screening and large scale cell culture. Moreover, as a rule of thumb, more analogue components in the circuitry introduce more instability issues, and the performances of the analogue circuits (such as linearity, bandwidth, noise, *etc.*) are easily influenced by noise, temperature drift and device degradation.

2.2.3 RECENT PROGRESS

Here we summarized many researchers' efforts as published in the technical literature. Table 2.1 is a summary of selected impedance-based setups for cellular analysis.

Table 2.1 A summary of recent impedance-based setups.

Author/Year	Method type	Amplitude/ Frequency	Electrodes quantity	Electrode space(min)
Antonio Affanni,2012(	LCR meter (HP E4980a, Agilent	0.1-V ac voltage	Single	250μm

Cheng *et al.*, 2013)	Technology, USA)	frequency range of 1 kHz–2 MHz,		
Shree Narayanana,2010(Narayanan et al., 2010)	Impedance analyzer, (HP 4192A, Agilent Technology, USA)	50mV excitation; frequency range of 1 kHz to 1MHz,	Multi-(20)	45µm
Fareid Asphahani,2011 , (Asphahani et al., 2011)	Lock-in amplifier. (SR810, Stanford Research Systems,USA)	10 mV sine wave frequency range of 500 Hz to 20 kHz	Multi-(32)	20 µm
Cornelia Hildebrandt,2010(Hildebrandt et al., 2010)	Impedance analyzer (4294, Agilent Technologies,USA)	10mV frequency range of 100 Hz to 1MHz.	Multi-(16)	1mm
Jhih-Lin Hong,2012 (Hong et al., 2012)	Impedance analyzer (6440B, Wayne Kerr Precision Component Analyzer,UK)	0.2–1.0 V frequency range of 20–101 kHz.	Single	10um
Stolwijk, Judith A.,2011 (Stolwijk et al., 2011)	Impedance analyzer (Solatron Instruments, SI-1260, UK)	AC signal with amplitude of 70 mV at 4 kHz	Single	250um
Qingjun Liu,2009(Liu *et al.*, 2009b)	Impedance analyzer (VersaSTAT3,Princeton Applied Research, USA)	sinusoidal AC voltage of 10mV amplitude (peak-to-peak) frequency range of 1Hz to 1MHz.	Multi-(10 x 10)	80um
Nirankar N. Mishra,2005 (Mishra et al., 2005)	An function generator (HP3325A, Agilent Technology, USA) and A data acquisition system	amplitude of 50.5mV frequency range of 1k to 8 kHz	Single	100um

	(PowerLab 4/20, ADInstruments, USA)			
Lei Wang,2010 (Wang *et al.*, 2010a)	DAQ card (PCI-6110, National Instruments, USA)	frequency range of 5k–250 kHz	Single	60um
H.S. Kim,2009 (Kim et al., 2009)	Impedance analyzer (4294A, Agilent Technology, USA)	500 mV frequency range of 40 Hz to 10 MHz.	Single	4um
Dana Krinke, 2009 (Robitzki et al., 2009)	Impedance analyzer (4294A, Agilent Technologies, USA)	alternating voltage of 10mV frequency range of 100Hz to 500 kHz	Multi	NA

In specific, measurements at the high frequency end of the spectrum (>1MHz) are more challenging to achieve with high precision, and measurement errors caused by cables and instrumentation become more obvious in this frequency range, demanding specialized reference and normalization techniques to reduce these effects for accurate and repeatable results (Barsoukov and Macdonald, 2005). It is interesting to note that most reported experiments are performed below 2MHz and there are no detailed reports to show the measurement speed of their setups. We speculate that might result from limitations in commercial instruments, which are related to measurement method, and an unawareness of challenges related to measurement speed.

2.3 PRINCIPLE OF ELECTRICAL IMPEDANCE TOMOGRAPHY TECHNOLOGY

Electrical impedance tomography is a developing medical imaging technology that is calling the attention of the researchers，due to its low-cost，wealth of information and non-invasive nature (Brown, 2001; Wang *et al.*, 2001). EIT technique normally applied to display the spatial distribution of the conductivity distribution inside a human body (Brown *et al.*, 1994; Griffiths and Jossinet, 1994; Edic *et al.*, 1995).

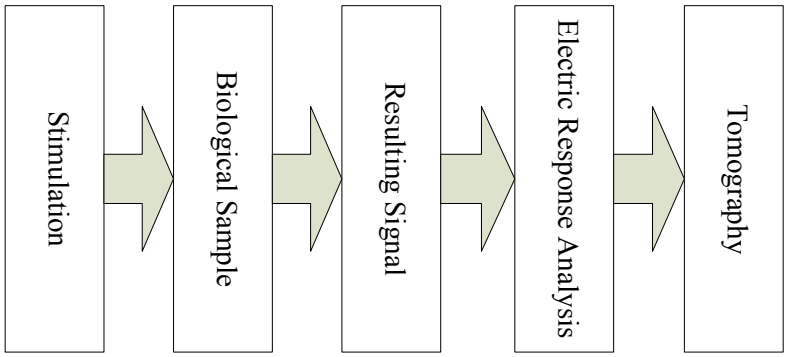

Figure 2.9 Working flow of EIT

As Figure 2.9 illustrated, in a EIT system, an excitation is applied to electrodes on the body surface, cause an electromagnetic field appearing within the volume. The resulting electrical potentials are measured and used to calculate the impedance distribution between electrodes.(Kotre, 1994; Metherall *et al.*, 1996) Finally, an image reconstruction process is applied to display this distribution of the interior of a body for medical use. The advantages in portability, low cost and safety suggests that the EIT technique becomes a novel imaging solution (Holder, 2005).

2.3.1 THEORY OF ELECTRICAL IMPEDANCE TOMOGRAPHY

Figure 2.10 shows a general principle diagram of a 2D EIT problem, itconsists of 16 electrodes attached on the surface of an observed object. One pair of electrodes injects a small stimulation current with frequency ω into the object.

The resulting potential distribution within Ω area is measured by another pair of electrodes.

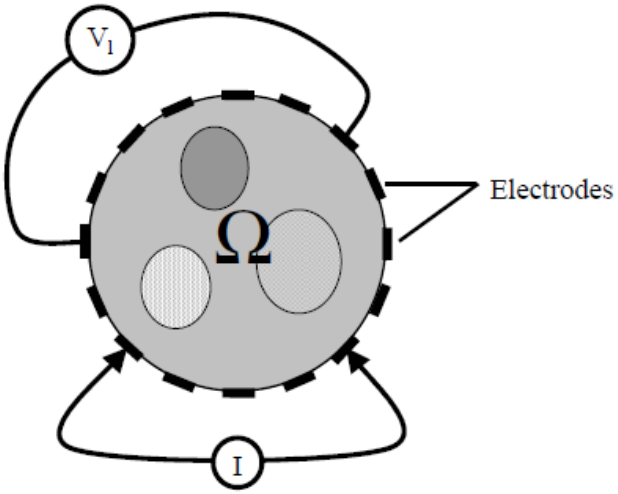

Figure 2.10 A general principle diagram of a 2-D EIT problem

The electromagnetic field within Ω area is governed by Maxwell's equations:

$$\nabla \times E = -\frac{\partial B}{\partial t} \tag{2.15}$$

$$\nabla \times H = J + \frac{\partial D}{\partial t} \tag{2.16}$$

The electric displacement field, denoted by D, and the magnetic induction B can be expressed by functions of electric field (E) and magnetic field (H) as follows:

$$D = \varepsilon E \tag{2.17}$$

$$B = \mu H \tag{2.18}$$

Where ε denotes the electrical permittivity and μ denotes the magnetic permeability. For practical biological samples, these parameters are anisotropic (Wang *et al.*, 1998; Aaron *et al.*, 1997; Plonsey and Barr, 1986), but here we assume the electrical permittivity ε, the magnetic permeability μ and the electric conductivity σ are isotropic to simplify the theory description. By

substituting the current density as $J = \sigma E$, and applying the plane-wave definitions for the electric field:

$$E = \hat{E} e^{i\omega t} \tag{2.19}$$

$$B = \hat{B} e^{i\omega t} \tag{2.20}$$

The equation (2.15) and (2.16) can be expressed as following:

$$\nabla \times E = -i\omega\mu H \tag{2.21}$$

$$\nabla \times H = J + i\omega\varepsilon E \tag{2.22}$$

The current density J can be expressed by:

$$J = J_o + J_s \tag{2.23}$$

In EIT applications, the current density J consists of two components: J_o denotes the current density caused by ohmic current $J_o = \sigma E$, and J_s is caused by bioelectrical sources inside the sample (for example, cell activities or electroneurographic signal). Normally, in the frequency range of EIT applications (over KHz), the J_s can be neglected because the effect is tiny. Therefore the EIT's Maxwell equations can be expressed as:

$$\nabla \times E = -i\omega\mu H \tag{2.24}$$

$$\nabla \times H = (\sigma + i\omega\varepsilon) E \tag{2.25}$$

Because the magnetic induction of the biological sample is too small to be considered (Kolehmainen *et al.*, 1997), the electric field E can be considered as a quasi-static field, therefore, the equation (2.24) can be simplified as:

$$E = -\nabla\phi \tag{2.26}$$

where ϕ is the electric potential. By substituting (2.26) into (2.25), and taking the divergence of both sides, the equation can be expressed as:

$$\nabla \cdot (\nabla \times H) = \nabla \cdot (\sigma + i\omega\varepsilon)E \tag{2.27}$$

$$0 = \nabla \cdot (\sigma + i\omega\varepsilon)\nabla\phi \tag{2.28}$$

Therefore the governing equation of EIT problem can be derived as following:

$$\nabla \cdot (\sigma + i\omega\varepsilon)\nabla\phi = 0 \tag{2.29}$$

The equation (2.29) is a second-order elliptic partial differential equation. In order to get the solution, the boundary conditions which are dependent on the electrode configuration and the measurement approaches have to be defined. If we measured the boundary potentials and currents, the distribution of electric conductivity σ can be derived by solving equation (2.29).

2.3.2 ARCHITECTURE OF EIT SYSTEM

There are many different EIT systems developed recently, as well as various measurement approaches applied. The most commonly used approaches are based on I-V method which inject a constant AC current and measure the resulting voltage. The general architecture of an EIT system based on I-V method is shown in Figure 2.11.

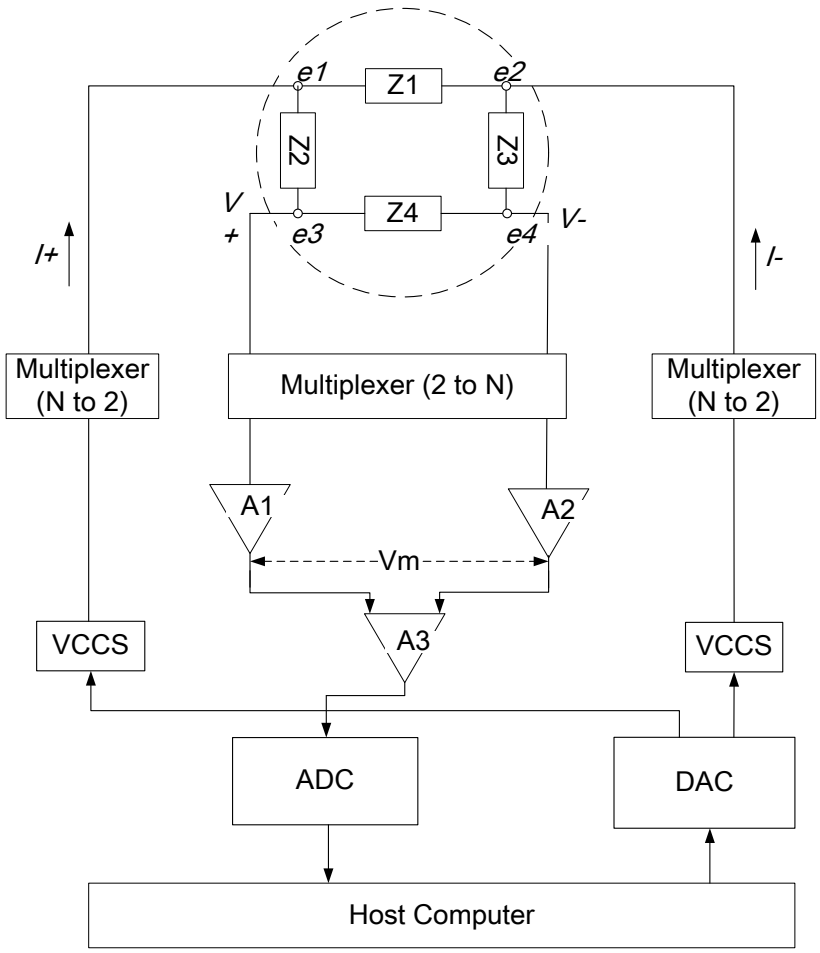

Figure 2.11 General structure diagram of EIT system based on I-V method

At the beginning, a pair of differential stimulation signals generated by a digital-to-analog converter (DAC) in voltage form. This signal is fed to two voltage-to-current converters (VCCS) and converted to a differential pair of current signals respectively. A 2-to-N multiplexer switches these current signals to one pair of electrodes at a time. Simultaneously, potentials on electrodes are buffered by operational amplifiers and fed into another N–to-2 multiplexer. By switching this multiplexer, the ADC can acquire any electrode voltages among the electrode arrays. The multiplexer then switches to next electrodes and repeats the similar procedure again.

Normally, there are hundreds or thousands of measurements should be performed in order to evaluate the boundary conditions as accurately as possible.

In multi-frequency EIT applications, these procedures will repeat at other frequencies which takes a long time. The digitized resulting voltages have been sent to the computer and used for calculating impedance distribution. Finally the impedance images are reconstructed and used to analyse the sample.

2.4 CHALLENGES IN CELLULAR IMPEDANCE MEASUREMENTS AND IMAGING

2.4.1 MEASURMENT SPEED

The time dependent response of cellular impedance exhibit the dynamic characteristics of living cells, which can reflect the biological activities happened simultaneously. Real-time monitoring cell metabolism by impedance-based approaches provide an alternative way of studying cell biology. From previous research results of literatures, the cell activities exhibit various durations because of the differences in type of cells, external stimulations and the cultural environments. For example, McConnell *et al.* studied the cellular response to muscarinic acetycholine receptor. The results showed that extracellular acidification variation caused by the muscarinic acetylcholine receptor is instantaneous response within 30 seconds after the addition of carbachol as the activation (McConnell et al., 1992). Also, for drug analysis applications, the cell characteristics change in few seconds (Liu et al., 2007). In wound healing assays, the cell wounding can happen within a few seconds under external AC excitation (Hsu et al., 2010) .

Unlike the impedance of tissues or organs, cellular impedance is more sensitive to external influences, which changes relatively faster and bigger. In order to measure the real-time changes of cellular impedance, the measurement approaches have to achieve relatively high speed corresponding to cellular activities. Especially in EIT application, in order to show the impedance image in

real time, the total time consumption of multiple measurements (normally from hunderds to thousands) has to be less than the duration of cell activity, which demands highspeed of measurement methods.

2.4.2 ACCURACY IN WIDE BANDWIDTH

The frequency spectrum of bio-impedance contains many biological characteristics which can be used to reveal the physiological and pathological mechanisms of measured samples. Due to the limit of measurement approaches and instruments, most previous related research is performed in the low frequency's range from kHz to MHz, which only covers a small part of the whole frequency range. To the best of our knowledge, there is no reported impedance-based cellular tomography system realized beyond 1MHz. The bandwidth of cellular impedance measurements depends on many of factors:

a) The resistance of microelectrodes and the parasitic capacitance of connection parts can lead to a rapid signal attenuation in the high frequency range due to its low-pass filter effect.
b) The thermal noise of metal electrodes will increase while the frequency is increased. In cellular impedance measurement instruments, the resistance of microelectrodes is normally much bigger than that of EIT application due to the smaller size of cells. It could introduce noise in the measurement results, especially in the high frequency range.
c) The performances of analog devices (signal-to-noise ratio (SNR), Common Mode Rejection Ratio (CMRR), Power Supply Rejection Ratio (PSRR), Total Harmonic Distortion (THD), linearity, Etc.) degrade while frequency increases, which will limit the performances of the measurement system.

2.4.3 NOISE

The electrode noise (thermal noise), the electromagnetic interference noise and the biological noise are the major kinds of noise exist in the cell-based measurement system(Wang and Liu, 2010). Because the signals in cellular measurements are too weak to detect, a little noise within the system can significantly change the results. The electrode noise cannot be removed theoretically, but the interference noise can be partially suppressed by dedicated circuit layout and guarding, and the biological noise and signal can be filtered by analogue or digital filters in the measurement system to some extent. However, the remaining noises are still apparent and will affect the system performance.

2.4.4 SYSTEM CALIBRATION

Calibration is a necessary step either in traditional impedance measurement experiments or in EIT applications. The purpose of the calibration procedure is to compensate the measurement error caused by external components (electrodes, wires, connectors, *etc.*) and interference (common noise, thermal noise, temperature and humidity of the environment, *etc.*). General calibration methods of impedance-based instruments such as open-short calibration, ground calibration, and reference calibration, can be performed via fixture or connection cables. In EIT application, phantoms which built by solution, gel, or electric components are used to calibrate imaging performance (Griffiths et al., 1989; Schneider et al., 2000; Kao et al., 2008).

However, due to the limit in volume of the cell container (whether the culture dish or MEA), all of the methods above are not applicable in cell-scale measurement. The measurement results actually consist of the impedance of fixture, electrode, electrode-solution interface, solution and cells. In most of the experiments, scientists use the comparison method to analyse the difference of

measured results, but there still are many uncertain factors changing during this process, which may cause a significant error in the results.

2.5 CONCLUSION

In this chapter, the cell-related theories have been reviewed at the beginning. The cell is the basic structural and functional unit of living organisms. It consists of a plasma membrane surrounding a cytoplasm containing numerous organelles. The cell membrane is selectively permeable and able to control what material enters and exits the cell. The cytoplasm comprises cytosol and the organelles. Cytosol is the gel-like substance enclosed within the cell membrane, and organelles are the sub-structures inside cells. Both intra- and extracellular liquids contain ions which can be considered to be electrolytes due to the free migration of charges. Thus, the cell exhibits different impedance characteristics due to the composition of the cell membrane and extra- and intracellular materials. If cellular impedance is measured over a broad frequency range, such a frequency-dependent response can be observed by cell impedance measurement approaches.

Lock-in amplifiers and impedance analyzers are commonly used approaches in cell impedance measurements. The principles of these methods are introduced briefly in the section 2.2. The lock-in technique is suitable for detecting the response of a system to an applied stimulus from the noise background, but the measurement speed is limited by the time constant of the low pass filters. The auto balancing bridge method is usually used in commercial impedance analyzers, which shows better bandwidth performance than other solutions in high frequency applications (beyond 1MHz), but as a tradeoff for its high accuracy, the slow measurement speed, sophisticated analog parts, bulky volume and high cost restrict its convenience in some cell-based experiments.

Section 2.3 introduced the theories of EIT technology. Electrical impedance tomography technology is a promising imaging technology, which features low-cost，wealth of information and is non-invasive The most commonly used approaches are based on I-V method which injects a constant AC current and measures the resulting voltage. The general architecture of an I-V method based EIT system is presented in detail.

Finally, section 2.4 summarized the current challenges in cellular impedance measurements. Speed, bandwidth, noise and calibration are major points to improve the performance of cell impedance instruments. Also, these problems are major features of my research in this thesis.

Chapter 3. DESIGN AND FABRICATION OF SYSTEM HARDWARE

The hardware is the basis of the proposed system. This chapter presents the design of the system hardware. The design and realization of five main parts in the system, including a microelectrode array, a stimulation circuit, a sensing circuit, a multi-function card and a PXI-E based computer are introduced in detail.

3.1 THE PRINCIPLE OF SYSTEM

There are two operation modes supported by the system: the impedance measurement (IM) mode and the impedance tomography (IT) mode. The IM mode can be used to measure the cellular impedance and IT mode is used to electrical impedance tomography of cell samples under observation.

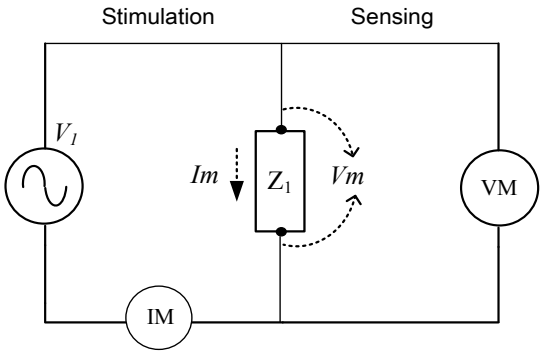

Figure 3.1 The principle diagram of IM mode

In order to simplify the theoretical analysis, the major structure of the proposed measurment method consists of two major parts: stimulation circuits and sensing circuits. As illustrated in Figure 3.1, in IM mode, the stimulation circuits generate an excitation signal applied to one pair of electrodes. An AC

current is flowing through the electrode-electrolyte-cell system (Z_1) and the resulting voltage signal between these two electrodes (*Vm*) is measured by the sensing circuits. Thus, the impedance of Z_1 can be derived by Ohm's law:

$$Z_1 = \frac{V_m}{I_m} \tag{3.1}$$

The IM mode can be applied to measure the cellular impedance between any two electrodes among the array. In this mode, the configuration of the measurement circuit is the two-terminal connection. In this connection mode, the excitation electrodes are also used for sensing the resulting potentials, which is easy to realize, but will add the electrode impedance to the measured results. It has to be compensated in the post processing of measured data.

Another configuration is named the four-terminal connection, also known as Kelvin sensing, which was invented by Lord Kelvin in 1861, who designed the Kelvin bridge to measure small resistances.The four-terminal connection is widely applied in bioimpedance measurement and electrical impedance tomography applications. (McEwan *et al.*, 2007; Fabrizi *et al.*, 2006)

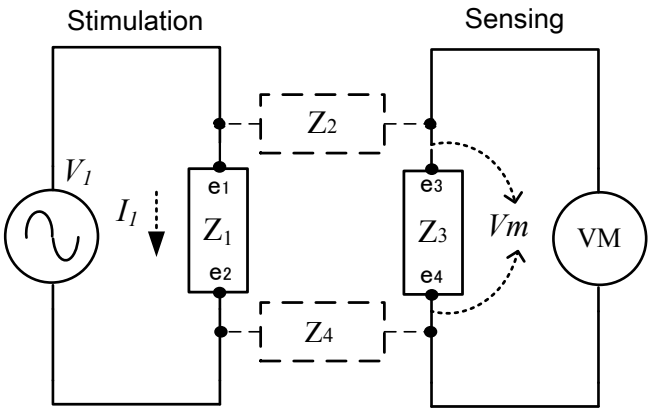

Figure 3.2 The principle diagram of IT mode

The general principle diagram of IT mode, which applies four-terminal connections is presented in Figure 3.2. The stimulation circuits in this mode are

similar to that in IM mode, but the sensing circuit measures the other two electrodes (e3 and e4) instead of the stimulating electrodes (e1 and e2) in the IM mode. The actual measured impedance is transferred impedance between Z_3 and Z_1, which can be calculated as follows:

$$Z_m = (Z_1 + Z_2 + Z_4) \| Z_3 = \frac{V_m}{I_m} \tag{3.2}$$

As shown in Figure 3.2, the stimulation circuits are used to generate an excitation signal which applies to a pair of electrodes. An AC current is flowing through the electrode-electrolyte-cell system (Z_1) and the resulting electric field will change the electrical potential of adjacent electrodes. The voltage difference (V_m) between the other two electrodes (e_3 and e_4) is measured by the sensing circuits. Subsequently, by measuring potentials of other electrodes, the impedance distribution image can be reconstructed by the EIT algorithm.

3.2 ARCHITECTURE OF SYSTEM HARDWARE

The brief hardware architecture diagram of the proposed system is shown in Figure 3.3. The system consists of five main parts: a microelectrode array, a stimulation circuit, a sensing circuit, a multi-function card and a PXI-E based computer.

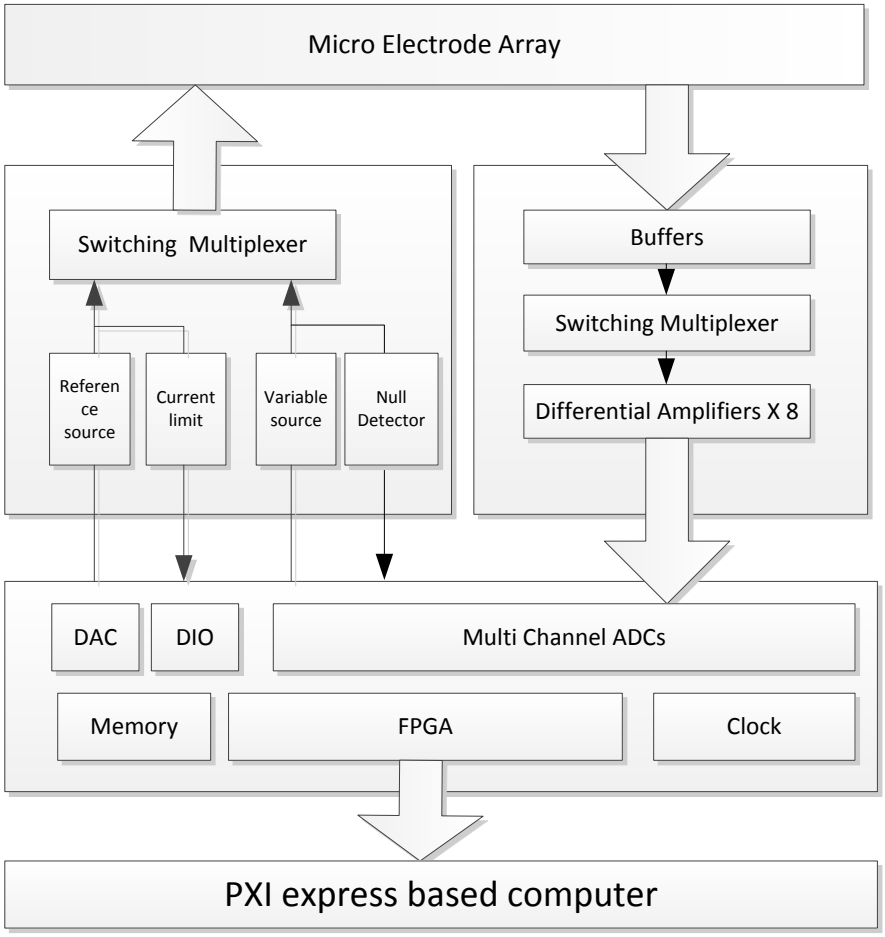

Figure 3.3 The hardware architecture of the system

3.3 MICROELECTRODE ARRAY

The microelectrode array (MEA) is a sensing part for cellular measurement. There are 72 electrodes allocated in two sub-arrays with different shapes (each array contains 36 electrodes) for various applications. The diameter of the electrode is 100 μm, and the space between each electrode is 150 μm. The selection of materials for electrode fabrication depends on the intended application, ionic species involved, inertness of the material to the environment, and their suitability to the fabrication process. In our application, gold electrodes are used, which are commonly applied in cellular analysis experiments (Arndt *et al.*, 2004; Xiao and Luong, 2005; Male *et al.*, 2010; Liu *et al.*, 2013) .

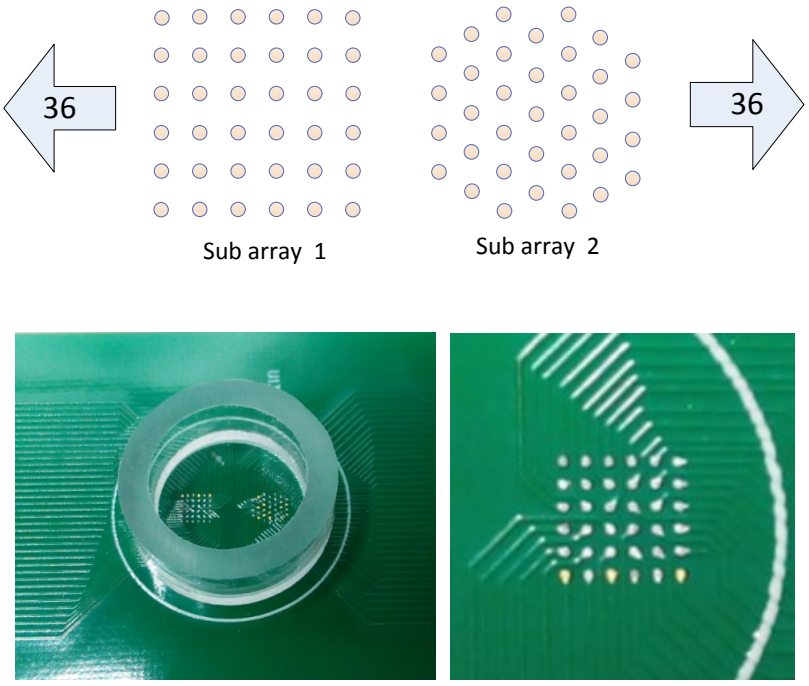

Figure 3.4 The structure of microelectrode array

3.4 STIMULATION CIRCUITS

The stimulation circuits are used for generating a small signal to stimulate the cells under test, normally this signal is AC voltage with limited output current. The circuit applied in the system is based on a digital auto balancing bridge (DABB) method, which are improved from the conventional analog auto balancing bridge (AABB) method. The general principle diagram of the DABB circuit is shown in Figure 3.5.

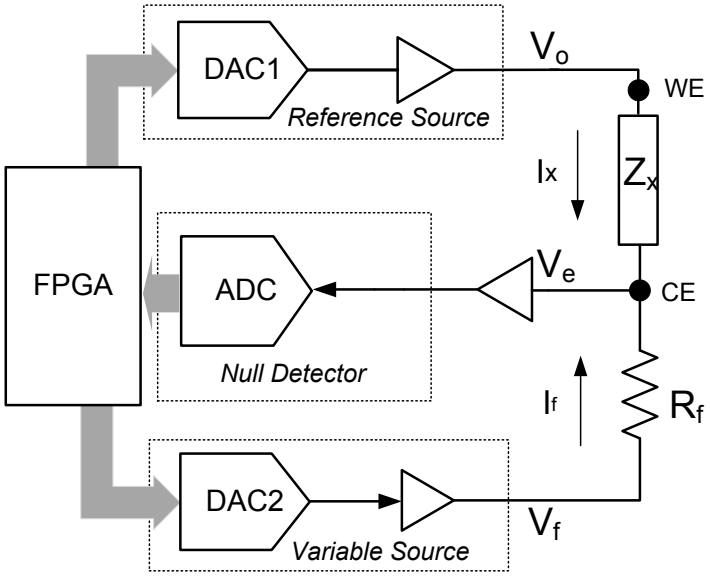

Figure 3.5 The principle diagram of DABB circuit

The architecture of the DABB circuit mainly consists of four parts: a reference source, a null detector, a variable source, and an FPGA. The digital analog converter (DAC) based programmable reference source is used to generate the reference voltage (V_o) applied to the working electrode (WE). Another DAC-based variable source is used to generate a variable voltage (V_f) applied to the counter electrode (CE). The null detector is used to detect the imbalance voltage (V_e) on the CE. The digital auto balancing algorithm implemented in the FPGA keeps adjusting the variable voltage V_f to reduce the imbalance voltage V_e gradually. When V_e is less than a user-defined threshold, the bridge is considered to be balanced. Subsequently, the injecting current I_x can be calculated in the FPGA (Li *et al.*, 2011). The principle and realization of DABB will be detailly introduced in chapter 4 later.

In order to select the working electrode and counter electrode in the electrode array, a switching circuit is designed. It is built from eight analog multiplexers. The architecture of the switching circuit is shown in Figure 3.6:

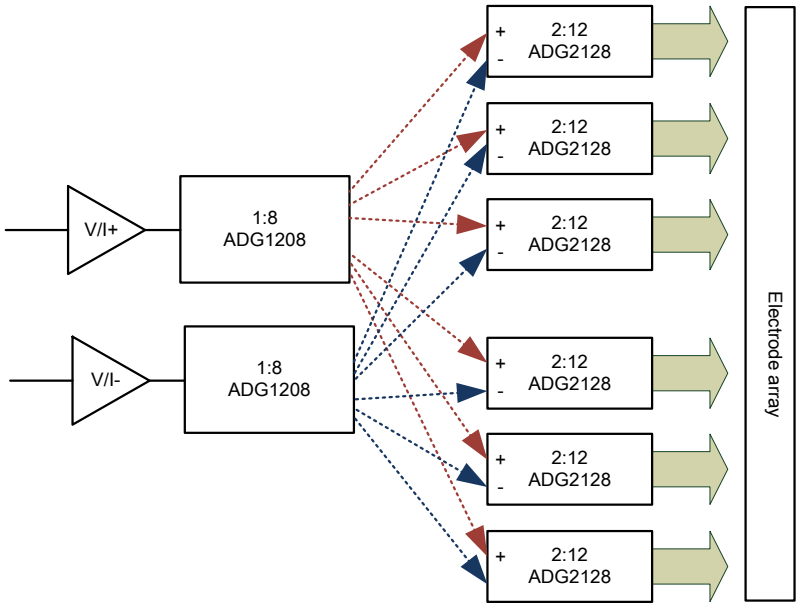

Figure 3.6 The circuit diagram of switching circuit

The switching circuit is composed of two stages. The first stage consists of two bi-direction8:1 multiplexer devices (ADG1208, Analog Devices, USA) which are monolithic analog multiplexers comprising eight single channels. The ADG1208 selects one of eight inputs to one output as configured by the 3-bit binary address lines. An enable input on both devices is used to enable or disable the device. When ADG1208 is inactivated, all channels are switched off. When the ADG1208 is on, each channel behaviour performsequally well in both directions.

The second stage is composed of six analog crosspoint switchers (ADG2128, Analog Devices, USA). The switch array is arranged so that there are six columns by 12 rows, for a total of 72 switch channels. The array is bidirectional, and the rows and columns can be configured as either inputs or outputs. Each of the 72 switches can be addressed and configured through the I2C-compatible interface. ADG2128 supports any simultaneous switch combination by digital programming. The ultralow capacitance and low charge injection of these multiplexers make

them ideal solutions for our applications, where low glitch and fast settling are required. The diagram of ADG1208 and ADG2128 is shown in Figure 3.7.

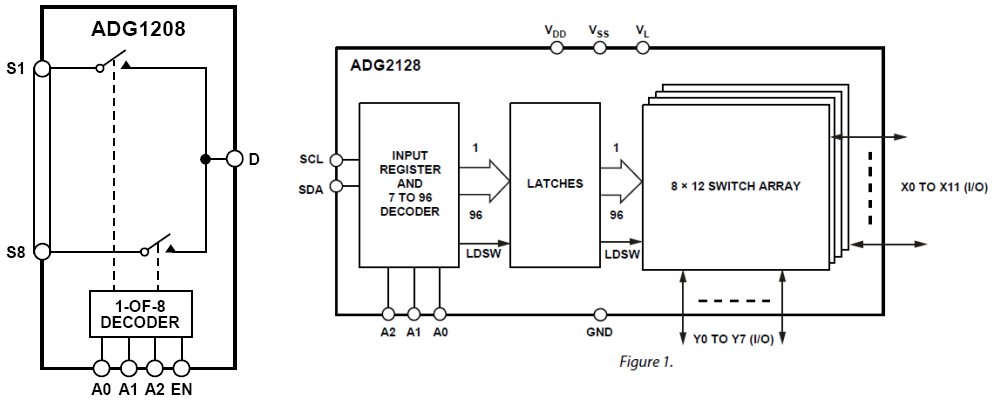

Figure 3.7 The structure of ADG1208 and ADG2128

In cellular impedance measurements, when large electric current applies to cells, thermal energy may be generated at the electrode site causing undesired heating of cells. In order to ensure cells survive during the measurements, the stimulated current needs to be limited to the 100 nA level (Zhang *et al.*, 2011). The traditional method of current limiting is connecting a large resistor in series with the cell-electrodes configurations. Although it is easy to implement and cost-efficient, the series resistor and the parasitic capacitor in circuits will be a low-pass filter which limits the system bandwidth.

In order to solve this problem, a digital dynamic current adjusting method is designed. With the current monitor function, it can limit the stimulated current to a safe level for maintaining cell viability without losing bandwidth performance. The current limiting circuit consists of a small sensing resistor (R), an instrument amplifier circuit (INA), an analog comparator (CMP) and a voltage reference (REF). A schematic diagram of circuits is shown in Figure 3.8.

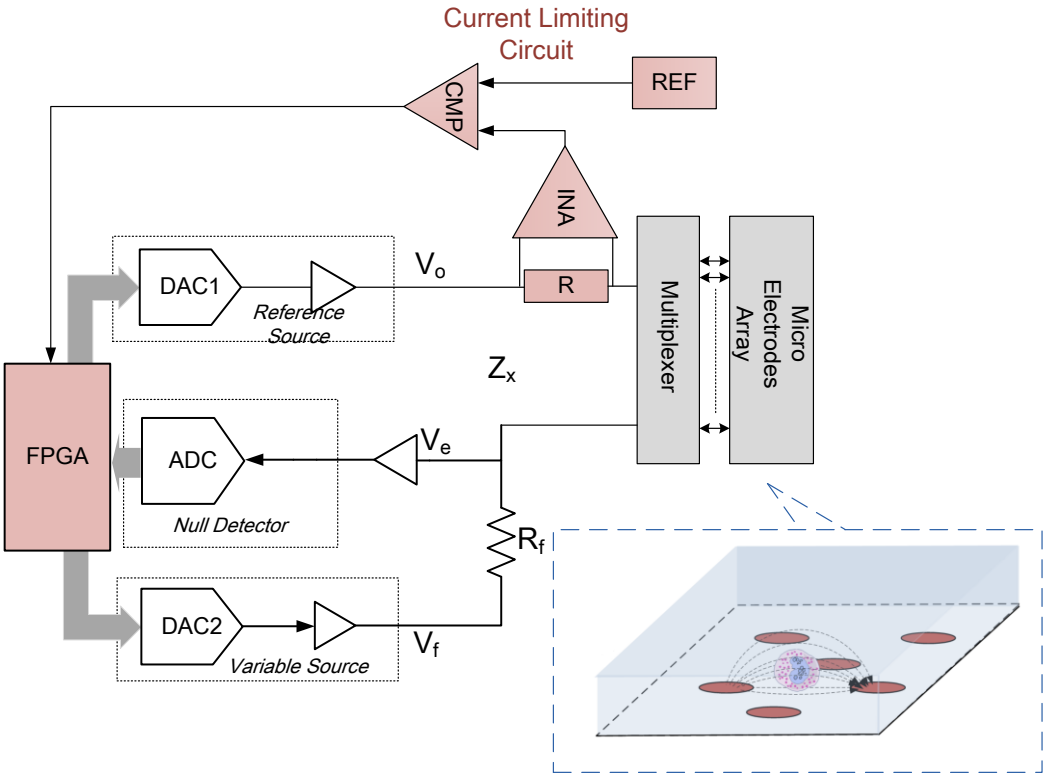

Figure 3.8 The diagram of current limiting circuit

The proposed approach is a convenient, high-speed, cost-efficient way to reduce the over current to a safe range. The brief principle of this monitor is shown in Figure 3.9. The instrument amplifier firstly measures the differential voltage across the current sensing resistor, then this voltage will be compared to a user-defined threshold voltage which is set by a voltage reference. The compared results will be sent to FPGA to measure the length of pulses. Therefore the FPGA can adjust the excitation voltage amplitude according to the pulse length from output of the comparator. Thus the amplitude of stimulated signals can be dynamically adjusted via DAC in real-time.

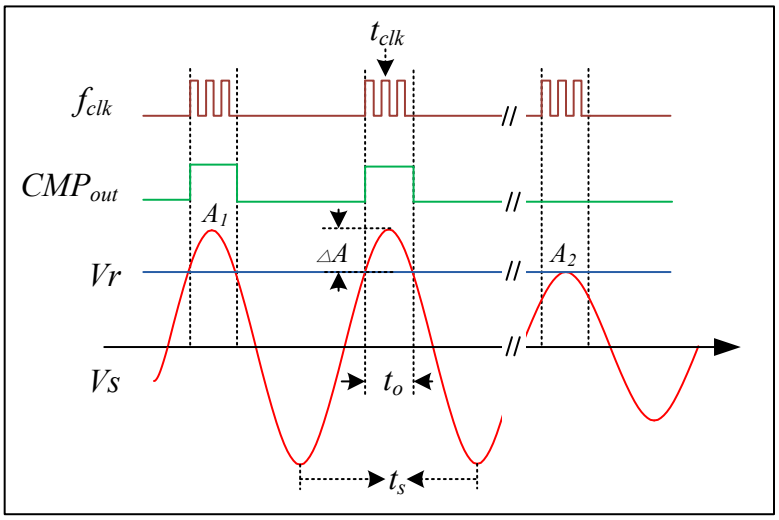

Figure 3.9 Principle of digital dynamically current adjusting

As Figure 3.9 shows, a high-speed comparator compares the output voltage amplitude between the instrument amplifier (V_s) and the voltage reference (V_r). When V_s is higher than V_r, which refers that the injecting current is over the safety limit, the comparator will output logic signal '1' to the FPGA. When V_s fall below V_r, the output of comparator will turn to logic '0'. Consequently, the pulse length of logic '1' approximately equals to the time of the over-current state (t_o). This pulse length can be counted by internal clock in FPGA. Assuming the clock frequency of the FPGA is f_{clk}, the length of t_o can be calculated by (3.3):

$$t_o \approx n \cdot \frac{1}{f_{clk}} = n \cdot t_{clk} \tag{3.3}$$

In (3.3),the variable n is count number of an accumulate counter in the FPGA and t_{clk} is the period of FPGA's counting clock. Therefore, the amplitude of original over-current voltage (A_1) can be calculated from (3.4):

$$A_1 = \frac{V_s}{\sin(2\pi f_s t)} = \frac{V_r}{\sin(2\pi f_s(\frac{t_s}{4} - \frac{t_o}{2}))} = \frac{V_r}{\cos(\pi f_s t_o)} \tag{3.4}$$

Once the adjusting gain value is calculated, the FPGA sends the control words to the auxiliary DAC to change the gain of the output signal, and the injecting

current will be reduced along with the output voltage. Compared to the traditional ADC-based current limitation method, this method only needs an analog comparator to monitor the amplitude of high speed signal. The FPGA can limit the amplitude of the current rapidly (<10ns).

A 4-OpAmp architecture is applied to realize a high-speed, high-accuracy variable gain instrument amplifier for tiny current sensing in the circuit. This architecture provides matched, high impedance inputs so that the circuits will have a minimal effect on the current path. As

Figure 3.10 shows, two high input impedance operational amplifiers A1 and A2 constitute the input stage. A fully-differential programmable gain amplifier (PGA) is the gain stage, which provides a wide gain adjusting range for adopting different current levels. The output stage consists of a differential amplifier with high common rejection ratio (CMRR). If the value of R5 = R6, R1 = R3, and R2 = R4, G_{A3} is the gain of the PGA, the total output voltage V_{out} can be calculated by (3.5):

$$V_{out} = (V_{in2} - V_{in1})(1 + 2\frac{R_5}{R_G})G_{A3}(\frac{R_2}{R_1}) \tag{3.5}$$

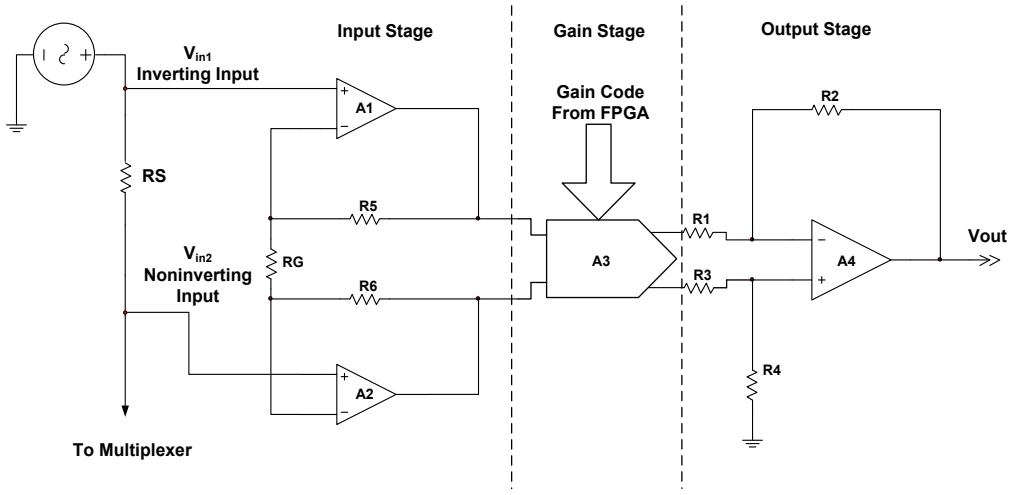

Figure 3.10 Structure of current sensing circuit

A digital programmable gain amplifier AD8369 is used as the gain stage in this circuit. The AD8369 is a high performance PGA, which provides a digitally adjusted variable gain from -5 dB to +40 dB in 3 dB Steps. It has excellent distortion performance: the two-tone, third-order inter-modulation distortion is -69 dBc at 70 MHz. Digital control of the AD8369 is realized via a serial interface and driven by the FPGA with standard CMOS logic level.

In order to compare the signal in real-time, a high-speed comparator is required. In our application, the desired frequency of the excitation signal is 10 kHz to 5 MHz. AD8611 (Analog Devices, USA) is selected to meet this bandwidth requirement. It is a high-speed comparator with latch function and complementary output. With closely matched, fast 4 ns propagation delays for rising and falling signals, it is a good choice for our application.

3.5 SENSING CIRCUIT

The sensing circuit consists of three major parts: buffering amplifiers, switching circuits and eight differential amplifiers. Buffering amplifiers are directly connected to the electrodes of MEA. They provide the electrical impedance transformation from electrodes to the subsequent switching circuit. The switching circuit is composed of three crosspoint switchs, which provide the electrode switching function which allows users to select any 16 electrodes (or 8 pairs) in the overall electrode array. The differential amplifiers are used to convert the differential voltage between the electrode pair to a single-end ground-referenced signal. The outputs of differential amplifiers are digitized by ADCs of the multi-function card. The diagram of sensing circuit is demonstrated in Figure 3.11.

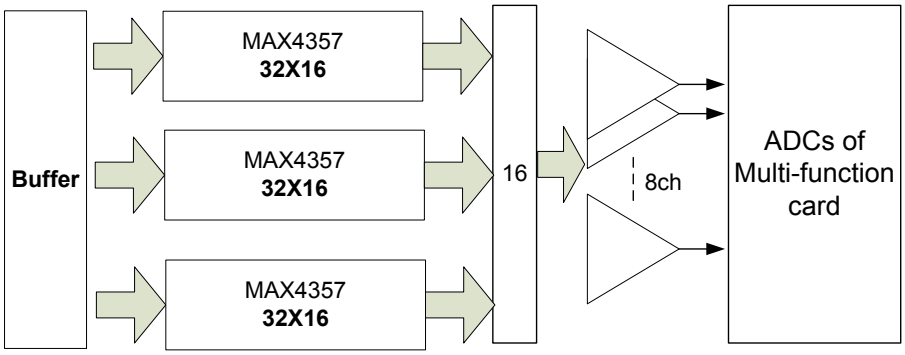

Figure 3.11 The structure of sensing circuit

In order to reduce the influence to stimulation circuit, the sensing circuit requires high input impedance amplifiers as signal buffers. We selected a low-noise, high speed, junction gate field-effect transistor (JFET) amplifier OPA653 (Texas Instrument, US) for the buffering circuit. The OPA653 combines a very wideband voltage-feedback operational amplifier with a JFET-input stage with internal gain setting resistors to achieve an ultra-high input impedance, wide dynamic range amplifier for fixed gain applications. With 500-MHz bandwidth (gain of 2) and excellent THD distortion performance (72-dBc at 10 MHz), the OPA653 provides excellent performance for our application. The diagram of the buffering circuit is presented in Figure 3.12.

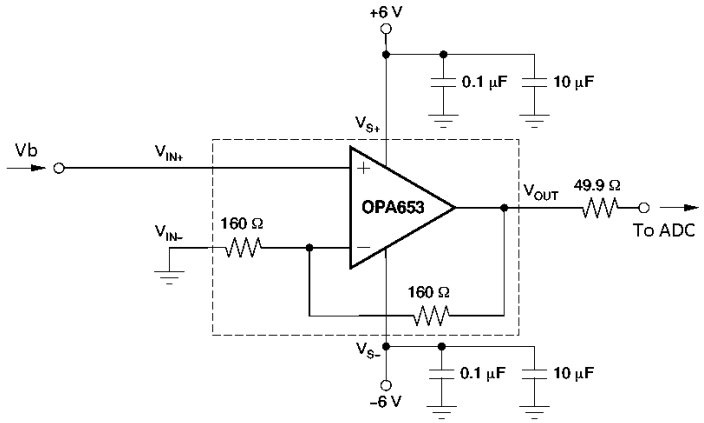

Figure 3.12 The circuit of buffering amplifier

In order to reduce the spatial occupation of the switching circuit, highly integrated crosspoint switchs (MAX4357, Maxim. USA) are applied to switch the

sensed voltages from the electrodes to the ADC circuits. The MAX4357 is a 32×16 highly integrated crosspoint switch matrix with input and output buffers, operates from dual±5V supply. It provides broad bandwidth for small signals (0.1dB Gain Flatness to 12MHz). The switch matrix configuration and output buffer gain are programmed through an 3-wire serial interface, which is controlled by the FPGA of the multi-function card. When MAX4357 powers-up, all outputs are initialized in the disabled state to avoid output conflicts in chip configurations. Excellent flexibility, high integration, and space-saving packaging make this non blocking switch matrix ideal for high density data acquisition systems.

The outputs of MAX4357 are fed to eight differential amplifiers for converting the differential voltage signals to a single-end signals. The amplifiers applied here are AD8099 (Analog Devices, US), which is an ultra low noise (0.95 NV/√Hz), high slew rate (1350 V/μs) and ultra low distortion (–92 dBc @10 MHz) voltage feedback op amp. It features a new, highly lineagr, low noise input stage that increases the bandwidth at low gains with high slew rates. It also has an external compensation allowing gains from +2 to +10, which allows the user to set the gain bandwidth product with a minimum tradeoff in bandwidth. The AD8099 settles to 0.1% in 18 ns and recovers from overdrive in 50 ns. With a wide supply voltage range (5 V to 12 V), low offset voltage (0.1 mV typical), wide bandwidth (700 MHz for G = +2), and a gain-bandwidth product up to 3.8 GHz, the AD8099 is an ideal solution for our switch circuits. The realized circuit board of switching circuit is shown in Figure 3.13.

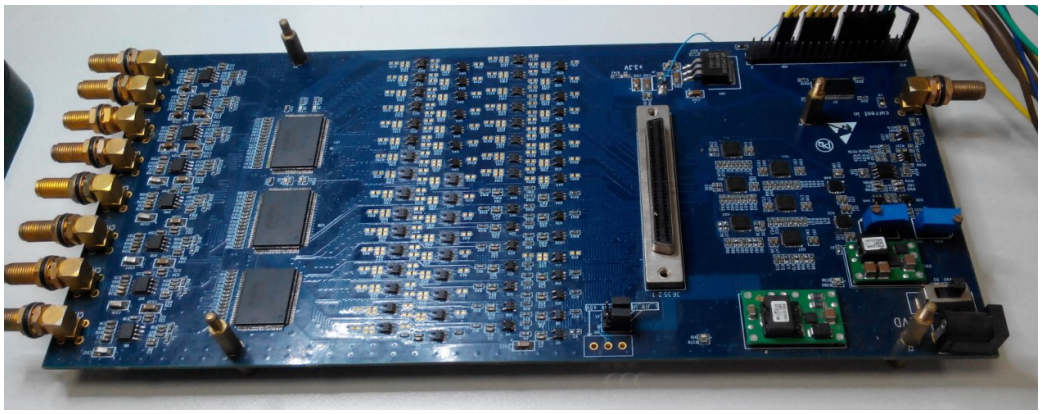

Figure 3.13 Photo of fabricated switching board

3.6 MULTI-FUNCTION CARD

The multi-function card is a highly integrated instrument for data acquisition, waveform generation and system control in our application. There are three major functions supported by this card, which can be controlled by a host computer via the PXI Express (PXI-E) interface. The card mainly consists of multi-channel ADCs. DACs, digital I/O buffers, clock generator, and FPGAs. The hardware architecture of the card is shown in Figure 3.14.

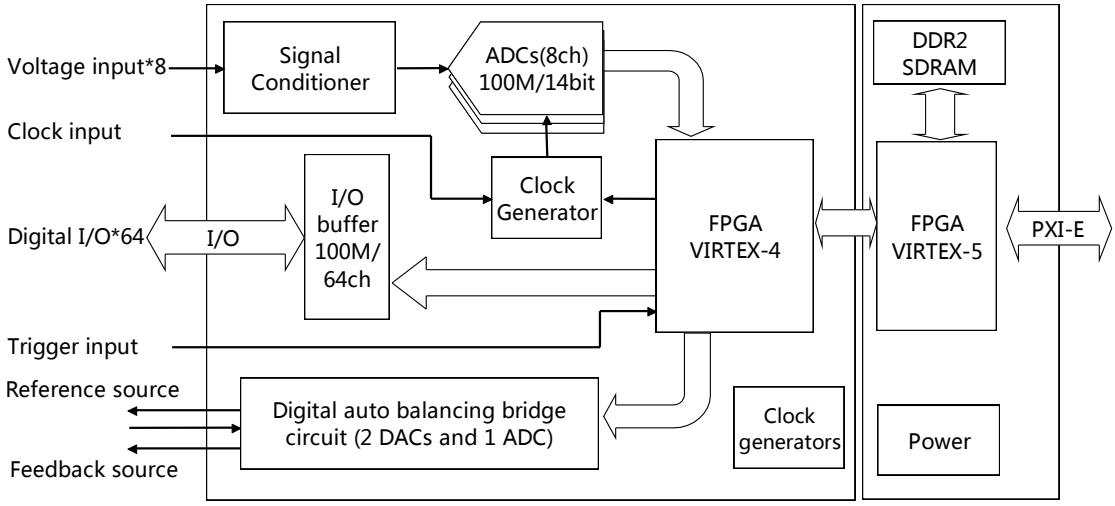

Figure 3.14 The architecture of the multi-function card

3.6.1 ANALOG-TO-DIGITAL CONVERTER

There are nine ADC channels provided by the multi-function card. Eight channels are used to digitize the sensed voltage on the electrodes, and one channel is used to realize the digital auto balance function as a null detector. Two high-performance 14-bit 105 MSPS Quad channel A-D converters (ADS6444, Texas Instruments, US) are utilized to build the eight-channel data acquisition circuit. They feature serial Low-voltage differential signaling(LVDS) data outputs in a 64-pin Quad Flat No-leads package(QFN) package. The ADS6444 has 3.5dB coarse gain options that can be used to improve SFDR performance. In addition, fine gain options also featured, which is programmable in 1dB steps up to 6dB. It also includes an internal phase lock loop to derive the bit clock from the incoming ADC sampling clock. The serial data streams are transmitted in LVDS signal. The diagram of ADS6444 is shown in Figure 3.15.

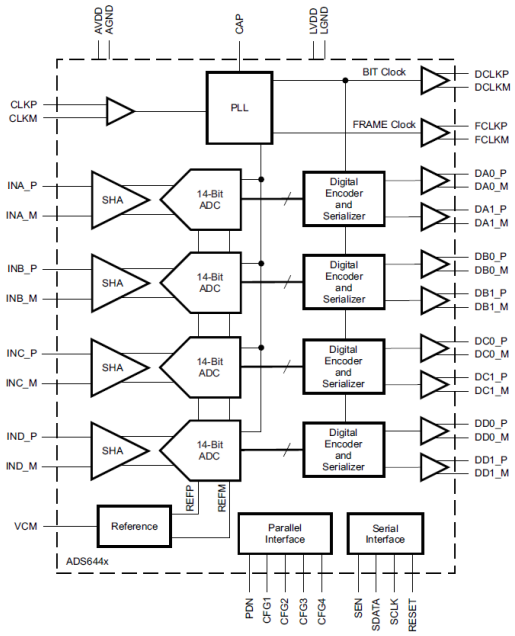

Figure 3.15 Structure of ADS6444

Another single channel ADC is designed for implementing the null detector in DABB circuit. The null detector is composed of a field effect transistor (FET) amplifier, a high gain amplifier, a differential amplifier and a high-speed ADC as Figure 3.16 depicts. In order to minimize the contact impedance effect, the

front-end amplifier should have high input impedance. The FET amplifier OPA657 is applied here, which combines a very wideband voltage-feedback operational amplifier with a JFET-input stage to achieve high dynamic range amplification. The input impedance of OPA657 can achieve 10^{12} Ohm. After the FET stage, we utilized a low noise (0.95 nV/√Hz), wideband amplifier AD8099 to provide a high gain, which can be adjusted up to 100 V/V. The differential amplifier is used to convert the single-end signal to the differential signal to match with the ADC's input stage. A 16-bit, 105 MSPS ADC (ADS5482) is employed to acquire the wide dynamic range signals.

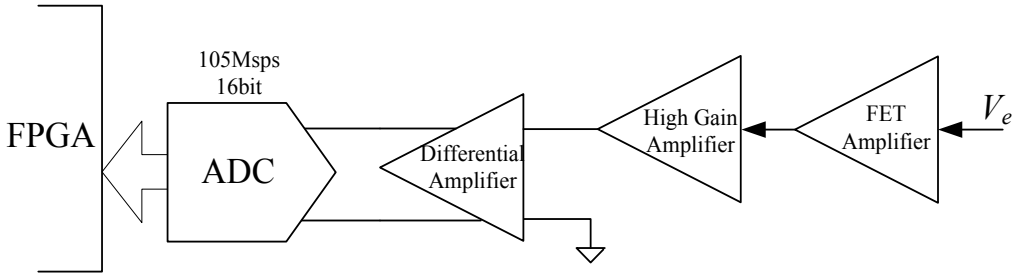

Figure 3.16 The structure of the null detector circuit

3.6.2 DIGITAL-TO-ANALOG CONVERTERS

DAC-based circuits are used for generating the reference signal and variable signal for realizing the DABB algorithm. In order to generate a variable voltage signal with high accuracy, two high speed (up to 400 MSPS) 16-bit DACs (AD9726, Analog Devices , USA) are applied in our system as a reference source and feedback source generator in DABB architecture. The AD9726 achieves an excellent dynamic performance (SFDR≥-78 dBc at fout=20 MHz). They are connected to FPGA with high speed Low-voltage differential signalling (LVDS) bus. The current output of AD9726 will be transferred to a voltage signal by a differential operational amplifier.

A low noise, low distortion, high speed amplifier ADA4930-1 utilized in the reference source circuitry as signal conditioning component. The ADA4930-1 are fabricated using silicon-germanium (SiGe) complementary bipolar process, enabling it to achieve very low levels of distortion with an input voltage noise of only 1.2 nV/ √ Hz. The output frequency of the reference source can be tuned by the direct digital synthesis (DDS) technique in the FPGA. The circuit diagram of the reference source is shown in Figure 3.17.

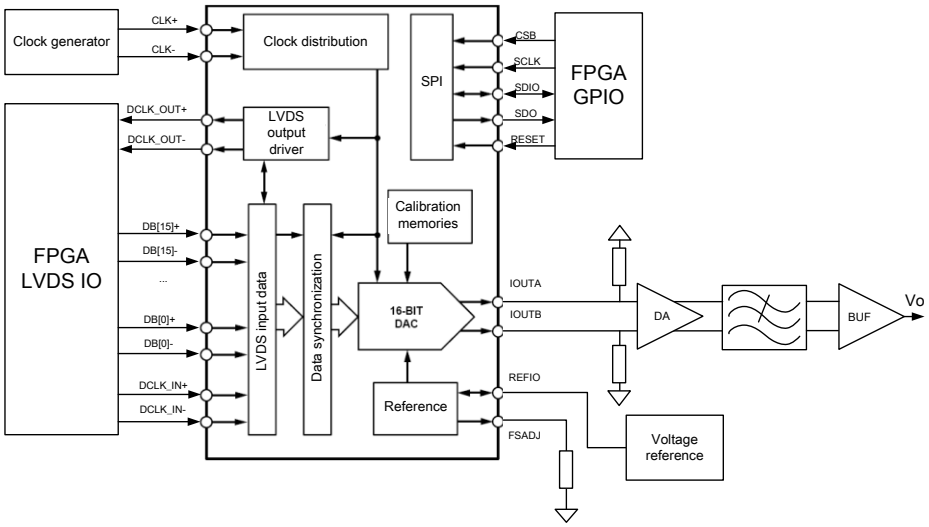

Figure 3.17 The structure of the reference source.

In typical DDS applications, a low-pass filter is utilized to suppress the effects of the image responses in the output spectrum. In order to keep the cutoff requirements on the low-pass filter reasonable, it is an accepted rule to limit the f_{OUT} bandwidth to approximately 40% of the f_{CLOCK} frequency. In our application, a passive 6th order elliptical filter is designed, which offers the steepest pass band to stop band transition among other filter types. The passband of the elliptical filter is 10 MHz and the stop band is 15 MHz with 60 dB attenuation. The circuit of this filter is shown in Figure 3.18.

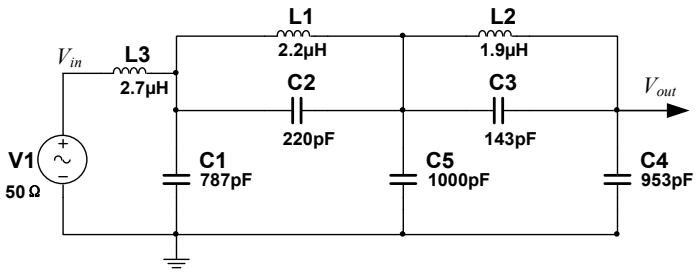

Figure 3.18 Structure of 6th order elliptical filter

In the architecture of digital auto balancing bridge, the feedback source is dynamically adjusted according to the imbalance voltage. In order to improve flexibility and accuracy of output adjusting, the DAC are combined with a high speed programmable gain amplifier (PGA) as a variable source, hence they can be adjusted by the FPGA in real-time. The circuit of the feedback source also includes a reconstruction filter and an output buffer amplifier. The DAC applied in the variable source is the same as that of the reference source. A digital-programmable gain amplifier AD8369 is used in this circuit. It is a high performance PGA which provides a digitally controlled variable gain from -5 dB to +40 dB in 3 dB steps. The digital control of AD8369 is achieved by using a serial interface and is driven with standard CMOS logic levels by the FPGA. A similar passive 6th order elliptical filter is utilized to suppress the DDS image harmonics. The schematic diagram of feedback source is shown in Figure 3.19.

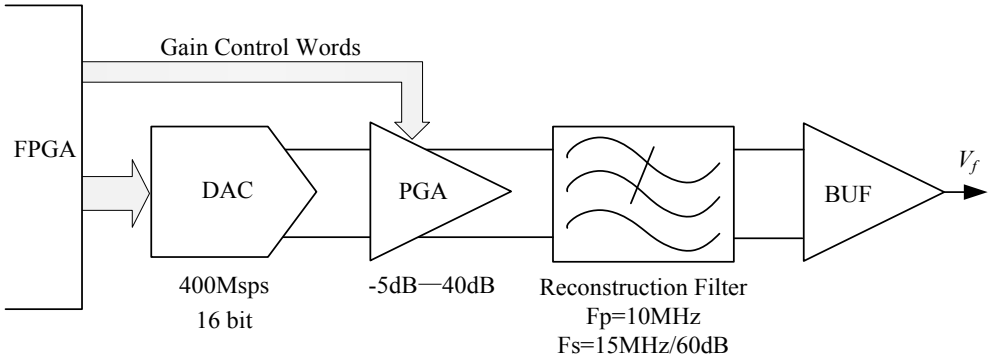

Figure 3.19 The structure of feedback source circuit

3.6.3 FIELD PROGRAMMABLE GATE ARRAYS

The FPGA provides an effective combination of high-speed peripheral control with the digital signal processing through parallel and pipelined architectrue. There are two different FPGAs implemented on the card. The first one (XC4VSX35, Xilinx, USA) is utilized to deal with the peripherals and signal processing. It features 34,560 logic cells and 3456 Kb Block RAMs for logic design and provides over 600 configurable I/Os with high speed SelectIO technology for peripheral connectivity. The obvious advantage of this type is that there are 192 XtremeDSP Slices which contain dedicated 18×18-bit two's complement signed multipliers, adder logics, and a 48-bit accumulators. These blocks are designed to implement high efficiency and high-speed DSP applications.

The second FPGA (XC5VLX50T, Xilinx, USA) is used to build the PXI-E communication between our system and the host computer. The Virtex-5 family FPGA provides advanced, high-performance logic fabric, and PCI express hard-IP system level blocks. It includes 36 Kbit block RAM/FIFOs, 25 x 18 DSP slices, ChipSync source-synchronous interface blocks, SelectIO technology with built-in digitally controlled impedance, improved clock management tiles with integrated Digital Clock Managers (DCM), phase-locked-loop (PLL) clock generators and system monitor functionality.

In order to realize high speed PXI-E communication in FPGA, a double data rate synchronous dynamic random access memory (DDR2 SDRAM) is used for data buffering. By transferring data on the rising and falling edges of the bus clock signal, DDR2 provides higher bus speed. Oppositely, the power requirement is reduced by running the internal clock at one quarter the speed of the data bus. Micron's 2GB DDR3-SDRAM MT16HTF25664HZ was applied in the system. Because the data can be transferred in 64 bits, DDR2 SDRAM gives a transfer rate up to 6.4GB/s. It is controlled by Xilinx's Memory Interface Generator IP core in FPGA.

3.7 CONCLUSION

In this chapter, the design of system hardware is presented in detail. The system consists of five main parts: a microelectrode array, a stimulation circuit, a sensing circuit, a multi-function card and a PXI-E based computer. The MEA includes 72 small-sized gold electrodes allocated in two sub-array (each array contains 36 electrodes). The stimulation circuits are used for generating a wideband signal to excite the cells under test. The circuit is based on digital auto balancing bridge (DABB) method which improved from the traditional analog balancing bridge method. It features high-speed, compact and low-cost compared to the traditional measurement approaches. The sensing circuit consists of three major parts: buffering amplifiers, switching circuits and differential amplifiers. It allows us to simultaneously measure signals on any 16 electrodes (or 8 pairs) in the array. The multi-function card is a highly integrated instrument for data acquisition, waveform generation and system control functions in our application. It's composed of ADCs. DACs, digital I/O buffers, clock generator, FPGAs and so on.

Chapter 4. A FAST BIOIMPEDANCE MEASUREMENT METHOD BASED ON DIGITAL AUTO BALANCING BRIDGE TECHNIQUE

In this chapter, a novel bioimpedance measurement method is proposed and realized. The new method is theoretically based on the auto balancing bridge method which was introduced in chapter 2, and developed from the traditional analogue auto balancing bridge circuitry. By using the digitally bridge balancing algorithm and multi-frequency excitation signal, the method has a significant improvement in measurement speed. Two different algorithms of digital auto balancing bridge (DABB) are proposed for single and multi-frequency situations.

4.1 THE INTRODUCTION OF LMS ALGORITHM

In the middle of last century, the research of adaptive signal processing technology has been promoted by the practical requirement in research of optimal electrical system. An adaptive filter is a computational device that attempts to model the relationship between two signals iteratively in real time. By employing a particular adaptive filter structure, the type and number of parameters can be adjusted. The adaptive algorithm applied to update the parameter values of the system can present various forms (Douglas, 1999).

Figure 4.1 shows a principle diagram of an adaptive filter. A input signal *x(k)* enters a component, named an adaptive filter which calculates an output signal *y(k)* at time *k*. The structure of the adaptive filter comprises adjustable parameters whose values affect how *y(k)* is calculated. The output is compared to a desired

signal *d(k)*, by subtracting them at time *k*. This difference signal *e(k)* called the error signal which is fed into a process which adjusts the parameters of the filter from time *k* to time *(k+1)* with a specific regulation. As the time increased, the output of the adaptive filter becomes closer to the desired signal through this adaptation process, such that the magnitude of *e(k)* decreases over time (Douglas, 1999).

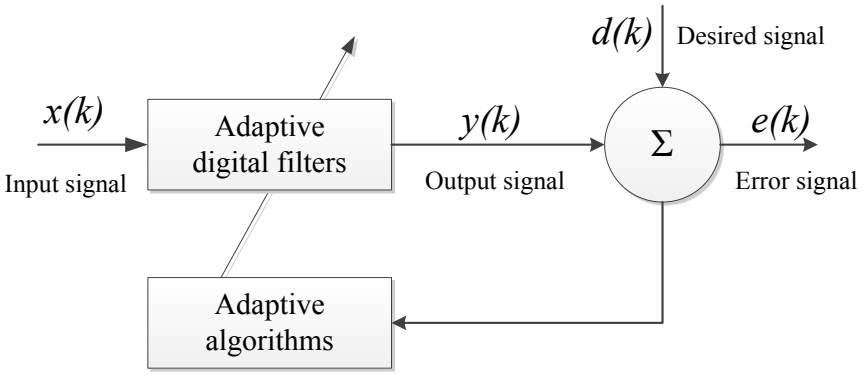

Figure 4.1 The principle diagram of adaptive filter

The filter component in an adaptive filter can utilize infinite impulse response (IIR) filter, finite impulse response (FIR) filter or nonlinear filter. In practical engineering application, FIR filter is the most common choice due to its stability and convenience in hardware implementation (Lim and Parker, 1983; Sankarayya *et al.*, 1997; Douglas *et al.*, 1998). The common form of an adaptive FIR filtering algorithm is:

$$W(n+1) = W(n) + \mu(n)G(e(n), X(n), \phi(n)) \tag{4.1}$$

where $W(\,)$ is the the filter coefficients vector, $G(\,)$ is a specific vector-valued nonlinear function, $\mu(n)$ is a step size parameter, $e(n)$ is the error signal, $X(n)$ is the vector of input signal, and $\phi(n)$ is the vector of relevant information about the input and error signals and/or the coefficients at prior times. Normally, in the simplest algorithms, $\phi(n)$ is not used, the only parameters needed to adjust the coefficients at time n are the error signal, input signal vector and step size (Douglas, 1999). The step size denotes the magnitude of the change

which is decided by the algorithm iteratively. Typically, a successful adaptive filtering application depends on how the value of $\mu(n)$ is selected or computed to get the best performance.

The Least Mean Squares (LMS) algorithm was invented by professor Bernard Widrow and his student Ted Hoff, in 1960 (Haykin and Widrow). It is a series of adaptive filters utilized to mimic a desired filter by searching the filter coefficients that relate to producing the least mean squares of the error signal. The LMS filter is a stochastic gradient descent method, which can only be adapted based on the error at the current time(Mathews and Douglas, 2003).

In order to find the optimal filter weights, the LMS filter updates the weights to converge to the best values. The algorithm firstly assumes a small weight (zero in most cases), and searchs the gradient of the mean square error at each step, thus the weights are updated. If the MSE-gradient is positive, the error would keep increasing positively, which means the user needs to reduce the weights. In the same way, if the gradient is negative, the user needs to increase the weights. The LMS algorithm approaches to the optimal weights by ascending/descending down the mean-square-error versus filter weight curve. The updating equation of LMS algorithm is:

$$W(k+1) = W(k) + 2\mu e(k)x(k) \tag{4.2}$$

where the convergence factor μ should be chosen from a range to guarantee convergence. Figure 4.2 depicts the realization of the LMS algorithm for a delay line input *x(k)*. Normally, one iteration of *N* stage LMS filter requires *N+2* multiplications for updating filter coefficient and *N+1* multiplications for generating the error (Diniz, 2002).

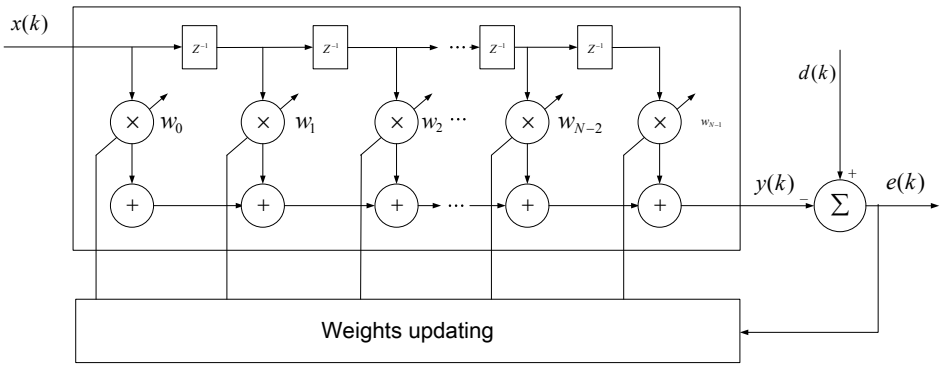

Figure 4.2 The architecture of LMS algorithms

According to the updating equation, the process of LMS algorithm can be summarized as Table 4.1.

Table 4.1 The procedure of LMS algorithm

Initial condition	$w(0) = 0$ or defined by initial values
Iterative calculation	Update k=k+1 (1) Input $x(k)$, $d(k)$ (2) Filter $y(k) = w^T x(k)$ (3) Error estimate $e(k) = d(k) - w^T x(k)$ (4) Update weights $w(k+1) = w(k) + 2\mu e(k)x(k)$

Compared to other adaptive algorithms such as recursive least squares (RLS), the LMS algorithms does not include any matrix calculations. Therefore, the LMS algorithm demands less computational resources and memory than other algorithms. Also, the realization of the LMS algorithm is less complicated than others (Bershad and Macchi, 1989; Eweda, 1994).

4.2 DESIGN OF LMS-BASED BRIDGE BALANCING ALGORITHM

The LMS-based bridge balancing algorithm was first proposed to control the balance of the AC bridge (Dutta *et al.*, 1987). It is widely used in digital adaptive filtering (Feintuch, 1976). It is based on the estimation of the gradient toward the optimal solution using the statistical properties of the input signal (Widrow and Stearns, 1985). LMS-based balancing method has been proved to have many advantages, including faster convergence, feasibility of tracking time-varying impedances and relative immunity to external interferences (Dutta *et al.*, 2001).

The principle of LMS-based digital auto balancing algorithm can be briefly described as follows. With a given input signal vector *x(n)* and a desired response vector *d(n)*, an appropriate filter weight vector *w(n)* can be found by minimizing the mean square of the difference between the output vector *y(n)* and *d(n)*. The formulas of the algorithm are listed below:

The filter output: $y(n) = w^H(n)x(n)$ (4.3)

The estimated error: $e(n) = d(n) - y(n)$ (4.4)

Update the weight vector: $w(n+1) = w(n) + 2\mu x(n)e^*(n)$ (4.5)

where *y(n)* is the filter output, *d(n)* is the desire output, *e(n)* is the filter error (the difference between the desired output and current output) used to update the weights, μ is the step size, and *w(n+1)* is the new weight vector meant to be used for the next iteration.

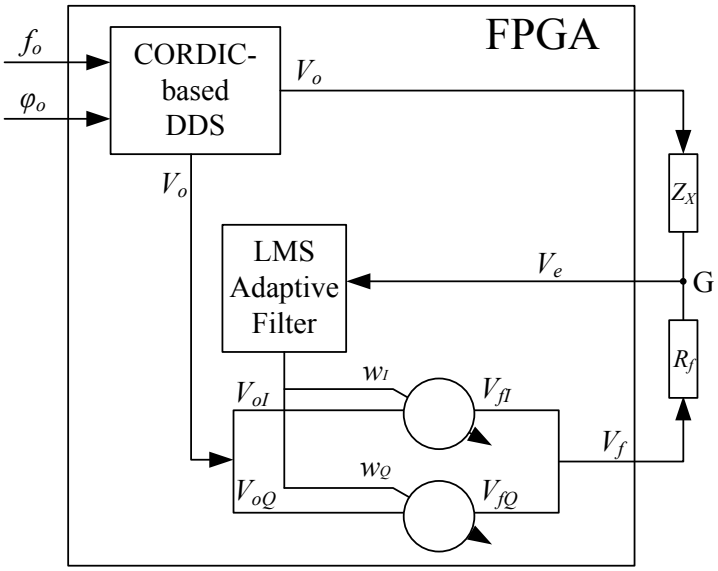

Figure 4.3 Principle diagram of LMS-based auto balancing algorithm.

As Figure 4.3 shows, the variable source V_f is the output of the LMS adaptive filter. The filter tends to minimize the mean square error of the imbalance voltage V_e (which depends on the V_f) by recursively altering the weights w_I and w_Q. The desired response vector V_f can be given in terms of in-phase and quadrature components as follows:

$$V_f = w_I A\sin(\omega_0 t) + w_Q A\cos(\omega_0 t) \tag{4.6}$$

To balance the bridge, the weights of the in-phase and quadrature components (w_I and w_Q) were iteratively updated in FPGA to minimize the instantaneous error voltage. The instantaneous error signal of the unbalanced bridge $e(k)$ can be described as:

$$e(k) = |\beta_1| A(w_I \sin(\omega_0 t) + w_Q \cos(\omega_0 t)) - |\beta_2| A\sin(\omega_0 t) \tag{4.7}$$

$$\beta_1 = |\beta_1| \angle\theta_1 = \frac{Z_r}{Z_x + R_f} \tag{4.8}$$

$$\beta_2 = |\beta_2| \angle\theta_2 = \frac{Z_x}{Z_x + R_f} \tag{4.9}$$

In (4.8), θ_1 denotes the phase shift between the variable source signal V_f and the error signal V_e, whilst θ_2 denotes the phase shift between the reference voltage source V_o and the error signal V_e. According to the principle of LMS algorithm, the new weights can be calculated by (4.10):

$$w(n+1) = w(n) - \mu\nabla_w |e(n)|^2 \tag{4.10}$$

Similarly, the weights w_I and w_Q can be adjusted by the steepest descent direction to minimize the mean square. Hence, at the k-th sampling time, the w_I and w_Q can be expressed as:

$$w_I(k+1) = w_I(k) - \mu \left.\frac{\partial e^2(t)}{\partial w_1}\right|_{t=k} \tag{4.11}$$

$$w_Q(k+1) = w_Q(k) - \mu \left.\frac{\partial e^2(t)}{\partial w_2}\right|_{t=k} \tag{4.12}$$

From (4.7), the weights update can be given by the following equations,

$$w_I(k+1) = w_I(k) + 2\mu e(k) A\sin(\omega_0 k) \tag{4.13}$$

$$w_Q(k+1) = w_Q(k) + 2\mu e(k) A\cos(\omega_0 k) \tag{4.14}$$

The auto balance algorithm continuously update weights until the bridge be balanced. Then the impedance calculation will be performed in FPGA. The step size μ is a convergence factor which defines how large or small is the signal passing through the filter; its value is very important for the convergence speed and the

LMS algorithm stability. To keep the system stable, the step size should be determined within the range of:

$$0 < \mu < \frac{1}{\lambda_{\max}} \tag{4.15}$$

where $\lambda_{\max}$ is the greatest eigenvalue of the autocorrelation matrix *R*, which can be expressed as:

$$R = E\{x(n)x(n)\} \tag{4.16}$$

where $E\{\ \}$ denotes the expected value, *x(n)* is input signal vector(Douglas, 1999). If this condition is not fulfilled, the algorithm becomes unstable and *w(n)* diverges. The maximum convergence speed is achieved when:

$$\mu = \frac{1}{\lambda_{\max} + \lambda_{\min}} \tag{4.17}$$

where $\lambda_{\min}$ is the smallest eigenvalue of *R*. Given that μ is less than or equal to this optimum, the convergence speed is determined by $\lambda_{\min}$, with a larger value yielding faster convergence. It means that the faster convergence rate can be achieved when $\lambda_{\max}$ is close to $\lambda_{\min}$, that is, the maximum achievable convergence speed depends on the eigenvalue spread of *R*.

4.3 THE CORDIC-BASED DIGITAL WAVEFORM SYNTHESIZER

In the digital auto balancing bridge, the reference signal and variable signal are generated by CORDIC-based digital waveform synthesizer (DDS) module. Coordinate Rotation Digital Computer (CORDIC) is an easy and efficient way for

calculating trigonometric and hyperbolic functions. It is built on the theory of complex phasor rotation. It offers an iterative method of carrying out vector rotations by arbitrary angles with only shift and add operations. By vector rotations, all the trigonometric functions can be derived from this method (Andraka, 1998).

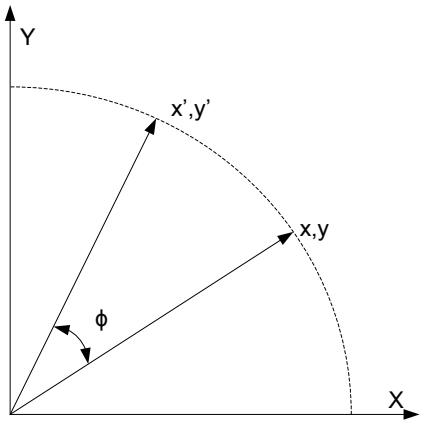

Figure 4.4 The principle diagram of CORDIC algorithm

As Figure 4.4 shows, the CORDIC algorithm is derived using the general rotation transform in the Cartesian plane, where (*X',Y'*) are the coordinates of the resulting vector after rotating a vector with coordinates (*X,Y*) through an angle of θ. Equations below can be derived:

$$x' = x\cos\theta - y\sin\theta \tag{4.18}$$

$$y' = y\cos\theta + x\sin\theta \tag{4.19}$$

The θ angle rotation is performed via several steps. Each step performs a small rotation. Therefore, several steps will make up one planar rotation. A single step is defined by the following equations:

$$X_{n+1} = X_n\cos\theta_n - Y_n\sin\theta_n \tag{4.20}$$

$$Y_{n+1} = Y_n\cos\theta_n + X_n\sin\theta_n \tag{4.21}$$

We can see (4.20) and (4.21) require 4 multipliers. By eliminating the factor $\cos\theta$ in (4.18) and (4.19), the simplified (4.22) and (4.23) are derived:

$$X_{n+1} = \cos\theta_n (X_n - Y_n \tan\theta_n) \tag{4.22}$$

$$Y_{n+1} = \cos\theta_n (Y_n + X_n \tan\theta_n) \tag{4.23}$$

In order to reduce multiplication, the $\tan\theta$ is defined as $\pm 2^{-i}$, where *i* denotes the time of rotations. Hence the tangent multiplication term in (4.20) and (4.21) can be instead by shift operations. The angle of each step is derived from:

$$\theta_n = \arctan(\frac{1}{2^n}) \tag{4.24}$$

Angle of all iterations summed equal to the rotation angle *θ*.

$$\sum_{n=0}^{\infty} S_n \theta_n = \theta, \quad S_n = \{-1; +1\} \tag{4.25}$$

This results in the following equation for $\tan\theta_n$:

$$\tan\theta_n = S_n 2^{-n} \tag{4.26}$$

Thus, the following equations are derived:

$$\begin{cases} X_{n+1} = \cos\theta_n (X_n - Y_n S_n 2^{-n}) \\ Y_{n+1} = \cos\theta_n (Y_n + X_n S_n 2^{-n}) \end{cases} \tag{4.27}$$

Now, besides the $\cos\theta_n$ coefficient, the algorithm has been simplified to operations composed by additions and shifts. The coefficient can be further removed by previously calculating the final result. At first, the coefficient should be rewrited as (4.28).

$$\cos\theta_n = \cos(\arctan(\frac{1}{2^n})) \tag{4.28}$$

The next step is calculating the equation above for all values of *n,* and then multiplying the results, which refers to as *K*.

$$K = \frac{1}{P} = \prod_{n=0}^{\infty} \cos\left(\arctan\left(\frac{1}{2^n}\right)\right) \approx 0.607253 \tag{4.29}$$

where *K* is a constant for all initial vectors, also for all values of the rotation angle. Normally, it is named as congregate constant. Commonly, the derivative *P* (*approx.* 1.64676) is defined for calculations.

Therefore, by these micro rotations, arbitrary angles can be obtained by performing a series of successively smaller elementary rotations. The iterative equation of rotation can now be expressed as:

$$\begin{cases} X_j = K(X_i \cos\theta - Y_i \sin\theta) \\ \\ Y_j = K(Y_i \cos\theta + X_i \sin\theta) \end{cases} \tag{4.30}$$

Because the coefficient *K* has been previously calculated and considered at a later stage, equation (4.27) may be written as:

$$\begin{cases} X_{n+1} = X_n - Y_n S_n 2^{-n} \\ \\ Y_{n+1} = Y_n + X_n S_n 2^{-n} \end{cases} \tag{4.31}$$

Here introduced a new factor *Z*, which represents the rest part of the angle θ that has not been rotated yet.

$$Z_{n+1} = \theta - \sum_{i=0}^{n} \theta_i \tag{4.32}$$

Assuming S_n is computed as a sign of Z_n for every step of the rotation.

$$S_n = \begin{cases} -1, if\ Z_n < 0 \\ \\ +1, if\ Z_n \geq 0 \end{cases} \tag{4.33}$$

Merging equation (4.24) and (4.33) results in a system which decreases *Z* to zero.

Therefore, by using the first CORDIC scheme, sine and cosine functions can be computed:

$$[X_j, Y_j, Z_j] = [P(X_i \cos(Z_i) - Y_i \sin(Z_i)), P(Y_i \cos(Z_i) + X_i \sin(Z_i)), 0] \tag{4.34}$$

By utilizing the following values as inputs

$$\begin{aligned} X_i &= \frac{1}{P} = \frac{1}{1.6467} \approx 0.60725 \\ Y_i &= 0 \\ Z_i &= \theta \end{aligned} \tag{4.35}$$

Therefore the results are calculated:

$$[X_j, Y_j, Z_j] = [\cos\theta, \sin\theta, 0] \tag{4.36}$$

CORDIC algorithm is commonly used when no hardware multiplier is available (e.g., simple microcontrollers and FPGAs) as the only operations it requires are addition, subtraction, bit-shift and look-up table. In our application, in order to reduce the resource consumption, the injecting signals are generated by CORDIC module. Since the CORDIC architecture eliminates the sine/cosine look-up table by real-time waveform computation, it can provide higher phase resolution, thus reducing spurious signals caused by phase quantization.

Figure 4.5 shows the CORDIC-based DDS architecture. The architecture is composed of three parts: the phase increment register, phase accumulator and CORDIC IP core. The phase increment register accumulates the frequency word

$\Delta\varphi$. The accumulated result will sum with the phase offset word φ_0, which is then fed to the CORDIC IP core as phase code. The output of the CORDIC IP core is a binary data stream, which will be sent to DAC to convert to an analog signal.

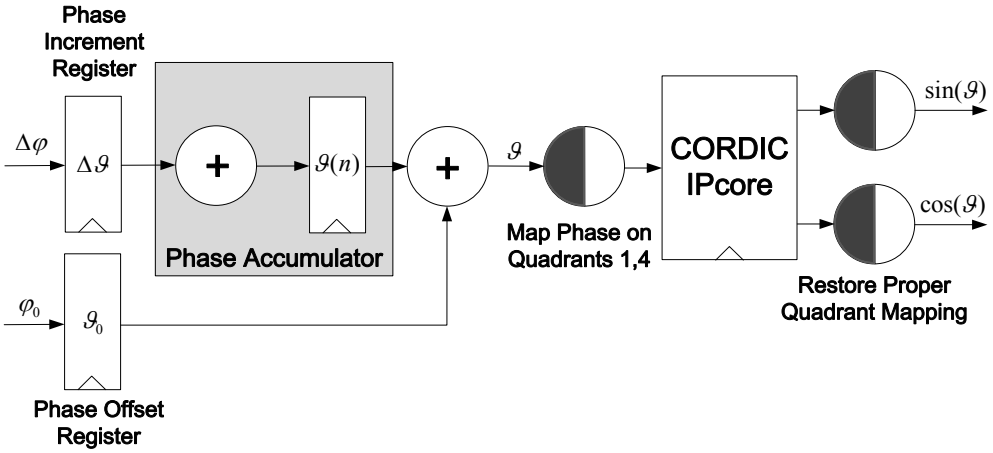

Figure 4.5 Architecture of CORDIC-based DDS.

The CORDIC algorithm in our system is implemented by Xilinx's LogiCORE IP CORDIC 4.0, which supports a fully parallel configuration with single-cycle data throughput at the expense of silicon area. Figure 4.6 shows the architecture of this IP core. The individual input vector elements, (X_in, Y_in), and the output magnitude (X_out) are expressed as fixed-point 2's complement numbers with an integer width of 2 bits. The output phase angle (P_out) is expressed as a fixed-point 2's complement number with an integer width of 3 bits. By advanced XtremeDSP DSP48A slices and parallel architecture, the frequency of the generated signal can be up to 50MHz.

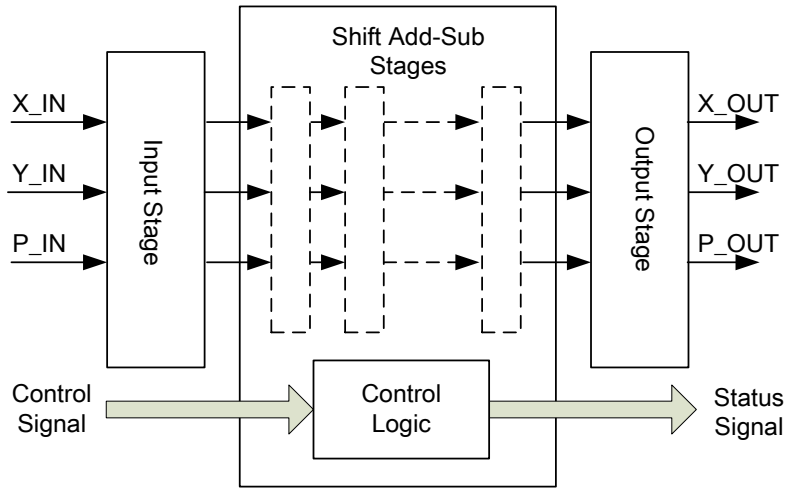

Figure 4.6 The architecture of Xilinx CORDIC IP

Due to the lower resource consumption of the CORDIC architecture, the multi-frequency excitation signal can be realized on one FPGA. Five CORDIC IP cores have been implemented in parallel for generating a multi-tone signal with five different frequencies. The architecture for multi-tone waveform generator is illustrated in Figure 4.7.

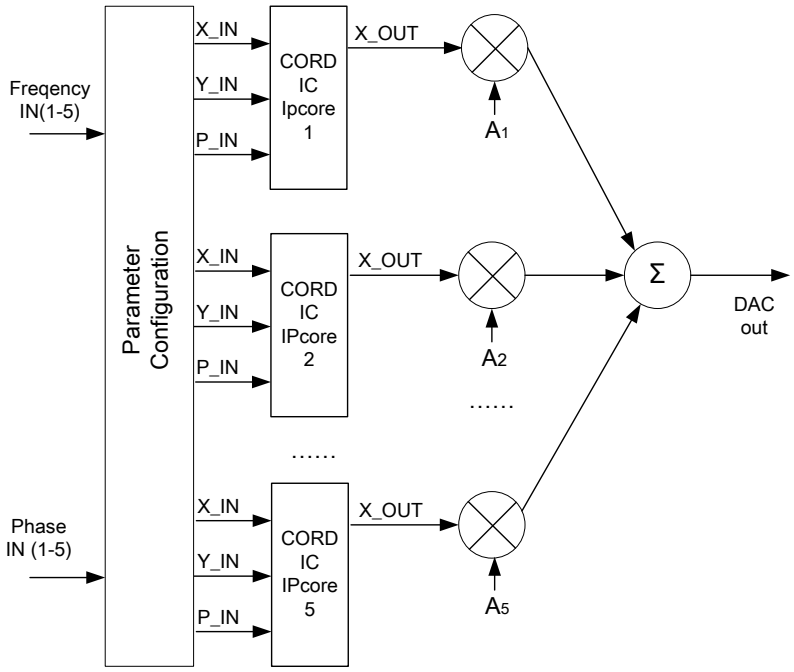

Figure 4.7 The multi-tone signal generator based on CORDIC IP cores

In the architecture above, there are five CORDIC IP cores combined together in FPGA. The parameter configuration module translated the user defined parameters (frequencies and initial phases of signals) into the acceptable format of IP cores. The outputs of every CORDIC IP core are multiplied with gain factors (A1-A5) for adjusting the amplitude of each signal. The multiplied results are then summed up in an adder. Finally the synthesized digital signal will send to the DAC for digital to analog convertion.

In order to evaluate the performance of the designed signal generator, a test signal with five frequencies (100kHz, 500kHz, 1MHz, 1.5MHz, 2MHz) was measured with an oscilloscope and spectrum analyzer. In Figure 4.8, the waveform in the time domain and the spectrum in the frequency domain shows that the generated signal contains five frequencies according to our configuration. It proves that the CORDIC based multi-tone generation method works well in our system.

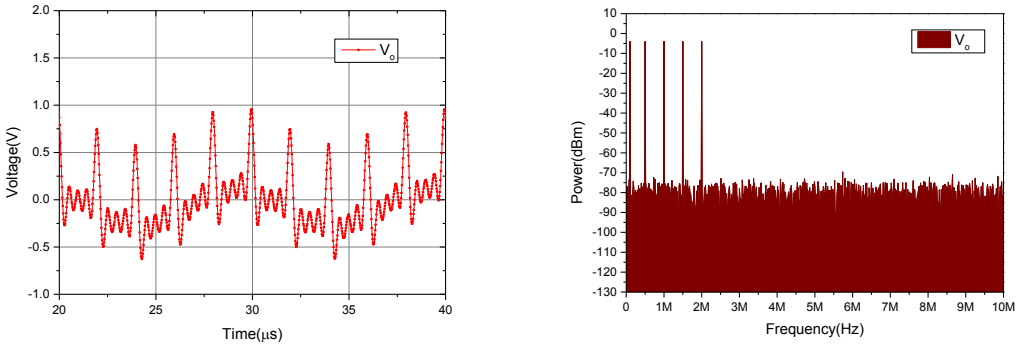

Figure 4.8 The waveform and frequency spectrum of generated multi-tone signal.

4.4 REALIZATION OF SINGLE-FREQUENCY DABB ALGORITHM

A brief architecture diagram of the realized single frequency digital auto balancing algorithm is illustrated in Figure 4.9. The sine and cosine component of the reference signal is generated from the digital waveform synthesizer by the DDS

technique. Each signal is sent to a parallel multiplier and is multiplied by the weight respectively. The weights w_I and w_Q are recursively updated by the imbalance voltage V_e and the convergence coefficient 2μ. Through a multiply-accumulate calculation, the updated in-phase and quadrature components will synthesize an updated output signal to drive the bridge.

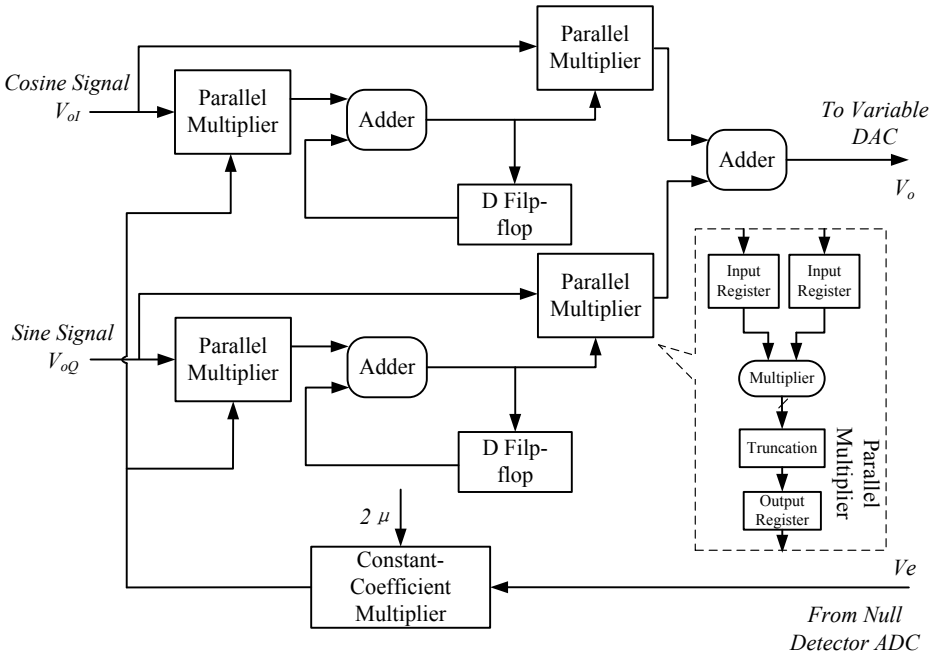

Figure 4.9 Function diagram of signal-tone algorithm in FPGA

This algorithm is fully implemented in the FPGA. We made use of 16-bit input quantization bit width to adapt our on-board devices (ADC and DAC). Eleven two's complement signed multiplier of XtremeDSP Slices are used in the algorithm. In order to maintain precision and avoid the overflow, the extended bits caused by the multiplication operation were truncated. The final implemented program utilizes 2,572 (16%) from the total of 15,360 Slices in the XC4VSX35 and can run at the maximum clock rate of 111.886MHz. All cores and hardware modules are described in very-high-speed integrated circuit hardware description language (VHDL) and synthesized with the Xilinx Synthesis Tool (XST). Simulations are performed in Modelsim, and Xilinx ChipScope is used for on-chip program debugging.

The performance of the bridge balancing is highly dependent on the step size parameter μ in LMS algorithm. To compare its impact, we have chosen three different values (μ=0.02, μ=0.1, μ=0.5) to view the filter results. The reference signal is a pure sine wave at 1MHz. A 0.1% precision resistor has been measured as the object under test which value equals to the reference resistor (*Zx=Rf*). The imbalance voltage (*Ve*) and the variable signal (*Vf*) have been acquired by ChipScope in the FPGA.

Figure 4.10 shows different convergent performances at different step sizes. With the setting μ=0.02 and μ=0.1, the balancing algorithm can be correctly performed and the error voltage can converge. The convergence rate of setting μ=0.1 is much faster than when μ=0.02. When we increased the step size to μ=0. 5, unstable oscillation occurred on the output of the variable source. The results reveal that a bigger value of μ causes a faster convergence, but at the cost of increasing the risk of oscillation, whilst a smaller value of μ results in a slower convergence but demonstrates more stable performance. In practical FPGA design, it takes values between 0 and 1/NS, where *N* is the number of filter steps and *S* is the highest value of power spectral density of the input voltage step, which depends on the impedance value under test.

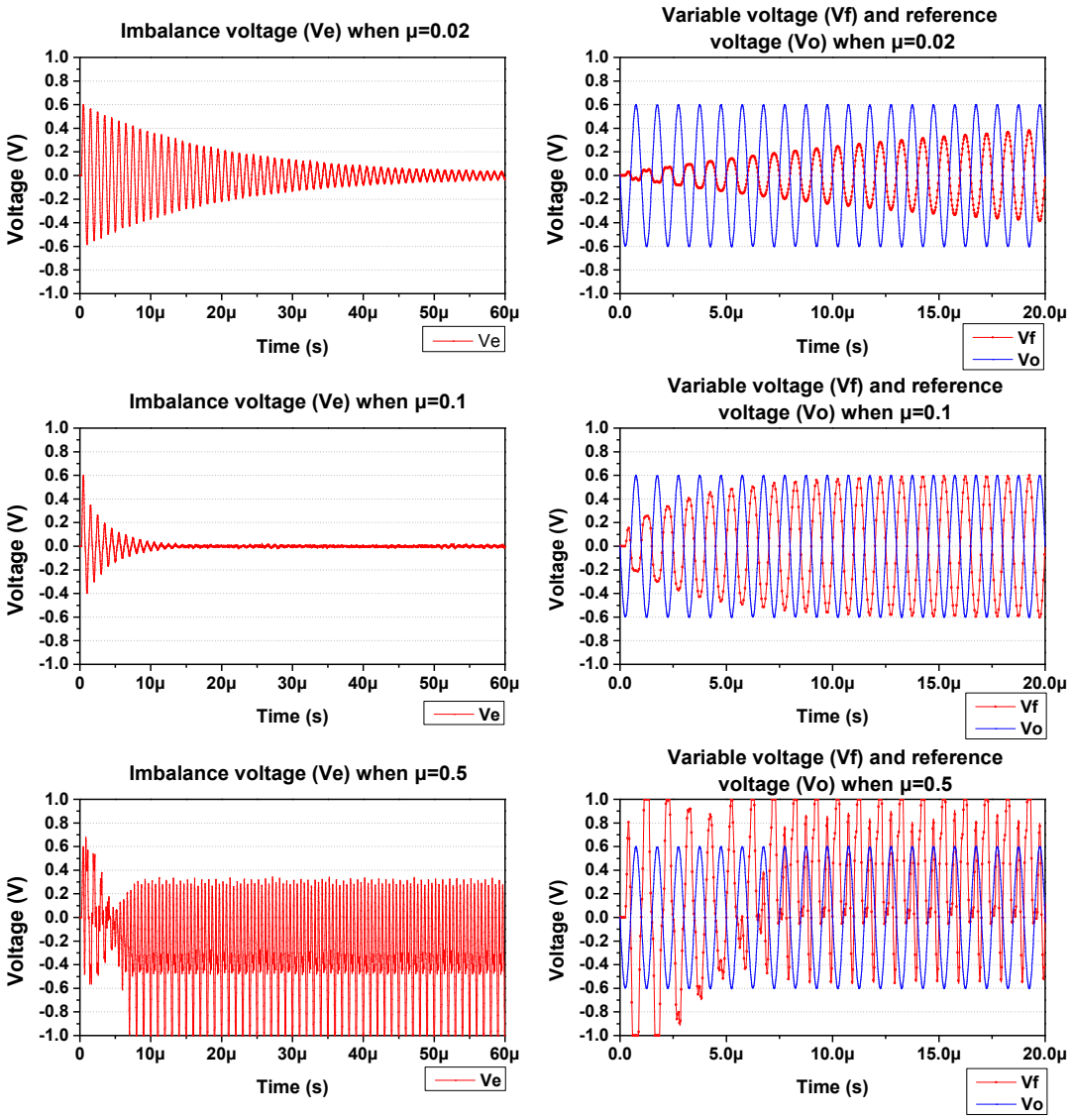

Figure 4.10 Performance of digital auto balancing algorithms for different step sizes.

In order to choose an appropriate step size, we selected eight different step sizes (from 0.001 to 0.2) in the theoretical range and compared their actual performance under three different impedance values (1k, 10k and 100k Ohm). The bars in the Figure 4.11 reveal that the convergence time decreased when the step size increased. Figure 4.12 shows that the larger step size slightly increases the magnitude of the error voltage after balancing. In our system, we have finally chosen μ=0.05 to guarantee stability in all our impedance range (100 to 10M Ohm) and frequency range (1k to 10M Hz) with a comparatively fast convergence rate.

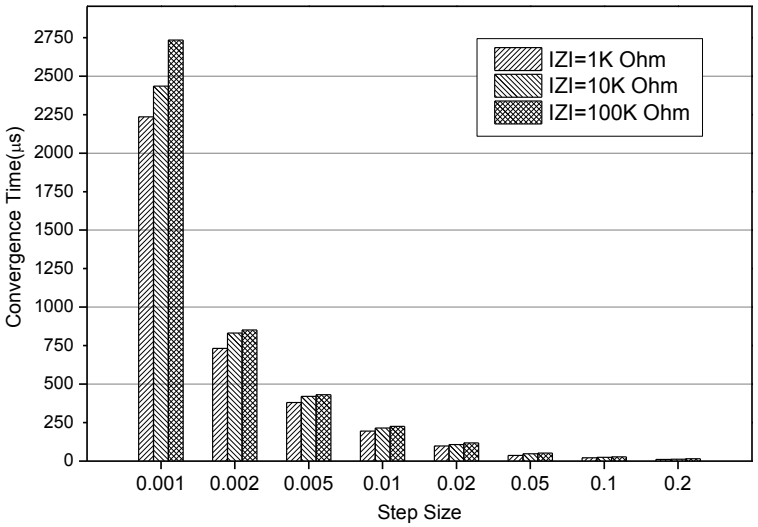

Figure 4.11 Convergence time under different step sizes.

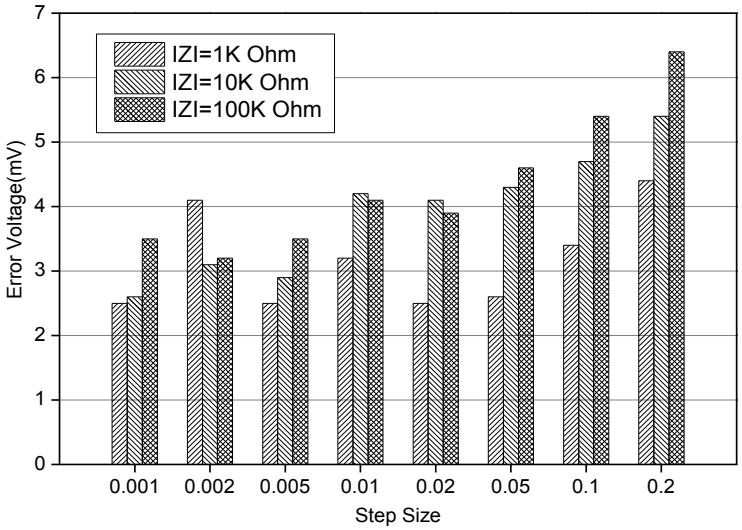

Figure 4.12 Error voltage after balancing under different step sizes.

4.5 MULTI-FREQUENCY DABB ALGORITHM BASED ON FBLMS

4.5.1 PRINCIPLE OF FBLMS ALGORITHM

In some applications, such as adaptive echo cancellation and adaptive noise cancellation, the computational efficiency of the LMS algorithm is necessary (Boll and Pulsipher, 1980). The standard LMS algorithm might spend a long time to perform the filtering and coefficients updating process (Farhang-Boroujeny, 1997).

This time might cause problems in particular applications because the adaptive filter has to operate in real time to filter the input signals.

There are many approaches invented to reduce the computational requirements of the LMS algorithm. Block LMS algorithm is proposed by G. A. Clark and his colleagues in 1981 (Clark *et al.*, 1981). The block LMS algorithm uses the calculation of a block of finite set of output values from a block of input values. Thus, the parallel-architecture-based processors can be used in block implementations of digital filters in order to increase the calculation speed. Compared to the traditional LMS, which derives from the steepest descent algorithm, the weights of block LMS are updated once per every block of data instead of updating on every clock cycle of input data. Because the updating is performed at block level, the error values can be calculated once per block of data, making it convenient for hardware implementation.

The fast block LMS algorithm (FBLMS) is developed based on the Block-LMS, but the heavy calculations are made in the frequency domain. These methods can also be used to improve the convergence properties of the LMS algorithm. It applies the fast Fourier transform (FFT) to transform the input signal *x(n)* to the frequency domain (Mikhael and Wu, 1989; Jae and Chong Kwan, 1989). The FBLMS algorithm updates the filter coefficients in the frequency domain, which reduces computational resources (Farhang-Boroujeny and Gazor, 1994; Benesty and Duhamel, 1992). The following Figure 4.13 illustrates the steps of this algorithm:

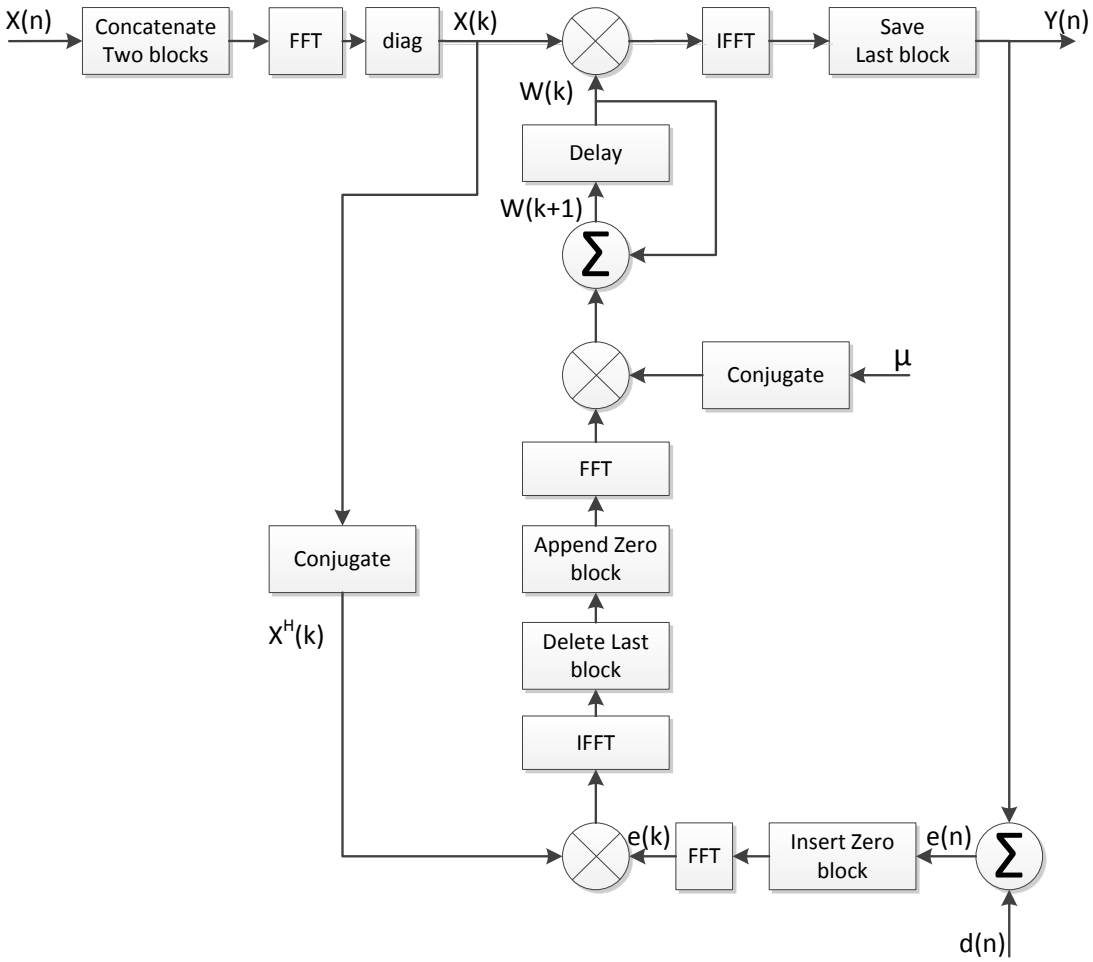

Figure 4.13 The process of fast block LMS algorithm

The figure shows how FBLMS algorithm completes adaptive processes. The steps are summarized as follows:

（1）. Concatenates the current input signal block to the previous blocks.

（2）. Carrys out the FFT to transform the input signal blocks from the time domain $x(n)$ to the frequency domain $x(k)$.

（3）. Multiplies the blocks of input signal $x(k)$ by the vector of filter coefficients $w(k)$

（4）. Performs an inverse FFT (IFFT) on the multiplication result.

（5）. Retrieves the last block from the result as the output signal vector $y(n)$.

（6）. Calculates the vector of error signal $e(n)$ by comparing the vector of input signal $d(n)$ with $y(n)$.

（7）. Inserts zeroes before the vector of error signal $e(n)$. This process ensures the error signal vector has the same length as the concatenated blocks of input signal.

（8）. Performs the FFT on the blocks of error signal, get results $e(k)$.

（9）. Multiplies the results $e(k)$ by the complex conjugate of the FFT result of the blocks of input signal $x^H(k)$.

（10）. Performs the IFFT on the multiplication result.

（11）. Fill the values of the last block of the IFFT result with zeroes, then does an FFT on the IFFT result.

（12）. Multiplies the FFT result by the step size μ

（13）. Adds the filter coefficients vector $w(k)$ to the multiplication result. This step updates the filter coefficients $w(k+1)$.

Compared to the typical LMS algorithm, the FBLMS algorithm has the following differences. Firstly, the typical LMS algorithm adjusts the coefficients sample by sample. But the FBLMS algorithm adjusts the coefficients block by block. The block size is equal to the length of the filter. Secondly, the FBLMS algorithm demands fewer multiplications than the typical LMS algorithm. If both the filter length and block size are N, the typical LMS algorithm needs N(2N+1) multiplications, whereas the FBLMS algorithm needs only (10Nlog2N+26N) multiplications. For instance, if N= 1024, the FBLMS algorithm operates 16 times faster than the typical LMS algorithm. Thirdly, the FBLMS algorithm can process multi-frequency signals in the frequency domain at one time. Thus the bridge can be balanced even in the multiple frequencies situation. The typical LMS algorithm can only be balanced at one frequency, which limits its speed in multi-frequency applications.

4.5.2 REALIZATION OF FBLMS-BASED BRIDGE BALANCE ALGORITHM

According to the principle diagram of the FBLMS algorithm, the hardware implementation in FPGA is illustrated in the following Figure 4.14.

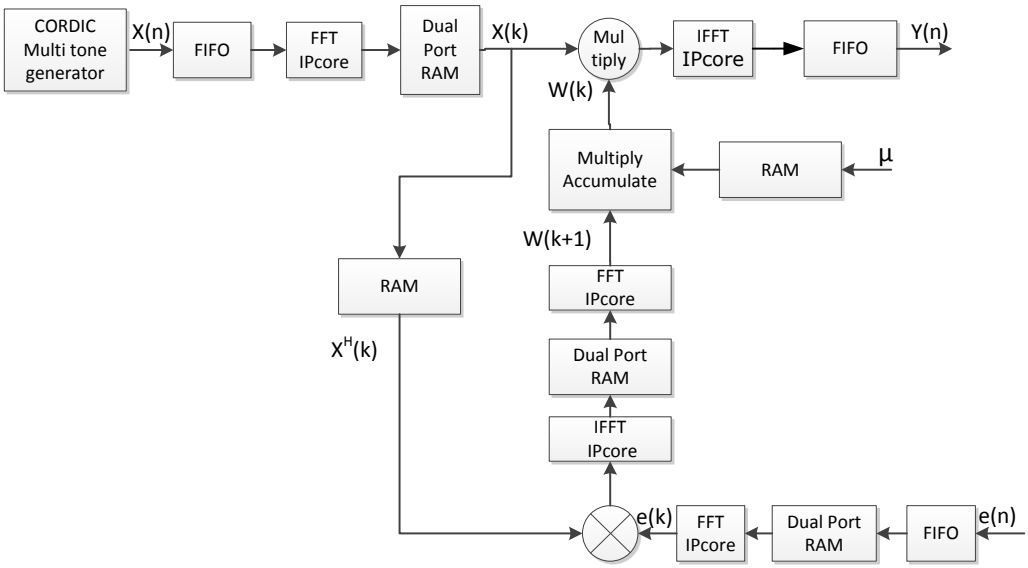

Figure 4.14 The implemented FBLMS-based bridge balancing algorithm

In FPGA, the reference signal is firstly generated from the CORDIC based multi-tone generator. The multi-frequency signal passes through a FIFO (first-in first-out), which concatenates the signal into blocks by controlling the read_enable signal. Then the block of signal is sent to FFT intellectual property(IP) core to perform the Fourier transform. The transformed signal will multiply the updated weights array $w(k)$. After that, the results are sent to IFFT IP core. The transformed signal passes through the FIFO and is sent to the DAC of the variable source of bridge.

The error signal $e(n)$ is digitized from the balance point of the external bridge, which implies the status of the bridge balancing. After rate converting (by FIFO) and insert zero operation (in a dual-port RAM), the error signal enters another FFT IP core for the Fourier transform. The transformed signal $e(k)$ is

multiplied by the complex conjugate of the FFT result of the input signal blocks $x^H(k)$. Subsequently, the results are sent to the IFFT IP core for transforming. In a dual port RAM, the data are then organized into blocks, and the values of the last block will be set to zeroes. The updated blocks then fed to an FFT IP core to generate the weights of the adaptive algorithm. By a multiply-accumulate component, the weights will be updated according to the step size μ .

The FFT and IFFT IP core is realized by the Xilinx Fast Fourier Transform LogiCORE IP (Xilinx. USA). It is a drop-in module for Xilinx's FPGAs. The FFT core can compute an N-point forward DFT or inverse DFT (IDFT) following the Cooley-Tukey FFT algorithm. For fixed-point inputs, the input data is a vector of N complex values represented as dual two's-complement numbers (width is up to 34 bits) for each of the real and imaginary components of the data sample. For floating-point inputs, the input data is a vector of N complex values represented as dual 32-bit floating-point numbers with the phase factors represented as 24- or 25-bit fixed-point numbers (Xilinx, 2011). Three arithmetic options (full-precision unscaled arithmetic, scaled fixed-point and block floating-point) are available for computing the FFT.

The type of transform (forward or inverse), point size, and the scaling schedule of FFT IP core are configurable during running time. The transform type, cyclic prefix length and scaling schedule can be configured frame-by-frame. There are four architecture configurations in this IP core: Pipelined, Streaming I/O, Radix-4, Burst I/O, Radix-2, Burst I/O, and Radix-2 Lite, Burst I/O, each one has difference in its resource cost and speed of performance. In our application, Pipelined, Streaming I/O architecture has been chosen to implement. The architecture of Pipelined, Streaming I/O FFT IP is shown in Figure 4.15 below.

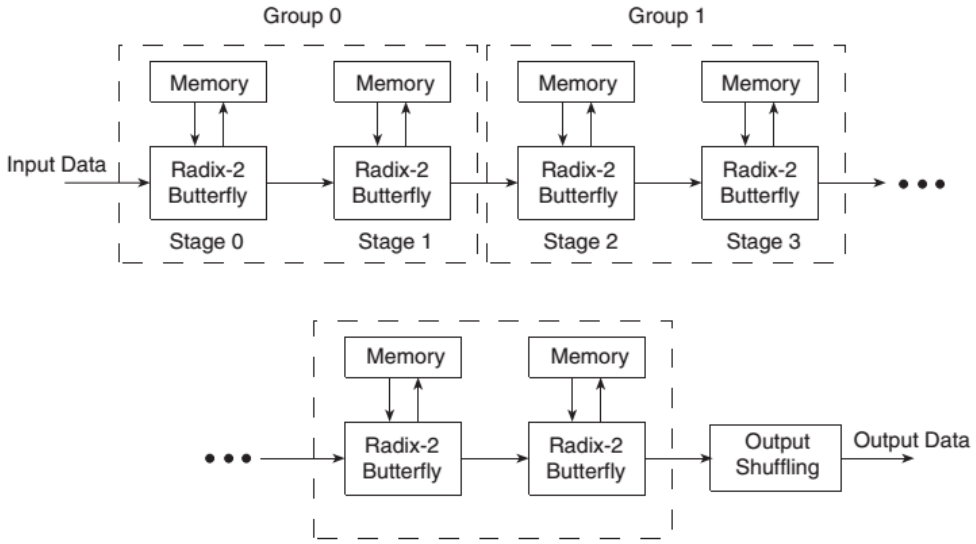

Figure 4.15 The architecture of the pipelined FFT IP Core(Xilinx, 2011)

The Pipelined, Streaming I/O architecture employs many pipelined Radix-2 butterfly processing units to compute the data stream. Each unit has its own memory to store the incoming and intermediate data. Transformation calculations on the current frame of data, loading incoming data for the next frame of data, and unloading the outcoming of the previous frame of data is simultaneously performed. Therefore, users can continuously input data and unload the results after the calculation latency (Xilinx, 2011).

In our application, the scaled fixed-point mode is chosen, which scaled data after every pair of Radix-2 stages. It maintains extra bits of precision to provide dynamic scaling. Compared to the block floating-point mode, this mode may save lots of hardware resources. By selecting an appropriate scaling schedule to avoid overflow, the scaled arithmetic is adequate for our application thus resources of the FPGA are saved. This architecture supports FFT point sizes up to 65536. Block RAM is used for storing data and phase factor by the number of stages, and the remaining stages use distributed memory in FPGA.

4.5.3 THE PERFORMANCE OF FBLMS BASED AUTO BALANCING ALGORITHM

In order to evaluate the performance of the FBLMS based DABB algorithm, a testing bridge circuit has been set up. The under test bioimpedance here is replaced by a precise resistor (1K Ohm, RT0805BRD071KL,Yageo, China). The feedback resistor also used the same type. The frequency of the reference signal is 1MHz. By using the bridge balancing algorithm, the bridge will get balanced afterwards. The unbalanced voltage (*Ve*) at the midpoint of the bridge is measured by ADC during the whole balancing time. The difference results from LMS-based DABB method and FBLMS-based DABB method are depicted in Figure 4.16 and Figure 4.17.

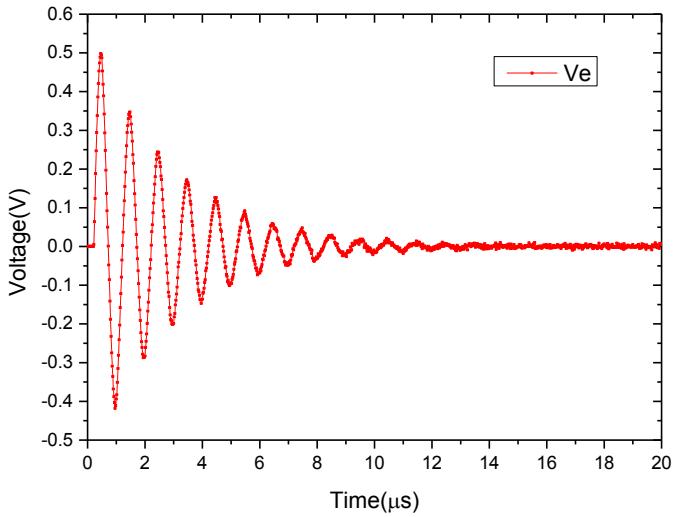

Figure 4.16 The unbalanced voltage (*Ve*) of the LMS-based bridge.

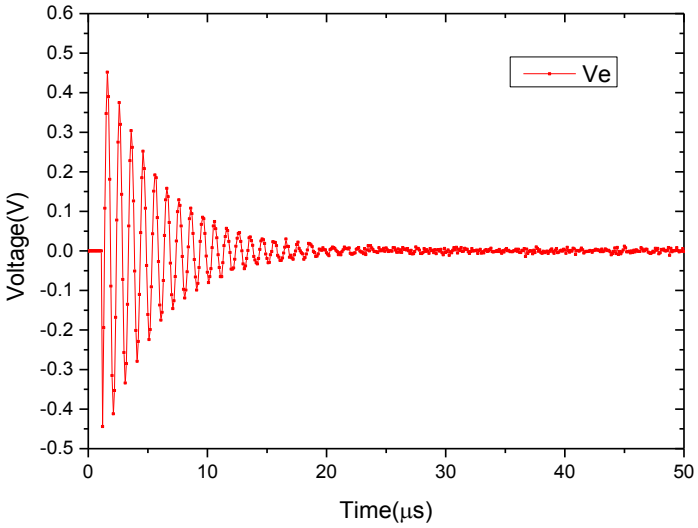

Figure 4.17 The unbalanced voltage (*Ve*) of the FBLMS-based bridge.

From the two waveforms shown above, we can see that in the aspect of the balancing speed of the bridge, in single frequency application, the LMS based DABB method is quicker than the FBLMS based method. With the same step size, compared to the LMS based method, the FBLMS based method uses double time for bridge balancing. Because the FBLMS algorithm processes the signal block by block whatever its single or multi-frequency signal, the time-cost will be longer than LMS algorithm. It means the LMS based DABB method will still be the best choice in single frequency application, due to its faster speed and simpler implementation.

Two methods are compared with the multi-frequency situation as well. The results are shown in Figure 4.18 and Figure 4.19 From the waveforms shown, the LMS based DABB can not converge under multi-frequency excitation., The FBLMS based DABB method shows its advantage in stable convergence. We can see the bridge is balanced after approximately 40 us. It proves that the FBLMS is a good choice for multi-frequency application. With a little increase in time, the FBLMS based method can measure 4 more frequencies than the standard LMS based method at one time.

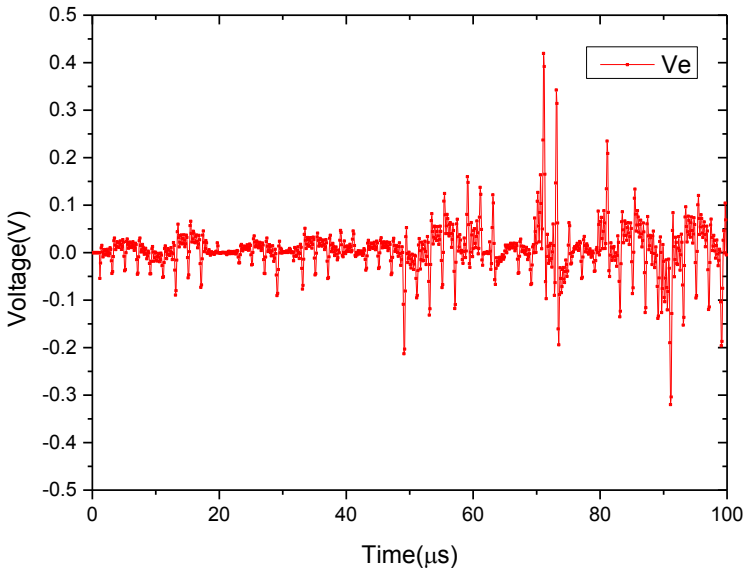

Figure 4.18 The unbalanced voltage (*Ve*) of the LMS based bridge in multi-frequency

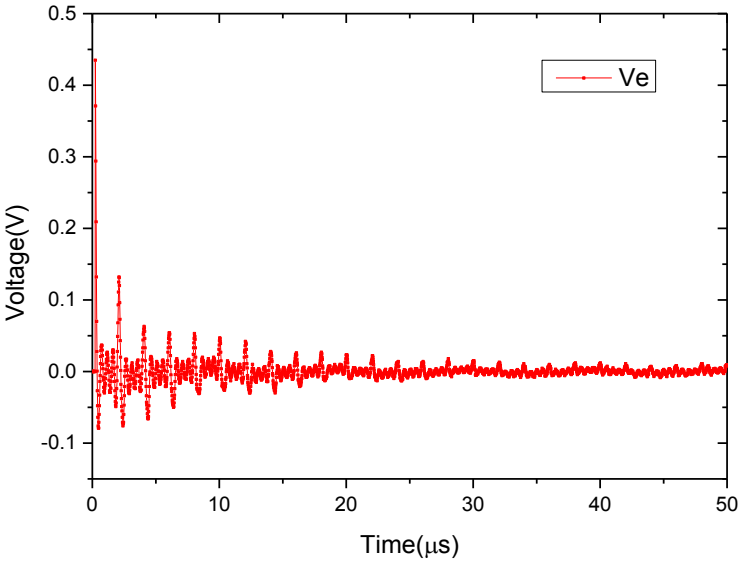

Figure 4.19 The unbalanced voltage (*Ve*) of the FBLMS based bridge in multi-frequency

The Figure 4.20 shows the reference signal (V_o) and the feedback signal (V_f) when the bridge is balanced. Each signal is captured by Chipscope software at the output port of the FPGA. Because the two impedances on the bridge are the same value resistors, theoretically, the feedback signal will be equal to the reference signal when the bridge is balanced, with opposite phases. From the measured

results, we can see the feedback signal is adjusted to the reference signal. It means the FBLMS algorithm works well in our digital auto balancing bridge method.

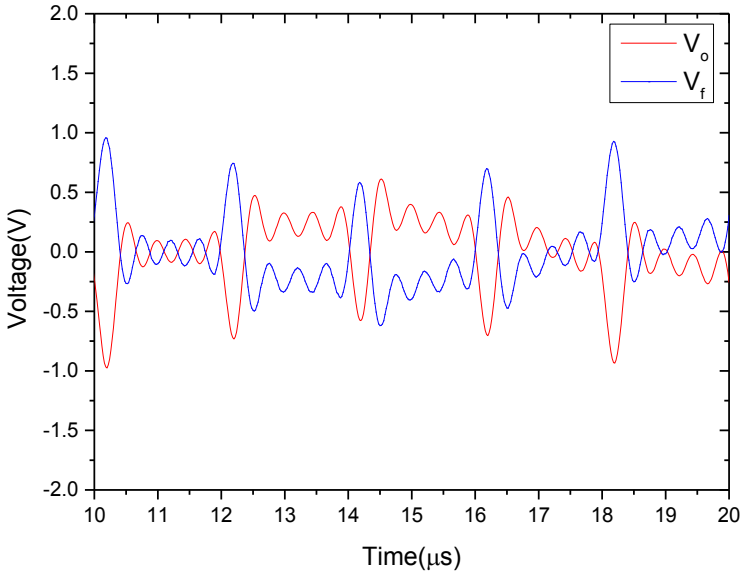

Figure 4.20 The reference signal (V_o) and the feedback signal (V_f) when bridge balanced

Finally, we listed the resource consumption of the FBLMS algorithm in FPGA (XC4VSX35, Xilinx, USA). From the Table 4.2 below, we can see that the FBLMS algorithm has high efficiency in resource utilization, which means that the algorithm can be implemented in smaller and lower price digital devices for higher cost-efficiency applications.

Table 4.2 Resource consumption of FBLMS based DABB method

Slice Logic Utilization	Used	Available	Utilization
Number of Slice Registers	4,250	30,720	13.8%
Number of 4 input LUTs	3,180	30,720	10.3%
Number of FIFO16/RAMB16s	67	192	34.9%
Number of DCM_ADVs	2	8	25%
Number of XtremeDSP Slices	26	192	13.5%

4.6 CONCLUSION

In this chapter, a novel bioimpedance measurement method, coined digital auto balancing bridge (DABB) method has been proposed and realized. This method is developed from the traditional analog balancing bridge method for unknown impedance measurement. The bridge balancing algorithm is the core of the DABB method. We described the principle of LMS-based bridge balancing algorithm and the implementation in FPGA.

The CORDIC algorithm is applied for generating a reference signal and a feedback signal. In our system, the CORDIC algorithm is implemented by IP Core in FPGA, that saves lots of storage resources. The realization of single-frequency DABB algorithm has been introduced. Besides, in order to apply the DABB method in multi-frequency measurements, we designed a new DABB method based on the fast block LMS algorithm. This method can process the multi-frequency signal in the frequency domain at one time. Thus the bridge can be balanced, even in the multiple frequencies situation. Whereas, the standard LMS algorithm can only be balanced at one frequency, which limits its speed in multi-frequency applications.

The testing shows the FBLMS based DABB method has advantages of stable convergence of multi-frequency applications. With a little increase in time consumption, the FBLMS based method can measure 4 more frequencies than the standard LMS based method at one time. It significantly improved the measurement speed of bioimpedance measurements.

Chapter 5. APFFT ALGORITHM FOR MULTI-FREQUENCY BIO-IMPEDANCE ANALYSIS

In multi-frequency bioimpedance measurements, the time cost of measurement can be significantly reduced by using multi-frequency excitation technique, which acquires more impendence information at different frequencies. However, when using multi-frequency excitation, the signal demodulator also needs to be improved for handling multi-frequency signals. In this chapter, a new algorithm-All phase Fast Fourier Transform (APFFT) is applied in bioimpedance analysis. It provides higher precision in phase and amplitude than traditional methods. The principle, analysis and evaluation of the APFFT algorithm are presented in this chapter.

5.1 INTRODUCTION OF APFFT ALGORITHM

In traditional EIT systems, mainly demodulation methods are analogue or digital quadrature demodulation, which perform well for single-frequency applications. However, in multi-frequency EIT (MFEIT) applications, these methods will make the system complicated and slow. Because one quadrature demodulator can only process a single frequency at a time, thus the system should either operate in sweeping mode or integrate several parallel quadrature demodulators if different frequencies are applied at one time.

In order to solve this problem, the Fast Fourier transform (FFT) algorithm is widely used for post-processing of bio-impedance spectra due to its convenience in hardware implementation. (Sun *et al.*, 2007; Kaczka *et al.*, 1995; Pochet *et al.*, 1992;

Davis and Lutchen, 1991b, a). The FFT algorithm is among the most important algorithms in the digital signal processing area. FFT has three major applications. First, the frequency spectrum of a digital signal can be obtained by FFT computing. From the calculated spectrum, the magnitude and phase of every frequency that makes up the signal can be derived. Second, the response of a digital system can be expressed as the FFT of the system's impulse response. At last, FFT is used as a middle step in other digital signal processing algorithms and methods. For example, digital convolution can be calculated indirectly by introducing the FFT, and the FFT is an indispensable algorithm in digital filter design.(Lee and Min, 1991; Chen *et al.*, 1990; Sunshine *et al.*, 1989; Christenson *et al.*, 1989) Because the input signal of the FFT and its result are both in discrete form, it is very suitable to be realized in computer or digital processors. Therefore, the FFT-based digital signal processing technologies developed rapidly with computer technology.

A main problem of applications of FFT is spectral leakage that causes deviations between the FFT results and the actual characteristics in the frequency domain. One feasible way to improve the spectral leakage problem is adding windows such like rectangle window, triangle window, Hanning window, Blackman window, Hamming window and so on. However, there is a tradeoff of no-windows and added-windows. Lower amplitude tails (or side lobe) always come with a wider main lobe. Similarly, a narrower main lobe always comes with higher amplitude tails. Therefore, neither of these windows can be qualified as the best one. This trade off must be carefully considered in practical use. That is the reason why there are so many FFT windows designed for diverse applications.

The theory of All Phase Fast Fourier Transform (APFFT) was proposed by Professor Zhaohua Wang and Zhengxin Hou of Tianjing University (Zhaohua *et al.*, 2003a). It is an improved algorithm of the traditional fast Fourier transform (FFT) which can improve the fence effect and truncation effect (Zhaohua *et al.*, 2003b).

The APFFT is proposed to solve the problem of spectrum leakage, which is a very practical algorithm to calculate the frequency spectrum. Compared with FFT, APFFT reduce spectral leakage caused by truncation error efficiently. It has excellent performance in suppressing spectral leakage and the property of phase invariant. Another merit of APFFT is that the phases calculated by APFFT need not being adjusted, and does not affected by the frequency offset. Thus, whether the signal is truncated at the entire cycle, a precise result could be derived from APFFT. Recently APFFT algorithm is widely applied in digital signal processing for precision measurement (Xiaodong *et al.*, 2013; Wentao *et al.*, 2013; Xiangdong *et al.*, 2010; Guo *et al.*, 2010; Huang *et al.*, 2007).

5.2 ANALYSIS OF MAJOR ERRORS IN DFT

The Fourier transform, which is named after Jean Baptiste Joseph Fourier, can be divided into four categories. There are Fourier transform, Fourier series, Discrete Time Fourier Transform (DTFT) and Discrete Fourier Transform (DFT). DFT is a discrete and periodic form of the Fourier transform of signals. The relationship between an N-point time sequence $x(n)$ and frequency sequence $X(k)$ is defined as DFT:

$$X(k)=\sum_{n=0}^{N-1}x(n)e^{-j\frac{2\pi k}{N}n} \tag{5.1}$$

$$x(n)=\frac{1}{N}\sum_{k=0}^{N-1}X(k)e^{j\frac{2\pi k}{N}n} \tag{5.2}$$

Suppose that the sampled input signal is a single frequency complex signal:

$$x(n) = Ae^{j(2\pi nk_0/N+\varphi_0)} \tag{5.3}$$

where φ_0 is the initial phase of the signal when $n=0$. Apply this signal to the DFT expression in (5.1), we have:

$$\begin{aligned} X(k) &= \sum_{n=0}^{N-1} x(n)e^{-j\frac{2\pi k}{N}n} = \sum_{n=0}^{N-1} Ae^{j(\frac{2\pi nk_0}{N}+\varphi_0)}e^{-j\frac{2\pi k}{N}n} \\ &= Ae^{j\varphi_0}\sum_{n=0}^{N-1} e^{j(\frac{2\pi nk_0}{N}-\frac{2\pi k}{N}n)} \\ &= Ae^{j\varphi_0}\sum_{n=0}^{N-1} e^{j\frac{2\pi}{N}(k_0-k)n} \\ &= Ae^{j\varphi_0}\frac{1-e^{j2\pi(k_0-k)}}{1-e^{j2\pi\frac{(k_0-k)}{N}}} \\ &= Ae^{j\varphi_0}\times e^{j\pi(k_0-k)(1-\frac{1}{N})}\times\frac{\sin\left[\pi(k_0-k)\right]}{\sin\left[\pi(k_0-k)/N\right]} \end{aligned} \tag{5.4}$$

There are three errors may exist in the DFT result:

(1) Aliasing

In signal processing disciplines, aliasing refers to an effect that causes different signals to become indistinguishable. This is another phenomenon encountered in FFT computation. Aliasing happens when there are insufficient samples acquired on each cycle of the input signal to recognize the signal. This occurs whenever the frequency of the input signal is greater than the Nyquist frequency. When a signal is aliased, the higher frequency components show up in the FFT spectrum at a lower frequency. The solution is either to increase the sampling rate or to pre-filter the signal in order to minimize its high frequency spectral content (Ishii and Wakamoto, 1983).

(2) Spectral Leakage

The DFT operation assumes that the time record repeats. Unless there are integral multiple of cycles of the sampled waveform in the data, a

discontinuity is created at the end of the record. This is referred to as spectral leakage. The resulting function will have unwanted additional frequency components due to the change from truncation. The only solution is that if the sampled signal is an integral multiple of cycles. Spectral leakage can be reduced either by taking more samples (wider windows of data), or by choosing a different window function. However, it can't be completely eliminated for most functions(Salor, 2009).

(3) The Picket Fence Effect

As has been stated before, the DFT spectrum is a discrete spectrum, consisting of estimates of what the spectral level is at specific frequencies. These frequencies are determined by the FFT points, and have nothing to do with the signal being analyzed. This means there may be, and probably are, peaks in the true spectrum of the signal that is between the lines of the FFT analysis. This also means that the peaks in a FFT spectrum will be measured too low in level, and the valleys will be measured too high. Moreover, true frequencies where the peaks and valleys lie will not be those indicated in the FFT spectrum (Girgis and Ham, 1980).

The spectral leakage problem can be analyzed by mathematical calculation. Assuming a sampled complex signal $Ae^{j(2\pi nk_0/N+\varphi_0)}$, perform N point DFT, the process is shown below:

$$
\begin{aligned}
X(k) &= \sum_{n=0}^{N-1} x(n) e^{-j\frac{2\pi k}{N}n} \\
&= \sum_{n=0}^{N-1} A e^{j(\frac{2\pi n k_0}{N}+\varphi_0)} e^{-j\frac{2\pi k}{N}n} \\
&= A e^{j\varphi_0} \sum_{n=0}^{N-1} e^{j(\frac{2\pi n k_0}{N}-\frac{2\pi k}{N}n)} \\
&= A e^{j\varphi_0} \sum_{n=0}^{N-1} e^{j\frac{2\pi}{N}(k_0-k)n} \\
&= A e^{j\varphi_0} \frac{1-e^{j2\pi(k_0-k)}}{1-e^{j2\pi\frac{(k_0-k)}{N}}} \\
&= A e^{j\varphi_0} \times e^{j\pi(k_0-k)(1-\frac{1}{N})} \times \frac{\sin\left[\pi(k_0-k)\right]}{\sin\left[\pi(k_0-k)/N\right]}
\end{aligned}
\tag{5.5}
$$

where the third component $\frac{\sin\left[\pi(k_0-k)\right]}{\sin\left[\pi(k_0-k)/N\right]}$ denotes the amplitude of spectrum. We can see that the DFT result of signal is combined the actual spectrum with a linear phase $e^{j\pi(k_0-k)(1-\frac{1}{N})}$. In respect of magnitude spectrum, if the sampling period is an integral multiple of signal frequency, the k_0 is an integer. Thus the precise magnitude can be derived when $k=k_0$. If $k\neq k_0$ (k is an integer), the product of $e^{j\pi(k_0-k)(1-\frac{1}{N})}$ and $\frac{\sin\left[\pi(k_0-k)\right]}{\sin\left[\pi(k_0-k)/N\right]}$ equals zero, thus the leakage problem can be avoided.

However, the precise integral ratio sampling is not feasible in practice, as there always be an error in the actual sampling process. When k_0 is not an integer, we cannot directly read out the actual precise magnitude from signal's DFT spectrum. Moreover, it becomes more complex in multi-frequency situation, because the leakage problem will get worse as the larger fractional part of $|k-k_0-0.5|$.

For example, a DFT spectrum when $k_0 = 4.3$, $N = 10$, $A = 1$, $\varphi_0 = \pi / 4$ is depicted in

Figure 5.1. We can see the error between the actual signal and the DFT result. The characteristic of the signal phase is shown in Figure 5.2. We simulated the spectrum of DTFT for comprehensively understanding. Because the DFT is uniform sampling of DTFT, it can be clearly revealed that the error between the actual signal and DFT result is obvious. The simulated results show that there is a relatively large error in magnitude and phase measurement of FFT results. By adding a particular window on signal, the leakage problem can be partially improved. However, the windows themselves also have phase characteristic, the calibration of the spectrum will be more difficult.

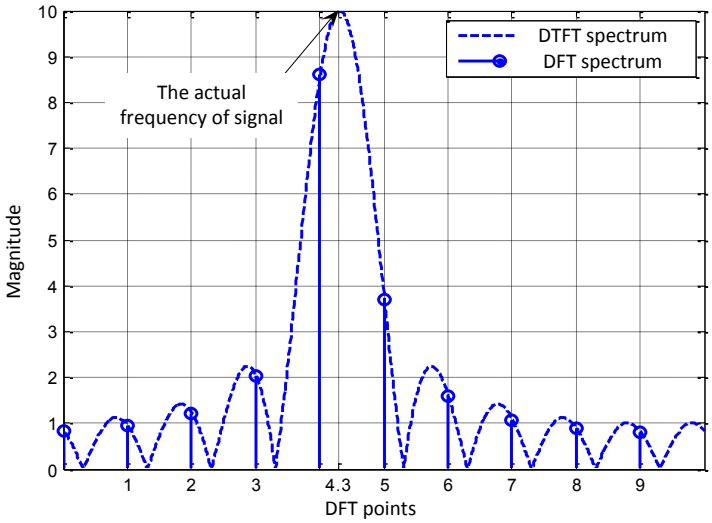

Figure 5.1 The magnitude of DFT result

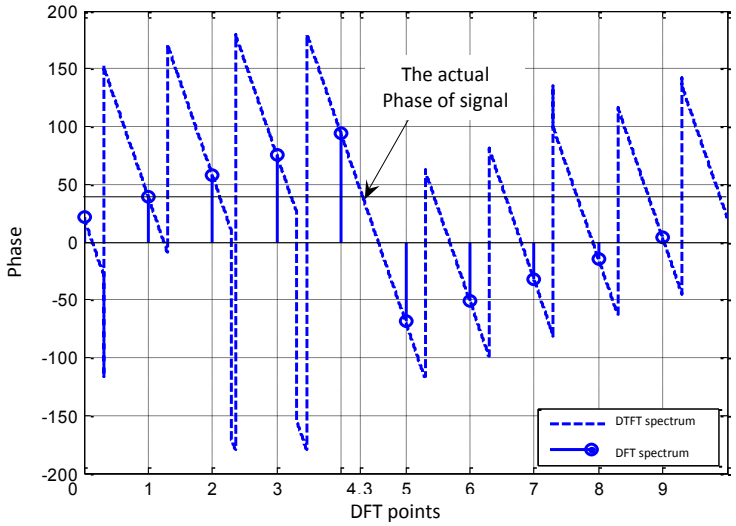

Figure 5.2 The phase of DFT result

Additional windows can be applied in both DFT and APFFT. Nevertheless, when using other windows, the situation would be more complicated. The APFFT discussed here is the basic form of APFFT based on a rectangle window. Other windows used in digital signal processing such as Kaiser and Hamming window can also be employed to improve the performance.

5.3 PRETREATMENT OF APFFT DATA

The pretreatment of APFFT is used to solve the data truncation error, which is the main factor to cause the spectral leakage. Notable here are the analysis of APFFT is based on Linear Time Invariant (LTI) Systems. In a practical application, most systems can be approximately treated as LTI Systems. This feature can simplify the analysis of the shift operation in APFFT pretreatment.

The pretreatment of no-window APFFT data is the simplest situation among all the pretreatment methods. The pretreatment of Single-windows data or double-windows data is more complicated to discuss, but they are both based on the pretreatment of no-window data (Zhaohua and Xiangdong, 2009).

In order to process an N (e.g. *N*=5) steps APFFT, the length of data should be prepared to $2N-1=9$ points for processing. The process can be explained by the following steps:

Step 1: Divide the data into subvectors, then find all *N* steps subvectors that contain *x(N-1)*. For example, in a five steps APFFT, the data are reorganized as Figure 5.3 shown:

$$
\begin{array}{lccccccccc}
 & x(0) & x(1) & x(2) & x(3) & x(4) & x(5) & x(6) & x(7) & x(8) \\
x_0: & & & & & x(4) & x(5) & x(6) & x(7) & x(8) \\
x_1: & & & & x(3) & x(4) & x(5) & x(6) & x(7) & \\
x_2: & & & x(2) & x(3) & x(4) & x(5) & x(6) & & \\
x_3: & & x(1) & x(2) & x(3) & x(4) & x(5) & & & \\
x_4: & x(0) & x(1) & x(2) & x(3) & x(4) & & & &
\end{array}
$$

Figure 5.3 Segmentation of no-window all phase data

Step 2: extend each subvector according to following rule as Figure 5.4 below

$$
\begin{array}{lccccccccc}
 & x(0) & x(1) & x(2) & x(3) & \underline{x(4)} & \underline{x(5)} & \underline{x(6)} & \underline{x(7)} & \underline{x(8)} \\
x_0: & x(5) & x(6) & x(7) & x(8) & x(4) & x(5) & x(6) & x(7) & x(8) \\
x_1: & x(5) & x(6) & x(7) & x(3) & x(4) & x(5) & x(6) & x(7) & x(3) \\
x_2: & x(5) & x(6) & x(2) & x(3) & x(4) & x(5) & x(6) & x(2) & x(3) \\
x_3: & x(5) & x(1) & x(2) & x(3) & x(4) & x(5) & x(1) & x(2) & x(3) \\
x_4: & x(0) & x(1) & x(2) & x(3) & \underline{x(4)} & \underline{x(0)} & \underline{x(1)} & \underline{x(2)} & \underline{x(3)}
\end{array}
$$

Figure 5.4 Periodic extension of no-window all phase data

Step 3: use the rectangle windows to truncate the extended data, and then sum up these data by column. Therefore the pretreated five steps APFFT data are derived as follows:

$$5x(4),\ 4x(5)+x(0),3x(6)+2x(1),\ 2x(7)+3x(2),\ x(8)+4x(3) \qquad (5.6)$$

The above process can be illustrated as shown in Figure 5.5. The pretreatment of APFFT can be considered as that the original data is multiplied with weights series (1 2 3 4 5 4 3 2 1) firstly, then the weighted

data be summed up by every 5 point. Therefore, the final APFFT data are derived. The original weights (1 2 3 4 5 4 3 2 1) can be resolved to a convolution of two weights series (1 1 1 1 1), and each series can be considered as a rectangle window. Therefore, the total weights can be treated as a window, which is derived by convolution of two rectangle windows whose length is 5.

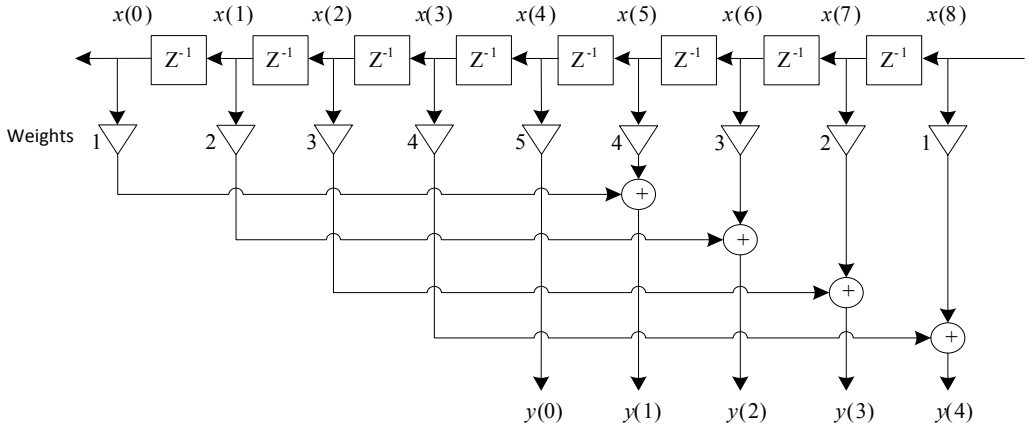

Figure 5.5 Pretreatment architecture of no-window all phase data

After the pretreatment procedure, a vector of five points data are obtained. These data is then calculated by FFT algorithm. The resulted spectrum called the APFFT spectrum. This process can also be expressed by formulas:

$$
\begin{aligned}
X_{ap}(k) &= \frac{1}{N}\sum_{i=0}^{N-1} x_i^{'}(k) = \frac{1}{N}\sum_{i=0}^{N-1} x_i(k) e^{j\frac{2\pi ki}{N}} \\
&= \frac{1}{N^2} e^{j\varphi_0} \sum_{i=0}^{N-1}\left[\sum_{m=0}^{N-1} x(m-i) e^{-j\frac{2\pi km}{N}} e^{j\frac{2\pi km}{N}}\right] e^{j\frac{2\pi ki}{N}} \\
&= \frac{1}{N^2} e^{j\varphi_0} \sum_{i=0}^{N-1} e^{-j2\pi(k_0-k)i/N} \cdot \sum_{m=0}^{N-1} e^{j2\pi(k_0-k)m} \\
&= \frac{1}{N^2} e^{j\varphi_0} \frac{1-e^{-j2\pi(k_0-k)}}{1-e^{-j2\pi(k_0-k)/N}} \cdot \frac{1-e^{j2\pi(k_0-k)}}{1-e^{j2\pi(k_0-k)/N}} \\
&= \frac{1}{N^2} e^{j\varphi_0} \frac{e^{j\pi(k_0-k)} - e^{-j\pi(k_0-k)}}{e^{j\pi(k_0-k)/N} - e^{-j\pi(k_0-k)/N}} \\
&\quad \cdot \frac{e^{-j\pi(k_0-k)} - e^{j\pi(k_0-k)}}{e^{-j\pi(k_0-k)/N} - e^{j\pi(k_0-k)/N}} \\
&= \frac{1}{N^2} e^{j\varphi_0} \frac{\sin^2(\pi(k-k_0))}{\sin^2\left(\pi(k-k_0)/\mathrm{N}\right)} \\
&= \left|\frac{1}{N} \cdot \frac{\sin(\pi(k-k_0))}{\sin(\pi(k-k_0)/N)}\right|^2 \cdot e^{j\varphi_0}
\end{aligned}
\tag{5.7}
$$

Finally, the amplitude of APFFT spectrum is

$$
|X_{ap}(k)| = \frac{1}{N} \cdot \left|\frac{\sin(\pi(k-k_0))}{\sin(\pi(k-k_0)/N}\right|^2 \tag{5.8}
$$

And the phase of APFFT spectrum is:

$$
\varphi = \varphi_0 \tag{5.9}
$$

The pretreatment is proposed to solve the truncation error in sampled data, which is the main source of spectral leakage. In the pretreatment of APFFT data, the *2N-1* discrete points have been firstly divided by *N* point windows into Ns data segments with length *N*. Then the data is aligned by the center of the original data(the N_{th} point). Subsequently, the aligned data has been summed up and multiplied by specific weights. Therefore, *N* point APFFT data are obtained. The APFFT method considered all possible combinations of truncation, so it can reduce the error caused by data truncation.

5.4 COMPARISON BETWEEN APFFT AND DFT ALGORITHMS

By conducting pretreatment of length $2N-1$ data, the length N of all-phase data are calculated. Subsequently, by using FFT algorithm to process these data, we can get all phase spectrum of the signal. There are many good features of all phase spectrum. Commonly, the FFT processes following pretreatment can be considered as an algorithm, which coined APFFT algorithm. The step size of APFFT algorithm is determined by the length N of divided section.

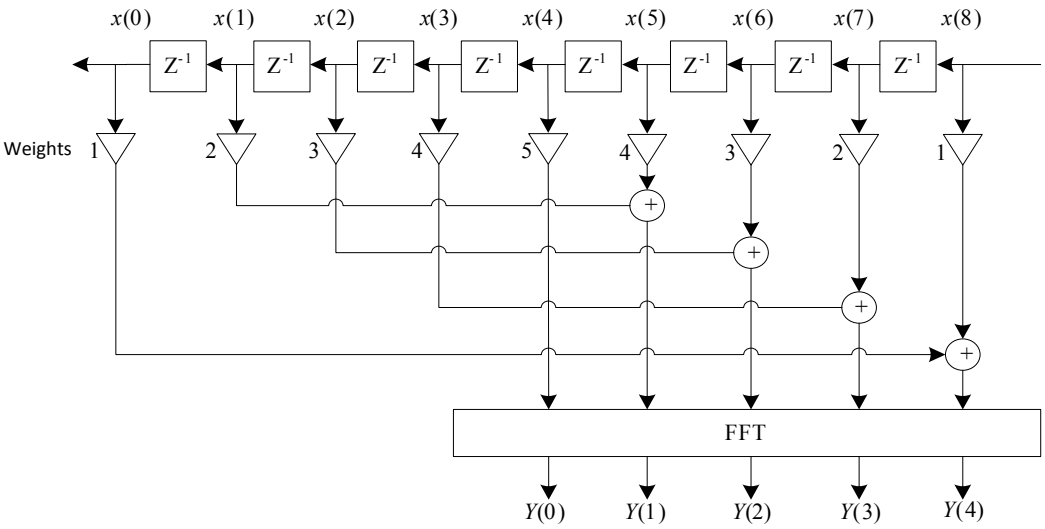

Figure 5.6 Spectrum analysis architecture of no-window APFFT

There are three ways to explain the calculation process of APFFT algorithm. The first one is illustrated as Figure 5.6 shown. It clearly shows the flow path of signals, offering help in hardware implementation. The second way is more direct to describe the theory, which is shown in Figure 5.7, it follows the pretreatment process of the APFFT algorithm.

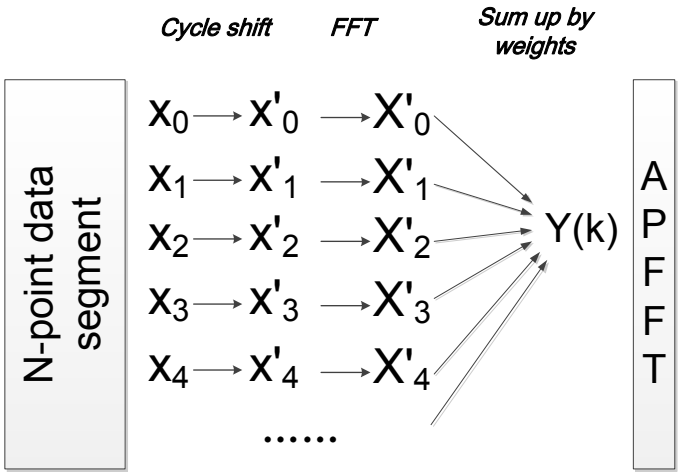

Figure 5.7 Flowchart of one analysis method of no-window APFFT spectrum

The third way is illustrated in Figure 5.8. The difference between Figure 5.7 and Figure 5.8 is that one performs a shift operation to the time domain signal firstly and then conducts FFT, another calculates the FFT results first and then performs phase compensation for phase calibration. Theoretically, the shift operation in the time domain equals to adding or subtracting a phase shift in the frequency domain. Therefore the third way is the same to the second way theoretically.

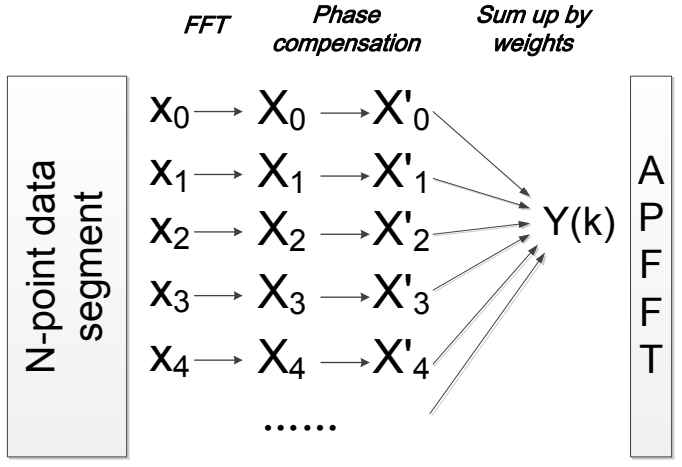

Figure 5.8 Flowchart of another analysis method of no-window APFFT spectrum

Currently we are following the third way to analyze the spectrum characteristic of APFFT algorithm. Dividing the $2N-1$ length single frequency

signal series $Ae^{j\frac{2\pi k_0}{N}m+\varphi_0}$ by length N from tail to head, assuming the first segment of data is x_0, and the subsequent segments of data are:

$$x_i(m) = x_0(m-i) \tag{5.10}$$

Assuming the DFT result of x_0 is X_0, the DFT results of each segment can be calculated:

$$X_i(k) = X_0(k)e^{-j\frac{2\pi k_0 i}{N}} \tag{5.11}$$

In order to align the time domain signal, every segment of data performs the phase compensation in the frequency domain:

$$X_i'(k) = X_i(k)e^{j\frac{2\pi k\times i}{N}} \tag{5.12}$$

From the results above, the spectrum of the single frequency signal $Ae^{j\frac{2\pi k_0}{N}m+\varphi_0}$ by no-windows APFFT processing is derived:

$$\begin{aligned}
Y(k) &= \sum_{i=0}^{N-1} X_i'(k) \\
&= \sum_{i=0}^{N-1} X_i(k)e^{j\frac{2\pi ki}{N}} \\
&= \sum_{i=0}^{N-1}\left[\sum_{m=0}^{N-1} x(m-i)e^{-j\frac{2\pi km}{N}}\right]e^{j\frac{2\pi ki}{N}} \\
&= Ae^{j\varphi_0}\times\sum_{i=0}^{N-1} e^{-j2\pi(k_0-k)i/N}\times\sum_{m=0}^{N-1} e^{j2\pi(k_0-k)m} \\
&= Ae^{j\varphi_0}\times\frac{1-e^{-j2\pi(k_0-k)}}{1-e^{-j2\pi(k_0-k)/N}}\times\frac{1-e^{j2\pi(k_0-k)}}{1-e^{j2\pi(k_0-k)/N}} \\
&= Ae^{j\varphi_0}\times\frac{e^{j\pi(k_0-k)}-e^{-j\pi(k_0-k)}}{e^{j\pi(k_0-k)/N}-e^{-j\pi(k_0-k)/N}}\times\frac{e^{-j\pi(k_0-k)}-e^{j\pi(k_0-k)}}{e^{-j\pi(k_0-k)/N}-e^{j\pi(k_0-k)/N}} \\
&= Ae^{j\varphi_0}\times\frac{\sin^2\left[\pi(k-k_0)\right]}{\sin^2\left[\pi(k-k_0)/\mathrm{N}\right]} \\
&= Ae^{j\varphi_0}\left|\frac{\sin\left[\pi(k-k_0)\right]}{\sin\left[\pi(k-k_0)/\mathrm{N}\right]}\right|^2
\end{aligned} \tag{5.13}$$

The result of (5.13) consists of two components, $Ae^{j\varphi_0}$ and (5.14):

$$\left|\frac{\sin(\pi(k-k_0))}{\sin(\pi(k-k_0)/N)}\right|^2 \tag{5.14}$$

where $Ae^{j\varphi_0}$ denotes the complex amplitude of signals, φ_0 is the initial phase of the signal. Because A and (5.14) are real numbers, an important characteristic of the APFFT algorithm can be derived, which is called the phase invariance. In other words, for a single frequency signal, any point on its APFFT spectrum represents its real, accurate phase, without any other compensation.

In previous analysis, we proved that after the DFT processing on the signal with rectangle windows, the result will be an added a linear phase shift $e^{j\pi(k_0-k)(1-\frac{1}{N})}$ to the actual phase. The precise phase of the signal can only be measured when the sampled points are an integral multiple of the signal period. The calibration of phase is a hard evaluate consuming much time. By using the APFFT algorithm, users can focus on analyzing the magnitude of the frequency spectrum. In the multi-frequency situation, although the phase will be affected by frequency leakages of surrounding signals, nevertheless the phase error reduced greatly due to the smaller leakage of APFFT algorithm compared to DFT algorithm. The component (5.14) is the square of the corresponding component in (5.4). The component in (5.4) is shifted DFT with a rectangle window. The no-window APFFT added a specific window to the original data, this window is the convolution of two rectangle windows, so we can obtain that the component (5.14) is the DFT result of convolution of two rectangle windows.

The component (5.14) and (5.4) are the main reasons for frequency leakage. Because of the square-root relationship, it can be learned that the spectrum leakage of APFFT is smaller than that of DFT (the main lobe is more obvious and the side lobe is smaller). This feature is a benefit for spectrum analysis, especially

in multi-frequencies and high dynamic range situations. Hence the APFFT algorithm can guarantee that the small signals will not be overwhelmed by large signals. It can clearly discriminate two nearby signals. Therefore, it shows advantages in measurement accuracy, especially for the magnitude and phase of the frequency spectrum.

The spectral leakage problem of the DFT algorithm can be improved by adding a window. Similarly, the no-window APFFT algorithm can become single or double window APFFT by adding windows. In the same condition, the APFFT applies double data than DFT to realize N point time-to-frequency transformation, which has smaller spectral leakage and phase invariance feature. Thus, APFFT has better performance in multi-frequency spectrum analysis.

The simulation in Matlab can clearly show the phase invariance of the APFFT algorithm. With factors $k_0 = 4.3$, $N = 50$, $A = 1$, $\varphi_0 = \pi/4$ in (5.13), the signal is transformed by 50 points APFFT algorithm. The resulted phase spectrum is shown in

Figure 5.9. We can see the phase results of APFFT are one constant values, which equal to theoretical values, even though the relationship between signal and sampling rate is far away from integral ratio.

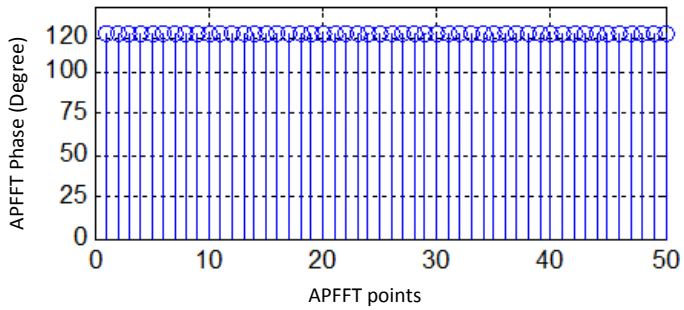

Figure 5.9 Phase invariance of APFFT for signal frequency signal

In the above signal, we add two frequency signals $k_1 = 10.3, k_2 = 15.3$, and initial phases are $\varphi_1 = \pi/3$, $\varphi_2 = \pi/2$ respectively. With a 50 points APFFT calculation, the transformed phase spectrum is shown in Figure 5.10.

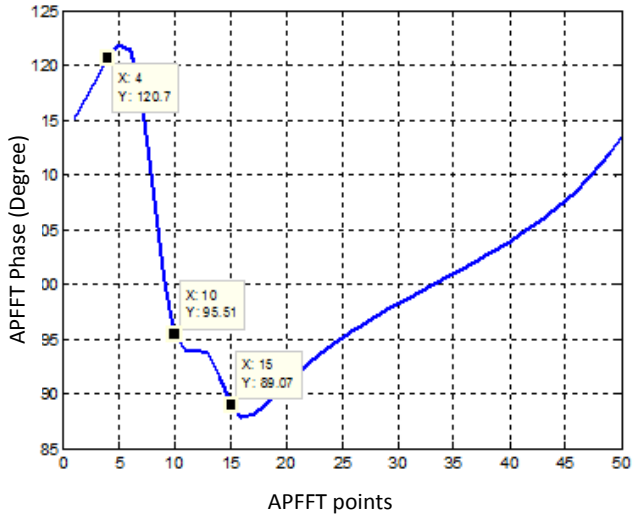

Figure 5.10 Phase invariance of APFFT for multi-frequency signal

Comparably, by 50 points FFT calculation, the resulted phase spectrum is shown in Figure 5.11.

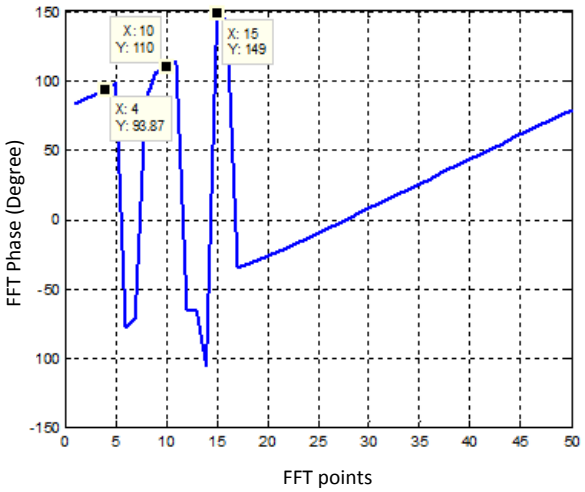

Figure 5.11 Phase variance of FFT for multi-frequency signal

Because the sampling frequency of FFT is not an integral multiple of the frequencies of signals, the leakage problem exists and affected the measurement precision. The results of two algorithms are listed in Table 5.1 below. It compared the phase values at the 4th point, the 10th point and 15th point of the resulted frequency spectrum.

Table 5.1 Comparison between APFFT and FFT in phase accuracy (no window)

	Phase at k=4.3	Phase at k=10.3	Phase at k=15.3
Real value	122.04°	96.12°	87.84°
APFFT	120.7°	95.51°	89.07°
FFT	93.87°	110°	149°

From the table, we can see that in APFFT, even without window, the calculated phases are close to the real phases. But the FFT algorithm introduced enormous phase errors up to 61.6° at frequency $k=15.3$ compared to the actual value. It shows the phase accuracy of un-calibrated FFT spectrum is unsatisfactory for measurement.

Another comparison is made between APFFT and FFT algorithm, both with window. Supposing a multi-frequency signal consists of five frequency components:

$$S = 2e^{j(10000\cdot\frac{2\pi}{N}n+\frac{1}{18}\pi)} + 2e^{j(20100\cdot\frac{2\pi}{N}n+\frac{1}{6}\pi)} + 2e^{j(30200\cdot\frac{2\pi}{N}n+\frac{5}{18}\pi)} + 2e^{j(40300\cdot\frac{2\pi}{N}n+\frac{7}{18}\pi)} + 2e^{j(50400\cdot\frac{2\pi}{N}n+\frac{1}{2}\pi)} \quad (5.15)$$

By using FFT and APFFT algorithm respectively, we derived the magnitude spectrums and phase spectrums in the frequency domain. In each algorithm, we applied Hanning windows. The FFT/APFFT point is 256 and the sampling rate is 400 kHz. In the results, the magnitude spectrums are normalized for better comparison. The simulated magnitude spectrums of FFT and APFFT are depicted in Figure 5.12 and Figure 5.13.

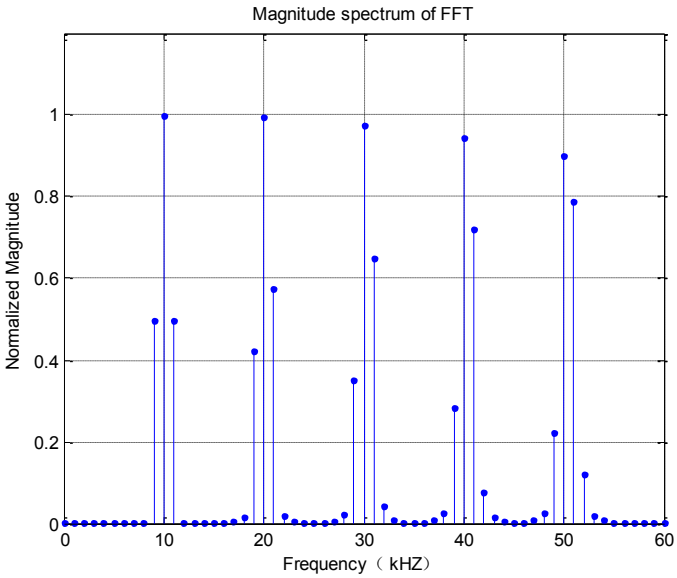

Figure 5.12 The magnitude spectrums of FFT (with Hanning window)

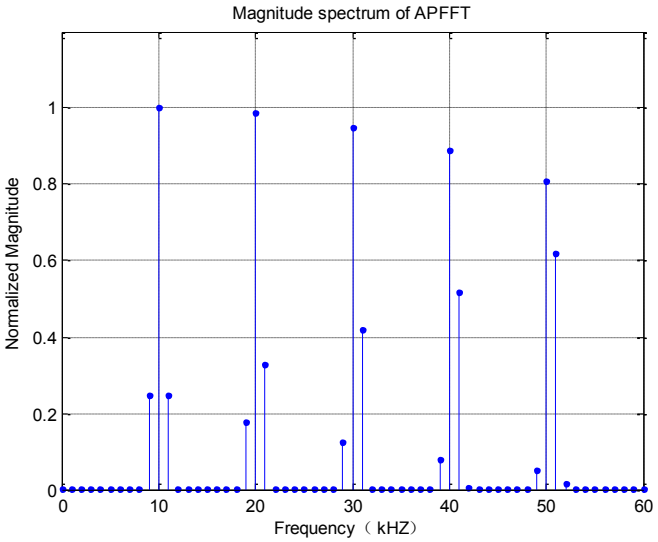

Figure 5.13 The magnitude spectrums of APFFT (with Hanning window)

From the magnitude spectrums of both algorithms, we can see the leakage of APFFT algorithm is obviously smaller than that of FFT algorithm. By adding Hanning window, the accuracy of the two algorithms are both improved. But the APFFT still has an advantage regarding the leakage problem.

Subsequently, the phase accuracy of each algorithm is simulated and analyzed. The resulting phase spectrums of FFT and APFFT are illustrated in Figure 5.14 and Figure 5.15.

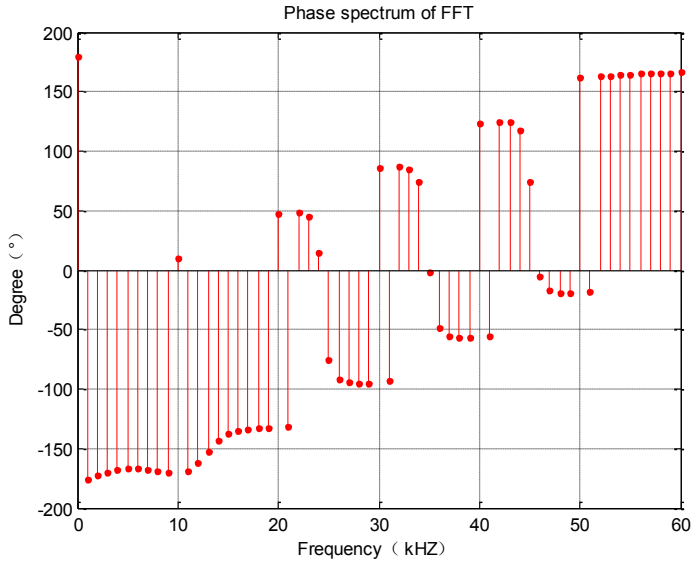

Figure 5.14 The phase spectrums of FFT (with Hanning window)

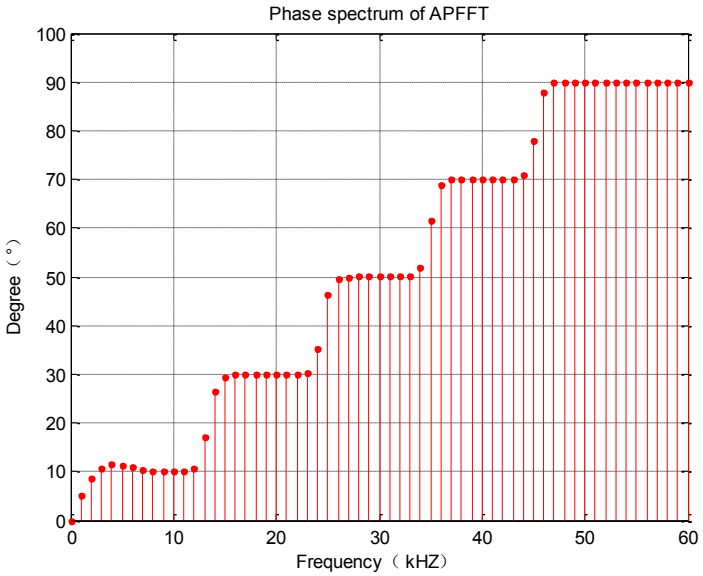

Figure 5.15 The phase spectrums of APFFT (with Hanning window)

The results clearly show the performances of phase accuracy of FFT and APFFT algorithm. We can see that the transformed phase of FFT has enormous fluctuation in the frequency domain. Whereas, the results from APFFT are stable and regular, which are close to the real situation. The detailed phases at five frequencies are listed in Table 5.2:

Table 5.2 Comparison between APFFT and FFT in phase accuracy(Hanning window)

	Phase at N=10kHz	Phase at N=20kHz	Phase at N=30kHz	Phase at N=40kHz	Phase at N=50kHz
Real phase	10	30	50	70	90
Phase by FFT	9.9945	47.9229	85.8487	123.7755	161.7097
Phase by APFFT	10.0000	30.0000	50.0000	70.0000	90.0000

Various windows on data may lead to different performances in phase accuracy. We have simulated the results of APFFT and FFT algorithm with various windows (the triangle window, Blackman window and Hamming window) to evaluate their effects. The results are showed in Figure 5.16 to Figure 5.18.

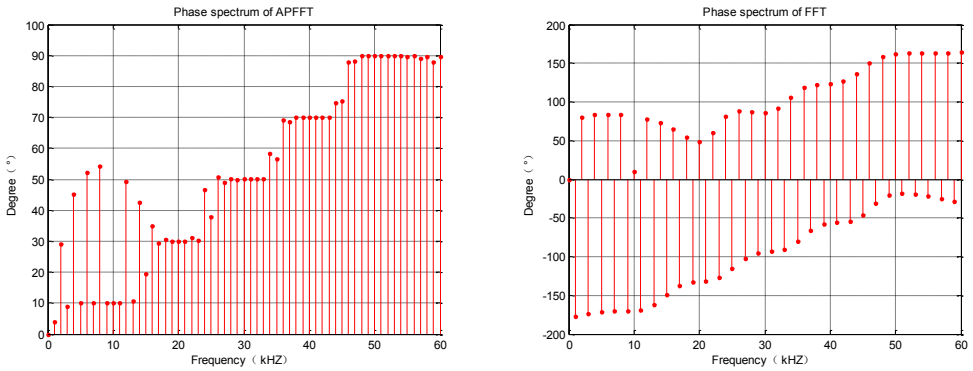

Figure 5.16 The phase spectrums of APFFT and FFT (with triangle window)

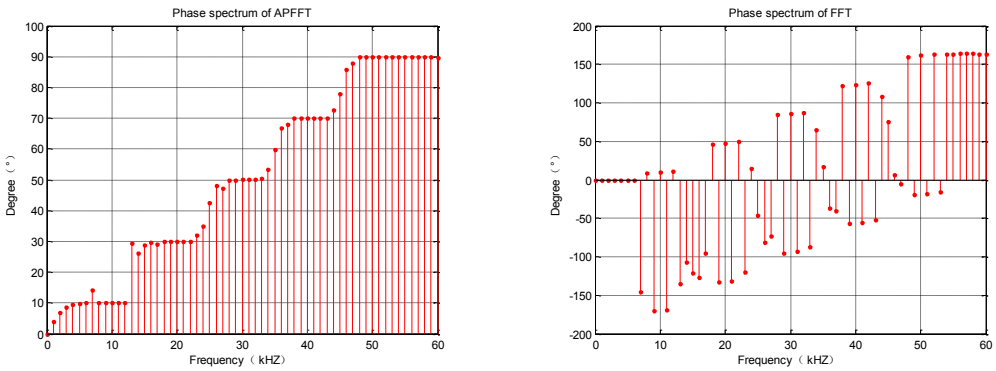

Figure 5.17 The phase spectrums of APFFT and FFT (with Blackman window)

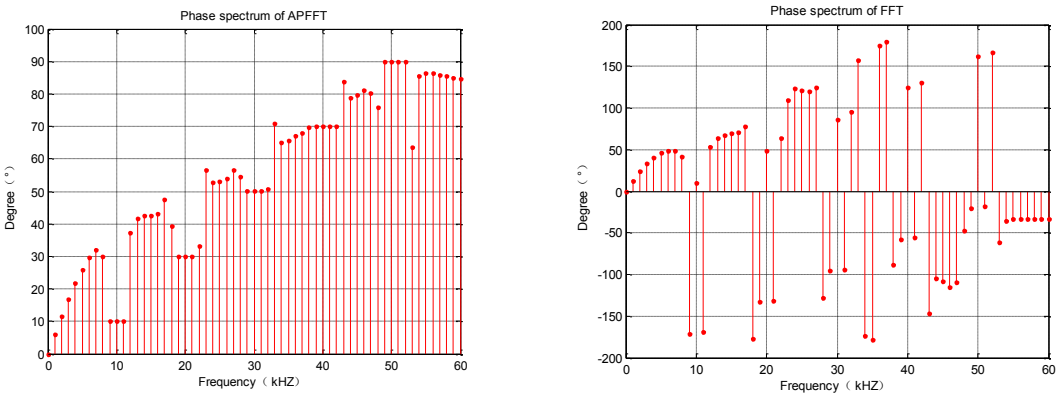

Figure 5.18 The phase spectrums of APFFT and FFT (with Hamming window)

From the simulations above, it can be revealed that with every window, all the phase accuracy of APFFT is better than that of FFT. In order to compare them in detail, the phase values in each frequency are listed in Table 5.3.

Table 5.3. The phase accuracy of APFFT and FFT (with different windows)

	Phase at N=10kHz	Phase at N=20kHz	Phase at N=30kHz	Phase at N=40kHz	Phase at N=50kHz
Real phase	10	30	50	70	90
Phase by FFT (with Blackman window)	9.9945	47.9229	85.8487	123.7755	161.7097
Phase by FFT(with Hamming window)	10.1023	48.0893	86.0762	124.0522	162.0151
Phase by FFT(with Triangular window)	10.0118	47.9569	85.8968	123.8162	161.6835
Phase by APFFT(with Blackman window)	10.0000	30.0000	50.0000	70.0000	90.0000
Phase by APFFT(with Hamming window)	10.0002	30.0003	50.0004	70.0002	89.9995
Phase by APFFT(with Triangular window)	10.0000	30.0000	50.0000	70.0000	90.0000

5.5 Comparison between APFFT and Digital Quadrature Demodulation

Digital Phase-Sensitive Demodulator (DPSD) are widely used in EIT system(He *et al.*, 2008). Digital quadrature demodulation (DQD) is a key method of

DPSD which performs well in single frequency EIT systems. DQD is based on the matched filter theory. The architecture of DQD can be illustrated in Figure 5.19 as follows:

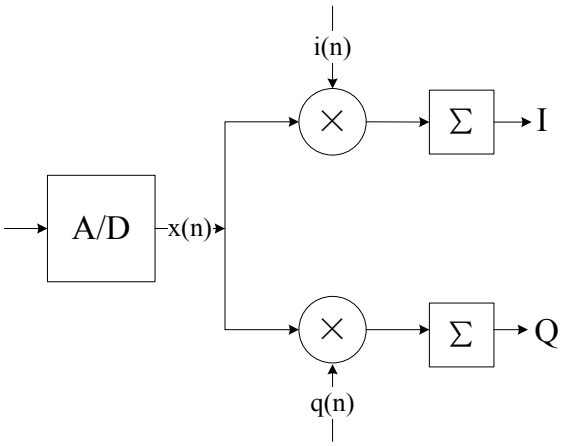

Figure 5.19 the architecture of digital quadrature demodulation.

Suppose N is the number of samples per ADC cycle. The sampling signal from ADC can be expressed by (5.16):

$$x(n) = V_m \cos\left(\frac{2\pi}{N} n + \varphi\right) \tag{5.16}$$

where $i(n)$ and $q(n)$ are in phase and quadrature phase signals with x(n) respectively:

$$i(n) = \cos\left(\frac{2\pi}{N} n\right) \tag{5.17}$$

$$q(n) = \sin\left(\frac{2\pi}{N} n\right) \tag{5.18}$$

I and *Q* are the in phase and quadrature phase output of the demodulator

$$\begin{aligned} I &= \sum_{n=0}^{N-1} i(n)x(n) = \sum_{n=0}^{N-1} \cos(\frac{2\pi}{N} n) V_m \sin(\frac{2\pi}{N} n + \varphi) \\ &= NV_m \frac{1}{2} \cos\varphi \end{aligned} \tag{5.19}$$

$$Q = \sum_{n=0}^{N-1} q(n)x(n) = \sum_{n=0}^{N-1} \sin(\frac{2\pi}{N}n)V_m \sin(\frac{2\pi}{N}n + \varphi) \\ = NV_m \frac{1}{2}\sin\varphi \tag{5.20}$$

The amplitude and phase of the signal is:

$$V_m = \sqrt{I^2 + Q^2} \tag{5.21}$$

$$\varphi = \arctan\frac{Q}{I} \tag{5.22}$$

It should be noticed that this method requires the sample frequency to be an integral multiple of the signal frequency. That means every cycle of the signal can be expressed in integral discrete points. This method requires a low-pass filter in each path. The advantages of the DQD method are significant. The signal processing path ensures perfect gain-matching between I and Q signals. All digital processing is easily matched for two signals. The concerns of gain balancing and analogue circuitry matching are obviated. Besides, the DC offsets and drifts on the signal will not affect the DQD. The quadrature phase shift is dependent upon the precise timing of the ADC.

The major weakness of DQD method is obvious. According to the DQD theory, this method is only adapted to single-frequency applications. In multi-frequency application, users need to use the frequency sweeping technique or build multiple DQD in parallel. For the frequency sweeping technique, the measurement speed is limited by sweeping speed; for the multiple DQD architecture, a large quantity of computational resources is required.

The basis of DQD is similar to the DFT algorithm. The DQD can be treated as a linear phase filter with a specific center frequency, and DFT is a filter group with uniformly-spaced center frequencies. The frequency of I and Q signals should be

strictly the same as the incoming signal, or it causes large errors in the demodulated amplitude and phase (similar to the spectral leakage introduced by non-integral period sampling in the DFT with rectangle windows.) .

Compared to the DQD method, APFFT algorithm can demodulate multiple signals at one time. There is no strict requirement on frequency of measured signals, which make it more flexible. The APFFT spectrum is a discrete spectrum. Therefore, if a frequency is located between two spectrum lines, errors exist in the measured amplitude and phase of the signal.

In the EIT system, the frequencies of the excitation signals are well-defined and dynamically adjusted by the signal source. Consequently, the values of signal frequencies and sample rate can be set accurately. In order to improve the measurement precision, the sample rate of the acquisition system and signal frequencies need to satisfy the equation (5.23)

$$\frac{f_s}{f_i} = k \times N,\ k < \frac{1}{2}(N-1) \tag{5.23}$$

where N is an integer, therefore the spectrum of signals can be rightly located in the k_{th} spectrum. Besides, the length of the incoming data from ADC should be 2N-1 points so that the pretreatment of the APFFT algorithm can be completed.

If the EIT system can satisfy the above two conditions, sampled data of the EIT system can be processed by the APFFT algorithm. The method can be implemented in either FPGA or DSP. It is also possible to process the sampled data on a computer.

In order to compare these two methods, a multi-frequency signal is defined:

$$\begin{aligned} V = & 4 \cdot \cos(1 \cdot 2\pi \cdot \frac{f_i}{f_s} \cdot n + \varphi_1) \\ & + 3 \cdot \cos(2 \cdot 2\pi \cdot \frac{f_i}{f_s} \cdot n + \varphi_2) \\ & + 2 \cdot \cos(3 \cdot 2\pi \cdot \frac{f_i}{f_s} \cdot n + \varphi_3) \\ & + 1 \cdot \cos(4 \cdot 2\pi \cdot \frac{f_i}{f_s} \cdot n + \varphi_4) \end{aligned} \tag{5.24}$$

In (5.24) we defined that the multi-frequency signal contains four frequencies (10 KHz, 20 KHz,30 KHz, 40 KHz), and the corresponding phases ($\varphi_1 \sim \varphi_4$) are 30°, 110°, 190°, 270°.

$$f_s = k \times f_i \times (N+1) \tag{5.25}$$

Where k is equal to 1.

The four frequencies are located at the 2nd, 3rd, 4th, 5th spectrum line of APFFT. In order to guarantee that the four spectrums can be displayed, the transform size of the FFT points N in APFFT should be 10 at least, and the total transform size of APFFT should satisfy 19 (2N-1) at least. In this condition, the lowest sample frequency is shown as (5.26)

$$f_s = f_i \times N = 100kHz \tag{5.26}$$

Firstly，65 points are sampled at a frequency of 320 KHz. APFFT is operated utilizing these points. The results are shown in Figure 5.20 and Figure 5.21 as follows:

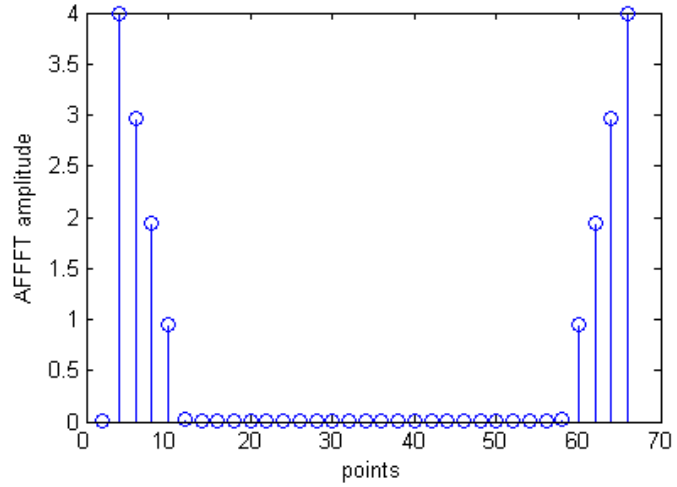

Figure 5.20 Amplitude spectrum of 65 points APFFT.

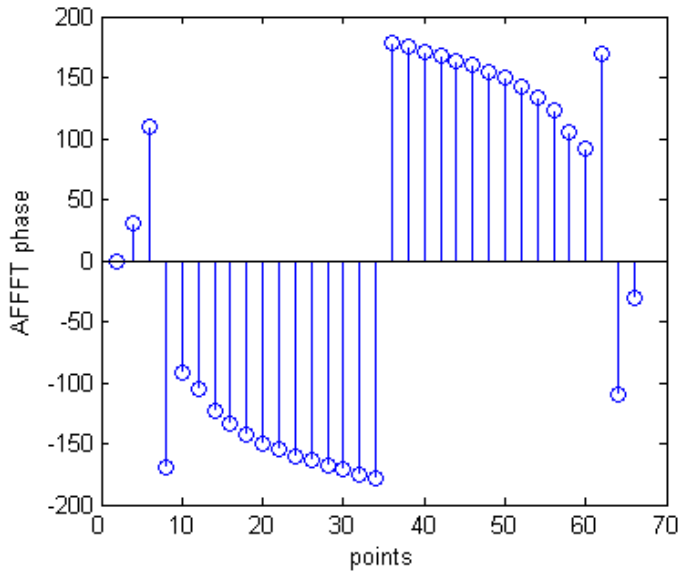

Figure 5.21 Phase spectrum of 65 points APFFT.

From the graphs above, we can see that the 2nd to 5th spectrums correspond with different testing frequencies. The Table 5.4 lists the detailed values of the corresponding amplitudes, phases, and their relative errors:

Table 5.4 Detailed values of the amplitudes, phases and relative errors

	Component 1	Component 2	Component 3	Component 4
Real amplitude	4	3	2	1
Amplitude after APFFT	3.98	2.96	1.94	0.95
Relative error of Amplitude	0.5%	1.3%	3.0%	5.0%
Real phase	30°	110°	190°	270°
Phase after APFFT	30.13°	110.23°	-170.04°(189.96°)	-91.30°(268.70°)
Relative error of phases	0.13°	0.23°	0.04°	1.30°

The testing results above infer that the APFFT has high performance on extracting amplitudes and phases. Furthermore, the precision of amplitudes and phases increases with the decreasing of signal frequency. This means that the precision of amplitudes and phases of APFFT improves with the sampled points per cycle.

Similarly, the mixed signal is sampled at frequency of 10×N KHz. The 10 KHz part of signal is demodulated with DQD and APFFT demodulator respectively. The transform sizes of the two methods are both 2N-1 ranged from 19 to 301. The errors of amplitude and phase are shown in Figure 5.22 and Figure 5.23 as follows

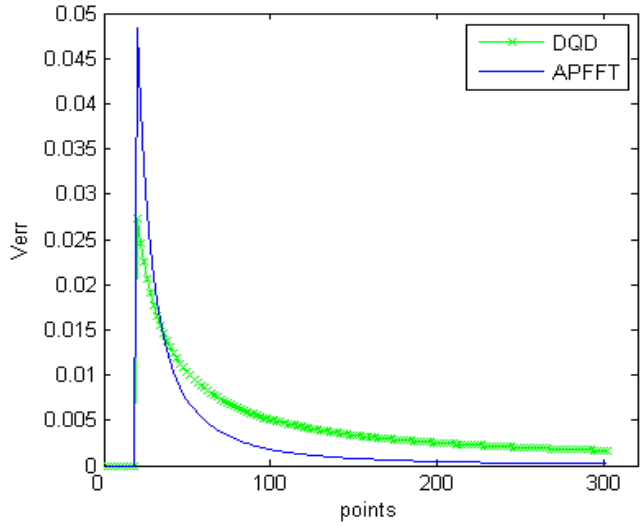

Figure 5.22 Errors of amplitude of 10 KHZ signal.

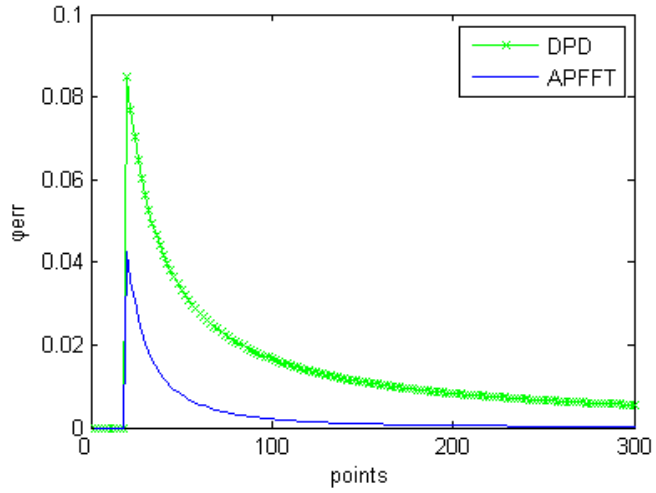

Figure 5.23 Errors of phase of 10 KHZ signal.

From the Figure 5.22 and Figure 5.23, it shows that the accuracy, especially in phase measurements, APFFT is much better than DQD at the same sample frequency and transform size. It proved that the main advantage of the APFFT method is phase accuracy. Also the advantage in amplitude measurement of APFFT becomes evident when using a longer transform size.

With the same transform size, the increasing of signal frequency negatively affects the errors of APFFT. We compared the performance of the two methods of processing the 40 KHz component of the signal. The result is shown in Figure 5.24 and Figure 5.25.

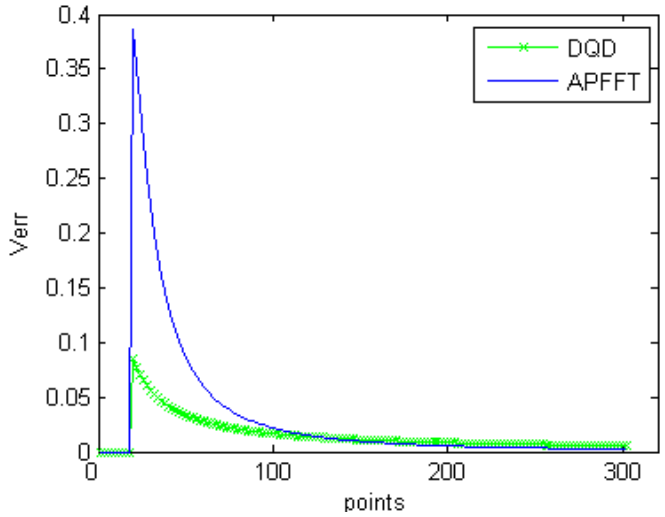

Figure 5.24 Errors of amplitude of 40 KHZ signal.

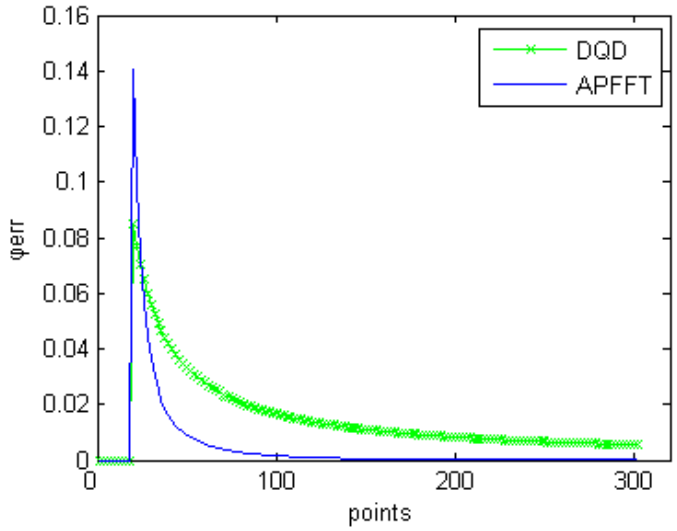

Figure 5.25 Errors of phase of 40 KHZ signal.

From Figure 5.24 and Figure 5.25, it infers that the amplitude performance of DQD keeps stable when the signal frequency increases 4 times and the amplitude accuracy of APFFT decreased in the same transform size. However, when the transform size reaches around 140, the amplitude performance of APFFT exceeds that of the DQD. If the transform size is long enough, the phase error of APFFT remains at a lower level compared with the DQD results.

Finally the complexities of the two methods are compared. For a 2N-1 point APFFT, the major calculation process is performing N-point FFT. For a N-point FFT

operation, $N + N\log_2 N$ is the total number of complex multiplications and additions. For an N step DQD, 2×N complex multiplications and 2(N-1) additions are required. The signals described in (5.24) are demodulated using two methods. The processing time of every 2N−1 points are shown in Figure 5.26 as follows:

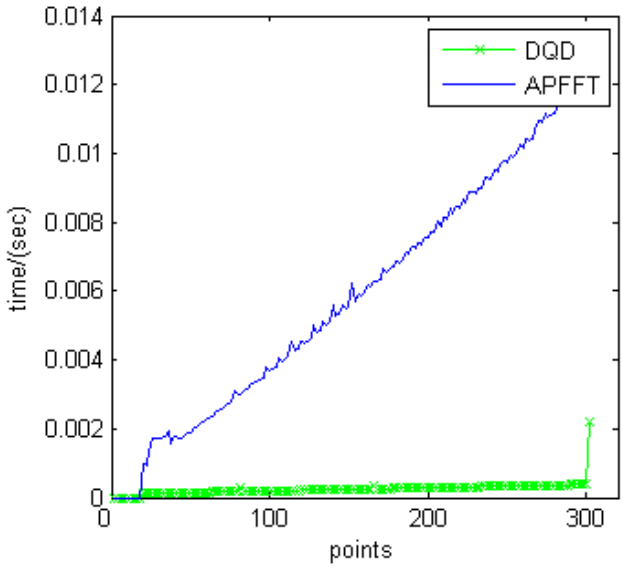

Figure 5.26 The processing time of every 2N−1 points.

From the comparison of the time consumption of two methods in Figure 5.26, we can see that the complexity of DQD is better than APFFT, which means the APFFT cost more computing resources than DQD. Therefore, the APFFT algorithm should be implemented on a high-speed computer, DSP or FPGA to guarantee its performance. Compared to the conventional method DQD, the advantage of APFFT demodulator is that APFFT demodulator has a better accuracy performance if the sampled data is long enough. As the data length increases, the merits of APFFT demodulator become more obvious.

The simulation results reveal that the accuracy of a multi-frequency EIT system can be improved significantly by increasing the sampling time slightly when an APFFT demodulator applied. The disadvantages of APFFT demodulator are high computational complexity and high resource consumption. However, if the accuracy performance is the first consideration, APFFT demodulator is a good

choice. Nevertheless, if the calculation resource is limited, the DQD should be the first choice.

5.6 CONCLUSION

In multi-frequency bioimpedance measurements, the time cost of measurement can be significantly reduced by using multi-frequency excitation technique, which acquires more impendence on different frequencies in each measurement. However, when using multi-frequency excitation, the signal demodulator also needs to be improved for handling a multi-frequency signal.

In this chapter, we applied a new algorithm-All phase Fast Fourier Transform (APFFT) in bio-impedance analysis applications. From the simulation results, it can be revealed that the phase accuracy of APFFT is better than that of FFT. Compared to the commonly used method, digital quadrature demodulation in EIT application, APFFT is much better in accuracy, especially in phase measurements, when using the same sampling rate and transform size. The disadvantages of APFFT demodulator are computational complexity and high resource consumption.

Chapter 6. TESTING AND EVALUATION OF SYSTEM

In order to evaluate the performances of the realized bio-impedance analysis system, the function validation and performance testing are indispensable procedures. In our system, the practical performances not only depend on the hardware circuitry, but also depend on the algorithms. In this chapter, the testing schemes and results are presented in the following sections.

6.1 TESTING OF HARDWARE PERFORMANCE

The critical hardware of our system consists of two excitation signal sources (a reference source and a feedback source in auto balancing bridge circuitry), a null detector and multi-channel ADCs, where the signal source circuitry is based on DAC circuits, and others are based on ADC circuits. In the aspect of ADC and DAC based circuits, some related terms of performance are introduced at first.

6.1.1 TESTING PARAMETERS

Signal-to-noise ratio (SNR): The ratio of the power in the single-frequency input signal to the power of the remaining energy in the specified bandwidth, not including DC or the harmonics. Because the highest frequency available in the ADC output is half of the sample rate, the specified bandwidth of the noise considered in the SNR calculation for an ADC is restricted to a half of the ADC sample rate. SNR can be expressed as (6.1):

$$SNR = \frac{P_{signal}}{P_{noise}} \tag{6.1}$$

where P_{signal} is the total power of the signal, P_{noise} is the total power of noise. In a logarithmic coordinates, SNR can be expressed as (6.2):

$$SNR_{dB} = 10\log_{10}\left(\frac{P_{signal}}{P_{noise}}\right) = P_{signal,dB} - P_{noise,dB} \tag{6.2}$$

where $P_{signal,dB}$ and $P_{noise,dB}$ are decibels of the total power of the signal and of the noise respectively.

Spurious Free Dynamic Range (SFDR): SFDR is the difference between the level of the desired output signal and the value of the highest amplitude output frequency that is not present in the input, normally expressed in decibels:

$$SFDR_{dB} = 10\log_{10}\left(\frac{P_{signal}}{Max(P_{spur})}\right) = P_{signal,dB} - Max(P_{spur,dB}) \tag{6.3}$$

Where the P_{spur} denotes the power of all the spurs except output signal, $P_{spur,dB}$ is its decibel form. Two units are commonly used to describe the SFDR, which are dBfs and dBc. The difference between them can be illustrated in Figure 6.1:

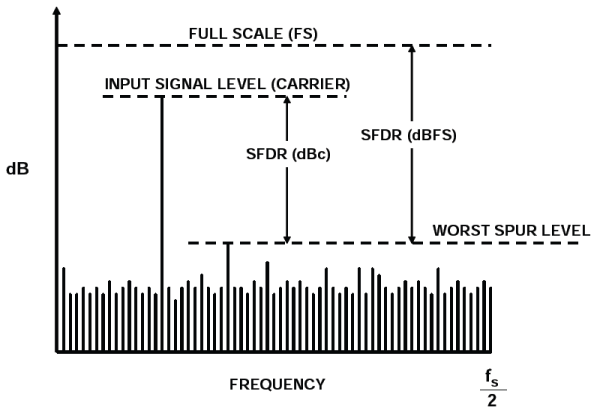

Figure 6.1 The graph to explain the principle of SFDR, dBFS, dBc

Total Harmonic Distortion (THD): The ratio of the power in the specified number of distortion products to the power in the fundamental frequency and

relates the RMS sum of the amplitudes of the harmonics to the amplitude of the fundamental, which can be expressed as (6.4)：

$$THD = \frac{P_{h2} + P_{h3} + \ldots + P_{hn}}{P_{signal}} = \frac{\sum_{n=2}^{n} P_{hn}}{P_{signal}} \tag{6.4}$$

where P_{hn} denotes the power of the n_{th} harmonics, which can be expressed in decibels：

$$THD_{dB} = 10\log_{10}\left(\frac{\sum_{n=2}^{n} P_{hn}}{P_{signal}}\right) \tag{6.5}$$

Signal-to-Noise-and-Distortion (SINAD): The ratio of the RMS signal amplitude to the mean value of the root-sum-square of all other spectral components, including harmonics, but excluding DC component. It is a good indication of the overall dynamic performance of an ADC because it includes all components which make up noise and distortion. SINAD is often plotted for various input amplitudes and frequencies. For a given input frequency and amplitude, SINAD is equal to THD + N, provided the bandwidth for the noise measurement is the same for both (the Nyquist bandwidth). SINAD can be expressed as (6.6):

$$SINAD_{dB} = 10\log_{10}\left(\frac{P_{signal}}{P_{noise} + \sum_{n=2}^{n} P_{hn}}\right) \tag{6.6}$$

where P_{hn} denotes the power of the n_{th} harmonics, normally using the first five orders in calculation.

6.1.2 *TESTING OF STIMULATION SIGNAL SOURCES*

In order to test the performance of the reference source and the feedback source, the testing scheme is proposed and shown in Figure 6.2. In this testing setup, the waveform generated by the under test source is sent to a spectrum analyzer (N9010A, Agilent, USA). The measured spectrum is used to calculate the SNR, THD, SINAD and SFDR.

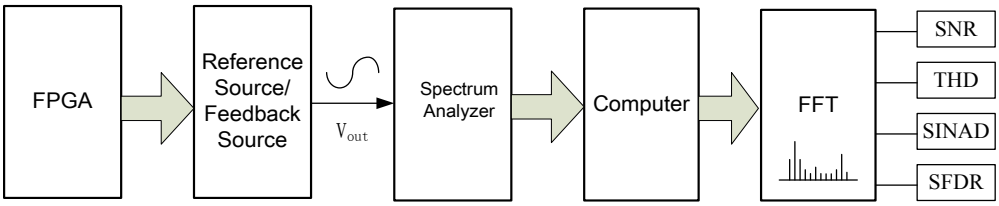

Figure 6.2 The testing setup of stimulation signal sources

In the testing, the amplitude of the signal is 1 Vpp, and the selected test frequencies are 10 points covering from 10KHz to 10MHz. The test results are shown in Figure 6.3 to Figure 6.6.

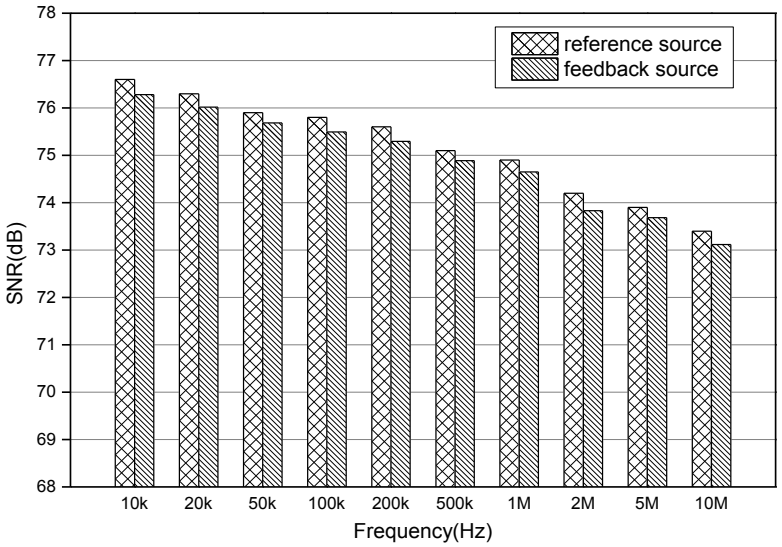

Figure 6.3 SNR of stimulation signal sources

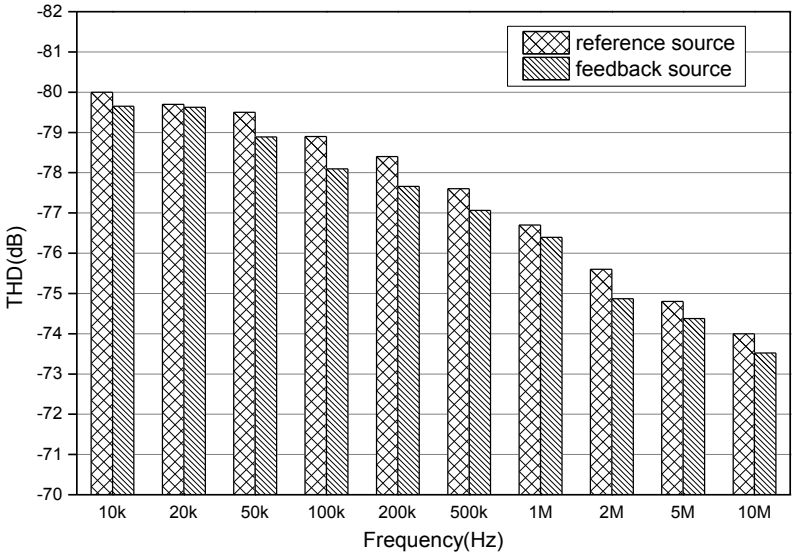

Figure 6.4 THD of stimulation signal sources

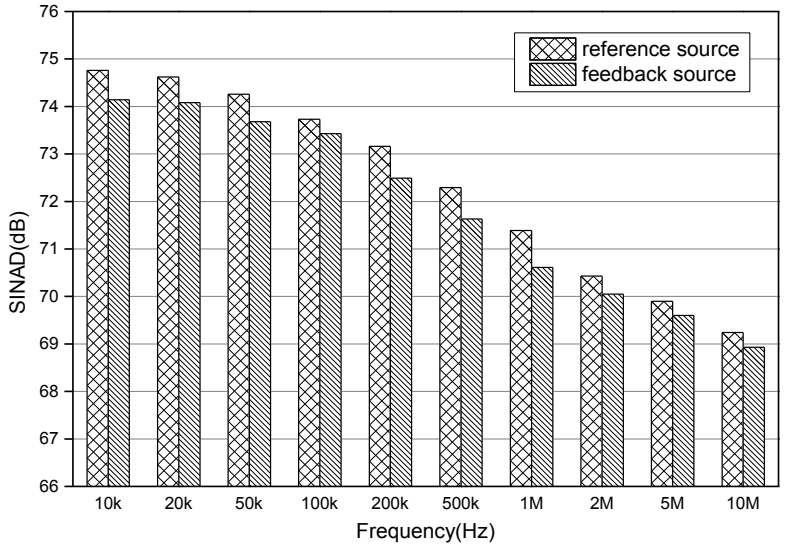

Figure 6.5 SINAD of stimulation signal sources

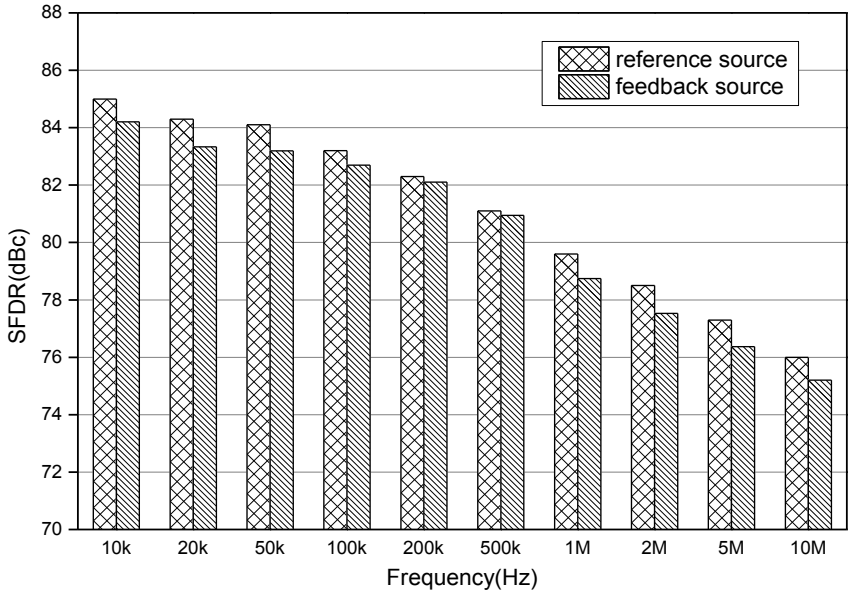

Figure 6.6 SFDR of stimulation signal sources

From the above four graphs, it can be seen that the slight degradation of each performance with the frequency increasing. It is mainly caused by the performance of the DACs. Because the circuitry of reference and feedback sources are similar mostly, the results from them are close as well. The performance of the feedback source is a bit lower than that of the reference source because the variable gain amplifier on the output's path introduced more noise.

6.1.3 TESTING OF NULL DETECTOR

The major dynamic performances of the null detector are similar to that of the signal source. The test setup of the null-detector is shown in Figure 6.7 below.

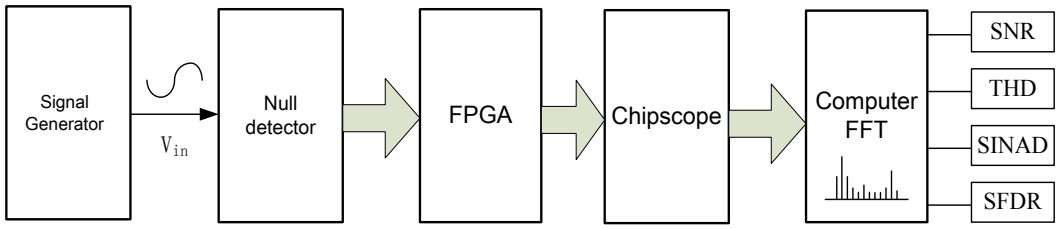

Figure 6.7 The testing setup of the null detector

In this architecture, the waveform is obtained from a commercial signal generator (N5171B, Agilent, USA). The null detector measures the waveform and sends the results to the FPGA. The data can be collected by on-chip Chipscope software and analyzed by FFT algorithm. The FFT spectrum is used to calculate the SNR, THD, SINAD, SFDR values of the null detector. In the testing, the amplitude of the reference signal is 1Vpp, and the selected testing frequencies are at 10 points from 10KHz to 10MHz. The sampling rate is 100Msps. The test results are shown in Figure 6.8 to Figure 6.11.

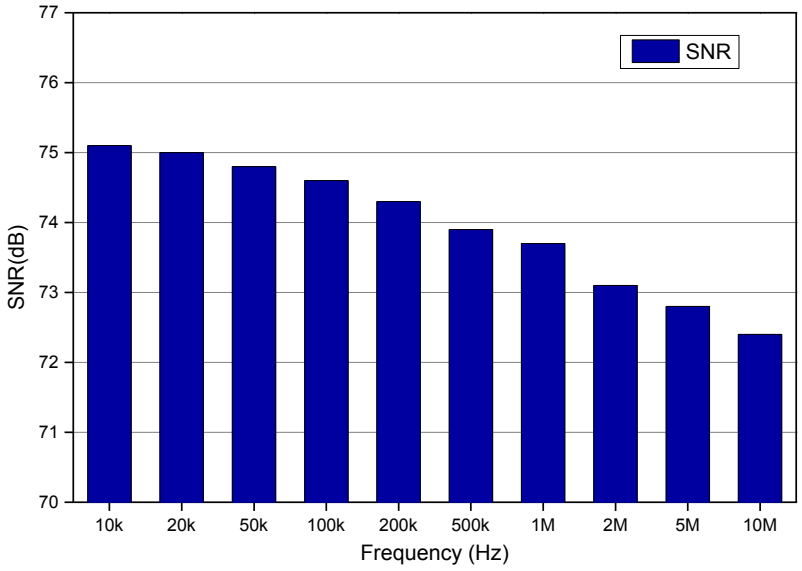

Figure 6.8 SNR of the null detector.

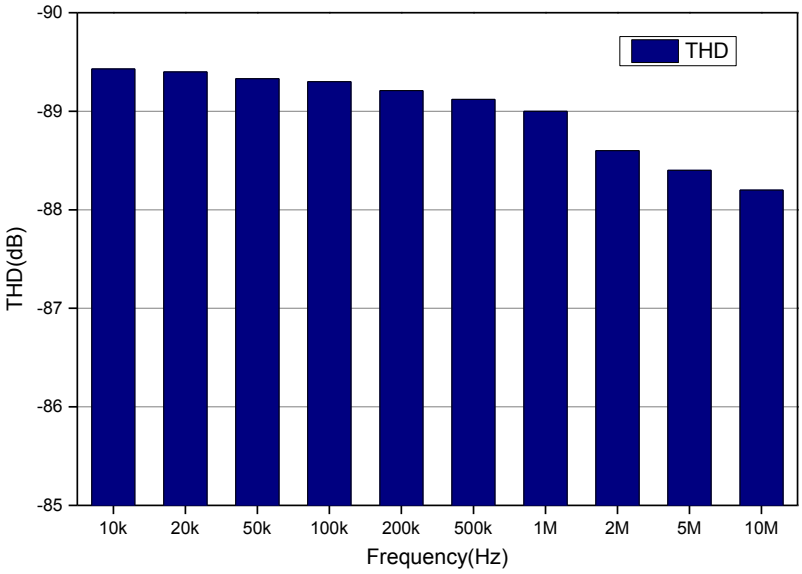

Figure 6.9 THD of the null detector.

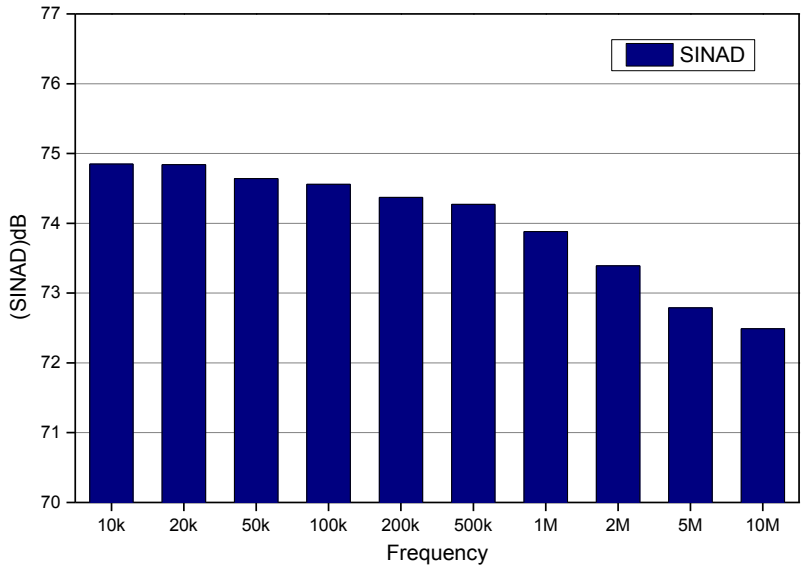

Figure 6.10 SINAD of the null detector.

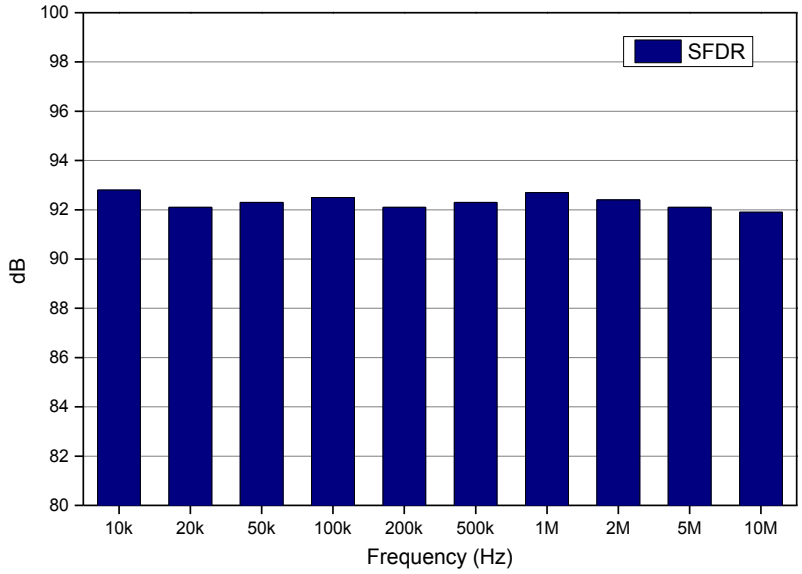

Figure 6.11 SFDR of the null detector.

From the graphs above, we can see that the SNR, THD and SINAD performance has slightly decreased with the increasing of the frequency of the input signal. The main reason is that the phase noise (or jitter) has a larger effect upon signals with high input slew rates. Because the reference signal is generated by an external signal generator, the THD and SFDR performances are better than that of the designed source circuitry. For that reason, the values of THD and SFDR haven't degraded obviously (1dB maximum). At 10MHz, the SNR of the null detector is up to 72 dB. The gaps between the labelled specification (80dB) and our test results are possibly caused by the error introduced by the front-end conditioning circuit and PCB layout.

6.1.4 TESTING OF MULTI-CHANNEL ADC

In multi-channel applications, the performance need to be considered is not only the SNR of each channel, but also the uniformity of every channel. In order to test the uniformity of every ADC channel in our system, we designed the testing scheme as

Figure 6.12 shown. The reference signal V_{ref} is generated by a commercial signal generator (N5171B, Agilent, USA). Multiple ADCs acquire the waveform, and then sends the results to the FPGA. The data are collected by Chipscope and analyzed by the APFFT algorithm for extracting phases and amplitudes. In the testing, the amplitude of the reference signal is identical to previous testing, which is 1Vpp, and the selected testing frequencies are at 10 points covers from 10kHz to 10MHz. The sampling rates of ADCs are 100Msps. The test results are shown in Figure 6.13 to Figure 6.14.

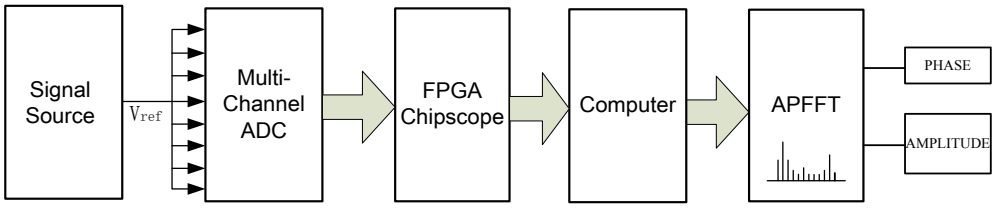

Figure 6.12 The testing set-up of multi-channel ADC circuit

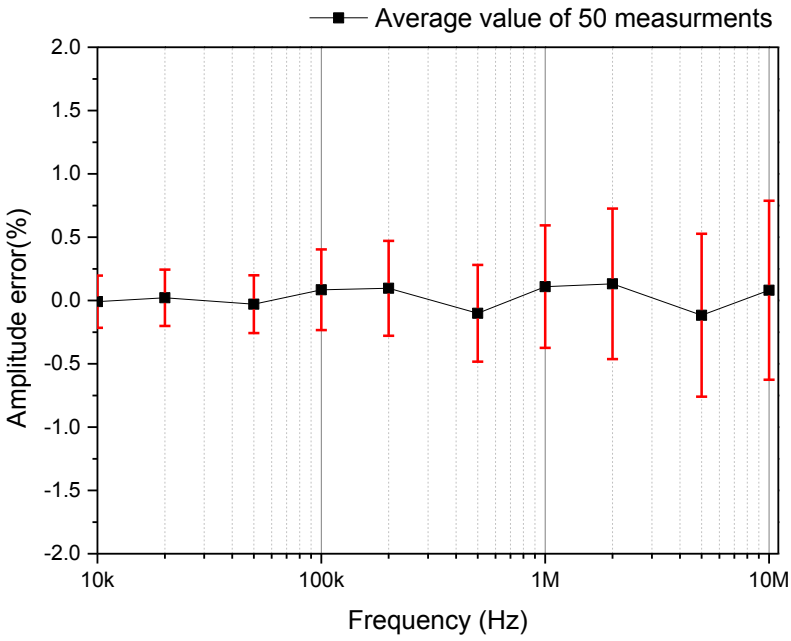

Figure 6.13 Testing results of amplitude uniformity of multi-channel ADC

The performance of amplitude uniformity is an important characteristic of multi-channel system. Figure 6.13 shows the test results including the average

amplitude error of eight channels and the average deviation between every channel. The graph reveals that the maximal deviation between each channel is less than 1%. This phenomenon results from hardware differences between signal conditioning circuits and ADC devices. In Table 6.1, the detailed results are presented.

Table 6.1 Testing results of amplitude uniformity of multi-channel ADC

Frequency (Hz)	Average amplitude error of multi-channels (%)	Deviation between multi-channels (%)
10k	-0.009	0.205
20k	0.021	0.222
50k	-0.029	0.228
100k	0.084	0.318
200k	0.096	0.374
500k	-0.101	0.382
1M	0.109	0.483
2M	0.131	0.594
5M	-0.116	0.643
10M	0.081	0.706

Phase uniformity represents the phase variation among each channel, which is another critical performance of a multi-channel system. Figure 6.14 shows the test results, including the average phase error of eight channels and the maximal deviation among all channels. The graph reveals that the maximal phase deviation between each channel is less than 1.5%.

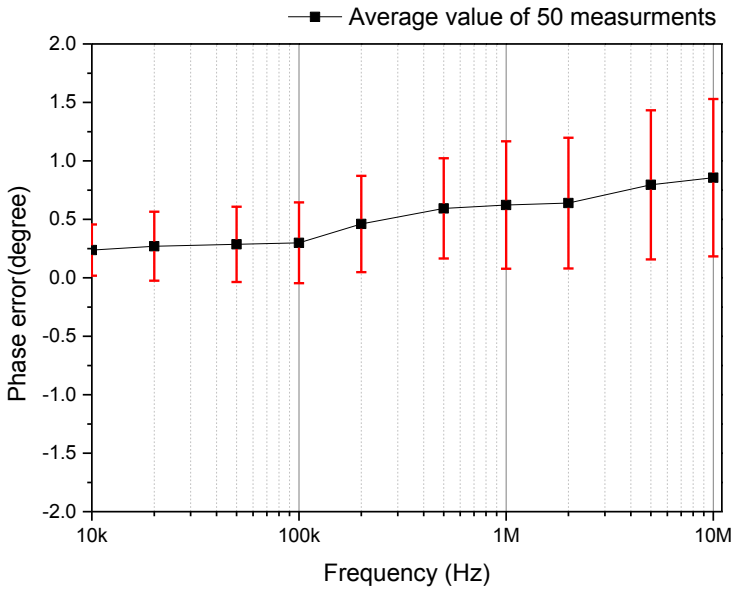

Figure 6.14 Testing results of phase uniformity of multi-channel ADC

In Table 6.2, the detailed results of phase uniformity testing are listed. The APFFT algorithm provided a precise phase resolution of measurements. With the frequency increasing, the deviation and phase error are getting larger, because of the jitter of the ADC sampling clock has a larger effect upon signals with higher input slew rates. The deviations are majorly caused by the differences in board layout and the skew rate of amplifiers and ADC circuits.

Table 6.2 Testing results of phase uniformity of multi-channel ADC

Frequency (Hz)	Average phase error of multi-channels (degree)	Deviation between multi-channels (degree)
10k	0.237	0.218
20k	0.270	0.295
50k	0.286	0.321
100k	0.299	0.345
200k	0.460	0.411
500k	0.593	0.428
1M	0.622	0.545
2M	0.638	0.558
5M	0.795	0.637
10M	0.856	0.673

SNR is a critical parameter of an ADC-based acquisition system. The test procedure is similar to the previous testing. The results are shown in Figure 6.15. From the graph, it can be seen that the average SNR approximately achieve 72 dB to 75 dB at different frequencies. With the increasing of input signal's frequency, the total SNRs of the each channel are slightly degraded due to the jitter of sampling clock.

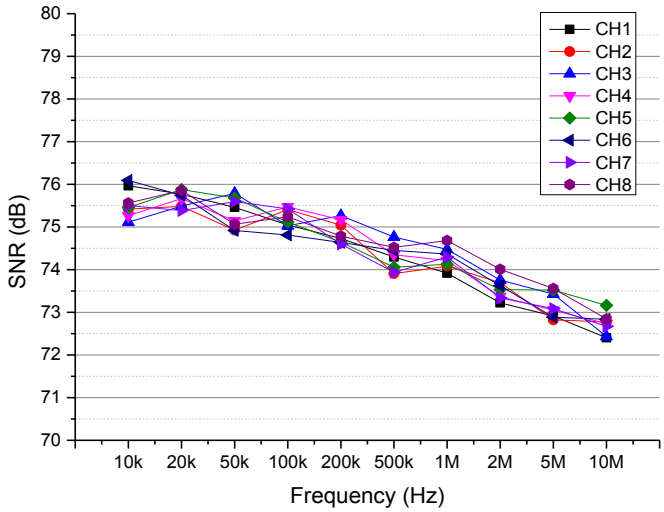

Figure 6.15 SNR test results of multi-channels ADC

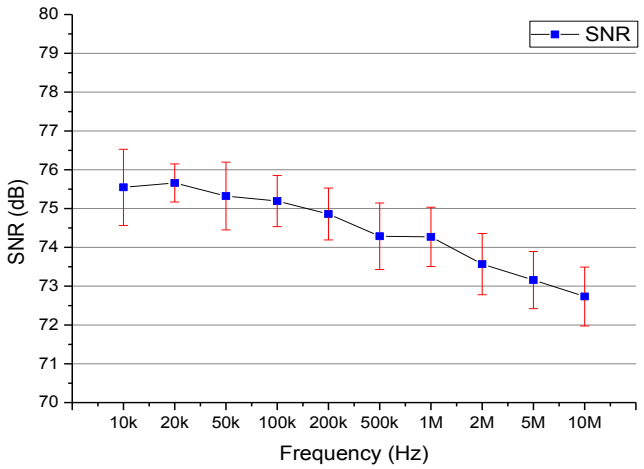

Figure 6.16 The average SNR of all channels and deviation among eight channels.

Figure 6.16 shows the average SNR of every channel and deviation among eight channels. The red bars denote the deviation, which revealed that the maximum difference among each channel is less than 2dB. These differences are caused by the inconsistency of the hardware and layout of the circuit board, which can only be compensated by post processing.

6.2 EVALUATION OF SYSTEM PERFORMANCES

6.2.1 MEASUREMENT ACCURACY

In order to verify the accuracy of the system, a reference impedance has been measured at different frequencies. An equivalent circuit model is built to simulate the impedance characteristic of cell suspension for testing. In this equivalent model, the resistor R_b represents the resistance of the buffer solution, the capacitor C_m represents the capacitance of cell membranes, R_m represents the cell membrane resistance and R_i represents the resistance of intracellular media. The parameters of circuit components are based on our previous work which measured bioimpedance of early-stage human breast cancer cell line MCF-7 (CLSCell Lines Service, Germany) (Guofeng *et al.*, 2012). The circuit model is composed of high precision (0.1%) passive resistors and capacitor as Figure 6.17 shows.

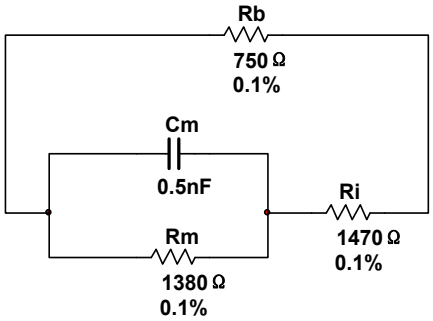

Figure 6.17**.** Equivalent circuit model of the cell suspension.

The measurements are performed within a frequency span from 1 kHz to 10 MHz. The results obtained by our system are shown in Table 6.3. Each measured

result is the mean value of 10 measurements. The results show that our system has good magnitude accuracy (error <0.2%) and phase accuracy (error <0.1%) in this frequency range.

Table 6.3 Magnitude and phase accuracy in different frequencies

Frequency [a]	Theoretical value [b]	Measured value [b]	Deviation	
			Magnitude	Phase
1k	593.7 ∠-0.03	593.3∠-0.05	0.07%	0.01%
10k	593.7 ∠-0.25	593.2∠-0.19	0.08%	0.01%
100k	587.8 ∠-2.36	587.3 ∠-2.31	0.09%	0.01%
1M	509.5 ∠-3.58	508.9 ∠-3.49	0.11%	0.03%
10M	496.8 ∠-0.42	494.9 ∠-0.62	0.18%	0.06%

[a] The units of frequencies are Hz.

[b] The units of theoretical values and measured values are Ohm(magnitude) and degree(phase).

Another testing is made to verify the measurement accuracy under different impedance magnitudes. In the biological field, the magnitude requirements of bioimpedance measurements are different due to diverse methods and characteristic of samples. The range of magnitude covers from tens (Chauveau *et al.*, 1999) to Megas (Mercanzini *et al.*, 2009) Ohm. In order to evaluate our system in a broader magnitude range, pure resistors, with values from 100 Ohm to 100 MOhm are used as an object under test in this testing. The testing frequency is 1MHz. The results are shown in Table 6.4.

Table 6.4 Comparison of accuracy in different impedance magnitudes.

|Z|[a]	Measured value (Ohm)	Deviation
10	11.17	11.70%
100	101.21	1.21%
1k	998.21	0.18%
10k	10.02k	0.20%
100k	100.26k	0.26%
1M	1.02M	0.20%
10M	9.83 M	1.70%
100M	116.82 M	16.82%

[a]|Z| are the labelled values of under test resistors (0.1% precision), the unit is Ohm.

The data in Table 6.4 reveal that our system has good accuracy (0.18%~1.70%) in the range from 1k Ohm to 10 MOhm. If the magnitude of impedance is too small (<100 Ohm) or too large (＞10 MOhm)，the errors will increase significantly. The possible reasons for these phenomena are: (1) in the situation of low impedance, the impedances of connectors and connection wires cannot be totally eliminated by calibration, and the slight errors lead to a relatively large deviation from the theoretical results; (2) in the situation of large impedance, the parasitic parameters (capacitance and inductance) in the system will cause the signal distortion and limit the bandwidth of analogue path, which increased the measurement error.

6.2.2 MEASUREMENT SPEED

The measurement speed has been tested at different frequencies from 10KHz to 10MHz. The equivalent circuit model above has been measured by our system with different bridge balancing algorithms (LMS-based and FBLMS-based). The time cost of each measurement is plotted in

Figure 6.18. From the test results, we can see that the LMS-based algorithm has higher speed in single measurements. Because of the complexity of its architecture, the FBLMS-based algorithm costs more time in bridge balancing, which increases its measurement time. However, when a multi-tone signal applied, the average measurement time consumption of the FBLMS-based method can be reduced to 20% (5 frequencies in per measurement), which makes it become the fastest method. The graph also demonstrates that the time cost of measurement increased with frequency. It results from the decreased convergence rate in the bridge balancing process. When frequency is increasing, the bridge costs longer time to become balanced, thus the measurement time is increased.

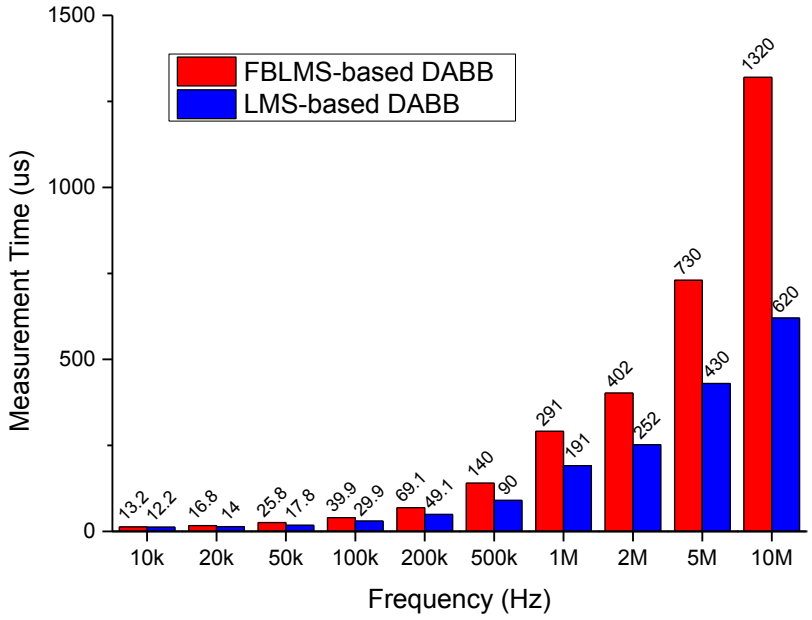

Figure 6.18 Comparisions of the time consumption for once measurement

Table 6.5 Time consumption of different method

	1 frequency	5 frequencies	10 frequencies
FBLMS-based DABB	1.3 ms	1.3ms	2.6 ms
LMS-based DABB	0.6 ms	3 ms	6 ms
Impedance analyzer (4294A, Agilent, USA)	>3 ms	>15 ms	>30 ms
Lock-in Amplifier (SR830, Stanford Research Systems, USA)	>40 ms	>200 ms	>400 ms

In Table 6.5, the time costs of different bioimpedance measurement methods are compared. From the results, it can be seen that the FBLMS-based DABB method has the best performance in multi-frequency measurement and the LMS-based DABB method has advantages in single-frequency condition. The FBLMS-based DABB method is over 10 times faster than a traditional impedance analyzer

(4294A, Agilent, USA) and 150 times faster than Lock-in Amplifier (SR830, Stanford Research Systems, Inc., USA) in multi-frequency situation such as EIT applications. When multiple channels work in parallel, the overall speed of the system can be further improved.

6.2.3 *MEASUREMENT REPEATABILITY*

The repeatability represents the deviation and fluctuation of results in multiple measurements. It is a very important parameter for a measurement instrument. It is also considered as the foundation for ensuring the measurement accuracy. The factors affect the repeatability including the drift of electronic components aging or exterior environment (temperature, humidity, vibration) and other related changes. In order to evaluate the stability of the system, we have measured a constant reference impedance 50 times at four frequencies (10KHz，100KHz，1MHz，10MHz). The errors of magnitudes and phases can be calculated as follows:

$$M_{e(n)}(\%) = 100 \cdot (M_n - \frac{\sum_{i=1}^{50} M_i}{50}) \tag{6.7}$$

$$P_{e(n)} = P_n - \frac{\sum_{i=1}^{50} P_i}{50} \tag{6.8}$$

where M_n and P_n denotes the n_{th} measured magnitude and phase of impedance respectively. Using this value to subtract the average value of fifty's measurement results, we derived the magnitude error $M_{e(n)}$ and $P_{e(n)}$ phase error of the n_{th} measurement. The measurement results are plotted in scatter graphs as Figure 6.19 to Figure 6.22 shown.

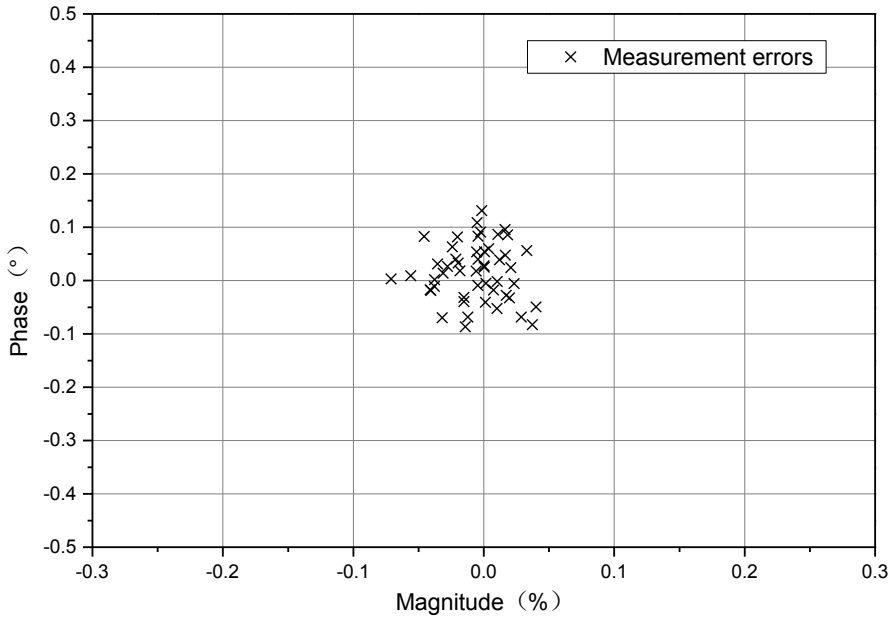

Figure 6.19 Repeated errors of measurement results at 10KHz

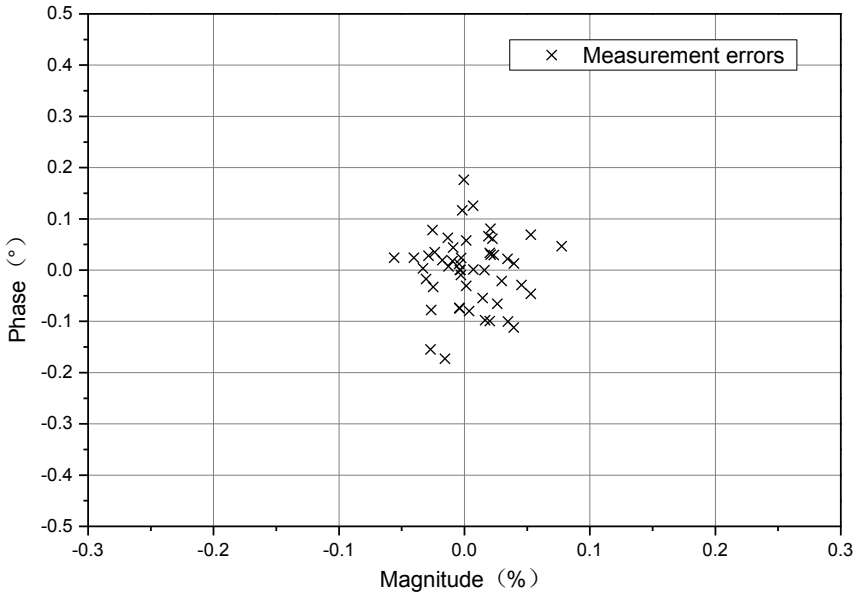

Figure 6.20 Repeated errors of measurement results at 100KHz

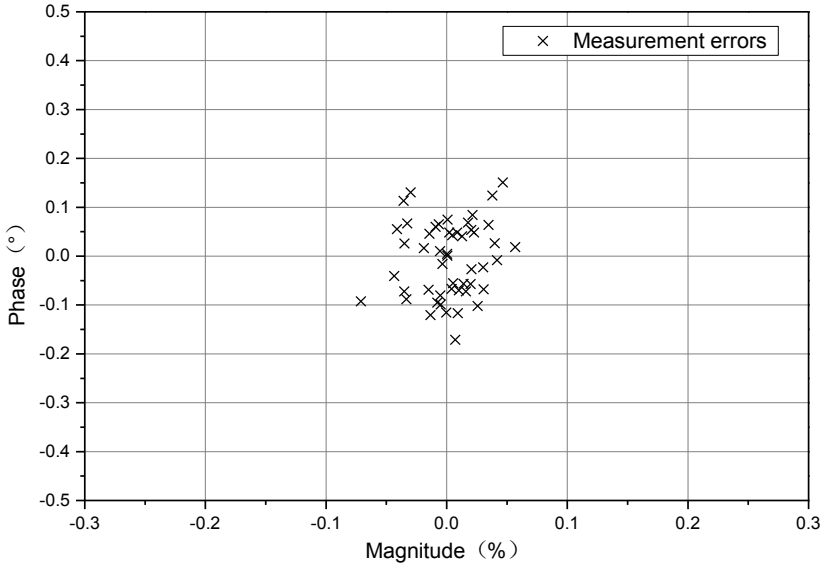

Figure 6.21 Repeated errors of measurement results at 1MHz

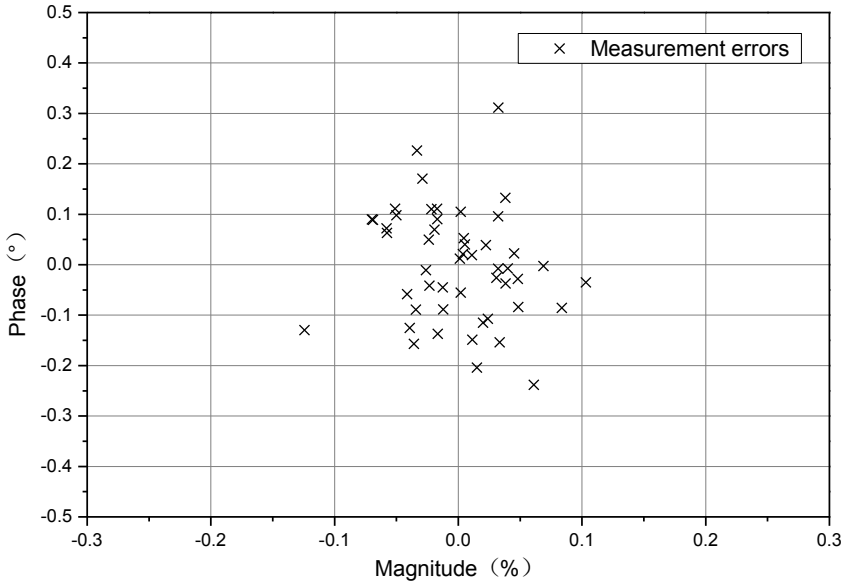

Figure 6.22 Repeated errors of measurement results at 10MHz

From the testing results above, the measurement repeatability of the system is maintained at 0.1% (in magnitude) and 0.2° (in phase). The repeatability performance is slightly degraded with increasing frequency. However, the overall performance of measurement repeatability has achieved a satisfy level.

6.2.4 *BIOLOGICAL EXPERIMENT*

The developed system is used for the biological experiment to verify its practical performance. A commercial impedance analyzer (Agilent 4294A) based on the traditional AABB technique is used as a reference for comparison. The 4294A has an accuracy of 0.08% (typical) and a frequency range 10Hz~110MHz. In this experiment, breast tissue cell suspensions are measured by our system and 4294A. Human breast tissue cell line MCF-10A (American Type Culture Collection, USA) were cultured in DMEM/F12 media (Invitrogen, UK) supplemented with 10% heat-inactivated fetal bovine serum, 100 IU/mL penicillin, 100 µg/mL streptomycin, 2 mmol/L L-glutamine (Invitrogen, UK), 20 ng/mL epidermal growth factor (Invitrogen, UK), 500 ng/mL hydrocortisone (Sigma, UK), 100 ng/mL cholera toxin (Sigma, UK) and 10 µg/mL bovine insulin (Sigma, UK). The cells were kept in an incubator at 37°C with 5% CO_2.

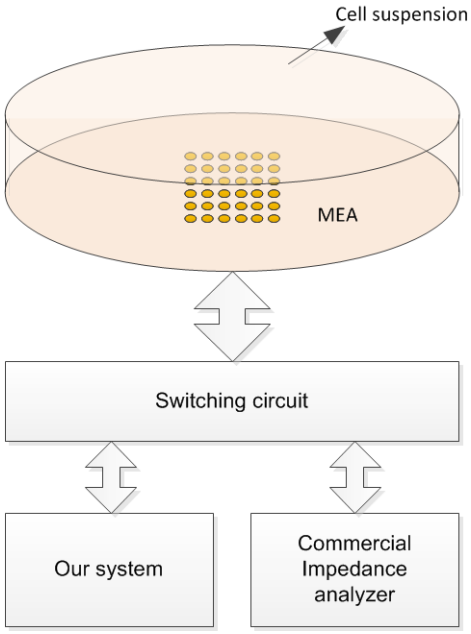

Figure 6.23 The test setup for biological experiment

For the impedance measurement, prepared cell suspensions were contained in the MEA-integrated culture dish, which connected to two systems via a switching circuit respectively as shown in Figure 6.23 shown. The frequency range of the measurement is from 10kHz to 10MHz with 50 points. The measurement

results of our system and 4294A are presented in Figure 6.24 and Figure 6.26. The deviations in magnitude and phase between the two systems are depicted in Figure 6.25 and Figure 6.27 respectively.

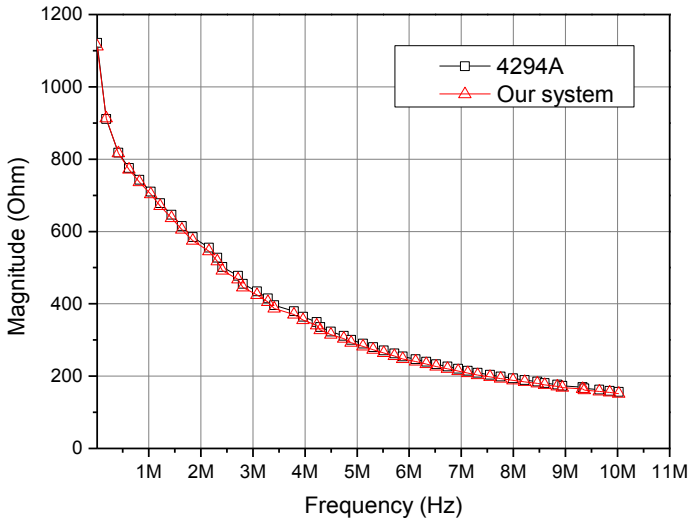

Figure 6.24 The measurement results from 4294A and our system (magnitude)

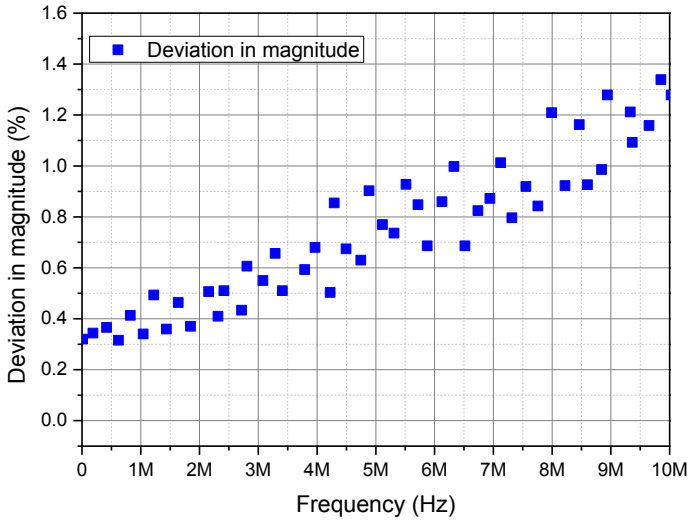

Figure 6.25 The magnitude deviation between our system and 4294A

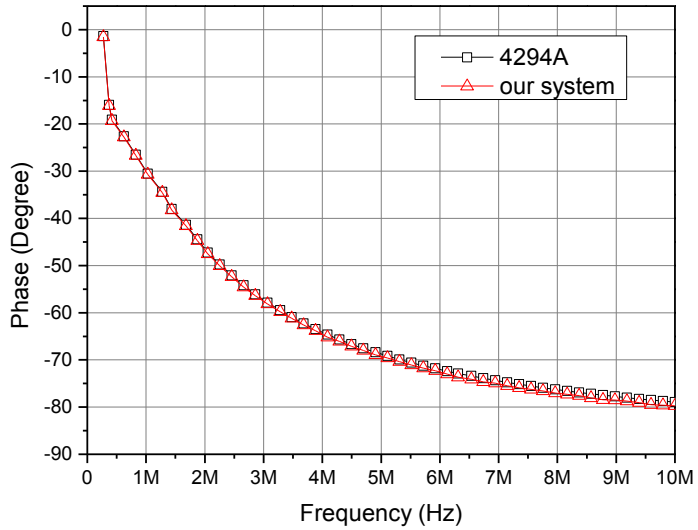

Figure 6.26 The measurement results from 4294A and our system (phase)

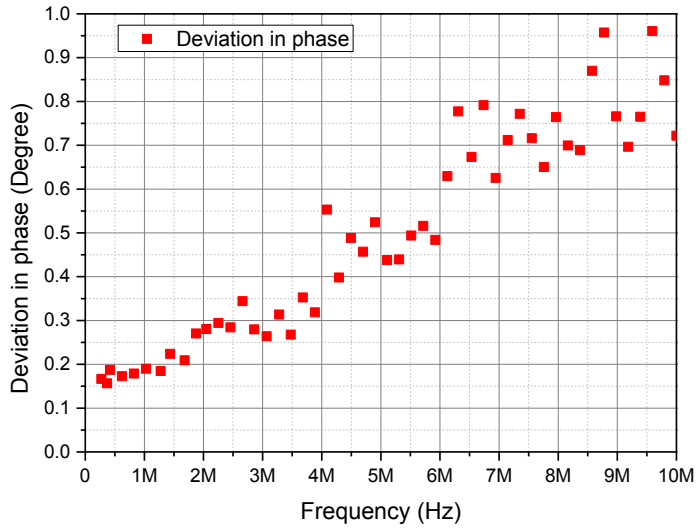

Figure 6.27 The phase deviation between our system and 4294A

From the graphs, it can be found that the results obtained by our system very close to the results by 4294A. The curves in Figure 6.25 and Figure 6.27 show that the deviations between our system and 4294A are less than 1.5% in magnitude and 1 degree in phase within the frequency range 10kHz to 10MHz. The comparison reveals that our system achieved a comparable accuracy as the traditional equipment in the practical biological experiments.

6.3 CONCLUSION

In this chapter, the evaluation process and results of our developed system are presented in detail. The performances of the main circuits of our system are tested firstly, which consists of SNR, THD, SINAD and SFDR. The test results reveal that the realized system hardware of system achieves the desired performance.

Subsequently, the performances of the overall system which including measurement accuracy, speed and repeatability are tested. In the accuracy test, an equivalent circuit model is built to simulate the impedance characteristics of the cell suspension for testing. The results reveal that our system has good accuracy (0.18%~1.70%) in the range from 100 Ohm to 10 MOhm. In the speed test, the equivalent circuit model has been measured by our system with different bridge balancing algorithms (LMS-based and FBLMS-based). The test results show that the LMS-based DABB method has higher speed in single frequency measurement and the FBLMS-based method has the advantage in a multi-frequency situation. The FBLMS-based DABB method is over 10 times faster than traditional impedance analyzer (4294A, Agilent, USA) and 150 times faster than Lock-in Amplifier (SR830, Stanford Research Systems, Inc., USA) in the multi-frequency situation such as EIT applications. In repeatability test, the errors of magnitudes and phases of 50 measurements are presented. It shows that the repeated deviation of the system is maintained in 0.1% in magnitude and 0.2° in phase, which means the overall performance of measurement stability has achieved a satisfactory level.

Furthermore, we compared our system with the commercial impedance analyzer based on the traditional AABB method (Agilent 4294A) in practical biological experiment. The comparison results show that our system achieved a comparable accuracy to the traditional equipment in the practical biological

experiments. The deviations between our system and 4294A are less than 1.5% in magnitude and 1 degree in phase within the frequency range 10kHz to 10MHz.

Chapter 7. CONCLUSIONS

7.1 ACHIEVEMENTS

The cell impedance analysis technique is a label-free, non-invasive method, which simplifies sample preparation and allows applications requiring unmodified cell retrieval. Unlike the traditional analysis methods that use fluorescence, radioisotope, luminescence, or light absorption, impedance-based methods directly measure the cellular impedance without labeling. The non-invasive nature of the measurement makes this technology suitable when further analysis of the target sample is required, and makes the overall analysis process simple.

However, traditional impedance measurement methods suffer from various problems for extracting cellular impedance information. Cellular impedance is more sensitive to external impacts and relatively changes are fast and acute. In order to measure the real-time changes of cellular impedance accurately, the measurement approaches have to achieve relatively higher speed corresponding to cellular activities. Moreover, the broader bandwidth of the measurement method is required for discovering the cellular impedance over a higher frequency range. Therefore, a high speed, wide bandwidth and highly accurate method is a key factor in realizing a real-time cellular impedance analysis system.

The method described in this thesis proposed an improved architecture and techniques for extracting precise cellular impedance in real-time over awide bandwidth. A cellular impedance measurement system is implemented, which includes an improved speed and bandwidth compared to its successor and compared to the state-of-the-art.

Chapter 1 gives an introduction to the general knowledge about cellular impedance. The origin and development of cellular impedance measurements and cell impedance imaging techniques are introduced briefly. In addition, recent progress and applications of cell impedance analysis are reviewed.

Chapter 2 gives an introduction to the common impedance measurement techniques and electrical impedance tomography (EIT) technique. The cell structure and its biological properties are introduced firstly. Several commonly used impedance measurement approaches including lock-in amplifiers and impedance analyzers are presented. The principle and the major deficiencies of these two methods are introduced in detail. Thesis also summarized the previously reported cell impedance analysis experiments and their configurations. In addition, the principle of the EIT technique and the architecture of the EIT system are introduced. Finally the current challenges in cellular impedance measurements and imaging are delineated.

Chapter 3 describes the hardware design of the proposed system in detail. The working principle of the system is introduced. The system consists of five main parts: a microelectrode array (MEA), a stimulation circuit, a sensing circuit, a multi-function card and a PXI-E computer. The stimulation circuits are used for generating a wideband signal to excite the cells under test. The circuit is designed based on digital auto balancing bridge (DABB) method, which improved from the traditional analog balancing bridge method. Its features are high-speed, compact and low-cost compared to the traditional measurement approaches. The sensing circuit consists of eight differential channels, which allows the user to simultaneously measure signals on any 16 electrodes (or 8 pairs) on the MEA. The multi-function card is a highly integrated instrument for data acquisition, waveform generation and system control functions in our application.

Chapter 4 describes a novel bioimpedance measurement method based on the digital auto balancing bridge method, which is developed from the traditional analogue auto balancing bridge circuitry for impedance measurement. The bridge balancing algorithm is the core of the DABB method. The thesis describes the principle of LMS-based bridge balancing algorithm and the implementation in FPGA. The CORDIC algorithm is applied for generating a reference signal and a feedback signal. In our system, the CORDIC algorithm is implemented by an IP core in FPGA, that saves lots of storage resources. However, the standard LMS algorithm can only be balanced at one frequency, which limits its speed in multi-frequency applications. A new DABB method based on the fast block LMS algorithm is designed for multi-frequency measurements, which can process multi-frequency signals in the frequency domain at one time. Therefore, the bridge can be balanced even in the multiple frequencies situation. The test results prove that the FBLMS based DABB method has advantages in stable convergence in multi-frequency applications. With a little increase in time cost, the FBLMS based method can measure more frequencies than standard LMS based method at one time. It significantly improved the total measurement speed of our system.

Chapter 5 describes a novel algorithm-All Phase Fast Fourier Transform (APFFT) which is suitable for post-processing of impedance measurement results in the multi-frequency situation. Compared with the classical algorithm Fast Fourier Transform (FFT), APFFT reduces spectral leakage caused by truncation error. It has excellent performance in suppressing spectral leakage and the property of phase invariance. Another merit of APFFT is that the phases calculated by APFFT need not to be adjusted, and are not affected by the frequency offset. In the aspect of post-processing of multi-frequency signal, performance of APFFT and FFT is compared. Simulation results show that the APFFT algorithm has better accuracy for extracting magnitude and phase from the measured signal. APFFT is also compared with the Digital Phase-Sensitive Demodulator (DPSD), which is a

widely used method in the EIT application. The simulation results indicate that the performance of a multi-frequency EIT system can also be improved by applying an APFFT demodulator.

Chapter 6 presents the evaluation process and results of our developed system in detail. The performances of the main circuits of our system are tested firstly, which consists of SNR, THD, SINAD and SFDR. The test results reveal that the realized hardware of the system achieved the desired performance. Subsequently, the performances of the overall system which including measurement accuracy, speed and repeatability are evaluated. The results of the accuracy test reveal that our system has good accuracy (0.18%~1.70%) in the range from 100 Ohm to 10M Ohm. In the speed test, the LMS-based DABB method exhibits higher speed in single frequency measurement and FBLMS-based method has the advantage in the multi-frequency situation. The FBLMS-based DABB method is over 10 times faster than commercial impedance analyzer and 150 times faster than commercial lock-in amplifier in multi-frequency applications. The repeated deviation of the system is maintained 0.1% in magnitude and 0.2° in phase, which means the system has achieved a satisfactory repeatability. Furthermore, our system is compared with a commercial impedance analyzer (Agilent 4294A) in a practical biological experiment. The comparison results show that our system achieved a comparable accuracy as the commercial instrument in the practical biological experiments. The deviations between our system and 4294A are less than 1.5% in magnitude and 1 degree in phase within the frequency range 10 kHz to 10MHz.

7.2 SUGGESTIONS FOR FUTURE WORK

Based on the presented achievements and developments in this work, the suggestions for future research can be summarized as follows:

1. The presented system realized high-speed measurement by DABB method, however, the performance of the DABB algorithm is limited to the performance of digital devices. When the frequency of the signal is increasing, the requirement of the sampling rate of the ADC and converting rate of the DAC rises up as well. That's the reason why high performance impedance measurement instruments keep using analogue methods. A possible solution is using some sampling algorithm such like equivalent sampling or random sampling to reduce the requirements of device

2. The bridge architecture applied in our system is adjusted by LMS-based or FBLMS-based auto balancing algorithm, which requires a convergence process to balance the bridge. When the frequency of signal is increasing, the time cost of convergence gets longer and the stability of the bridge degraded. Therefore, further research must be conducted for accelerating the bridge balancing process with higher stability. Non-iterative algorithms or other improved adaptive algorithms may be used to enhance the performance of the measurement speed in the future.

3. The major goal of our work is developing a high-performance impedance measurement platform for cell analysis. There are too many issues that need to be considered in practical biological experiments. The convenience, the volume and the cost-efficiency of our system could be further improved. Therefore, further biological validation is necessary for improving our system.

4. The APFFT algorithm shows good accuracy in extracting magnitude and phase information from signals. Nevertheless, it spends more calculation resources and takes a long time for signal processing. Currently we realized it on computer via software, thus it is only suitable for post-processing of signals. In order to

reduce the processing time of the system, this algorithm could be implemented in high-speed FPGA or DSP devices in future.

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