University of Sussex

Development of Microfabricated Ion Traps for Scalable Microwave Quantum Technology

Bjoern Lekitsch

Submitted for the degree of Doctor of Philosophy
University of Sussex, Brighton, United Kingdom.
November 2013

Declaration

I hereby declare that this thesis has not been and will not be submitted in whole or in part to another University for the award of any other degree.

Signature:

Bjoern Lekitsch

UNIVERSITY OF SUSSEX

Bjoern Lekitsch, Doctor of Philosophy

Development of Microfabricated Ion Traps for Scalable Microwave Quantum Technology

Abstract

Microfabricated ion traps are an important tool in the development of scalable quantum systems. Tremendous advancements towards an ion quantum computer were made in the past decade and most requirements for a quantum computer have been fulfilled in individual experiments. Incorporating all essential capabilities in a fully scalable system will require the further advancement of established quantum information technologies and development of new trap fabrication techniques.

In my thesis I will discuss the theoretical background and experimental setup required for the operation of ion traps. Measurement of the important ion trap heating rate was performed in the setup and I will discuss the results in more detail.

I will give a review of microfabrication processes used for the fabrication of traps, outlining advantages, disadvantages and issues inherent to the processes. Following the review I will present my work on a concept for a scalable ion trap quantum system based on microwave quantum gates and shuttling through X-junctions.

Many of the required building blocks, including ion trap structures with current-carrying wires intended to create strong magnetic field gradients for microwave gates were investigated further. A novel fabrication process was developed to combine current-carrying wires with advanced multilayered ion trap structures. Several trap designs intended for proof of principle experiments of high fidelity microwave gates, advanced detection techniques and shuttling between electrically disconnected ion traps will be presented. Also the electrode geometry of an optimized X-junction design with strongly suppressed rf barrier height will be presented.

Further, I developed several modifications for the experimental setup to extend the existing capabilities. A plasma source capable of performing in-situ cleans of the trap electrode surfaces, which has been demonstrated to dramatically reduce the heating rate in ion traps, was incorporated. I will also present a vacuum system modification designed to cool ion traps with current-carrying wires and transport the generated heat out of the vacuum system. In addition a novel low-noise, high-speed, multichannel voltage control system was developed by me. The device can be used in future experiments to precisely shuttle ions from one trapping zone to another and also to shuttle ions through ion trap junctions.

Lastly I will outline the process optimization and microfabrication of my ion trap designs. A novel fabrication process which makes use of the extremely high thermal conductivity of diamond substrates and combines it with thick copper tracks embedded in the substrate was developed. Large currents will be passed through the wires creating a strong and controllable magnetic field gradient. Ion trap designs with isolated electrodes connected via buried wires can be placed on top of the current-carrying wires, allowing the most advanced electrode designs to be fabricated with current-carrying wires.

Acknowledgements

General Acknowledgements

First and foremost, I wish to express my gratitude to my supervisor, Winfried Hensinger, for giving me the opportunity to work in the Sussex IQT group. His enthusiasm and dedication for our research greatly inspired me. I will never forget the many interesting discussions we had over the years.

I would also like to thank my second supervisor Barry Garraway for all the guidance and help he offered me. Many thanks also go to Micheal Kraft and Ibrahim Sari for supporting my work at the Southampton nanofabrication centre.

I want to thank my colleagues Altaf Nizamani, Robin Sterling, James Siverns, Marcus Hughes, James McLoughlin who setup the experiment before I joined the group and introduced me to the world of ion trapping. Sebastian Weidt, who joined the research group shortly after me, was of great help during our first challenging experiments and has always been extremely helpful. Marcus Hughes, for spending countless hours with me working on the experiment and our microfabrication paper. Kimberly Lake, who was always of great help and who motivated me with her great enthusiasm for physics. Special thanks goes to David Murgia, Simon Webster and Gouri Giri, who provided me with great feedback while working on my thesis. Gouri Giri also assisted me with the development of our voltage control system and was of invaluable help during my time fabricating at the Southampton nanofabrication centre. I would also like to thank the other group members, Darren De Motte, Eamon Standing, Joe Randal and the many undergraduate students who have supported our work on the experiments.

Many thanks also go to Alan Mayers and the other members of the mechanical workshop at Sussex, who gave me good advice whenever designing new parts for the experiment and for their great work when manufacturing these for us. I would also like to thank the staff members of the Southampton nanofabrication centre for the constant support and help with the challenging fabrication processes. A thank you must also go to the group led by Wolfgang Lange and Mathias Keller, who provided us with guidance and shared equipment whenever needed.

I am very greatful to my family for always encouraging, motivating and believing in me. Without their love and support I would have not been able to finish this endevour. My greatest thanks goes to my fiancee Nicky Santoyo, for always being there for me and who I will never be able to thank enough for what she did for me over the last two years. Finally, I'd like to thank my close friends: Sebastian Deuser, Frank Klaiber, Felix Waehlisch, Christoff Haller, Marco Stolle, David Christian, Luisa Bohlender, Svenja and Wolfgang Huemmer, who have always been supportive, helpful and provided me with distractions when needed.

Detailed Acknowledgements

Much of the work presented in this thesis would not have been achievable without the input and help of other members of the group and the Southampton nanofabrication centre. In the following section I will outline their contributions to my thesis chapters.

Chapter 3 - Ion Trapping Setup and Initial Experiments

The ion trapping setup was built before I joined the group by Altaf Nizamani, Robin Sterling, James Siverns, Marcus Hughes and James McLoughlin. More specifically, the external cavity diode lasers were constructed by James McLoughlin and Robin Sterling. Laser locking systems were designed and implemented mainly by Robin Sterling and Kimberly Lake with support from Altaf Nizamani, James Siverns, Marcus Hughes and James McLoughlin. The imaging setup was designed and constructed by James Siverns and Marcus Hughes. The first vacuum system was developed and assembled by Altaf Nizamani with the help of James McLoughlin and Robin Sterling. The second vacuum system was developed by Robin Sterling and James Sayers and assembled by Robin Sterling, Sebastian Weidt and Kimberly Lake. The helical resonator was designed and built by James Siverns. The macroscopic blade trap was designed by Robin Sterling and individual parts assembled by Altaf Nizamani, James Siverns, Marcus Hughes, James McLoughlin and Robin Sterling.

Doppler cooling wavelengths were measured by Altaf Nizamani, Robin Sterling, James Siverns, Marcus Hughes, James McLoughlin, myself and Sebastian Weidt.

The theory of the heating measurement was reproduced by myself with some assistance of Altaf Nizamani and James McLoughlin. The measurement was performed by myself, Marcus Hughes, Sebastian Weidt, Altaf Nizamani, James McLoughlin, James Siverns and Robin Sterling.

Chapter 4 - Microfabrication Techniques

This chapter is partially based on common work of myself and Marcus Hughes presented in the publication 'Microfabricated Ion Traps'.

Chapter 5 - Concept for Scalable Ion Trap Quantum Computing

The concept presented in this chapter was developed by myself. The analysis of the error correction codes is loosely based on prior work of myself, Austin Fowler, Simon Devitt, Altaf Nizamani, Kimberly Lake, Sebastian Weidt and Winfried Hensinger.

Chapter 6 - Asymmetric Ion Trap Designs

The two-dimensional array, discussed in this chapter is based on the example case presented in 'Optimisation of two-dimensional ion trap arrays for quantum simulation' and the geometry was optimized by James Siverns, Sebastian Weidt, Kimberly Lake, myself and Marcus Hughes.

Chapter 7 - Vacuum Chamber Modifications and Voltage Control System

The development of the voltage control system presented in this chapter was assisted by Gouri Giri.

Chapter 8 - Microfabrication of Ion Trap Designs

The fabrication process was developed by myself with help of Ibrahim Sari and Marcus Hughes. Optimization of process steps was performed by myself assisted by Ibrahim Sari, Kian Shen Kiang and Hwanjit Rattanasonti. All of the fabrication steps for the ion trap designs were performed by myself.

Publications and conference contributions

Journal publications

Versatile ytterbium ion trap experiment for operation of scalable ion-trap chips with motional heating and transition-frequency measurements,
James J. McLoughlin, Altaf H. Nizamani, James D. Siverns, Robin C. Sterling, Marcus D. Hughes, Bjoern Lekitsch, Björn Stein, Seb Weidt, and Winfried K. Hensinger,
Phys. Rev. A 83, 013406 (2011).

Microfabricated ion traps,
Marcus D. Hughes, Bjoern Lekitsch, Jiddu Broersma and Winfried K. Hensinger,
Contemporary Physics 52:6, 505-529 (2011).

Optimization of two-dimensional ion trap arrays for quantum simulation,
James D Siverns, Seb Weidt, Kim Lake, Bjoern Lekitsch, Marcus D Hughes and Winfried K Hensinger,
New J. Phys. 14, 085009 (2012).

Conference contributions

Development of ion chips and coherent manipulation of ytterbium ions,
B. Lekitsch, R. C. Sterling, M. D. Hughes, J. D. Siverns, J. J. McLoughlin, S. Weidt, K. Lake, A. H. Nizamani, P. Srinivasan, H. Rattanasonti, J. Maclean, C. Mellor, M. Kraft and W. K. Hensinger
Poster at IonTech 2012, COST-IOTA Workshop 7-9 May 2012, at Siegen, Germany.

Contents

List of Tables

List of Figures

Chapter 1

Introduction

Quantum information technology holds tremendous potential to advance research fields, computational methods and modern communication technologies. Simulations based on quantum bits (qubits) and quantum operations (entanglement gates) can be used to efficiently simulate quantum systems, impossible for classical computers, as proposed by Feynman [1] over 30 years ago. Since then many basic quantum simulations of material properties [2–8] have been realized and many different applications of quantum systems have been investigated to simulate theoretical models [9–12]. The knowledge gained from large scale quantum simulations has great potential to extend our knowledge of basic physical principles, lead to the development of more advanced theoretical models and ultimately result in new technologies and materials.

Extending Feynman's idea of universal quantum simulators Deutsch proposed a universal quantum computer [13], which can be seen as the quantum equivalent to the universal Turing machine (UTM) [14]. It can perform tasks and solve algorithms efficiently, which would be impossible for a UTM, making use of the quantum nature of the device. Consequentially many algorithms to be used by a quantum computer were proposed, including algorithms by Shor [15] and Grover [16] and many others [17–20].

Shor's algorithm allows for the efficient factorizing of large numbers and has been implemented in small scale quantum systems [21, 22]. Grover's algorithm improves the search of very large unstructured databases and has also been demonstrated in a quantum system [23]. Large scale realization of both algorithms would have great impact on today's information technology. Searching of large unstructured databases is an important part of finding relevant information in the world wide web or large metadata databases.

Grover's algorithm provides a dramatic speed up compared to current classical algorithms, but not comparable to the exponential gain of Shor's algorithm [24]. The efficient factorization of large numbers would make it possible to decipher the commonly used RSA encryption technology [25], allowing most of today's encryptions to be circumvented [26].

Quantum systems also provide a method to achieve absolutely secure communication channels. Using two entangled qubits and transmitting information via quantum state teleportation results in perfectly safe communication, due to the no-cloning theorem. It states that unknown quantum states can't be cloned [27] and therefore transmitted information cannot be intercepted without detection [28, 29]. Quantum systems allowing for secure communication, based on the no-cloning theorem, have been experimentally demonstrated in the laboratory [30, 31] and recently between satellites and a ground station [32].

The tremendous achievements and possibilities of quantum systems has motivated great research efforts towards the realization and optimization of quantum simulators and universal quantum computers by many research groups in different fields of physics. Characterizing the progress of different quantum system technologies towards this goal helps to identify promising technologies and outline major goals for future developments. Such a characterization can be made by making use of the requirements placed on quantum systems to realize a universal quantum computer. D. P. DiVincenzo presented a discussion [33] summing up the requirements a system must fulfill to become a universal quantum system:

State initializations of the qubits in a simple fiducial state needs to be performed.

Decoherence time of qubits in the system needs to be much longer than the gate times.

Universal gates for one and two qubits operations [34].

Readout of any arbitrary qubit in the system.

Physical scalability with well characterized quantum bits.

Among the many quantum systems being researched, some of the most promising approaches [35] include: neutral atom systems, most prominently based on atoms trapped in optical lattices [36], magneto-optical traps (MOTs) [37] or optical cavity hybrid systems [38]; superconductor based systems with qubits making use of Josephson junctions [39–41]; photonic quantum systems based on linear optics [42, 43] or weak cross-Kerr coupling [44]; and trapped ion quantum systems [45–47], which can be grouped into

systems addressing physical scalability with the movement of trapped ions [48] or hybrid systems using ion-photon entanglement [49].

Possibly the most promising of all is the trapped ion quantum system, making use of traps providing means to store and manipulate ionized atoms, well isolated from the environment. Ion trap systems have achieved almost all of the required criteria [50,51] and allow for a physically scalable system. Robust and high fidelity **state preparation** [52] and **readout** [53–55] of qubits with long **decoherence times** [56] and fast **universal gates** [45,51,57,58] have been demonstrated. Additionally many advances in the field of error correction [59–64] have been made.

This success is based on a well developed tool kit which has its origin in the development of an electrodynamic mass spectrometer by W. Paul in 1953 [65,66], which was also used to trap ions [67,68] shortly after. Commonly used ion trap technologies are the Paul [65,66] and Penning traps [69,70]; only Paul traps will be considered for scalable ion trap systems in this thesis. To improve the accuracy of spectroscopy measurements, laser cooling of trapped ions was developed [71,72], followed by the first experimental demonstration of a two qubit quantum gate [45] and theoretical work towards the realization of large scale ion trap architectures [73].

A theoretical discussion of the principles of ion traps, the atomic structure of the ion used and basics of quantum operations will be given in chapter 2. Asymmetric ion trap geometries, stable trapping and laser cooling of ions will be discussed in detail. The defining characteristic of asymmetric (also known as surface) ion traps is that all electrodes are placed below the trapping zone in one plane. The electrode geometry is asymmetric with respect to the trap centre, unlike symmetric traps where the electrodes are placed symmetrically in planes above and below the trapping centre. Asymmetric traps have the disadvantage of lower trap depth compared to symmetric traps with similar applied potentials and ion electrode distances. Due to the electrode configuration they allow laser access in almost the entire plane parallel to the surface and also provide free optical access to the trapped ion from above the surface. Also the fabrication of asymmetric traps is based on standard microfabrication technologies without the need for extremely thick dielectric layers between electrodes [74], giving them an advantage in relative ease of fabrication.

In chapter 3 the operation of a macroscopic ion trap and the necessary experimental setup will be discussed. I then outline a number of experiments performed in the described trap,

including trapping of different isotopes, measurement of the secular frequencies in all trap axes and determination of the heating rate of the system.

Chapter 4 will give an overview of microfabricated surface ion traps, based on work done by the author for [75]. Important considerations concerning the electrical properties of an ion trap will be discussed. Causes of micromotion and models explaining the anomalous heating found in ion traps will be outlined. Then an overview of fabrication technologies commonly used in trap fabrications will be discussed and the advantages, disadvantages and underlying problems of these different processes will be analyzed. A new fabrication process developed by the author more suitable for the desired trap structures will also be introduced.

Chapter 5 will present a concept for a scalable ion quantum system. Physical scalability of ion trap quantum systems came into reach after the development of the first microfabricated ion trap [76,77] and the demonstration of shuttling of ions through junctions [78–81] shortly after. Gates making use of strong magnetic field gradients and microwave transitions have been realized recently [82, 83] and hold the promise of dramatically improving the scalability of the ion trap quantum systems [84]. In chapter 5 entanglement requirements and error rates of quantum error codes that are used to form logical qubits will be analyzed. Logical qubits are made up of a large number of physical qubits and use an error correction code to perform $\sim 10^{16}$ error protected quantum operations, enough for any quantum algorithm or simulation proposed so far [85]. Depending on the fidelity rate of physical qubit operations more than 1000 physical qubits will be necessary to achieve one logical qubit. Based on the requirements of the used error correction code a scalable ion trap architecture will be presented in 5. The architecture is based on a two-dimensional array of X-junctions with entanglement zones as illustrated in Fig. 1.1. Individual building blocks of the array will be discussed in detail and required technology developments identified.

Based on a newly developed fabrication process detailed ion trap designs will be presented and resulting mask designs will be outlined in chapter 6. Individual design steps, the design process and process limitations will be described. The optimization of an X-junction electrode for minimal rf barrier height, development of current-carrying wire structures intended to generate large magnetic field gradients and designs motivated by the scalable architecture outlined in chapter 5 will be presented. Trapping parameters and numerically simulated electric fields of the traps in question will be described.

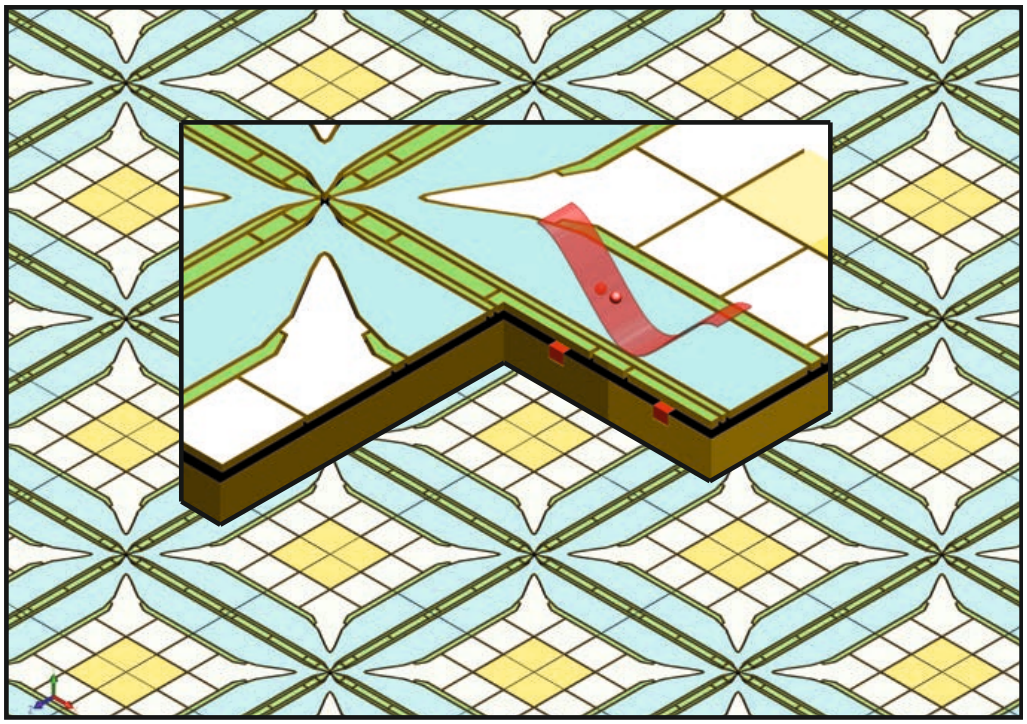


Figure 1.1: Illustration showing a two-dimensional trapping array made up of X-junctions forming a two-dimensional grid. Ions can be shuttled from one junction arm to another and joined with ions from other junctions in entanglement zones. In the inset a more detailed view of an entanglement gate based on magnetic field gradients is given.

In chapter 7 additions to the experimental system, including an argon sputter gun, an in-vacuum system designed to transport heat away from ion traps with current-carrying wires and a new multichannel voltage control system, will be presented. The argon plasma source can be used to perform *in situ* cleans of the trap electrodes, which has been shown to dramatically reduce the heating rate in ion traps [86, 87]. The in-vacuum heat transport system is required to operate traps with current-carrying wires without overheating them. Additionally the heat bridge should also allow the trap to be cooled to cryogenic temperatures from the outside of the vacuum system. The voltage control system is based on low-noise components and can generate high speed, high voltage arbitrary waveforms intended for ion shuttling.

Lastly the process optimization and microfabrication of the developed ion trap designs will be presented in chapter 8. The novel fabrication process was developed at the Southampton Nanofabrication Centre and makes use of highly thermally conductive diamond substrates and combines it with thick copper tracks embedded in the substrate. Individual process steps will be described in detail and results presented.

Chapter 2

Ion Trapping and the Yb Ion

In this chapter the basic electromagnetic principles behind the operation of Paul traps [67] will be explained. Paul traps with surface trap electrode geometries, where all electrodes are placed in one plane [75, 77], will be investigated in more detail. Analytical and numerical methods to obtain the electric fields for these traps will be given and results presented. Laser cooling and atomic levels of the Ytterbium (Yb) ion will be discussed and the requirements to perform quantum gates will be briefly outlined. The fundamentals of microfabricated ion trap designs and experiments were reviewed in 'Microfabricated ion traps' [75] and this chapter is partially based on work for this publication.

2.1 Electric Fields and Ion Motion in Paul Traps

Gauss's Law states that the divergence of an electric field $\mathbf{E}(\mathbf{x})$ in free space must be zero $\boldsymbol{\nabla}\cdot\mathbf{E}(\mathbf{x}) = 0$, with $\mathbf{E}(\mathbf{x}) = \boldsymbol{\nabla}\cdot\Phi(\mathbf{x})$ resulting in $\boldsymbol{\nabla}^2\Phi(\mathbf{x}) = 0$, which is the Laplace equation and is also stated by Earnshaw's Theorem [88]. As a direct result the electrostatic force $\mathbf{F}(\mathbf{x})$ stemming from an electric potential $\Phi(\mathbf{x})$ must be divergenceless and cannot hold a point charge in a stable equilibrium. Looking at the two-dimensional potential Fig. 2.1 (b) of hyperbolic shaped electrodes Fig. 2.1 (a) one can see that a saddle potential with confining saddle points in one direction and unstable points in the other is generated. Stable trapping of ions in all three dimensions is not possible using solely static electric potentials.

To circumvent this limitation an alternating potential $\phi(t)$ is applied to the electrodes, which results in a rotation of the created saddle potential and as will be shown later in this

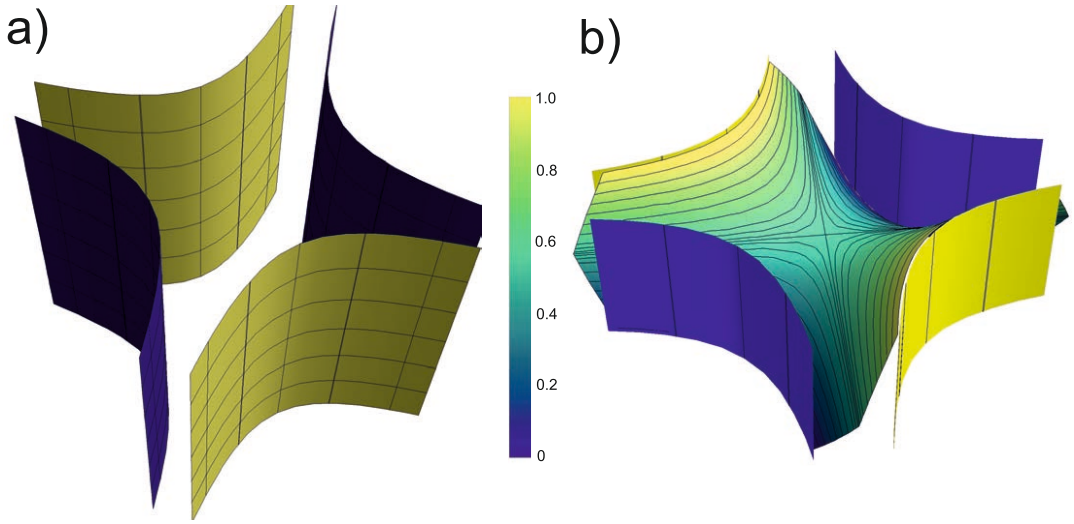


Figure 2.1: (a) Hyperbolic shaped electrodes, opposite plates have the same potential ϕ and obverse plates will have the same potential with inverse polarity $-\phi$. (b) Two-dimensional saddle potential with stable trapping in one direction.

chapter, when averaged over time this results in a stable trapping potential as shown Fig. 2.2. Using this, stable trapping of ions in two [65] or three dimensions [67] is possible. Most modern ion traps [75,89,90] use a combination of two-dimensional confinement provided by an oscillating potential $\Phi(t)$ and confinement in the third dimension via static potentials.

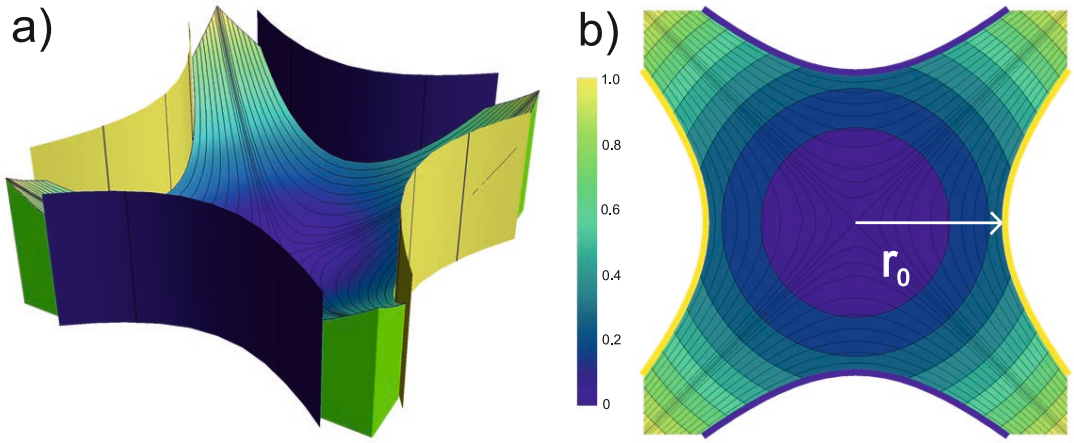


Figure 2.2: Time averaged trapping potential generated by an alternating potential $\phi(t)$ applied to the hyperbolic electrodes.

2.1.1 Ion Motion in the Pseudopotential Approximation

To investigate how the ion behaves inside such an electric potential we will derive and solve the equations of motion for the ion. The calculations will follow the derivations presented

in [66], [70] and [91].

We start with a simple homogenous electric field E_h generated by two parallel plates as shown in Fig. 2.3 (a) with an alternating potential $\phi(t) = V\cos(\Omega t) + U$ applied to one of the plates, where Ω is the drive frequency, V the voltage amplitude of the alternating potential and U a static voltage added as an offset to the oscillating voltage. The one dimensional equation of motion of the trapped ion of mass m and charge e in the x-axis is then:

$$m\ddot{x}(t) - eE_h\cos(\Omega t) + eE_s = 0 \tag{2.1}$$

The static electric field E_s arises from the static voltage offset U applied to the electrodes and can be kept at zero in most ion trap experiments [89]. For most of the following derivation E_s will therefore be neglected. The solution for equation 2.1 can be gained by direct integration to be

$$x(t) = x_0 - a\cos(\Omega t)\ for\ U = 0 \tag{2.2}$$

with a being the constant amplitude of the oscillation equal to $a = \frac{eE_h}{m\Omega^2}$. Plotting the ion motion inside the parallel plates Fig. 2.3 (b) it can be seen that averaged over time there is no force acting on the ion as it is only oscillating back and forth, returning to the starting point x_0 after one oscillation period Fig. 2.3 (b).

A non-zero time averaged force acting on the ion is required for trapping and can be obtained by slightly bending the plates Fig. 2.3 (c). The generated electric field becomes inhomogeneous $E_{ih}(x)$. Corresponding differential equations of motion can generally not be solved analytically and require numerical solutions [91].

In the present case of a weakly inhomogeneous field a few assumptions and approximations can be made to solve the equation without relying on numerical techniques. The field variations of $E_{ih}(x)$ in x have to be smooth and the frequency Ω has to be high enough to keep the amplitude $a = \frac{eE_{ih}}{m\Omega^2}$ of the oscillation small compared to the motion of the ion caused by the inhomogeneity of the field. We can then replace E_h in equation 2.1 with $E_{ih}(x)$ and solve the new equation by superimposing a slow drift term x_s with a fast oscillating term $x_f = -a(t)\cos(\Omega t)$, which results in

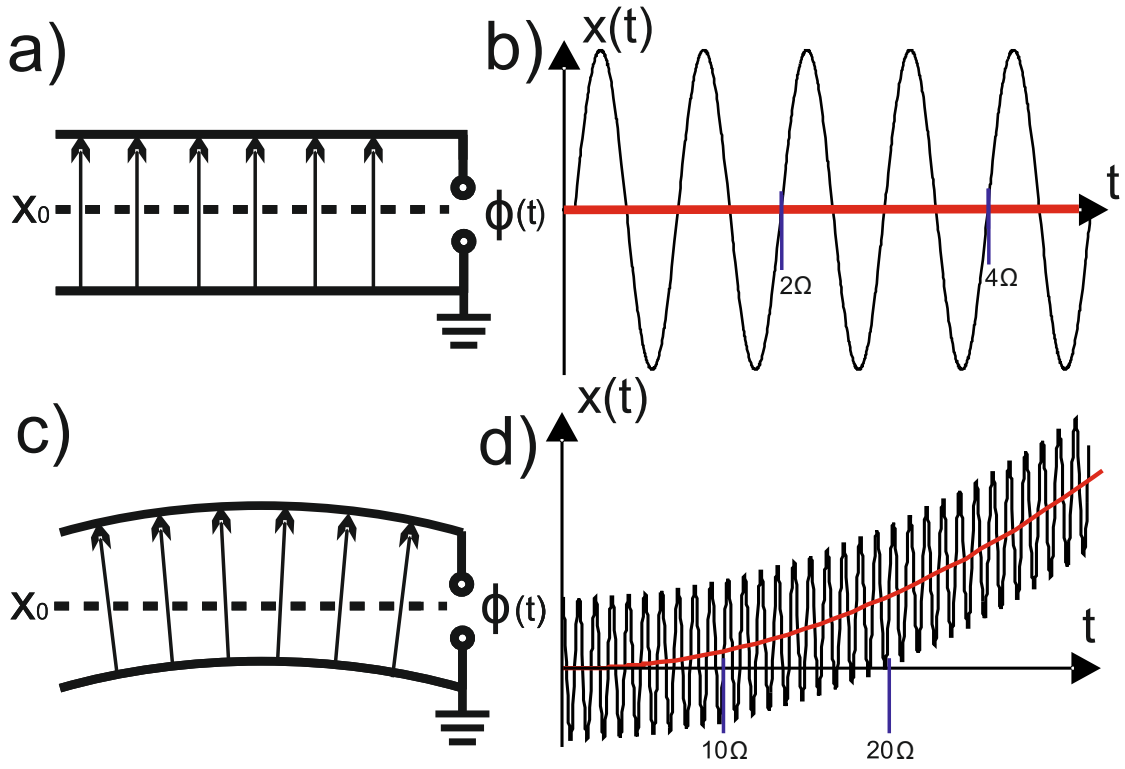


Figure 2.3: (a) Parallel plates with applied potential ϕ and corresponding E field. (b) Ion motion $x(t)$ vs time and the time averaged motion in red. (c) Slightly bent parallel plates with the same applied potential ϕ and now inhomogeneous electric field. (d) Ion motion $x(t)$ vs time in the inhomogeneous field and time averaged motion in red.

$$x(t) = x_s(t) - a(t)\cos(\Omega t) \tag{2.3}$$

with the now time-dependent amplitude *a(t)*. We then approximate the inhomogeneous electric field $E_{ih}(x)$ with a 1st order Taylor Series expansion:

$$E_{ih}(x_s - a(t)\cos(\Omega t)) = E_{ih}(x_s) - a(t)\frac{\partial(E_{ih}(x_s)\cos(\Omega t))}{\partial x} \tag{2.4}$$

Due to the assumed slow variation of the field we can also assume that $\dot{a} << \Omega a$ and $\ddot{x}_s << \Omega \dot{x}_s$. Substituting equation 2.3 and 2.4 into the equation of motion 2.1 results in the following equation for the ion motion inside the slightly bent parallel plates:

$$m\ddot{x}_s(t) + m\Omega^2 a(t)\cos(\Omega t) = eE_{ih}(x_s)\cos(\Omega t) - ea(t)\frac{\partial(E_{ih}(x_s)\cos^2(\Omega t))}{\partial x} \tag{2.5}$$

Assuming that the amplitude $a(t)$ varies in time only due to the motion of the ion along $x_s(t)$ we can replace $a(t)$ with $a(x_s)$. Now if we time average the equation over one period with, $\langle\cos^2(\Omega t)\rangle = 1/2$ and $\langle\cos(\Omega t)\rangle = 0$ equation 2.5 takes the form:

$$\langle m\ddot{x}_s(t)\rangle = -\frac{1}{2}ea(x_s)\frac{\partial E_{ih}(x_s)}{\partial x} \tag{2.6}$$

Substituting $a(x_s) = \frac{eE_{ih}(x_s)}{m\Omega^2}$ and using the general vector analysis relation,

$$\mathbf{E}\nabla\mathbf{E} = \frac{1}{2}\nabla(\mathbf{E} * \mathbf{E}) \tag{2.7}$$

we can further simplify equation 2.6 to:

$$\langle m\ddot{x}_s(t)\rangle = -\frac{e^2}{4m\Omega^2}\frac{\partial E_{ih}^2}{\partial x} \tag{2.8}$$

The force $F = m\ddot{x}_s(t)$ arises from the alternating inhomogeneous electric field E_{ih} and its direction is determined by the gradient $\frac{\partial E_{ih}^2}{\partial x}$. The electric force on the ion will always point towards the weakest points of the field E_{ih}. Making the following substitution

$$\psi(x_s) = \frac{e^2}{4m\Omega^2}E_{ih}^2 \tag{2.9}$$

the equation of motion can be brought into the form,

$$\langle m\ddot{x}_s(t)\rangle = -\frac{\partial\psi(x_s)}{\partial x} \tag{2.10}$$

The time-independent potential $\psi(x_s)$ describes the time averaged ion motion Fig. 2.3 (d) for the discussed case. This effective potential ψ is commonly called the pseudopotential [70], and also includes the neglected static term from equation 2.1, with $E_s = -\frac{\partial\Phi_s}{\partial x}$ and $E_{ih} = -\frac{\partial\Phi_{ih}}{\partial x}$ taking the form:

$$\psi(x_s) = \frac{e^2}{4m\Omega^2}\frac{\partial\Phi_{ih}^2}{\partial x} + e\Phi_s \tag{2.11}$$

The solution to the equation of motion is now trivial as the pseudopotential is time-independent and the corresponding ion motion is illustrated in Fig. 2.3 (d). If the solution for the slow drift term x_s is overlaid with the fast oscillating term $x_f = -a(t)\cos(\Omega t)$, where $a(t)$ represents the time-dependent amplitude of the oscillation in the inhomogeneous electric field, the motion becomes the oscillating trajectory shown in Fig. 2.3 (d). Although the introduced pseudopotential was only derived for one dimension it can also be generalized to three dimensions, as demonstrated in [70, 92, 93].

2.1.2 Mathieu Equations and Stability Parameters

We now come back to the inhomogeneous saddle potential presented in Fig. 2.2 created by the two-dimensional hyperbolic electrodes shown in Fig. 2.1 (a) and derive the equations of motion for an ion trapped in this potential. The hyperbolic potential allows for the equations of motion to be solved analytically and a detailed description of the trapped ion motion without approximations can be made. The following derivations are based on derivations presented in [66]. We start with the general three-dimensional electric quadrupole potential:

$$\Phi = \frac{\phi(t)}{2r_0^2}(\alpha x^2 + \beta y^2 + \gamma z^2) \tag{2.12}$$

Where $\phi(t)$ is the oscillating potential applied to the hyperbolic electrodes, r_0 is the distance between trap centre and the closest electrode point, see Fig. 2.2 (b). In the present case of a two-dimensional potential the general quadrupole equation can also be

simplified with $\gamma = 0$ and to satisfy Laplace's equation $\nabla \cdot \Phi = 0$ we set $\alpha = 1 = -\beta$. Consequentially opposite plates will be kept at potential $\phi(t)$ and obverse plates will have the same potential with inverse polarity $-\phi(t)$ [65]. The resulting two-dimensional inhomogeneous hyperbolic potential then takes the form:

$$\Phi = \frac{\phi(t)}{2r_0^2}(x^2 - y^2) \tag{2.13}$$

We can write the applied potential as $\phi_0(t) = U + V\cos(\Omega t)$, Ω is again the drive frequency, V the alternating voltage amplitude and U the static offset. The force acting on the trapped ion, also known as pondermotive force, can be derived as $\mathbf{F} = -e\nabla\Phi(x, y, t)$. When time averaged, the force $\mathbf{F}$ will not vanish due to the inhomogeneous nature of Φ and will have a net component pointing towards the weakest region of the potential, which in this case is the centre of the trap [66]. Considering that the movement of the ion in the x and y direction is uncoupled, we can then write the equations of motion for the trapped ion as,

$$\ddot{x}(t) + \frac{e}{mr_0^2}(U - V\cos(\Omega t))x = 0 \tag{2.14}$$

and

$$\ddot{y}(t) + \frac{e}{mr_0^2}(U - V\cos(\Omega t))y = 0 \tag{2.15}$$

These equations are uncoupled linear differential equations of second order with a periodic coefficient $(\cos(\Omega t))$, which puts them in the category of Mathieu equations [94, 95]. The general Mathieu equation has the form:

$$\frac{d^2 i}{d\zeta^2} + (a_i - 2q_i\cos(2\zeta))i = 0 \tag{2.16}$$

If we make the following substitutions,

$$i = [x, y],\ a_x = -a_y = \frac{4eU}{mr_0^2\Omega_T^2},\ q_x = -q_y = \frac{2eV}{mr_0^2\Omega_T^2},\ \zeta = \frac{\Omega_T^2 t}{2} \tag{2.17}$$

the equations of motion are brought into the same form. Mathieu equations have an infinite number of solutions, but only stable periodic solutions result in trapping of ions.

Other solutions would lead to the loss of a trapped ion. The Floquet theorem [95] can be used to obtain stable solutions which are illustrated as stability regions in the a and q space Fig. 2.4. The marked areas represent regions, where a and q give stable periodic solutions, the region boundaries represent periodic but unstable solutions. Where regions of stability for the x and y motion overlap, stable trapping of the ion is possible, further illustrated in the inset of Fig. 2.4.

For the case of $a \neq 0$, where a static offset voltage U is applied to the electrodes, a solution for x and y is given in [89] for the region $a_i < q_i^2 << 1, i \in x, y$. An approximation for the more common case of $a_i = 0$ and $q_i^2 << 1$, $i \in x, y$ can be made and we can write the equation of motion in the x-axis as [75],

$$x(t) = x_0 \cos(\omega_x t) \left[1 + \frac{q_x}{2} \cos(\Omega t)\right] \tag{2.18}$$

where ω_x is the so-called secular frequency in the x-axis and equal to:

$$\omega_x = \frac{\Omega}{2}\sqrt{a_x + \frac{q_x^2}{2}} \tag{2.19}$$

Plotting the resulting motion versus time in Fig. 2.5 (a) illustrates that the ion motion consists of a large oscillation known as the secular motion, overlaid with a faster oscillating micromotion. The micromotion oscillating with frequency Ω, the drive frequency, is caused by the ion feeling the fast alternating potential, whenever the ion is not at the nil of the potential. This micromotion is commonly called intrinsic micromotion. When the ion is pushed out of the rf nil by a static potential we speak of extrinsic micromotion.

Comparing the solution for $x(t)$ with the solution 2.3 used to solve the ion's equation of motion in an inhomogeneous electric field in section 2.1.1, we can see that micromotion corresponds to the fast oscillating term $x_f(t) = x_0 \cos(\omega_x t) \frac{q_x}{2} \cos(\Omega t)$. Due to the confining nature of the hyperbolic quadrupole potential the slow drift term in equation 2.3 is now an oscillation around the trap center. In Fig. 2.5 (b) the x and y movement during one oscillation period $\Delta t = \frac{1}{\omega_x}$ inside the trapping potential shown in 2.5 (c) is plotted for different starting points. The plot illustrates the oscillation close to the centre and also the increase in micromotion with distance from the center.

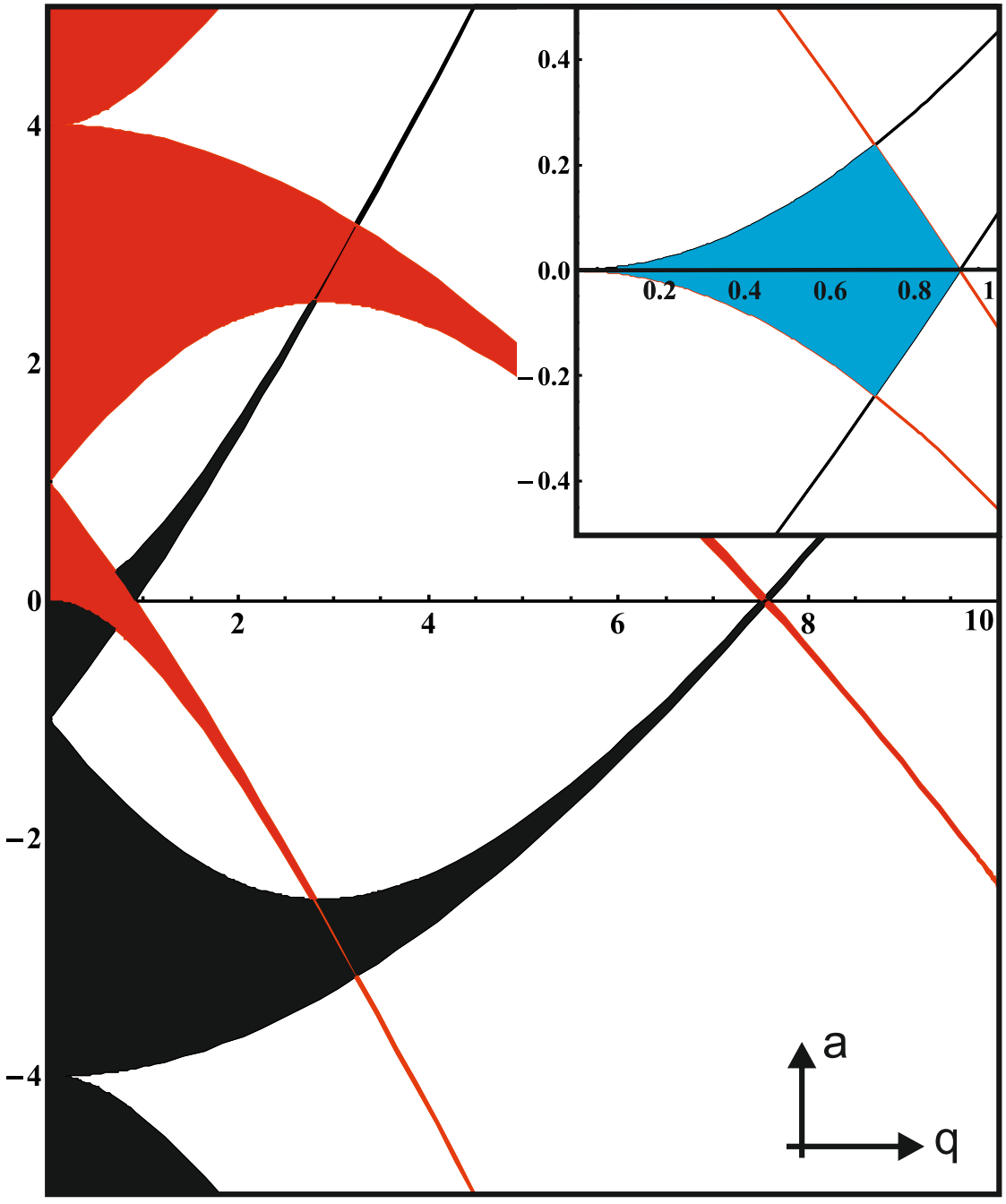


Figure 2.4: (a) Stability diagram showing the regions of stable solutions for motion along the x-axis (red) and y-axis (black) in a, q space. The inset (b) shows the main stability region for both axes marked as blue.

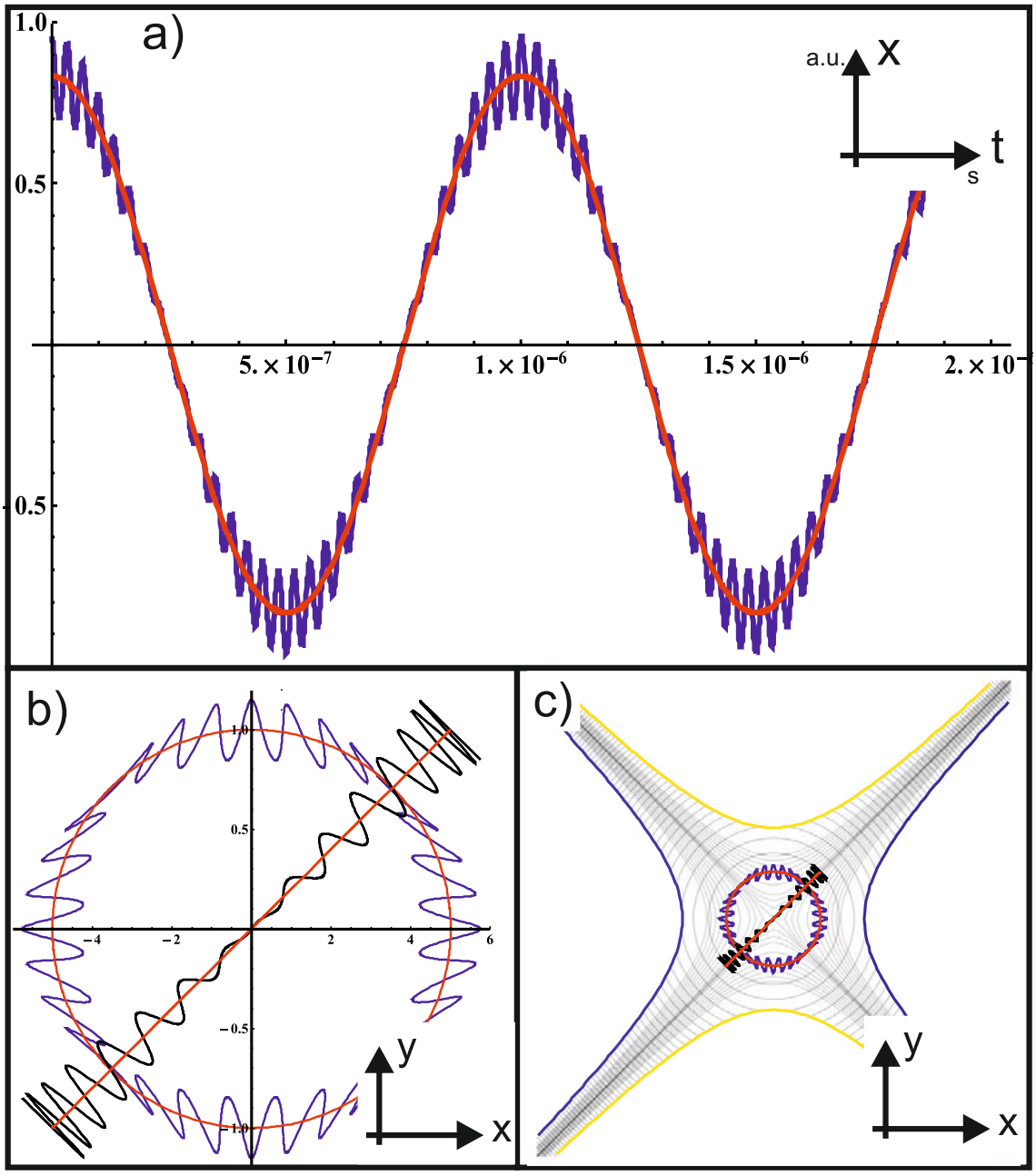


Figure 2.5: (a) Ion motion (blue) along the x-axis vs time, the large oscillation (red) is overlaid with a higher frequency micromotion. (b) Ion motion in x and y-axis during one oscillation period for two different starting points. The increase of micromotion with distance from the centre becomes visible. (c) Illustration of the same motion with the trap electrodes and potential (not to scale).

Looking at the previously introduced time-averaged harmonic pseudopotential for this case given in [89] and shown in Fig. 2.2:

$$\psi(r) = \frac{1}{2q} m\omega_r^2 (x^2 + y^2) \tag{2.20}$$

Making the approximation $\omega_r \sim \omega_x$, that the secular frequency is similar[1] in x and y-axis, the equation of motion in the pseudopotential approximation, using equation 2.1 is equal to,

$$\ddot{x}(t) = \omega_x^2 x \tag{2.21}$$

As expected the slow oscillating drift term x_s from equation 2.3 is a solution to this equation. The pseudopotential approximation allows for an accurate description of the secular motion and will be used almost exclusively for the following trap simulations. Nevertheless the stability parameters of the Mathieu equation still need to be calculated and have to be inside a stable trapping region.

2.1.3 Analytical Simulations of Electric Fields in Surface Traps

In the previous discussion of the ion motion we used electrode geometries with known analytic functions describing the electric fields. Unfortunately most ion trap geometries don't have analytic functions describing the trapping fields. Numerical simulations are required to find the electric fields and commonly used methods will be discussed in section 2.1.4. Fortunately, for surface trap geometries an approximation can be made that provides a method to obtain the electric field analytically. Such analytical methods were presented in [96] and [97].

Deriving Electric Fields of Surface traps

Certain approximations have to be made for this approach, starting with the so-called gapless-plane approximation. We assume that the electrodes occupy the entire surface plane $z = 0$ (extending infinitely in this plane) and that the gaps between the electrodes are infinitely small. The gapless plane approximation provides accurate results only if the

[1] will be identical in a perfect symmetric hyperbolic potential

gaps are much smaller than the electrode size. When calculating the field inside junctions where gaps can have the same size as electrodes, this method is less accurate.

Following the derivation given in [96] the potential $\Phi_i(\mathbf{x}')$ at the surface of electrode i, with $\mathbf{x}' = (x, y, 0)$, must be equal to the potential ϕ_i applied to the electrode and must be constant over the entire electrode surface S with area a. The potential $\Phi_i(\mathbf{x})$, $\mathbf{x} = (x, y, z)$ must be zero if $z \to \infty$ and have a finite value for $x \to \infty$ and $y \to \infty$ [96]. While not being a strict requirement, for the rest of the derivation it will also be assumed that all electrodes have a rectangular shape shown in Fig. 2.6.

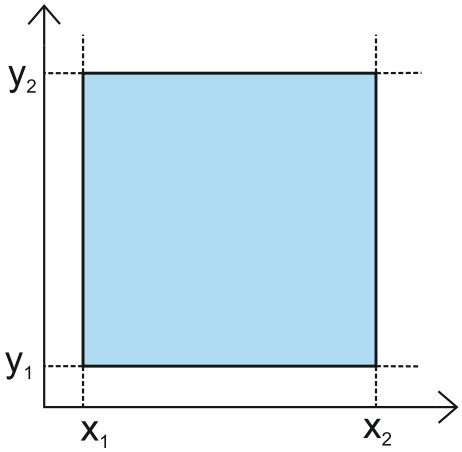


Figure 2.6: Rectangular shaped electrode with coordinates, x_1, y_1, x_2, y_1, x_1, y_2 and x_2, y_2.

The potential $\Phi(\mathbf{x})_i$ created by a rectangular electrode i of width $x_i = x_{2,i} - x_{1,i}$ and height $y_i = y_{2,i} - y_{1,i}$, see Fig. 2.6, held at the potential ϕ_i while all other electrodes are held at 0 V was derived in [96] and the potential of the rectangular electrode i is equal to:

$$\Phi_i(\mathbf{x}) = \{\frac{\phi_i}{2\pi}\{\arctan\left[\frac{(x_{2,i}-x)(y_{2,i}-y)}{z\sqrt{z^2+(x_{2,i}-x)^2+(y_{2,i}-y)^2}}\right] \tag{2.22}$$

$$-\arctan\left[\frac{(x_{1,i}-x)(y_{2,i}-y)}{z\sqrt{z^2+(x_{1,i}-x)^2+(y_{2,i}-y)^2}}\right] \tag{2.23}$$

$$-\arctan\left[\frac{(x_{2,i}-x)(y_{1,i}-y)}{z\sqrt{z^2+(x_{2,i}-x)^2+(y_{1,i}-y)^2}}\right] \tag{2.24}$$

$$+\arctan\left[\frac{(x_{1,i}-x)(y_{1,i}-y)}{z\sqrt{z^2+(x_{1,i}-x)^2+(y_{1,i}-y)^2}}\right]\}\} \tag{2.25}$$

This provides only a solution for the potential created by one electrode, to acquire a solution of $\Phi(\mathbf{x})$ for the entire electrode geometry, all individual electrode potentials $\Phi_i(\mathbf{x})$ have to be added together:

$$\Phi(\mathbf{x}) = \sum_i \Phi_i(\mathbf{x}) \tag{2.26}$$

Basis Function Technique

This method of combining individual electrode potentials to acquire the collective potential of the entire geometry is commonly known as the basis function technique. Analytically and numerically acquired electric fields of trap electrodes can be combined to form the entire trap geometry using this technique. A justification for this method will be briefly outlined following the proof given in [98].

The potential on the surface S with area a is again $\Phi(\mathbf{x}')$ and the solution for the potential $\Phi(\mathbf{x})$ with the previously discussed boundary conditions 2.1.3, is given by [98]:

$$\Phi(\mathbf{x}) = \frac{1}{4\pi\varepsilon_0}\int_V \rho(\mathbf{x}')G(\mathbf{x},\mathbf{x}')d^3\mathbf{x}' - \frac{1}{4\pi}\oint_S \Phi(\mathbf{x}')\frac{\partial G(\mathbf{x},\mathbf{x}')}{\partial n'}da' \tag{2.27}$$

Where n is normal to the surface S and $G(\mathbf{x},\mathbf{x}')$ is the Green function. The first term of the equation is a volume integral over the charge $\rho(\mathbf{x})$ inside the boundary. In an empty ion trap the volume integral of $\Phi(\mathbf{x})$ will vanish. The second term is a surface integral over the surface potential $\Phi(\mathbf{x}')$ multiplied by the normal derivative of the Green function. As it is possible to write the potential on the surface $\Phi(\mathbf{x}')$ as a sum of the individual electrode potentials, with the rest of the electrodes kept at zero:

$$\Phi(\mathbf{x}') = \sum_i \Phi_i(\mathbf{x}') \tag{2.28}$$

the total potential can then be written as:

$$\Phi(\mathbf{x}) = -\frac{1}{4\pi}\sum_i \oint_{S_i} \Phi_i(\mathbf{x}')\frac{\partial G_i(\mathbf{x},\mathbf{x}')}{\partial n_i'}da' \tag{2.29}$$

From this equation it becomes clear that the total potential of $\Phi(\mathbf{x})$ is indeed the sum of the potentials Φ_i created by individual electrodes i. In the previously discussed boundary

conditions it is assumed that the voltages across each individual electrode is static and the total potential of the electrode geometry can be written as

$$\Phi(\mathbf{x}) = \sum_i V_i \Theta_i, \quad \Theta_i = -\frac{1}{4\pi} \oint_{S_i} \frac{\partial G_i(\mathbf{x}, \mathbf{x}')}{\partial n_i'} da' \tag{2.30}$$

with Θ_i being the basis function of the ith electrode with a voltage of 1V applied, other electrodes being held at 0 V. As implied by the boundary conditions, the justification of the basis function technique is only valid for electrostatic fields. For a typical ion trap the drive frequency will be on the order of or lower than 100 MHz, resulting in a minimum wavelength of 3×10^6 μm. The rf electrodes in an ion trap usually have a length on the order of $10 - 100 \times 10^3$ μm, which is several orders of magnitude smaller than the wavelength of the applied rf potential and therefore this assumption can be made.

Two-Dimensional Potentials of Linear Surface Traps

Using the described basis function technique and equation 2.22, the potential of a surface trap geometry can now be assembled using individual rectangular electrodes. In most surface traps [75, 77, 99, 100] the alternating potential is used to provide confinement in two dimensions and the confinement in the third is provided by a static potential, with the exception of two-dimensional trapping arrays [101, 102]. For the following investigation of trap depth and directions of principle motion in linear traps, only the alternating two-dimensional pseudopotential will be of interest. We therefore simplify equation 2.22 for two dimensions and the electrodes will be extended to infinite $y_1 \to -\infty$ and $y_2 \to \infty$ in y-direction, resulting in:

$$\Phi(x, z) = \frac{\phi}{\pi} \{ \arctan \left[\frac{(x_2 - x)}{z} \right] - \arctan \left[\frac{(x_1 - x)}{z} \right] \} \tag{2.31}$$

We start by calculating the pseudopotential for a trap geometry made up of two rf and three dc rails, also known as a 5-wire geometry [75], and illustrated in Fig. 2.7 (a). Making use of the basis function technique we can find the pseudopotential for this geometry:

$$\psi(x, z) = \frac{e^2}{4m\Omega^2} (\nabla(\Phi(x, z)_{a1,a2} + \Phi(x, z)_{b1,b2}))^2 \tag{2.32}$$

Here e is the charge of the trapped ion, which is commonly equal to the elementary

charge. In Fig. 2.7 (a) the resulting pseudopotential for an example case is plotted in two dimensions, showing a potential minimum at x_0 where the ion is trapped and the so-called escape point x_∞, at which the ion leaves the trapping potential should it acquire enough energy Ξ to reach it. For this example the applied potential is equal to $\phi = 200 \cos(2\pi\ 31 * 10^6 t)$. The potential plotted along the z-axis at $x = 0$ shown in Fig. 2.7 (b) illustrates this in more detail and also shows the trap depth as the potential distance between z_0 and z_∞, $\Xi = 0.11$ eV. Inset in Fig. 2.7 (b) shows a magnified section of the potential at the trapping point z_0. The potential lines are fitted with a parabolic function and the corresponding secular frequency is equal to $\omega_z = 2\pi \times 2.408$ MHz.

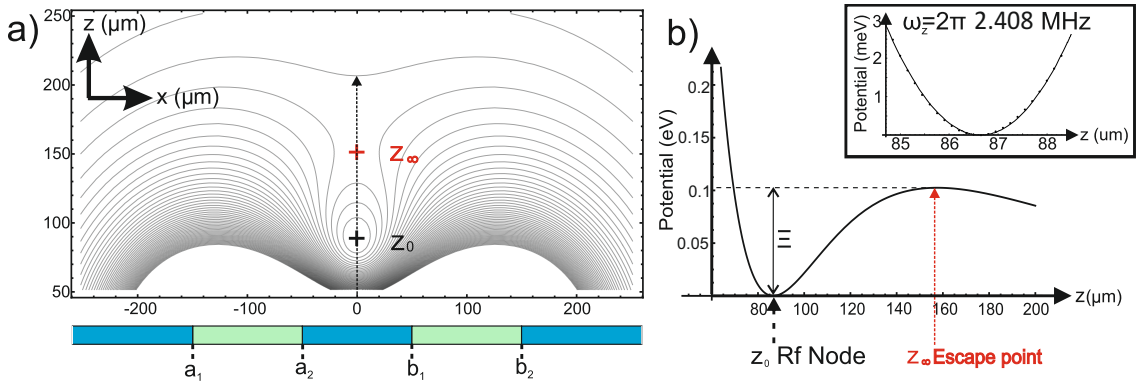


Figure 2.7: (a) shows the two-dimensional pseudopotential of a 5 wire geometry, the escape point z_∞ and rf node z_0 are marked. The potential applied to the green marked rf electrodes (a1-a2, b1-b2) is of amplitude $V_{rf} = 200$ V and frequency $\Omega = 2\pi \times 31$ MHz. All other electrodes (marked blue) are kept a 0 V. (b) Shows the two-dimensional potential at $x = 0$. A magnified version at z_0 is shown in the inset.

This method was used to investigate different electrode geometries and the corresponding trap depths in [103]. They showed that the equation for the trap depth for an ion height h is given by:

$$\Xi = \frac{e^2 V_{rf}^2}{\pi^2 m \Omega_{rf}^2 h^2}\kappa \quad \text{with } h = \frac{\sqrt{abc(a+b+c)}}{b+c} \tag{2.33}$$

Here κ is a geometric factor with $a = b_1 - a_2$, $b = a_2 - a_1$, $c = b_2 - b_1$ and given by:

$$\kappa = \left[\frac{2\sqrt{abc(a+b+c)}}{(2a+b+c)(2a+b+c+2\sqrt{a(a+b+c)})}\right] \tag{2.34}$$

Using equation 2.33 we can estimate the trap depth for the electrodes described in Fig. 2.7 to be 0.108 eV, which is in agreement with the depth that was read off the potential shown in Fig. 2.7 (b). For symmetric rf electrodes $b = c$ and setting the ratio of $b/a = 3.7$ gives

the highest geometric factor $\kappa = 0.023$ and the maximum depth that can be achieved for a given ion height h. Such high ratios $b/a = 3.7$ between rf rail separation and width however lead to wide rf rails and consequentially to a higher capacitance of the rf electrodes. Depending on the vertical structure of the trap the capacitance can become so high that it leads to a dramatic decrease in the rf resonator performance as shown in [104]. Rf resonators are used to apply low-noise high voltage potentials to ion traps and are essential for the trap operation. As presented in [103], ratios of at least $b/a = 1.5$ maintain a high $\kappa = 0.0177$ without the trap depth dropping below 75% of the original value.

Besides trap depth and secular frequency the angle between principal axis and trap surface normal can be investigated. Principal axes are the axes of secular motion of the ion in the trap and for the present case Fig. 2.7, of symmetric electrodes, normal and parallel to the trap surface. While the principal axis angles are not important for trapping an ion, they become critical when trying to efficiently laser cool the ion in all axis.

Principal Axis Rotation

To cool all uncoupled ion motions there needs to be a component of the laser cooling beam along all axes of motion. As the cooling beams are generally parallel to the surface (to avoid light scattering from the trap surface) a principal axis normal to the surface will not be cooled. The principal axis can be rotated using asymmetric rf rails ($b = 300$ μm, $c = 100$ μm for example) and all axes will be cooled. The pseudopotential of a trap with asymmetric rf electrodes is shown in Fig. 2.8 (a) and the rotation is clearly visible. Another option to rotate the principal axis without widening one rf rail is to combine the rf quadrupole potential with a dc quadrupole potential, using four dc voltage rails as presented in [100]. The pseudopotential for this case is shown in Fig. 2.8 (b). Two inner dc electrodes of width 10 μm and two outside the rf rails of width 25 μm, with less than 2 V applied result in a 16.29 $^\circ$ rotation. For this configuration almost any arbitrary rotation controllable via the applied dc potentials can be achieved and the capacitance does not increase due to wider rf rails.

Hessian Matrix

To calculate the exact rotation angle with respect to the trap surface one can make use of the Hessian Matrix $\mathcal{H}$ [105]. The Hessian matrix contains the second derivatives of a

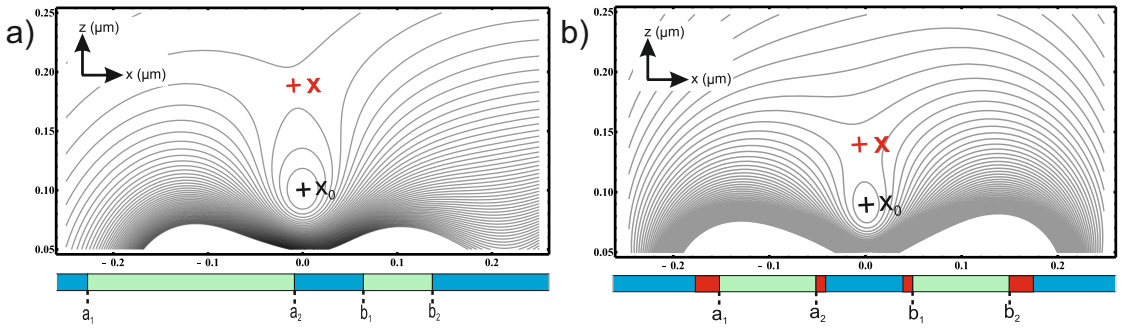


Figure 2.8: (a) Rotated pseudopotential for an asymmetric electrode geometry with 3:1 rf electrode width ratio, resulting in a rotation of 8.51 °. (b) Principal axis rotation using four dc rails (red), achieving a rotation of 16.29 ° with < 2 V applied to the electrodes.

multi variable function, in the case of an ion trap the pseudopotential ψ at the rf node x_0, z_0, and is a real and symmetric matrix. The two-dimensional Hessian Matrix $\mathcal{H}$ for ψ is,

$$\mathcal{H}(\psi(x,z)) = \begin{pmatrix} \frac{\partial^2\psi}{\partial^2 x}(x_0,z_0) & \frac{\partial^2\psi}{\partial x \partial z}(x_0,z_0) \\ \frac{\partial^2\psi}{\partial z \partial x}(x_0,z_0) & \frac{\partial^2\psi}{\partial^2 x}(x_0,z_0) \end{pmatrix} \tag{2.35}$$

and represents the potential curvature at the rf node x_0, z_0. The eigenvector $\mathbf{e}_{max}$ corresponding to the largest eigenvalue λ_{max} showing the direction of largest curvature, the eigenvector $\mathbf{e}_{min}$ with the smallest eigenvalue λ_{min} the direction of least curvature. The eigenvectors are orthogonal to each other[2] and are aligned with the principal axes of motion. Since the eigenvalues λ_i give the curvature of the field in the direction of the eigenvector $\mathbf{e}_i$ they can also be used to determine the frequency of the secular motion $\omega_{\mathrm{sec},i}$ in the corresponding principal axis with the relationship [80]:

$$\omega_{\mathrm{sec},i} = \sqrt{\frac{m}{\lambda_i}} \tag{2.36}$$

Now to determine the angle α between the surface normal $\mathbf{n}$ and the eigenvector $\mathbf{e}_i$ we can use the dot product of two vectors

$$\cos\alpha = \frac{\mathbf{n}\cdot\mathbf{e}_i}{\|\mathbf{n}\|\|\ \mathbf{e}_i\|} \tag{2.37}$$

with $\|\mathbf{n}\| = \sqrt{\mathbf{n}\cdot\mathbf{n}}$. The rotation angle for the example presented in Fig. 2.8 (a) is $\alpha = 8.51$ °, with corresponding secular frequencies $\omega_x = 2\pi \times 2.17$ MHz and $\omega_z = 2\pi \times$

[2] $\mathcal{H}$ is a real symmetric matrix

2.15 MHz. Using a static quadrupole to rotate the axes as shown in Fig. 2.8 (b) the following values were calculated: $\alpha = 16.29\ ^\circ$, $\omega_x = 2\pi \times 2.58$ MHz and $\omega_z = 2\pi \times 2.21$ MHz.

We can also compare the secular frequencies derived from the Hessian matrix eigenvalues λ_i for the symmetric case shown in Fig 2.7, $\omega_z = 2\pi \times 2.41$ MHz with the secular frequency equation 2.19 given for the pseudopotential approximation with $a = 0$:

$$\omega_{x,\mathrm{hyp}} = \frac{eV}{\sqrt{2}m\Omega R^2} = 2\pi \times 8.71 \text{ MHz} \tag{2.38}$$

The rather large discrepancy is not entirely unexpected as the equation 2.19 for $\omega_{x,\mathrm{hyp}}$ and the q-parameter equation 2.17 were defined for a perfect quadrupole field. In the following section discrepancies and issues caused by deviations from the perfect hyperbolic field will be discussed in more detail.

Perturbations in Surface Trap Potentials

In [106] this discrepancy was investigated further and a geometric factor η was defined to compare values of q and ω for non-hyperbolic traps with the values given by the pseudopotential approximation. The geometric factor is defined as $\eta = \omega_{x,hyp}/\omega_x = q_{x,\mathrm{hyp}}/q_x$. As previously discussed the secular frequencies can be obtained by determining the Hessian matrix eigenvalues at the trapping position of the simulated pseudopotential. The geometric factor does not have to be considered for this calculation. When calculating the q-parameter using equation 2.17, the pseudopotential approximation can not be used and the resulting value will be false if η is not taken into consideration. Using a more basic definition of $q_x = 2\sqrt{2}\ \omega_x/\Omega$ given in [107] that only depends on the drive frequency Ω and the secular frequency ω_x, this issue can be avoided.

A different effect caused by deviations from a perfect quadrupole potential arises if fields of higher order[3] $N_{\mathrm{per}} > 2$ cause perturbations and instabilities of the ion motion at certain frequencies [108]. These instabilities can occur when the secular frequencies are equal to:

$$n_x\omega_x + n_z\omega_z = \Omega, \text{ with } N_{\mathrm{per}} = \mid n_x \mid + \mid n_z \mid \text{ and } n_x, n_z \,\epsilon\, \mathbb{N} \tag{2.39}$$

Using the relation between a and q parameter and the secular frequency given in equation

[3] $N_{\mathrm{quadrupole}} = 2$

2.19, a new stability diagram can be plotted which contains the possible instabilities, dramatically complicating it as shown in Fig. 2.9.

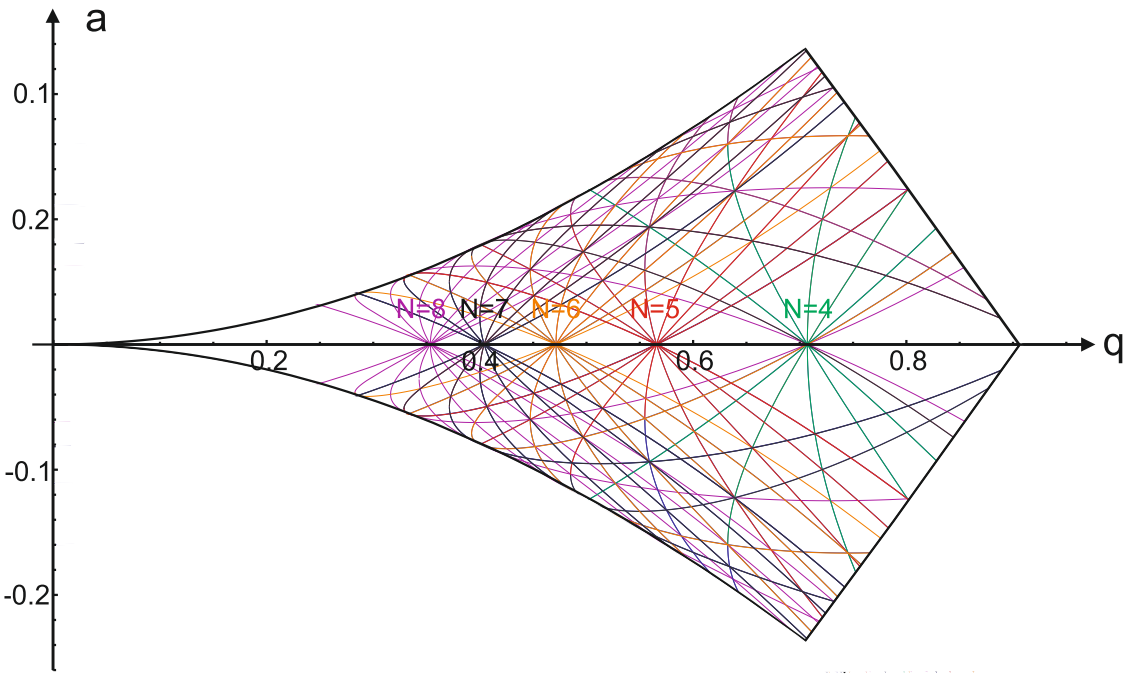


Figure 2.9: Modified Stability diagram with lines representing instability caused by perturbations to the quadrupole field of order N.

Higher order fields $N_{\text{per}} > 6$ are of smaller magnitude and were experimentally not observed in [108]. Although the instability lines become denser for $q < 0.5$ this region is preferable for trapping, since the perturbations will not affect trapping.

Additionally the pseudopotentials of the previously discussed asymmetric electrode geometries will vary significantly from a perfect quadrupole potential at positions corresponding to the trap depth. If we look at the pseudopotential of an asymmetric trap along the z-axes at $x = 0$ shown in Fig. 2.10 we can see that there are two positions z_{min} and z_{exit} that correspond to a potential value of Ξ. Position z_{min} is commonly not considered to be of importance for trapping, but investigations presented in [109, 110] have shown that the ion trajectory can become unstable at this point if the deviation from a perfect quadrupole is too large.

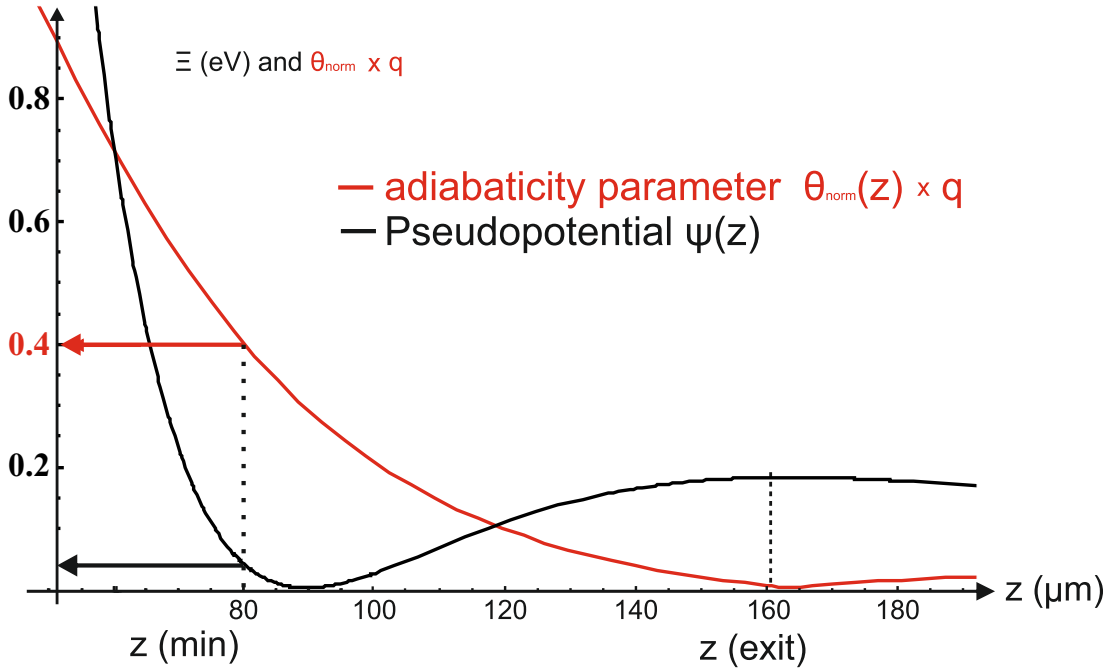


Figure 2.10: Adiabaticity parameter and pseudopotential plotted for $x = 0$ vs ion height and potential barrier height at $z_{exit} = 0.18eV$. At $z_{min}, \Xi = 0.51$ the adiabaticity parameter $\theta_{norm}(x_0, z_{min})$ is larger then 0.4 and stable trapping is not possible.

The instabilities are caused by the increasing inhomogeneity of the electric field. The inhomogeneity of the trapping field $E(x, y, z)$, can be quantified using a so-called adiabaticity parameter θ, that depends on the gradient of the electric field defined in [91]:

$$\theta = \frac{2e \mid \nabla E(x, y, z) \mid}{m\Omega^2} = \frac{2e \mid \triangle \Phi(x, y, z) \mid}{m\Omega^2} \tag{2.40}$$

In a homogenous field θ is zero, in a perfect quadrupole potential as shown in Fig. 2.2 it is constant, and for the pseudopotential $\psi(x, z)$ shown in Fig. 2.7 it is a function of x and z.

At the rf nil position (x_0, z_0) the field shown in Fig. 2.7 is a perfect quadrupole field and we will normalize the adiabaticity parameter to $\theta(x, z)_{\text{norm}} = \theta(x, z)/\theta(x_0, z_0)$. For values of $\theta_{\text{norm}}(x, z)$ q, larger then 0.4 it has been shown theoretically [91], [109] and experimentally [110] that the ion trajectories become unstable and the ion can be lost despite sufficient trap depth and suitable stability parameters $a = 0$, $q < 0.5$.

If we plot $\theta_{\text{norm}}(x_0, z)$ q and the pseudopotential $\psi(x_0, z)$, see Fig. 2.10, it can be seen that $\theta_{\text{norm}}(x_0, z_{\text{min}})$ $q = 0.514$, stable trapping is not possible although the ion's energy is below the trap depth. To achieve the maximum trap depth the q-parameter needs to be

lowered from [4] $q = 0.293$ to $q = 0.228$, which brings the value of $\theta_{norm}(x_0, z_{min})$ q below 0.4 and the maximum trap depth is again determined by the pseudopotential value at the exit point z_{exit} .

2.1.4 Numerical Simulations of Electric fields

For many linear ion trap structures the analytical method described and used in the last section is sufficient. For complex trapping structures with large gaps and non rectangular shaped electrodes its use is limited. In the centre of junctions, where several linear trapping sections are combined, the gaps are typically of the same size as the electrodes and the analytical method is insufficient. In these cases a numerical simulation has to be used to obtain the electric field of the ion trap geometry.

Comparison between Numerical Simulations and Analytical Approximation

A comparison between pseudopotentials acquired using the analytic gapless plane approximation method and a numerical method of a linear section with large gaps is shown in Fig. 2.11. For the numerical simulation a linear section with 5 μm high electrodes, 10 μm wide gaps between the 70 μm wide rf rails, 20 μm wide central ground rail and outer ground electrodes was simulated. This structure also has a ground plate placed 10 μm below the surface of the electrodes. In the analytical approximation two 70 μm wide rf rails separated by 40 μm were used. For both simulations the trap voltage is set to $V = 120$ V and drive frequency is $\Omega = 2\pi \times 55$ MHz. The two pseudopotentials are compared in Fig. 2.11.

The comparison highlights the issues when using a gapless plane approximation, the ion height differs greatly between the two potentials $z_{0,\text{An}} = 42.4$ μm, $z_{0,\text{Num}} = 35.9$ μm, also the derived secular frequencies $\omega_{z,\text{An}} = 2\pi \times 3.83$ MHz, $\omega_{z,\text{Num}} = 2\pi \times 5.05$ MHz and trap depth $\Xi_{z,\text{An}} = 0.08$ eV, $\Xi_{z,\text{Num}} = 0.11$ eV vary greatly. For this comparison extreme geometries were used, more common gap widths and electrode size would give more similar results for both methods.

[4] to lower the q parameter the drive frequency was changed from $\Omega = 2\pi \times 30$ MHz to $\Omega = 2\pi \times 34$ MHz

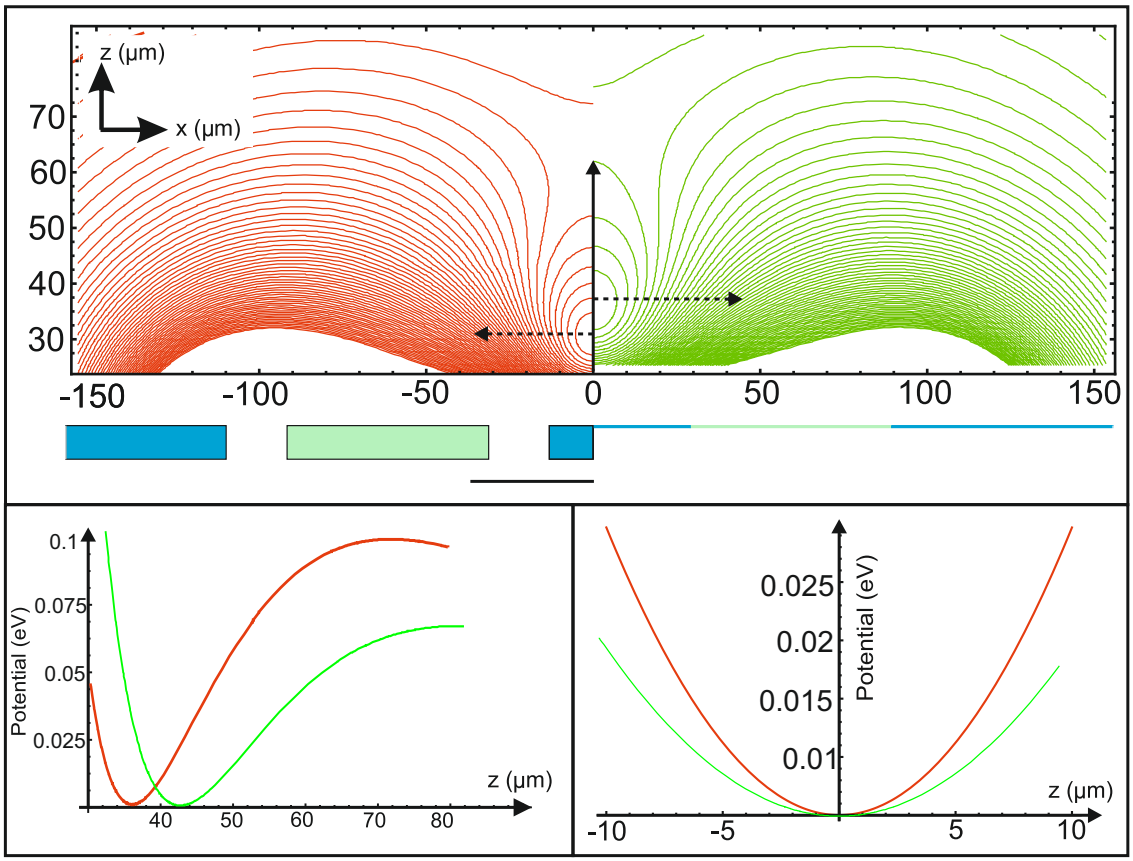


Figure 2.11: Comparison of the pseudopotential between the analytic gapless plane approximation (70 μm wide rf rails, marked green, separated by a 40 μm ground rail, marked blue) and a numerical method. For the numerical approach an electrode geometry with 10 μm gaps between 70 μm wide rf rails, 20 μm wide central ground rail and an additional ground plate 10 μm below the electrodes was simulated.

Numerical Simulation Tools

The two most commonly used numerical methods for ion trap simulations are the boundary element method (BEM) and finite element method (FEM) [98,111,112]. A brief description of both methods will explain why the BEM was used for almost all simulations in this thesis.

FEM simulations determine the electric field of electrodes by laying a mesh over the defined volume of interest V, in our case the entire trapping region and electrodes. For each node of the mesh, Laplace's equation under the corresponding Dirichlet boundaries conditions is solved. The electric field of the trap is obtained by adding up all individual results [98]. The computationally challenging part is to solve large three-dimensional sparse matrices. Also the resulting fields will have unphysical discontinuities between nodes, which need to be smoothed. Depending on the volume and simulation accuracy unreasonable amounts of calculations need to be performed [112].

The BEM simulates the electric field inside a volume of interest created by charge distributions on the boundary of the volume. In contrast to the FEM the mesh is now placed on the boundaries. For each individual area of the mesh the Laplace's equation of the corresponding Dirichlet problem is solved. Solving these requires a two-dimensional matrix inversion, which is the challenging part of this method. The solutions for each mesh point can then be used to accurately express the electric field at any point inside the volume of interest. The BEM is optimized for geometries, like ion trap electrode geometries, where all relevant structures are placed on the boundaries.

The electric field produced by the BEM is more accurate and shows no discontinuities caused by laying a mesh over the volume of interest. Additionally only two-dimensional instead of three-dimensional matrices have to be solved, making BEM the quicker method [112].

Several commercial programs are available that perform BEM simulations. One of the most popular tools for ion trap simulation is Charged Particle Optics (CPO) [5], which was used when designing the macroscopic trap used for experiments described in section 3.5.1 by Robin Sterling [113].

For the design process of microfabricated ion traps presented in this thesis a program known as the BEMSolver was used. This tools is based on the CERN tool Root and com-

[5] by Electronoptics

bines a matrix inversion technique with a tool to read in the electrode structures from a .dxf file. Compared to CPO it makes it possible to shift the design process to a CAD program like AutoCAD and is also able to simulate a larger amount of individual polygons. As an example Fig. 2.12 (a) shows a junction designed in AutoCAD and the pseudopotential in Fig. 2.12 (b) visualized from the BEMSolver output using Mathematica.

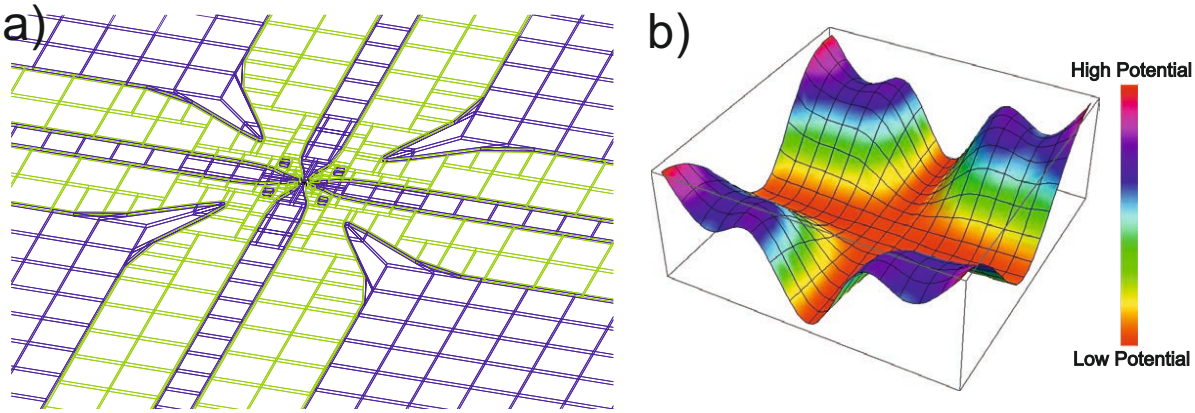


Figure 2.12: (a) Junction structure designed in AutoCAD consisting of four-sided '3D Polygons'. The file is read in by the BEMSolver and the electric field is simulated in a defined region. (b) The output data from the BEMSolver can be visualized using Mathematica. Here a 3D plot shows the pseudopotential in x and y-direction at the ion height.

2.2 Manipulation of Ion Motional States

The pseudopotential presented in the last sections can be approximated with a harmonic potential well for ions with low motional energy. To describe the uncoupled motion in one axis of motion a one-dimensional quantum harmonic oscillator can be used. The Hamiltonian for such an oscillation is:

$$H = \hbar\omega(a^\dagger a + \frac{1}{2}) = \hbar\omega(N + \frac{1}{2}) \tag{2.41}$$

Here ω is the secular frequency, $a^\dagger$ and a are operators which raise and lower the motional state of the ion respectively. The operators can be expressed as $a^\dagger|n\rangle = \sqrt{n+1}|n+1\rangle$ and $a|n\rangle = \sqrt{n}|n-1\rangle$. When an ion moves up one motional level it gains one motional quantum of kinetic energy $\hbar\omega$. In equation 2.41 the number operator N represents the ion's total number of motional quanta.

Based on the quantum harmonic oscillator description of the ion motion we can now

discuss mechanisms that lower or increase the number of motional quanta for the ion's motion.

2.2.1 Doppler Cooling of Motional States

Laser cooling reduces an ion's motional quanta number using the momentum transfer of photons to the ions. A semi-classical description of laser cooling is given below, following [114]. For any momentum transfer between a photon and the ion a two-level dipole transition has to be excited. We assume a two-level system with transition frequency ν_{trans}, whose upper state has a width $\Gamma = \frac{1}{\tau}$, with a decay time τ on the order of 10^{-6} sec and laser light at frequency ν_{laser}. If the ion absorbs a photon it gains its momentum $p = \hbar k$, where k is the wavevector of the photon. The system is now in the upper state and due to spontaneous emission it will scatter a photon in an arbitrary direction after $\langle t \rangle = \tau$. The photons are scattered in a random direction and the resulting momentum transfer will average to zero over time.

To simplify further calculations only the cooling of motion in the x-direction will be considered. The wavevector in the x-direction will be k_x. The steady-state population ρ_{excited} of the excited state is given by [114],

$$\rho_{\text{excited}}(v_x) = \frac{s/2}{1 + s + (2\Delta_{eff}/\Gamma)} \tag{2.42}$$

s is the so-called saturation parameter and depends on the intensity I of the cooling beam $s = I/I_{\text{sat}}$, I_{sat} is a constant of the transition. The effective frequency shift of the ion from resonance is $\Delta_{\text{eff}} = \nu_{\text{trans}} - \nu_{\text{laser}} + \Delta_{\text{Dop}}$. The ion's velocity v_x with respect to the wavevector k_x results in a Doppler shift of the laser frequency experienced by the ion,

$$\Delta_{Dop} = -k_x v_x \tag{2.43}$$

The rate of scatter events is then given by $R(v_x) = \Gamma \rho_{\text{excited}}(v_x)$. Each scattering event exerts a force $F = \hbar k_x$ onto the ion, pushing it away from the laser direction. If the scattering rate were to be higher while the ion is moving towards the cooling beam than when moving away the net momentum transfer from photon scattering would reduce the motional energy of the ion.

During one secular oscillation of the ion the Doppler shift oscillates between the positive

and negative value of the maximum Doppler shift $\Delta_{\text{Dop, max}} = \sqrt{2E/m} \cdot k_z$, which depends on the motional energy E and mass m of the ion.

The probability $P_{Doppler}(\Delta_{Dop})$ of a certain Doppler shift during the oscillation is presented in Fig. 2.13. Overlapping the Doppler shift probability with the Lorentzian transition line profile $L = \Gamma\sqrt{1+s}$ illustrates that the probability of a photon absorption is higher when the ion has a Doppler shift corresponding to movement towards the beam (region marked red) then when moving away (blue) if the laser beam is detuned to a shorter frequency then the dipole transition. The ion loses motional energy and is cooled.

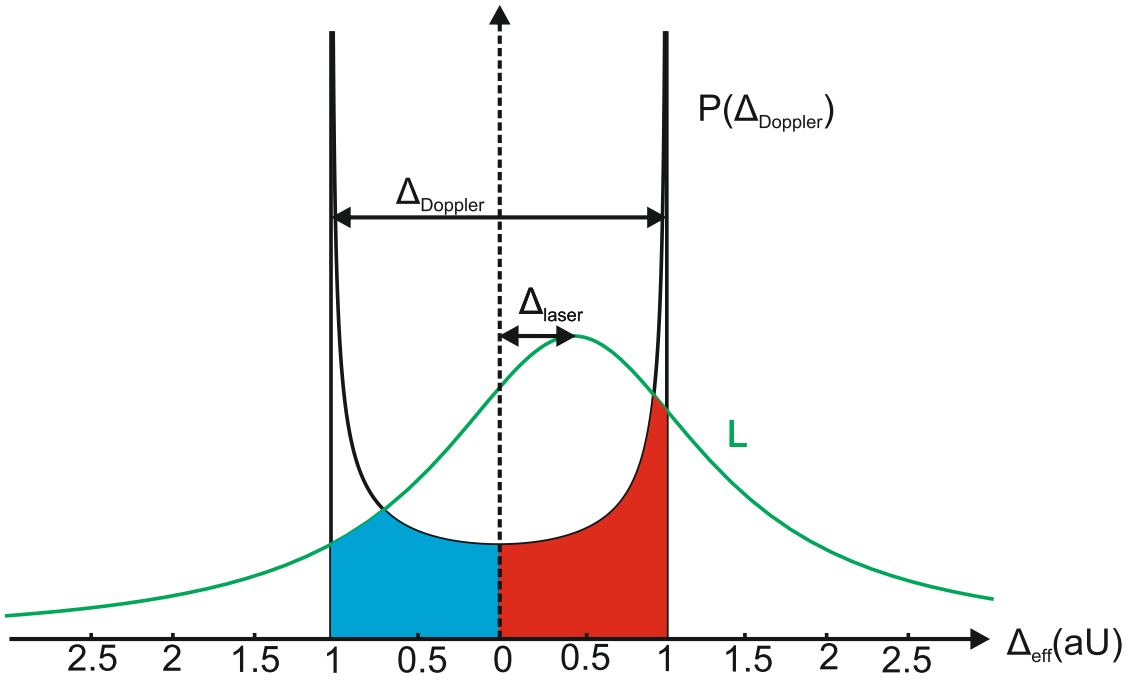


Figure 2.13: Doppler shift probability $P_{Doppler}(\Delta_{Dop})$ and Lorentzian transition line width L. Centre of the probability $P_{Doppler}(\Delta_{Dop})$ is shifted by $\Delta_{laser} = \nu_{trans} - \nu_{laser}$ equal to the laser detuning from resonance. Red areas mark the overlap of Doppler probability of the ion moving towards the beam with L, blue area for the ion moving away from the beam.

The ion will continue to cool until the Doppler cooling rate reduces to equal the heating rate, caused by isotropic emission of the absorbed photons [115] during cooling.

$$\left(\frac{dE}{dt}\right)_{recoil} = \frac{4(\hbar k_z)^2}{\times} 32m\frac{dN}{dt} \tag{2.44}$$

An equilibrium between heating and cooling is reached for a detuning of $\Delta_{\text{laser}} = \frac{\Gamma}{2}$ and the resulting limit of the Doppler cooling is equal to [115],

$$E = \frac{1}{2}\hbar\nu_{\text{trans}} = k_B T \tag{2.45}$$

2.2.2 Heating of Motional States

In addition to photon recoil there exist other sources of heating caused by electric noise, which increase the ion's motional energy during periods without cooling. Most quantum operations have to be performed without a cooling beam and if the electric noise causes too much heating, the fidelity of these operations can be severely reduced. Detailed descriptions of the influence of electric field noise on heating rates based on the perturbation theory were given in [116] and [117]. Electric field noise power spectral density $S_E(\omega)$ is related to the increase in number of motional quanta dN/dt according to:

$$\frac{dN}{dt} = \frac{q^2}{4m\hbar\omega}\left(S_E(\omega) + \frac{\omega^2}{2\Omega^2}S_E(\Omega \pm \omega)\right) \tag{2.46}$$

The second term $S_E(\Omega \pm \omega)$ only occurs in the two radial axes, and is caused by perturbations at frequencies $\Omega \pm \omega$. Commonly the dominant source of electric field noise at frequencies $\Omega \pm \omega$ will be the rf voltage source, other noise sources are heavily filtered at frequencies above ω and due to the commonly very low ratio $\omega^2/(2 \times \Omega^2)$ this term can be neglected if a high quality rf source is used. The heating rate is then given by:

$$\frac{dN}{dt} = \frac{q^2}{4m\hbar\omega}S_E(\omega) \tag{2.47}$$

Inherent to any electric circuit a temperature dependent noise, called Johnson noise, will be present. The noise is induced by the voltage generating circuits and additional noise is picked up from external sources on the wiring to the electrodes. The noise density corresponding to Johnson noise can be described as $4k_BTR(\omega)$, which depends on the temperature T and frequency dependent resistance $R(\omega)$. Noise densities $S_{supply}(\omega)$ and $S_{external}(\omega)$ correspond to noise inherent to voltage supplies connected to dc electrodes and electromagnetic interference picked up on the wiring of the dc electrodes. Both can only be determined experimentally.

If the ion trap field noise density $S_E(\omega)$ is caused by these noise sources it would scale with a r_0^{-2} dependency, r_0 being the distance of the trapping centre to the closest electrode. When measuring the electric field noise scaling in an ion trap it was found that it scales

with $\sim r_0^{-4}$ as presented in [118]. An additional term $S_{\text{anomalous}}(\omega)$ must be added and we can write the heating rate as [116]:

$$\frac{dN}{dt} = \frac{q^2}{4m\hbar\omega}\left(\frac{4k_BTR(\omega)}{r_0^2} + S_{\text{supply}}(\omega, r) + S_{\text{external}}(\omega, r) + S_{\text{anomalous}}(\omega, r)\right) \tag{2.48}$$

The additional term $S_{\text{anomalous}}(\omega)$ is commonly dominant over the previously discussed noise densities and the cause is not yet fully understood. The related motional heating is commonly known as anomalous heating. There are indications that the noise is independent of the supplied voltage and depends on the trap electrode temperature [118–120] and possibly chemical composition of the electrode surfaces [86, 87, 121]. The corresponding field noise also shows a $S_E \propto 1/\omega$ dependency and so the heating rate scales with $\propto 1/\omega^2$. A more detailed investigation into causes of field noise will be given in chapter 3.

2.3 Internal States of Yb Ions and Yb Quantum Information Processing

In this thesis the $^{171}Yb^+$ and $^{174}Yb^+$ ions will be used and the internal states relevant to Doppler cooling and quantum information processing will be discussed next. Similar to other commonly used ions Yb^+ has one orbiting electron in the most outer shell, making it a hydrogenic ion and resulting in a simple level structure [75]. Ytterbium isotopes with even atomic mass numbers $^{176}Yb^+$, $^{174}Yb^+$, $^{172}Yb^+$, $^{170}Yb^+$ have no nuclear spin and therefore energy levels without hyperfine splitting. Isotopes with uneven atomic mass numbers have a nuclear spin and hyperfine split levels.

The high natural abundance of $^{174}Yb^+$ (31.83%, [122]) and lack of hyperfine levels makes it an ideal isotope for initial trapping and first experiments, but less suitable for quantum information processing.

Hyperfine levels of $^{171}Yb^+$ can be used as quantum bits. Commonly either hyperfine levels $^{171}Yb^+$, $^{43}Ca^+$, $^{9}Be^+$, $^{111}Cd^+$, $^{25}Mg^+$ or the optical transitions $^{40}Ca^+$, $^{88}Sr^+$, $^{172}Yb^+$ between the ground state and a metastable state [75] of ions are used as qubit states. Hyperfine states have lifetimes of years, optical metastable states on the order of seconds.

2.3.1 Photoionization of Yb Atoms and Relevant Energy Levels

The relevant energy level diagram for ionizing Yb via photoionization is similar for all isotopes and is shown in Fig. 2.14. Photoionization has compared to electron impact ionization the benefit that the ion can be ionized directly in the trapping centre and no charge built up on trap electrodes can occur. Photoionization is used to obtain Yb^+ from a neutral Yb beam based on a two stage ionization process, rather then using the direct transition at $\lambda_{ionize} = 199$ nm. Laser sources at 199nm are more expensive and complicated to operate compared with semiconductors diode lasers that can be used for two stage ionization. The ytterbium atom is excited to the $^1P_1$ state from the ground state $^1S_0$ and then ionized by any laser of wavelength $\lambda < 394$ nm. The exact wavelength of the $^1S_0 \rightarrow ^1 P_1$ transition will vary from isotope to isotope, wavelengths for important Yb isotopes can be found in [123].

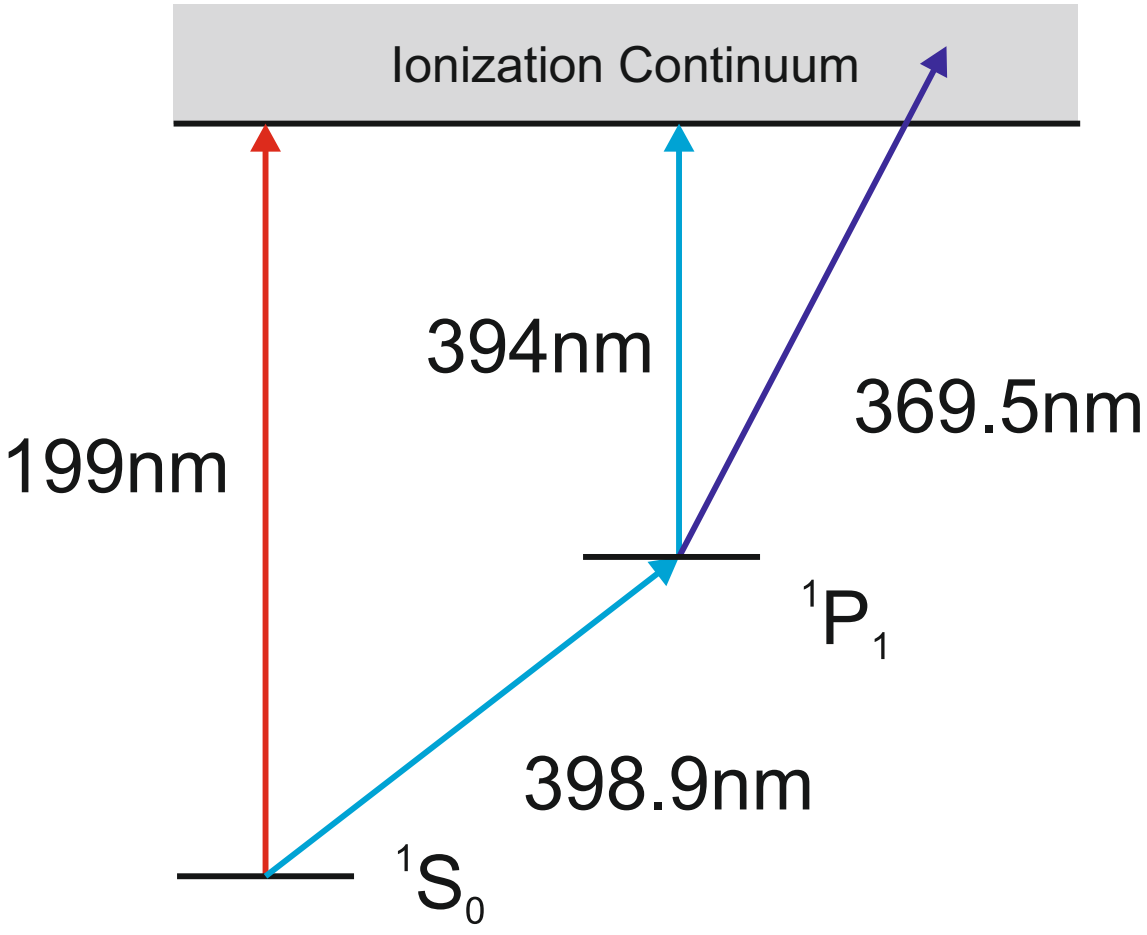


Figure 2.14: Energy level diagram for the photo-ionization of neutral Yb atoms [124].

2.3.2 Energy Levels used for Doppler Cooling of Yb Ions

The transition used to Doppler cool $^{174}Yb^+$ is the $^2S_{1/2} \leftrightarrow^2 P_{1/2}$ dipole transition shown in Fig. 2.15, with a transition wavelength of $\sim$ 369nm. Linewidth and decay rate of the transition is $\Gamma/2\pi = 19.6$ MHz, allowing for fast cooling and fluorescence detection. The two level transition is complicated by a potential decay into $^2D_{3/2}$ from the $^2P_{1/2}$ state with a 0.5% probability. To bring the ion back into the $^2S_{1/2}$ state the $^2D_{3/2} \leftrightarrow^3 D[3/2]_{1/2}$ transition is driven using a laser at $\sim$ 935nm, allowing further decay from $^3D[3/2]_{1/2}$ to $^2S_{1/2}$. Under certain conditions, usually caused by collision of the ion with background gas, the ion can be transferred from $^2D_{3/2}$ to the $^2F_{7/2}$ state where it would go dark and remain until eventually lost. To avoid this scenario another laser at 638 nm is used depopulating the $^2F_{7/2}$ state via the $^2F_{7/2} \leftrightarrow^3 D[5/2]_{5/2}$ transition from which the ion decays back to $^2D_{3/2}$ state.

To efficiently Doppler cool $^{174}Yb^+$ ions three different lasers at 369 nm, 935 nm and 638 nm are used to drive the three transitions. All of these wavelengths can be produced directly with semiconductor diodes, which reduces cost and complexity of the required laser setup.

The cooling transitions for $^{171}Yb^+$ varies from the $^{174}Yb^+$ transitions due to the nonzero nuclear spin causing a splitting of the states. Figure 2.16 shows the energy levels of $^{171}Yb^+$ relevant for Doppler cooling. We can see that the dipole transition levels are split into hyperfine levels. The two hyperfine levels $^2S_{1/2} \mid F = 0\rangle$ and $^2S_{1/2} \mid F = 1\rangle$ have long lifetimes and can be efficiently addressed with laser and microwaves making them ideal qubits for quantum information processing.

As the ion can now decay into the $^2S_{1/2} \mid F = 0\rangle$ state the dipole transition $^2S_{1/2} \leftrightarrow^2 P_{1/2}$ can not be driven by a single wavelength anymore. Sidebands applied to the 369 nm laser at 14.7 GHz can drive the $^2S_{1/2} \mid F = 0\rangle \leftrightarrow^2 P_{1/2} \mid F = 1\rangle$ transition. Sidebands applied to the 935 nm laser at 2.21 GHz are used to drive the $^2D_{3/2} \mid F = 2\rangle \leftrightarrow^3 D[3/2]_{1/2} \mid F = 1\rangle$ transition. The 638nm laser wavelength is scanned to depopulate both $^2F_{7/2}$ hyperfine levels.

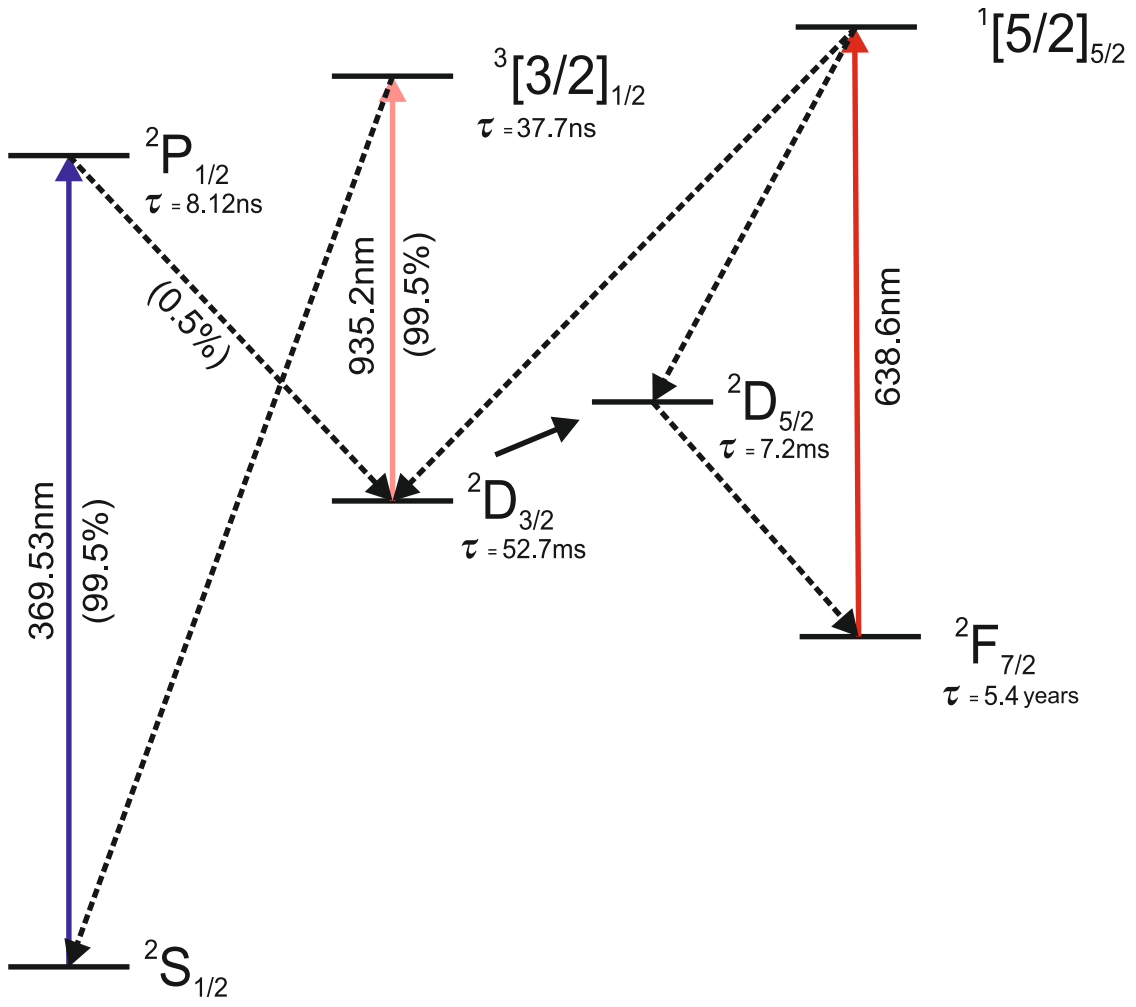


Figure 2.15: Relevant internal states of $^{174}Yb^+$ Doppler cooling with the life times of the relevant states. Laser driven dipole transitions are shown as solid lines with corresponding transition wavelength. Possible state decays are shown as dashed line with branching ratios and decay rates [124].

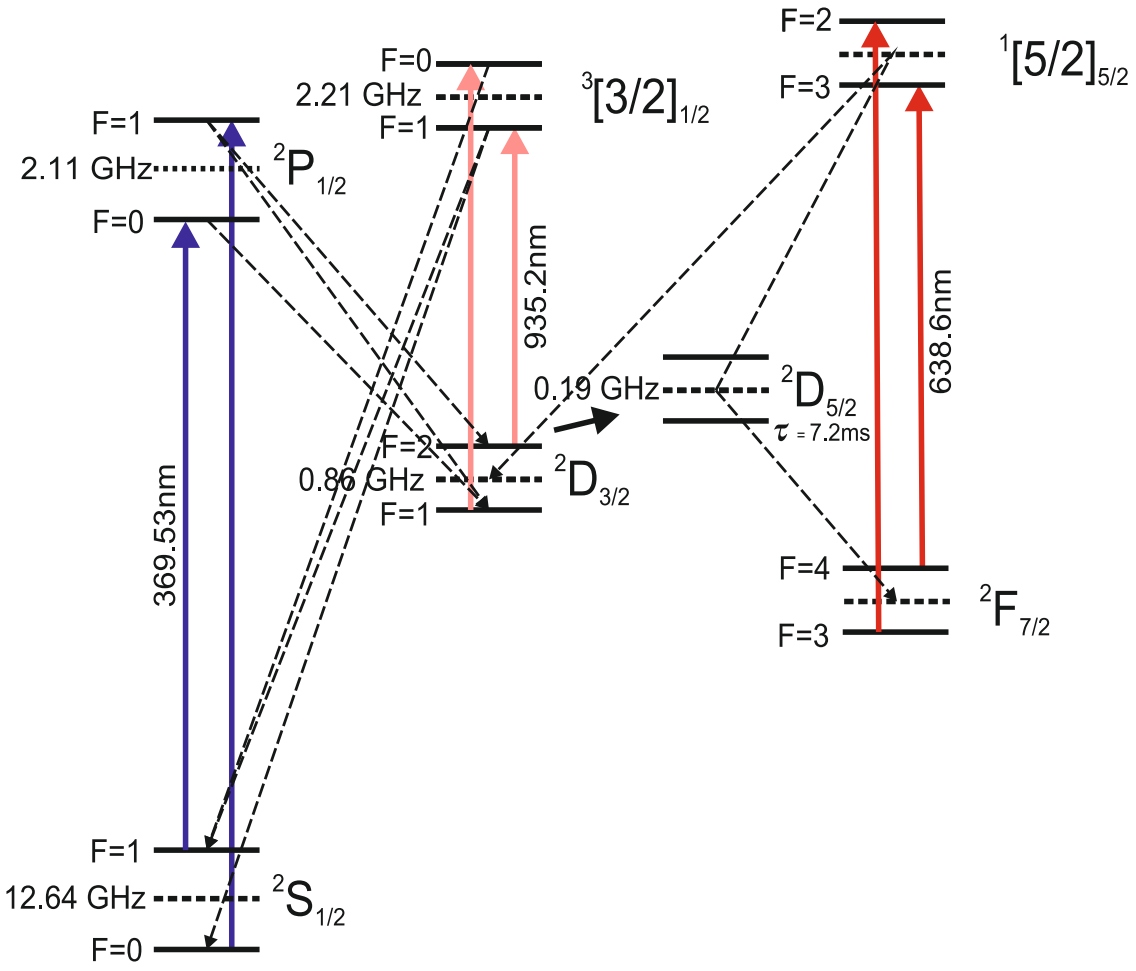


Figure 2.16: Internal states for $^{171}Yb^+$ Doppler cooling including the hyperfine splitting and possible decays [124].

2.3.3 Microwave Based Motional State Coupling

To entangle the previously discussed qubit states $^2S_{1/2} \mid F = 0\rangle$ and $^2S_{1/2} \mid F = 1\rangle$ of two $^{171}Yb^+$ ions the internal qubit states can be coupled to shared motional states of ions trapped in the same harmonic potential well. Coupling motional states to internal states requires the ions to be in so-called Lamb-Dicke regime reached when [125],

$$\eta^2(2n+1) << 1 \tag{2.49}$$

where $\eta = kx_0$ is the Lamb Dicke parameter, x_0 the amplitude of the secular motion, k the wavevector of an applied laser beam and n the ions motional quanta number. Additionally motional sidebands of the ions corresponding to the quantized Doppler shift need to be resolved. The strength of the sidebands is directly proportional to the Lamb Dicke parameter η, which needs to be on order of $\eta = 0.01$ [126] to resolve the sidebands.

If we try to resolve the sidebands of $^{171}Yb^+$ using microwaves instead of lasers, the Lamb-Dicke parameter becomes extremely small due to $\eta = k_\mu x$ with $k_\mu \sim 2\pi/2 \cdot 10^7$ nm compared to a laser driven transition $k_{laser} \sim 2\pi/369$ nm. This will prevent any sideband cooling and coupling of motional and internal states. A way to enhance the Lamb-Dicke parameter for microwaves was proposed in [127], by placing the ion in a magnetic field gradient $\triangle B$.

The gradient adds a position dependent component to the Zeeman splitting of the hyperfine levels during the secular motion and therefore increases/decreases the frequency difference between the hyperfine levels during on oscillation, as shown in Fig. 2.17. The motion dependent frequency shift depends on the strength of the gradient.

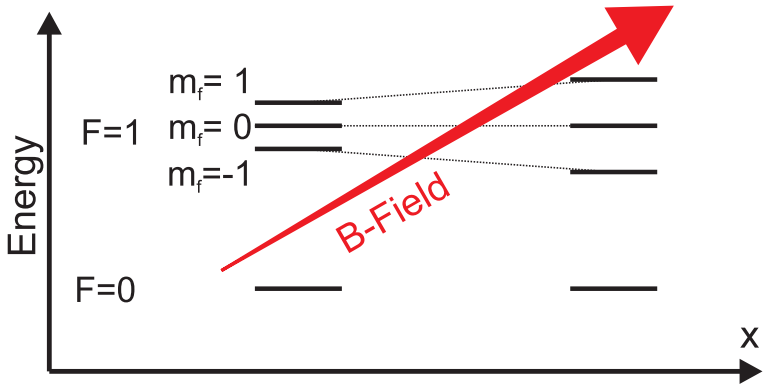


Figure 2.17: The gradient and therefore position dependent Zeeman shifts are illustrated for the magnetic field sensitive state $F = 1$.

A new effective Lamb-Dicke parameter $\eta_{\text{eff}} = \sqrt{\eta^2 + \varepsilon_c^2}$, where ε_c depends on the strength of the magnetic field gradient can be introduced. Experimentally a high enough η_{eff} was achieved to perform quantum operations with microwaves and resolve the sidebands [82, 83]. Due to the position depend shift of the hyperfine level we can also individually address qubit states of ions in a chain. Tuning the microwaves to the specific splitting will result in the state transition of only one ion in the chain, while the others are largely unaffected.

The absolute B-field strength created by current wires or permanent magnets for this scheme is on the order of 10-20 Gauss. This is expected to have a negligible effect on the trap stability and is only marginally larger than the strength of applied magnetic fields during normal trap operation [90].

Chapter 3

Ion Trapping Setup and Initial Experiments

Laser and imaging systems, vacuum chambers and voltage supply systems required to trap ions will be described in the following chapter. A macroscopic ion trap was used for initial Yb^+ trapping and various experiments including heating measurements presented in [90]. The model used for the heating measurements will be explained and results discussed in more detail.

3.1 Laser Systems and Locking

Ionizing and cooling Yb ions requires several lasers operating at different wavelengths (369 nm, 399 nm, 638 nm, 935 nm) as described in section 2.2.1 and 2.3.1. An additional laser at 780 nm is used as a reference to stabilize the others. All of the required wavelengths are accessible via direct diode lasers, but to generate light at 369 nm a sophisticated diode cooling setup is required. Instead a commercial frequency doubling system was used, based on a direct diode and tapered amplifier generating light at 738 nm, which is then frequency doubled.

Diode lasers are semiconductor devices that make use of an active region (in most cases a quantum well structure) were electrons and holes, supplied via highly doped p and n-regions, recombine. Applying an electric field across the laser structure forces the electrons and holes into the active region, resulting in the necessary population inversion and spontaneous emission of photons at wavelengths corresponding to the bandgap in the active

region as shown in Fig. 3.1 (a). When the wave guiding structure and active layer are placed in a cavity, see Fig. 3.1 (b), stimulated emission becomes dominant as the losses of the propagating cavity modes are compensated by the electrical pumping and the system starts to lase.

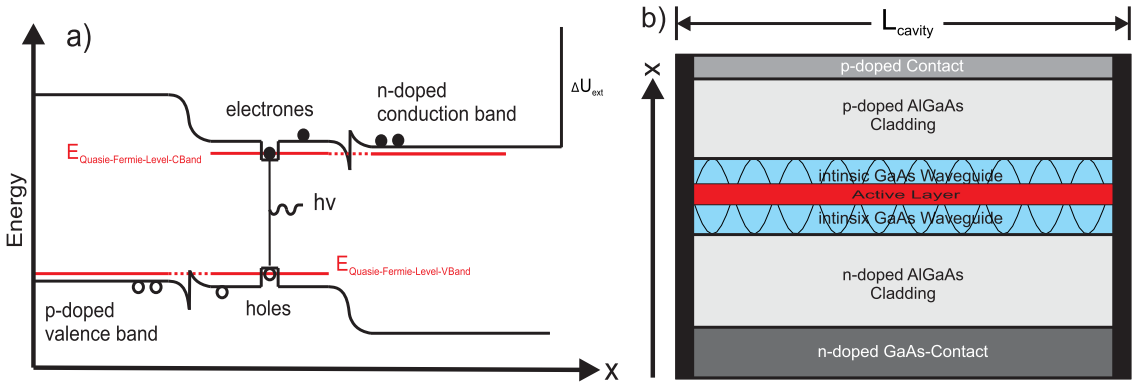


Figure 3.1: (a) Bandgap structure across the laser structure. At the quantum well the gap between conduction and valence band is the lowest. Holes and electrons will recombine there. The applied voltage forces the holes and electrons into the well resulting in population inversion (more holes on the left side and more electrons on the right side). (b) Horizontal structure of the laser with the two cavity mirrors.

The emission wavelength of the laser is determined by the active layer emission peak and length of the cavity, such a diode is also called Fabry-Perot laser. The emission spectrum is $\sim 2 * 10^6$ MHz broad, which is unsuitable for ion trap experiments where linewidths of a few MHz and sometimes as narrow as several Hz are necessary.

3.1.1 External Cavity Diode Lasers (ECDL) and Frequency Doubling System

External Cavity Stabilization

Several methods can be used to stabilize and narrow the linewidth of semiconductor lasers, for this thesis only the so-called external cavity method is used and will be discussed further [128].

This technique stabilizes and narrows the linewidth by placing the laser diode inside an additional external cavity. The front cavity mirror is made up of an angled refractive diffraction grating, which reflects part of the beam back into the laser. The back mirror of the laser cavity works as the second mirror. The diverging beam profile of the laser diode requires that the beam is collimated using an aspheric lens before the grating.

Now cavity modes of both cavities will have to overlap to achieve efficient lasing. The internal laser cavity can be tuned by changing the laser current and temperature, causing a change of the laser waveguide refractive index. The external cavity is tuned by mounting the diffraction grating on a piezoelectric actuator (PN PSt 150/4/5bS, Piezomechanik GmbH) allowing us change the grating angle and wavelength reflected back into the diode. The active layer gain peak, the cavity mode of the internal cavity and the external cavity need to be aligned for optimal laser power and narrow linewidth.

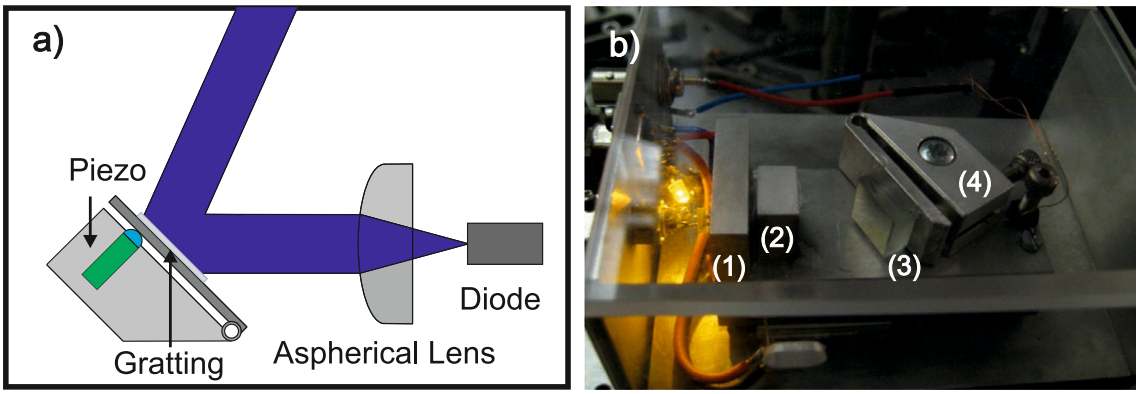


Figure 3.2: (a) Schematic of the external cavity diode laser setup, showing the laser diode, aspheric lens and grating. The violet beam represents the output beam overlapped with the reflected beam and also reflected out of the laser system. (b) Shows a picture of the in-house build ECDL. Laser diode is marked with (1), Collimating aspherical lens is (2), the diffraction grating is at (3) and the piezo with mount is at position (4).

With the ECDL setup slow drifts due to temperature fluctuations and faster frequency changes due to vibrations can be compensated if a feedback of the changes is given to the piezo controller. The ECDL setup is described in more detail by James McLoughlin in [129].

399 nm Stabilized Direct Diode Laser System

Laser light at 399 nm used for photo-ionization is provided by an in-house built ECDL system. The setup uses a commercial laser diode (PN DL-4146-301S, Sanyo) driven and temperature stabilized by a laser controller (PN ITC502, Thorlabs). The diode is placed inside an external cavity setup, see Fig. 3.2, with diffraction grating (PN GH13-24V) and aspheric lens (PN A390TM-A, Thorlabs). The laser output of the setup reaches up to 4 mW of stabilized 399 nm laser light.

369 nm Commercial Stabilized Doubling System

To drive the dipole Doppler cooling transition laser light at 369nm is required, which is generated by a commercial frequency doubling system (PN TA-SHG 36, Toptica photonics). An ECDL produces light at 738 nm with $\sim$ 60 mW output power, which is then amplified by a tapered amplifier to $\sim$ 350 mW. The light is then frequency doubled by a SHG (Second Harmonic Generation) crystal (Lithium Triborate). The conversion efficiency of SHG crystals scales with the incident laser intensity, hence the crystal is placed in a bow-tie cavity. The cavity increase the intensity of light at 738 nm passing through the crystal and improves the conversion efficiency further via a multi-pass configuration. Under optimal conditions the doubler system produces up to 60 mW output power of 369 nm light.

When cooling $^{171}Yb^{+}$, transitions from both ground-state hyperfine levels need to be addressed, see Fig. 2.16. We do this by applying sidebands at 14.7 GHz to the laser light. Such high frequency sidebands can not be applied directly to the laser diode and therefore an electro optic modulator (EOM) driven with 7.35 GHz is placed between the ECDL and tapered amplifier, resulting in 14.7 GHz sidebands on the 369 nm light.

935nm Stabilized Direct Diode Laser System

Efficient Doppler cooling requires uninterrupted excitations and decays between the main dipole transition levels at 369 nm. With a low probability (0.5%) the ion decays to a different state and needs to be repumped into the ground state of the cooling transition, see Fig. 2.15. The required laser light for this transition at 935 nm is generated by an ECDL setup similar to the 399 nm setup. A commercial laser diode (PN RLT940-100GS, Reithner) is used in combination with an aspheric lens (PN C330TM-B, Thorlabs) and diffraction grating (PN GH13-1210, Thorlabs). The 935 nm ECDL reaches output powers of up to 20 mW. Sidebands at 3.08 GHz need to be applied to the 935 nm laser light when trapping $^{171}Yb^{+}$, see Fig. 2.16. Due to the lower frequency the 935 nm laser diode can be directly modulated by adding an oscillating current, with frequency $f = 3.08$ GHz, onto the dc laser current.

638nm Stabilized Direct Diode Laser System

Should the ion get hit by background gas molecules/atoms it can be knocked into a dark state with extremely low decay rate. In the dark state the ion can't be detected or cooled and will be lost after a certain amount of time due to motional heating. Laser light at 638 nm (PN DL-6148-030, Sanyo) collimated with an aspheric lens (PN A390TM-B, Thorlabs) onto a grating (PN GH13-24v, Thorlabs) is used to repump the dark states. The setup produces frequency stabilized emissions with up to 20 mW of power. The wavelength is scanned instead of applying sidebands when trapping $^{171}Yb^{+}$ as the dark state is only reached very rarely (on the order of several minutes).

3.1.2 Laser Locking Schemes

All of the used lasers have a tunable external cavity, which can be used to stabilize or 'lock' the laser's emission to a certain wavelength. To lock the lasers a signal is required which allows the piezo actuators of the cavity to adjust for deviations from the chosen wavelength.

A stable reference source, in our case a laser at 780 nm, is locked to the stable atomic transition of rubidium, which are unaffected by temperature changes or vibrations. Stabilised 780 nm reference laser light and 739 nm or 935 nm laser light are send through the same cavity and transmission peaks of both are compared in a so-called transfer cavity lock scheme. Laser wavelengths are also measured directly using a wavemeter and the feedback is used to lock the 399 nm and 638 nm laser.

Transfer Cavity Lock

The transfer cavity lock compares the reference signal at 780 nm, with the 738 nm, and 935 nm laser output. In principle also the 369 nm or 399 nm laser light can be compared but cavity mirrors with high reflectivity at both 369 nm and 780 nm would require a custom optical coating and special mirror substrate, making it very expensive. The 638 nm laser will be scanned for most experiments and therefore can not be locked to a single wavelength.

The locking scheme was designed and installed by Robin Sterling and is based on absorption lines of a neutral Rubidium atom vapour cell providing a stable and precise reference wavelength. In the described setup an ECDL at 780 nm is used, consisting of a diode

laser (PN GH0781JA2C, Thorlabs) with aspheric lens (PN GH0781JA2C, Thorlabs) and grating (PN GR13-185, Thorlabs). The 780 nm is locked to the absorption lines of the 87 Rb $^2S_{1/2} \leftrightarrow ^2 P_{3/2}$ transition at 780 nm [130].

The 738 nm and 935 nm lasers are locked to the stable 780 nm reference using Fabry-Perot confocal (FPC) cavities with highly reflective and low transmission loss mirrors. Polarising beam splitters (PBS) are used to combine the 738 nm or 935 nm laser with the reference laser and both are sent through a FPC cavity. Using another PBS the beams are separated again and each sent onto photodiodes (PN Si PIN photodiode S5972, Hamamatsu). Electronically controlled piezo actuator attached to one of the mirrors are used to control or modulate the length of the cavity. The 935 nm laser is locked to the 780 nm reference by modulating the cavity and comparing the resulting transmission signals with a software proportional, integration and differential (PID) controller. Due to the slow scanning of the cavity length ($\sim$ 70 Hz) and realtime software processing speed, the feedback update rate is limited to $\sim$ 10 Hz.

For the 738 nm laser an improved transfer cavity lock was used, where the 780 nm laser light is passed through an acoustic optic modulator (AOM) that modulates the wavelength. The cavity does not have to be scanned anymore and the piezo is only used to stabilize the cavity length and to keep it on resonance with the 738 nm laser. An in-house built hardware PID controllers analyze the signals from the photodiodes and feedbacks to the 738 nm laser and cavity piezo with an update rate of $\sim$ 1 kHz.

The setup and working principal of the transfer cavity lock is described in more detail in [113].

Wavemeter Lock

Setting the exact wavelength of the 935 nm and 738 nm laser before trapping an ion is accomplished using a wavemeter (PN HighFinesse W7). Additionally the wavemeter is also used to lock the 399nm and 638nm laser by sending the measured output wavelengths to the previously discussed LabView Real-Time computer. The LabView software processes the data and sends a feedback signal to the laser piezo drivers. The accuracy of the wavemeter is specified to 60 MHz below 1100 nm and 200 MHz below 370 nm, [90]. To avoid long term drifts or systematical errors, the wavemeter can be calibrated using the 780 nm reference laser or suitable external laser references.

Besides setting the laser to the required wavelength before trapping and locking certain lasers (399 nm, 638 nm) the wavemeter is essential to measuring the exact transition wavelengths of the cooling transitions of the Yb-isotopes, described in the following section 3.5.3.

3.1.3 Optical Table Setup

A schematic of the entire laser setup during the initial ion trapping experiments is shown in Fig. 3.3. Small fractions of the laser beams are coupled into multi-mode fibres and sent to the wavemeter switcher. On the way towards the ion trap the beams are coupled into single-mode optical fibres. If changes are made to the diffraction grating or otherwise to the beam angle, only the fibre coupler has to be realigned instead of realigning the entire optical system. Single-mode fibres also provide spatial output profiles with a gaussian shape. Flipper mirrors can be used to couple the beams into a second set of fibres leading to a second experiment. As a result, changing the active setup from one vacuum system to another only requires small adjustments to the fibre couplers. The schematic also shows the optical isolators close to the EDCLs (369 nm system has isolators built in), which make sure that no light is reflected back into the diodes. The EOM is used to modulate 14.7 GHz sidebands onto the 369 nm laser as discussed. The AOM serves as a fast beam switcher for heating measurement experiments.

3.2 Imaging Setup

Detecting fluorescence of trapped ions during Doppler cooling requires an efficient imaging setup optimized for 369 nm emissions. Collecting scattered photons with minimal background light, low noise and highest possible efficiency is especially important for high fidelity state detection experiments. An imaging system suitable for this task was designed by James Siverns and is explained in more detail in [131]. Efficient photon collection starts with the appropriate objective lens system and a maximal collection angle. A triplet lens (PN 54-17-29-369, Special Optics) with a resolution of < 1 μm [131] is positioned 23.54 mm away from the trapped ions, collecting 2.2% of the emitted photons. The objective has a magnification at the ions position of $M_{triplet} = -17.5$, and an image distance of 549.7 mm. At the image distance an iris (PN SM1D12SZ, Thor Labs) acts as a spatial filter reducing scattered light from the electrodes and other background noise. The iris is followed by an

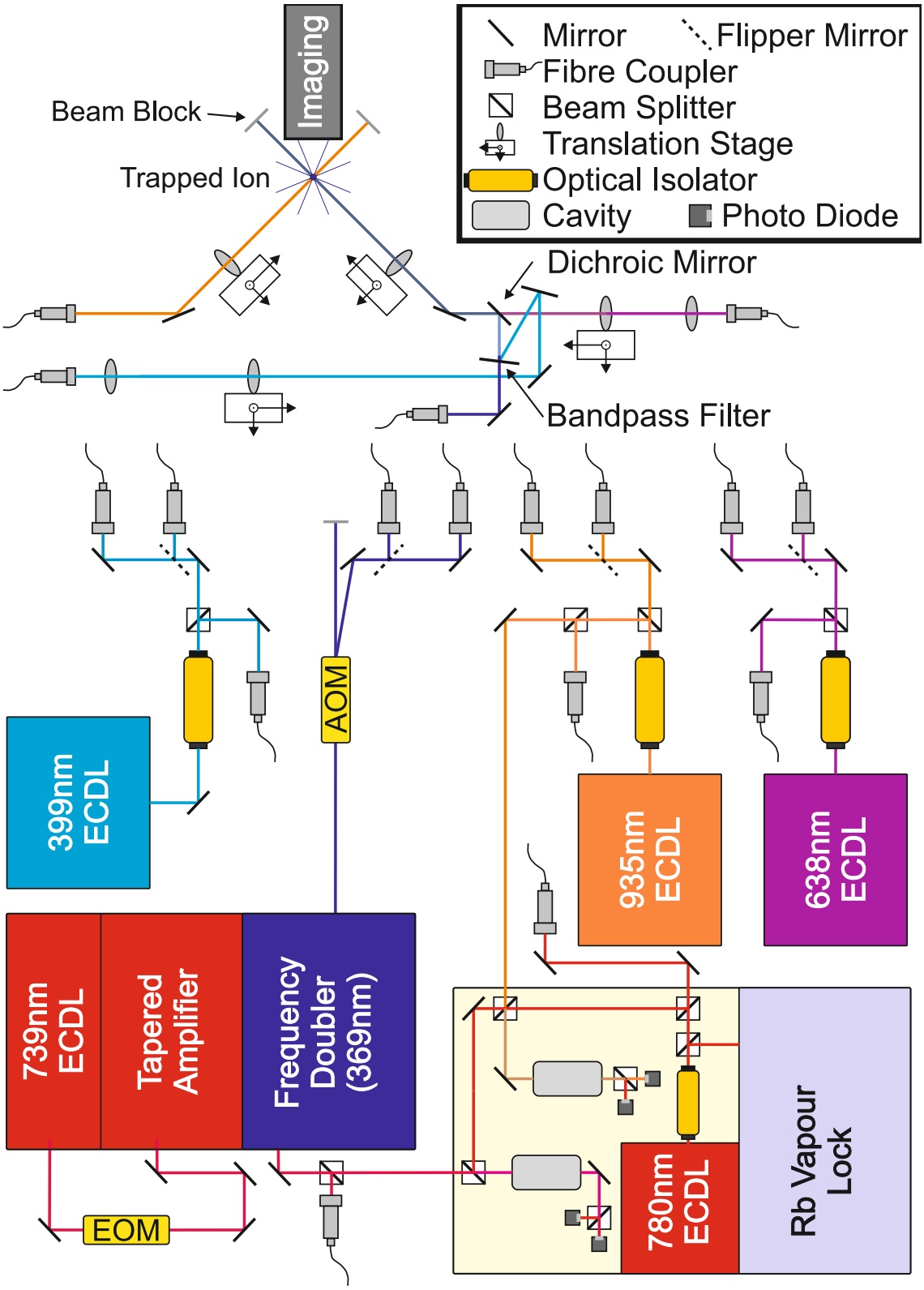


Figure 3.3: Overview of the laser and locking setup used for the experiments discussed in this chapter.

adjustable doublet lens system providing a way to adjust the image size on the detector via the doublet magnification $M_{doublet} = -16 \rightarrow -0.45$. Lenses and iris are placed inside adjustable tubing (PN SM1ZM, Thor Labs) mounted onto a translation stage shown in Fig. 3.4. The same lens system is also reproduced for the second vacuum system, see Fig. 3.4.

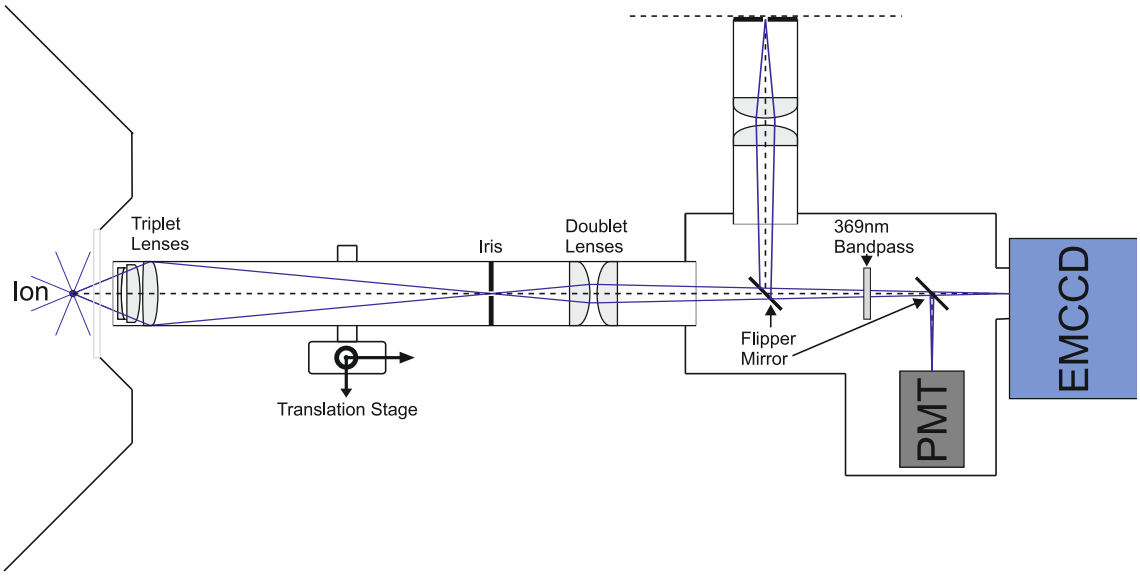


Figure 3.4: Schematic of the imaging setup for two vacuum systems. Flipper mirrors allow imaging of two vacuum system with the same EMCCD and PMT. Translations stages are used to exactly position the focus of the imaging system on the trapped ions.

Both imaging tubes end inside a light-proof construction where a first flipper mirror allows to switch between ion trap systems. Followed by a narrow band 369nm light filter (PN FF01-370136, Semrock) removing any potential scatter from ambient light or the other laser sources. A second flipper mirror deflects the collected photons onto a photomultiplier tube (PN H8259-01, Hamamatsu) or electron multiplying CCD array (PN iXon 885 EMCCD, Andor) [90].

3.3 Vacuum Systems

Trapped ions can lose information encoded in the qubit states or be entirely lost from the trap when hit by background gases. To reduce the chance of collisions, ion traps are housed at a pressure of $\sim 10^{-12}$ Torr in an ultra high vacuum (UHV) system. Reaching and maintaining such a pressure requires a sophisticated setup of UHV compatible materials, special UHV pumps and suitable cleaning and baking procedures.

Ultra High Vacuum Technologies, Procedures and Pumps

Before designing an UHV system, compatible materials have to be selected. Low outgassing rates, tolerance to elevated temperatures during baking at 200°C, resistance to the cleaning procedure (ultrasonic acetone cleaning) and low porosity are essential. Commonly used materials in UHV systems include oxygen free copper (OFC), low oxygen stainless steel, aluminium, glass, polyether ether ketone (PEEK), polytetrafluoroethylene (PTFE), Kapton, non-porous ceramics and ceramic cements.

If a new material has to be used in the UHV system and no references for use at UHV pressures can be found, one can make a rough estimate of the outgassing rate O_R as long as the Total Mass Loss (TML) and the mass of the material M is known. A large TML data base for a variety of materials used in vacuum systems, but not UHV systems is published by the National Aeronautics and Space Administration (http://outgassing.nasa.gov/). An estimate for O_R can be made by following the calculation in [132]:

$$O_R = \frac{m_{nom} TML}{A_{nom}} \frac{p_{std} V_{std}}{M_{mat} \Delta t} = \frac{TML}{M} 0.1555 \ \ \text{Torr} \cdot \text{liter} \cdot \text{cm}^{-2} \cdot \text{s}^{-1} \tag{3.1}$$

Here M_{mat} is the molar mass of the material and under standard conditions $p_{std} = 760$ Torr, $V_{std} = 22.4$ liter·mol, $A_{nom} = 0.3167$ cm^2 and $m_{nom} = 2.5 \cdot 10^{-4}$ kg. This allows a rough estimate to be made for materials that have not been used in a UHV chamber before.

In addition to selecting the correct materials virtual leaks have to be avoided. Structures, where two plates are pressed against each other can trap air and need to be avoided otherwise gases will gradually leak and prevent the chamber from reaching UHV. Machining grooves into surfaces and using screws with vent holes will prevent these virtual leaks.

Before assembling the vacuum system, suitable individual parts should be baked at 200°C for two weeks under normal atmosphere. During the baking, chamber surfaces will form thick oxide layers reducing H_2 and CO leaking out of the steel when evacuated [133]. All system parts need to be cleaned thoroughly using an ultrasonic bath with acetone and isopropyl alcohol (IPA).

After assembly, the system is connected to multiple vacuum pump stages and baking is repeated under vacuum. The first pump stage uses a diaphragm (PN SA0150MCCF, K.J. Lesker) and turbo molecular pump (PN M S03525, Pfeiffer Vacuum), reaching pressure as

low as 10^{-8} Torr. Turbomolecular pumps use a turbine rotor rotating at 90,000 rpm, with angled rotor blades forcing molecules hitting the blades towards the outlet of the pump. Turbomolecular pumps are especially effective when pumping heavy molecules and atoms, but struggle with very light particles like He and H_2.

After reaching at least 10^{-6} Torr the second pump stage consisting of an ion getter pump (PN 9191145, Varian) and a titanium sublimation pump (PN 9160050, Varian) can be activated. Strong electric fields are applied between two plates inside the ion getter pump ionizing the gas molecules and accelerating them into the titanium cathode of the pump, where they will be chemically bound. All light and heavy molecules, except noble gases [134], can be pumped very efficiently with most ion getter pumps.

When the baking procedure is complete the TSP is run for 4-5 days in short cycles[1] and the pressure can be further reduced to 10^{-12} Torr. This pump evaporates fresh titanium from filaments onto the chamber walls of the pump. Most molecules and atoms hitting the fresh titanium stick to the wall (noble gases don't stick to titanium) and are later buried under a new layer of titanium.

Measuring such low pressures is possible using a hot filament ion gauge (PN UHV-24p Bayard-Alpert, Varian). Ion gauges excite and accelerate electrons which ionize the background gas and lead to a measurable current. One has to keep in mind that the measured current and therefore measured pressure will depend on the background gas composition.

3.3.1 Vacuum Chambers

Two vacuum chamber designs are currently in use, the first design houses the macroscopic symmetric trap used for initial trapping and experiments discussed in this chapter, see Fig. 3.5 (a). A second chamber with larger hemisphere allowing for better optical access and to house larger mounting structures was designed later and is shown in Fig. 3.5 (b). The new chamber also features a larger chip bracket that can accommodate 200pin chip carriers. Modifications to the vacuum system presented in chapter 7 and new ion trap architectures discussed in chapter 6, were designed to be used with the new chamber.

Vacuum System One

The main chamber of the first vacuum system was constructed by welding a stainless steel (316L) 4.5" spherical octagon (PN MCF450-**SO**20008-C Kimball Physics) onto a

[1] ∼1min every 2-3 hours

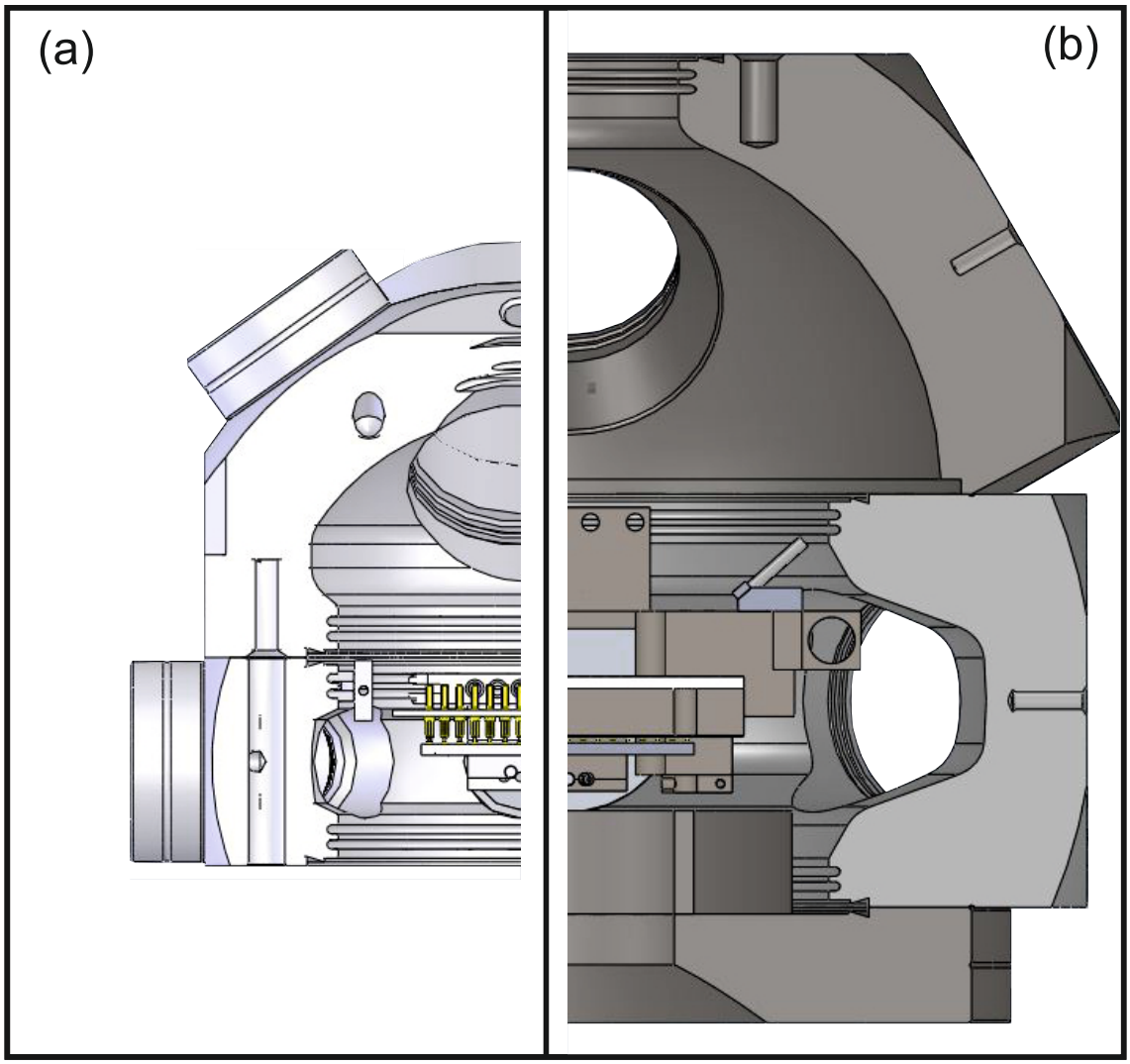


Figure 3.5: SolidWorks illustrations with cuts through half the chambers allowing a comparison between vacuum system one (a) and vacuum system two (b).

4.5” Magdeburg hemisphere (PN MCF450-**MH**10204/8-A Kimball Physics), see Fig. 3.6. A total of 10 viewports allow for flexible optical access from different angles, making it possible to house asymmetric and symmetric traps.

Symmetric traps are mounted on a custom carrier mount, asymmetric traps are mounted on a commercial 101-pin ceramic pin grid array (CPGA) chip carrier (PN PGA10047002, Global Chip Materials). Both, the chip carrier and custom carrier mount feature the same pin footprint, and fit into a custom made in-house built chip bracket, see Fig. 3.6 (2). The bracket is constructed from two PEEK plates that sandwich 90 gold coated pin receptacles (PN 0672-1-15-15-30-27-10-0, Mill-Max). Kapton insulated copper wires are crimped to the back of the receptacles on one side, shown in Fig. 3.6 (1) and connected to two 50 pin D-sub connectors on the other side. These connectors are plugged into 6” D-sub vacuum feedthroughs (PN IFDGG501056A, K.J.Lesker). Pin receptacles and thick bare copper wires are used to connect the rf electrodes and ground to a high voltage feedthrough (PN EFT 0521052 from K.J.Lesker). To prevent shorting, ceramic beads (PN 36-4090, RS Components) are used for insulation. Mounting plates and groove grabbers (PN MCF450-GG-CT02-A, Kimball Physics) attach the chip bracket to the hemisphere.

Four atomic ovens providing a neutral Yb flux are mounted onto the chip bracket, two are loaded with enriched Yb and two with natural Yb. Asymmetric traps and symmetric traps require the flux to come from different directions, making four ovens necessary. The atomic ovens are constructed from a $\sim$ 20 mm long stainless steel tube (ID 0.0325”), which is crimped flat at one end and welded shut with a constantan foil. The tubes are filled either with 90% enriched ^{171}Yb wire (PN OA0036, Oak Ridge National Laboratory) or natural Yb (PN GO0196, Goodfellow Cambridge Limited). Passing a high current (5-7 A) through the constantan foil via attached insulated copper wires for several minutes heats the oven up to 400°C, which is enough to break the naturally formed oxide layers and evaporate Yb.

Six 1.33” ConFlat (CF) flange viewports (PN VPZL-133Q, K. J. Lesker) are placed on the spherical octagon, which are used for optical access to surface traps. Optical access for symmetric traps is provided via two 1.33” and one 2.75” CF flange viewports (PN VPZL-275Q, K. J. Lesker) on the hemisphere. A custom designed (by Altaf Nizamani) 4.5” CF flange recessed viewport (manufactured by K. J. Lesker) is used on the front of the hemisphere. The custom design is required to position the imaging objective 23.54 mm away from the trap center, which is necessary for a high collection efficiency. All viewports

are made of UV-grade quartz fused silica glass, which has a custom antireflection (AR) coating (by Laseroptics), reaching transmissions rates of 97% for all wavelengths used. The entire system is described in more detail by Altaf Nizamani in [135].

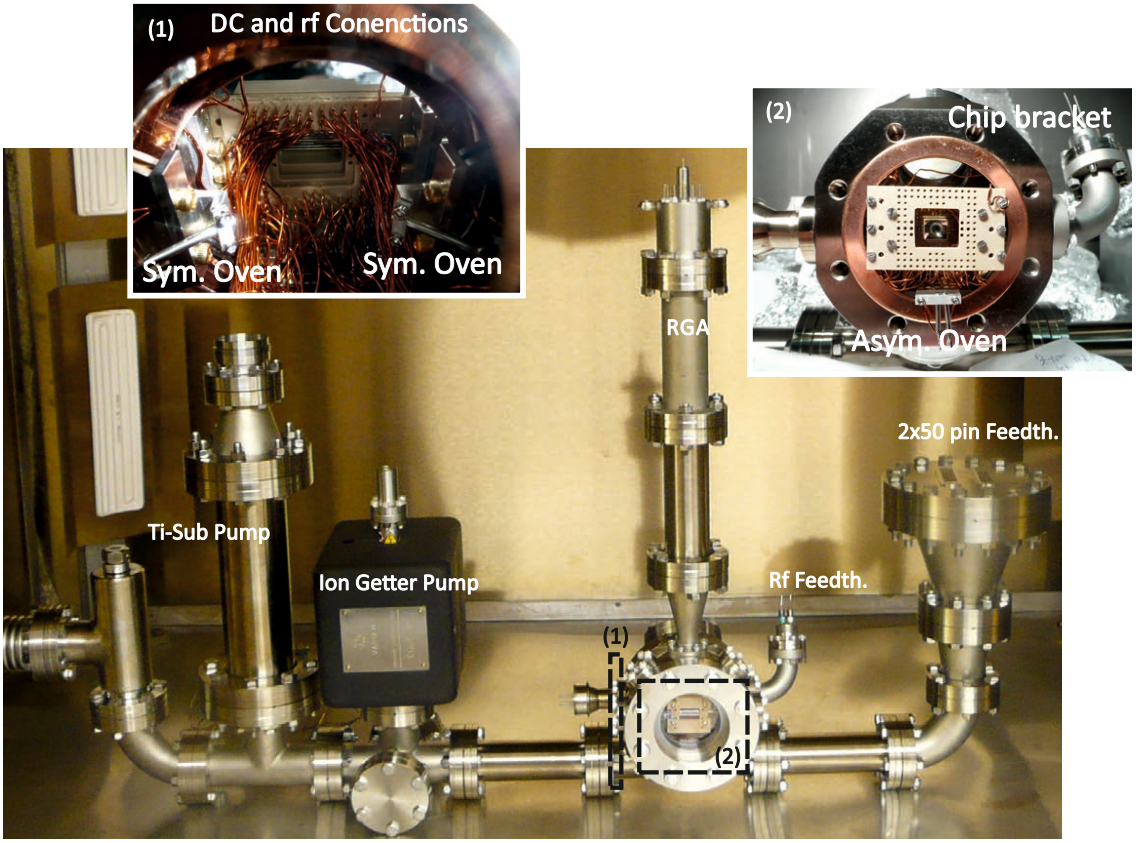


Figure 3.6: Picture of the assembled vacuum system one inside the oven chamber used for baking. The two insets show the wiring inside of the chamber (1) and the chip bracket (2).

Vacuum System Two

To house a new experiment [102], a second vacuum system was designed and assembled by Robin Sterling [113], which was optimized for larger chip carriers and better optical access. Welding a 6" spherical octagon (PN MCF600-SphOct-F2C8, Kimball Physics) together with a 6" weldable cluster (PN MCF450-WeldClstr-E1C4, Kimball Physics) increases the volume of the main chambers dramatically as shown in Fig. 3.5. The increased space is used to house larger CPGA chip carriers (PN PGA10047002, Global Chip Materials) with a 200 pin footprint shown in Fig. 3.7(2). The chip bracket was redesigned to fit the larger carriers and additional adjustment rails were added. Mounting screws are added allowing a fine adjustment of the chip carrier position and angle with respect to the front window.

Previously used 1.33" viewports were replaced with larger 2.75" ports, otherwise the viewports are identical to system one. Also the front window is replaced with a larger custom

recessed 6" view port in this system. Additionally some of the feedthroughs and pumps were rearranged and additional SMA feedthroughs were attached to the system. The entire system is shown in Fig. 3.7.

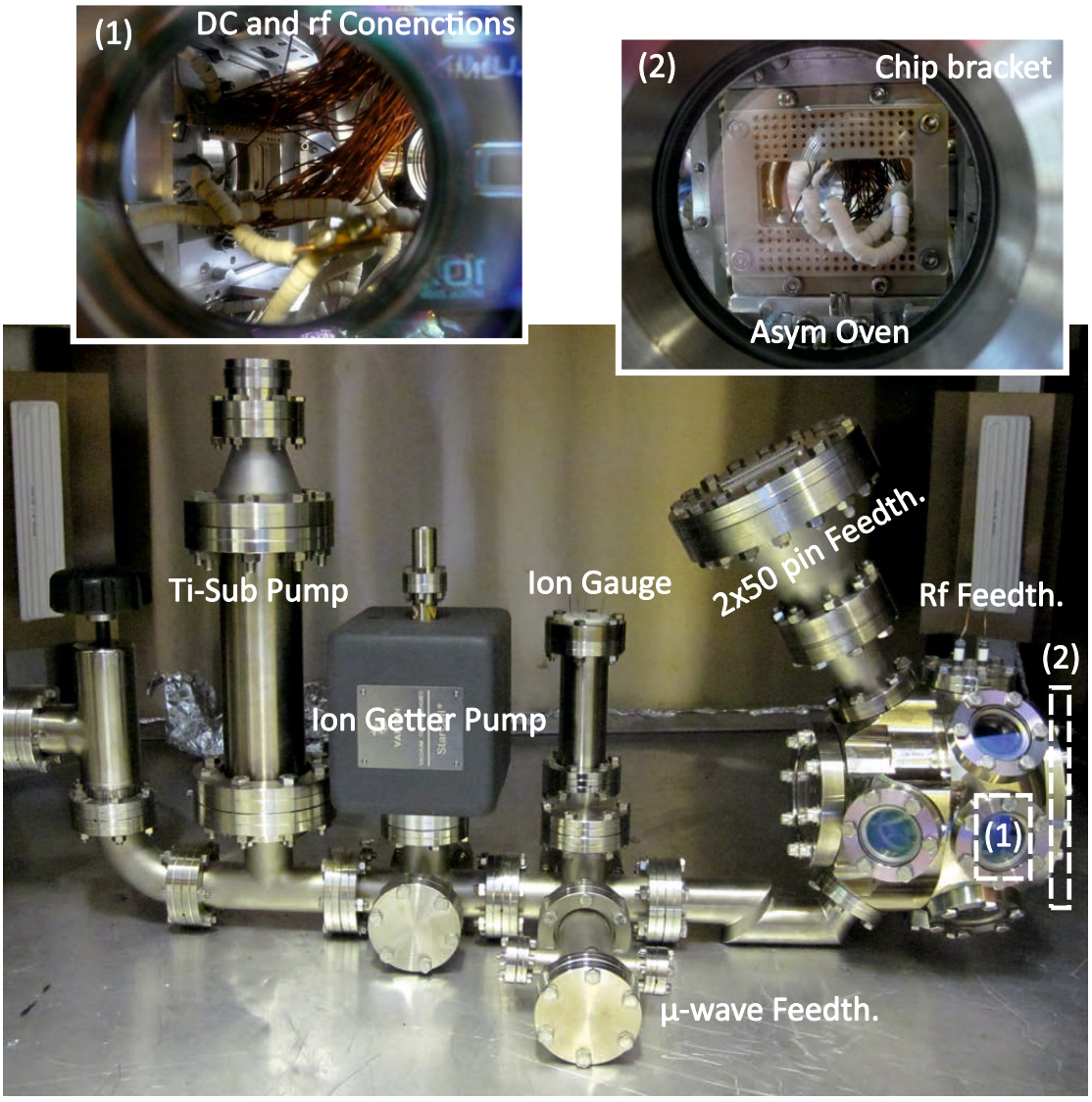


Figure 3.7: Assembled vacuum system two inside the same baking oven as system one. Inlets shown the wiring inside the chamber (1) and the chip bracket facing the front window (2).

3.4 Dc Voltage Supply, Helical Resonator and Trap Characteristics

Generating and delivering stable, noise free rf and dc voltages is essential for the operation of ion traps. As discussed in section 2.2.2 any electrical noise at frequencies close to the secular frequencies ω or $\Omega \pm \omega$, where Ω is the drive frequency, lead to an increase in

heating rate [116, 117]. Fluctuations of the rf voltage amplitude V or frequency Ω will additionally cause a change in secular frequencies ω. Fluctuations of the dc voltages result in changes of the axial secular frequency (ω_z) and the ions positions z_0.

Static voltages can be heavily filtered using low-pass filters to minimize noise close to the secular frequencies reaching the dc electrodes. The voltages U_i are supplied by non-switching bench top power supplies [2].

Generating clean, stable rf voltages with amplitudes on the order of several hundred volts is necessary to achieve high trap depths as discussed in section 2.1. A resonator circuit with a very narrow frequency bandpass and high voltage amplification is ideal for this task. High quality factor (Q) helical resonators can achieve these requirements. Helical resonators also provide an impedance matching between rf source and ion trap, sufficiently amplify the input voltage and can reach very high loaded Qs of more than 200 [104]. The helical resonator used for experiments described in this chapter is shown in Fig. 3.8.

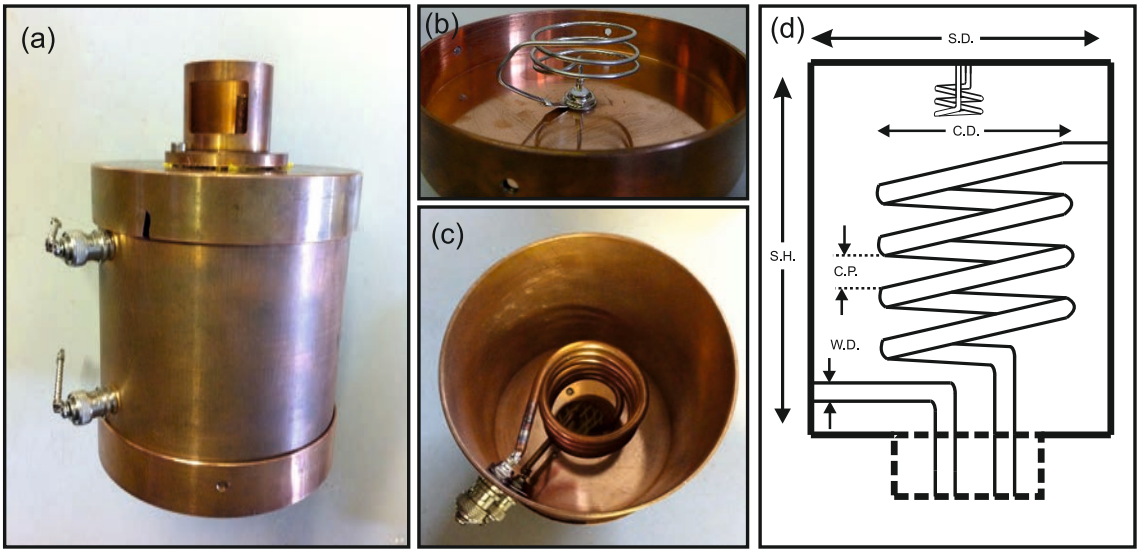


Figure 3.8: Picture (a) shows the entire helical resonator, connectors to the vacuum HV feedthrough point upwards. Top cover (b) and inside of the resonator (c) are shown next. The schematic (d) shows a resonator with shield height S.H., diameter S.D., wire diameter W.D., coil diameter C.D. and coil pitch C.P.

When designing the resonator and calculating the Q, all components of the resonant circuit have to be considered. A detailed guide on helical resonator and how to design one suitable for a specific setup is given in [104]. Following the guide we see that the quality factor Q will be determined by the total inductance L, capacitance C and resistance R of the resonating system, but can also be expressed in terms of resonant frequency f_0 and

[2] switched mode power supplies have an inherent noise at close to 500kHz and should be avoided in an ion trap setup if possible

Shield Height S.H. (mm)	76 ± 1
Shield Diameter S.D. (mm)	105 ± 1
Wire diameter W.D. (mm)	52 ± 2
Coil diameter C.D. (mm)	4.0 ± 0.1
Coil Pitch C.P. (mm)	7 ± 3
Number of Turns	7.75

Table 3.1: Table with all relevant helical resonator parameters used for experiments described in this chapter [90].

bandpass bandwidth Δf:

$$Q = \frac{1}{R}\sqrt{\frac{L}{C}} = \frac{f_0}{\Delta f} \text{ and } f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{3.2}$$

Magnitude of the generated rf voltage V depends on the Q factor, rf power P and geometric factor $\kappa = (L/C)^{1/4}$ defined in [104]:

$$V = \kappa\sqrt{2PQ} \tag{3.3}$$

The resonant circuit inductance, capacitance and resistance are affected by the feedthrough, in-vacuum wiring, chip bracket and carrier, wire bonds and rf electrodes. For the operation of the macroscopic trap described in the following section 3.5.1, a helical resonator with the dimensions shown in table 3.1 was used.

A total capacitance of $C = 17 \pm 2$ pF was measured for the entire trapping setup, including the ion trap, wiring and feedthrough and a resistance between rf electrodes and resonator was measured to be $R \sim 0.1\ \Omega$. The Q of the entire resonant circuit was measured to be $\sim$200 at a resonant frequency $f_0 = 21.49$ MHz. After trapping it was possible to exactly determine the geometric factor κ, from the input power P and exact peak rf voltage[3] V to $\kappa = 12.9 \pm 1.4$.

The rf voltage is generated by a commercial function generator (PN HP 8640B, Hewlett Packard) and amplified using a high power (max output 30W) rf amplifier (PN NP-541, MiniCircuits). The exact output power is measured using a directional coupler and power meter (PN NAUS 3, Rhode and Schwarz) placed between the amplifier and the helical resonator.

Microfabricated asymmetric traps can have much larger trap capacitances of 15-20 pF [113]

[3] calculated from measured radial secular frequencies, see section 2.1.2

compared to macroscopic trap capacitances, which commonly have a capacitance on the order of 1-5 pF. The additional capacitance will reduce the Q of the resonator and a different design might be necessary to achieve sufficient narrow bandpass filtering. To limit the impact of large trap capacitances on the Q it is important to keep wiring and feedthrough capacitance at a minimum. Electrical characteristics of microfabricated ion traps will be discussed further in chapter 4.

3.5 Macroscopic Ion Trap, Trapping and Initial Experiments

For initial trapping in a new experimental setup a macroscopic ion trap with high ion electrode distance and large trap depth is ideal. It provides good optical access, large trap depths and low motional heating. Hence an asymmetric blade trap was designed by Robin Sterling, achieving a compromise between large ion-electrode-distance and satisfying the size constraints of the small carrier mount footprint ($\sim 3 \times 3$ mm).

3.5.1 Blade Trap

The trap consists of two layers of gold-plated stainless steel electrodes placed symmetrically around the trap center, see Fig. 3.10. The blade electrodes are separated by 343(14) μm and 554(14) μm using PEEK spacers, providing enough space for optimal optical access for the 369 nm laser beam and limiting scattering, show in Fig. 3.9 (a). The dc electrodes are segmented allowing confinement in the axial direction by applying a static potential illustrated in Fig. 3.9 (b). Additionally three gold coated steel rods are placed close to the trap centre allowing the compensation of micromotion caused by stray fields, of which two are currently connected.

The electrode separation in the x and y-directions is close to symmetric, compared to microfabricated symmetric traps, where the ratio between electrode separations can be on the order of 15:1 [76]. This results in an almost hyperbolic potential and the geometric factor discussed in section 2.1.3 is close to one resulting in maximum trap depth for the chosen ion-electrode distance.

Minimum separation between rf and dc electrodes is 50 μm, making it possible to apply very large rf voltages and achieve high trap depths of several eV. The entire electrode construction is placed on a gold coated steel plate with peek insulations providing shielding of any possibly exposed dielectric from the trapping zone shown in Fig. 3.10 .

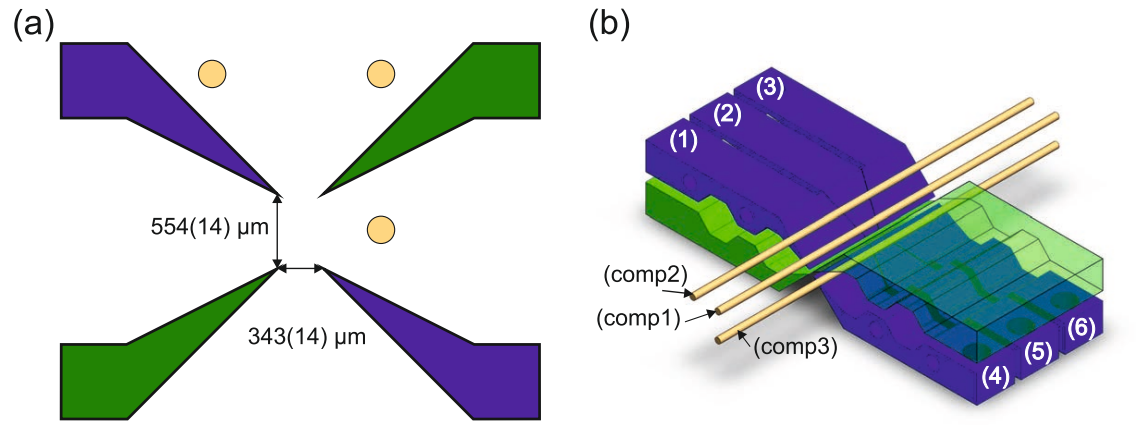


Figure 3.9: (a) cross-section of the ion trap electrodes showing the dc electrodes in blue, rf in green and compensation in yellow. (b) three-dimensional drawing of the blade trap with labelled dc electrodes.

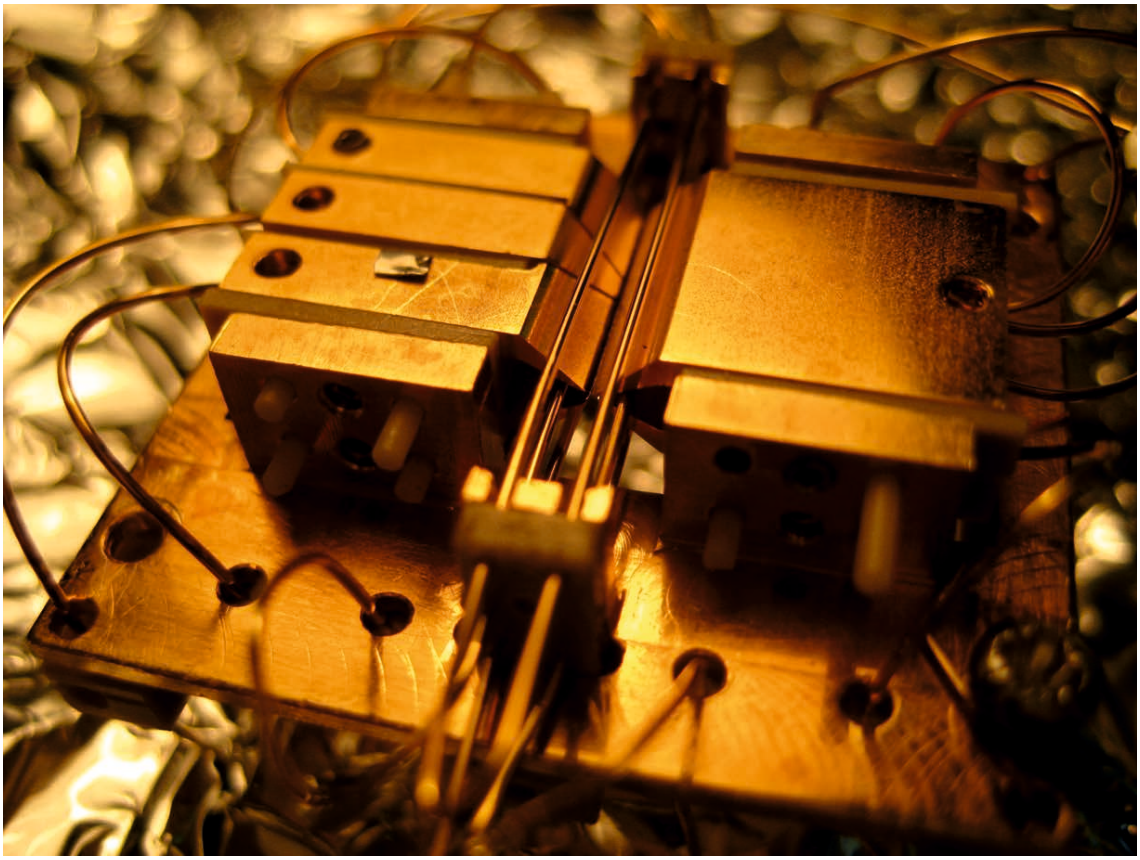


Figure 3.10: Picture of the assembled blade trap with wiring and mounting plate.

Dc 1 (V)	148.88(1)
Dc 2 (V)	7.36(1)
Dc 3 (V)	25.03(1)
Dc 4 (V)	0 V
Dc 5 (V)	0 V
Dc 6 (V)	0 V
Compensation 1 (V)	169.22(1)
Compensation 2 (V)	169.22(1)
Compensation 3 (V)	-2.7 (1)
RF (V)	680 (10)

Table 3.2: Table with dc and rf voltages applied to the electrodes labelled in Fig. 3.9 (b) for initial trapping and experiments.

During assembly and baking some of the electrodes slightly shifted and resulted in shorting of one dc electrode to GND. The exact geometry was determined after assembly and baking using scattered laser light and the imaging system. The measured dimensions, shown in Fig. 3.9, were then used to simulate the exact trap potential using the earlier discussed numerical BEM tool CPO [4].

For initial trapping an rf voltage $V = 680(10)$ V and drive frequency $\omega = 2\pi \times 21.48$ MHz were used and the corresponding simulated pseudopotential of the trap is shown in Fig 3.11. The entire set of voltages applied to the electrodes is summarized in table 3.2.

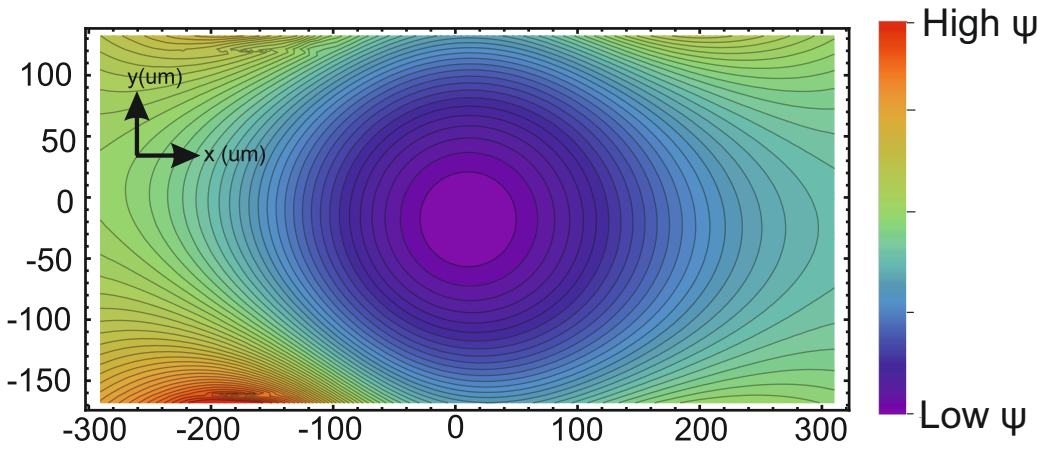


Figure 3.11: Pseudopotential simulations of the blade trap showing the potential in x and y axis at z_0.

[4] Simulations performed by Robin Sterling

3.5.2 Initial Trapping

The first $^{174}Yb^{+}$ ions were trapped on the 9th of December 2009, and the first experiments and detailed characterization of the blade trap followed soon after. After trapping $^{174}Yb^{+}$ several other isotopes were trapped $^{176}Yb^{+}$, $^{172}Yb^{+}$, $^{171}Yb^{+}$ and $^{170}Yb^{+}$. Single and multi-ion crystals were trapped for several hours, shown in Fig. 3.12, demonstrating the high trap depth and stable trapping.

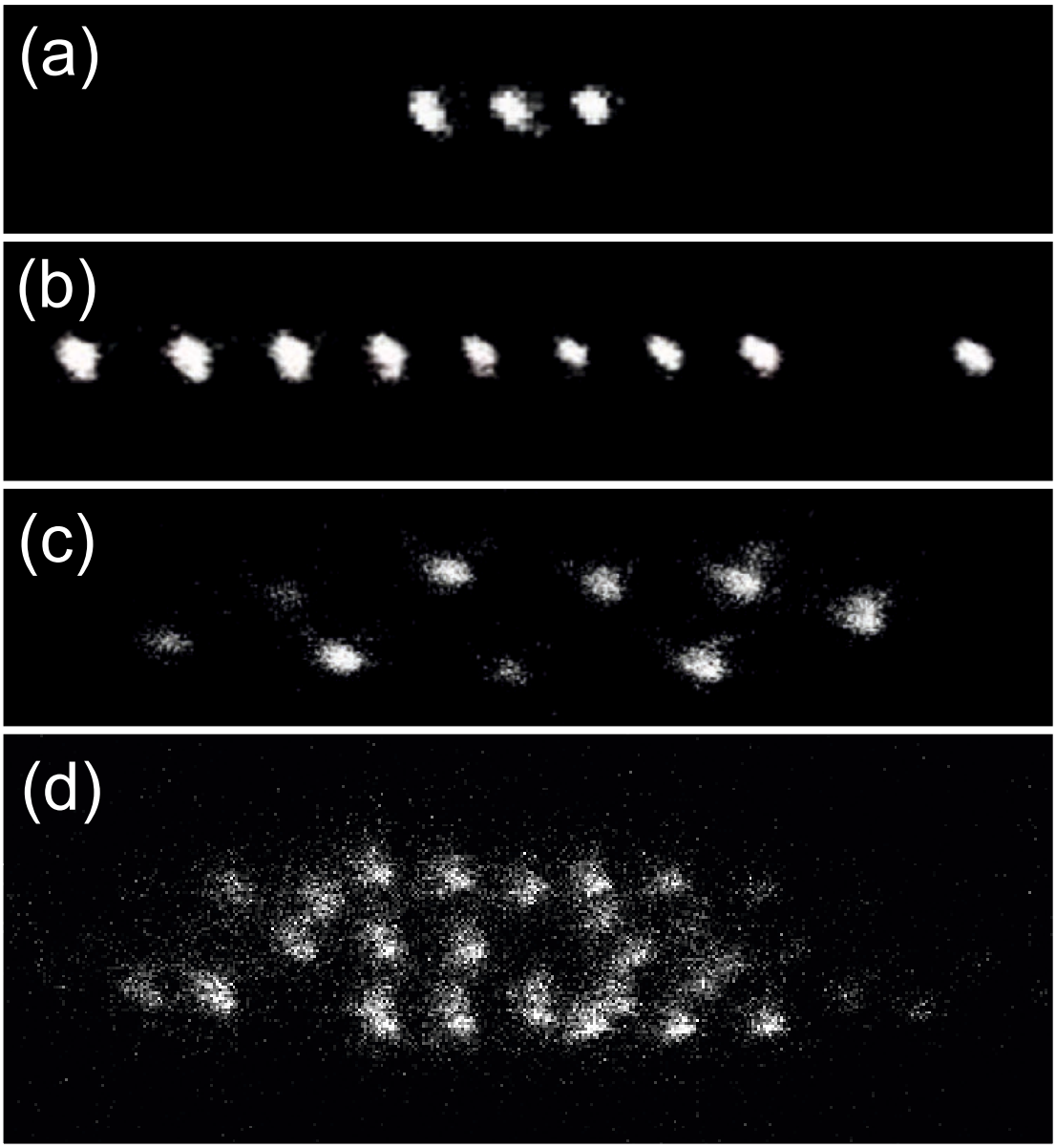


Figure 3.12: Pictures showing trapped Yb^{+} ions. (a) String of three crystallized $^{171}Yb^{+}$ ions, (b) longer string containing different Yb isotopes, only $^{171}Yb^{+}$ is cooled and fluoresces. For (c) and (d) the secular frequency in axial direction was reduced, as a result Yb^{+} ions arrange in a zig-zag configuration.

3.5.3 Measurement of Transition Frequencies of Several Yb Isotopes

Being able to trap the previously mentioned Yb isotopes and having access to a very precise wavemeter made it possible to determine the exact wavelengths of Doppler-cooling-relevant transitions. The ionizing transition wavelengths were determined using a different setup by Altaf Nizamani and James McLoughlin prior to first ion trapping [123].

After trapping new ytterbium isotope the wavelengths for the 369nm and 935nm wavelength transitions were determined by scanning the respective laser and observing the fluorescence. At maximum florescence the peak wavelength of the transition is reached and the wavelength can be read off the wavemeter. To reduce systematic noises and long term drift effects the wavemeter was calibrated prior to every measurement.

When trapping $^{171}Yb^{+}$ the setup needs to be slightly extended. The more complicated cooling transition diagram described in section 2.3.2 requires the appropriate sidebands to be applied to the cooling lasers for efficient cooling. Also an external static magnetic field needs to be applied ($\sim$ 0.5 mT) [90] using a set of Helmholtz coils. The magnetic field is used to shift the degenerate states of $^{2}S_{1/2};|\ F=1\rangle$ [136], which would otherwise superimpose to form dark states if driven with a laser of constant polarization. Applying a magnetic field causes Zeeman shifts of the degenerate states by unequal amounts, which reduces the population of the dark state.

The transition wavelength can then be measured similar for the other isotopes. Measured wavelengths for all trapped isotopes are summarized in table 3.3

Isotope	369nm Transition	935nm Transition
$^{170}Yb^{+}$	369.52364(6)	935.19751(20)
$^{171}Yb^{+}$	369.52604(6)	935.18768(20)
$^{172}Yb^{+}$	369.52435(6)	935.18736(20)
$^{174}Yb^{+}$	369.52494(6)	935.17976(20)
$^{176}Yb^{+}$	369.52550(6)	935.17252(20)

Table 3.3: Doppler cooling transition wavelengths measured for a variety of Yb isotopes [90].

3.5.4 Measuring Secular Frequencies

Secular frequencies of all motional axes were measured by applying an oscillating potential of frequency f_{osc} to one of the dc electrodes. The oscillating voltage is generated using an rf frequency generator and connected to a dc electrode via the filter box. The corresponding

low-pass filter was temporarily disconnected allowing the high rf modulation to reach the dc electrode. Frequency f_{osc} is scanned, and when close to a secular frequency causes a drop in fluorescence and decrystallization of the ion. The oscillating potential excites the secular motion, increasing its amplitude and consequentially the Doppler shift of the ion.

To improve the accuracy of the measurement, the frequency f_{osc} is scanned towards the secular frequency from higher ($f_{osc} > \omega/2\pi$) and lower values ($f_{osc} < \omega/2\pi$). When the exact frequency is found, the dialed-in frequency values are confirmed using an oscilloscope. Using the rf and dc potentials described in section 3.5.1 the secular frequencies were measured as $\omega_x = 2\pi \times 2.069 \pm 0.001$ MHz, $\omega_y = 2\pi \times 2.110 \pm 0.001$ MHz for the radial frequencies and for the axial frequency $\omega_z = 2\pi \times 1.030 \pm 0.001$ MHz, [90].

Based on the these results, known trap dimensions, electric field simulations and the applied drive frequency $\Omega \sim 2\pi \times 21.48$ MHz it is then possible to calculate the exact trap depth $\Xi = 4.9(2)$ eV and applied rf voltage amplitude V= 680(10) V.

3.6 Heating Rate Measurement and Discussion

Following the earlier experiments a heating measurement was performed by detecting the ion fluorescence during Doppler recooling, based on the model described in [114]. By blocking the cooling beam for a certain 'delay time' we let the ion heat up. After unblocking the cooling beam we observe the fluorescence rate of the ion. Based on the fluorescence rate evolution during this 'recooling' cycle it is possible to determine how much energy the ion gained during the delay time. Repeating the experiment for several different delay times we can extrapolate the heating rate.

Similar to section 2.2.2 we will assume that the heating rate is dominated by anomalous heating, which might depend on the surface quality of the electrodes. It was considered that ytterbium, deposited onto electrodes during ion loading, could result in a considerably higher heating rate compared to other ion species. Should the heating rate be much higher than expected, successful application of sideband cooling might be prevented.

3.6.1 Micromotion Compensation

Before performing a heating rate measurement, extrinsic micromotion caused by static stray fields pushing the ion out of the rf nil needs to be minimized. Several methods

to minimize micromotion are described in [137]. The ion is trapped at least 10 min prior to the compensation, allowing the charge build up caused by the ionized Yb flux to discharge. Using the camera described in section 3.2 we can directly observe movement of the ion when reducing or increasing the rf potential. The applied rf voltage is reduced and potentials on dc electrodes and compensation rods are changed to bring the ion back into its original position. Afterwards the rf voltage is set back to the original value. The steps are repeated multiple times while decreasing the rf voltage further, until the ion stays in the same position.

To confirm the successful micromotion compensation, the power broadened linewidth of the 369 nm Doppler cooling transition is mapped out. Recording the florescence count of the ion using the PMT while scanning the wavelength of the 369 nm laser provides the full width half maximum (FWHM) of the transition linewidth, which is equal to $L = \Gamma\sqrt{1+s}$ for a perfectly compensated ion. Micromotion compensation steps were repeated until we couldn't reduce the FWHM any further.

The saturation parameter s depends on the intensity of the 369 nm laser beam at the ion's position, following $s = I/I_{sat}$, where I_{sat} is a transition dependent constant. Determining the exact laser intensity can be difficult, which is why the maximum fluorescence count was used instead to determine the saturation parameter. The excited state population $\rho_{excited}$ (section 2.2.1) is proportional to the fluorescence rate during Doppler cooling $dN/dt \propto \Gamma \cdot \rho_{excited}$. For $s \to \infty$ the population $\rho_{excited}$ will be 1/2. After micromotion compensation the laser intensity was increased until a maximum fluorescence count was reached, halving the count rate yields a saturation parameter of $s \sim 1$. Repeating the transition linewidth measurement yielded a FWHM of ~ 40 MHz, which is significantly higher than the expected 27.86 MHz. A possible cause for the broader linewidth will be discussed in section 3.6.2.

3.6.2 Experimental Recording of Fluorescence Curves

The heating measurement makes use of the model described in [114] based on the fluorescence evolution during Doppler recooling. Doppler cooling described in section 2.2.1 will be used as basis for the following description. The model assumes that the observed fluorescence changes during recooling happen in one dimension. If the secular frequency in one axis is much lower compared to the other two ($\omega_z << \omega_{x,y}$) the heating in this axis will be much higher ($dN/dt \sim \omega^2$) and the assumption can be made. In our ion trap the

confinement in the axial direction is provided by static potentials and can therefore be adjusted appropriately. The theoretical background of the model is described in App. A.

Utilizing the model, heating rates for a single trapped $^{174}Yb^{+}$ ion and different secular frequencies in the axial direction ω_z were measured. Secular frequencies in the radial directions were $\omega_x = 2\pi \times 2.069 \pm 0.001$ MHz, $\omega_y = 2\pi \times 2.110 \pm 0.001$ MHz. The secular frequency in the axial direction was varied between $\omega_z = (178, 287, 355) \pm 0.001$ kHz. After successful micromotion compensation the 369 nm cooling laser was detuned 6 MHz from resonance.

Data acquisition and control of the experiment is handled by a special LabView program running on an FPGA card (PN NI-PXI-7842R, National Instruments). The program was written by Altaf Nizamani and is able to directly record output signals coming from the PMT and also to control the acousto-optic modulator (AOM). Fluorescence counts coming in the form of TTL pulses from the PMT are saved in 50 μs bins on the card's memory. The 369 nm beam is turned off by the AOM, allowing the ion to either heat up, or be Doppler cooled. In Fig. 3.13 the timings for the measurement are illustrated. First the beam is turned on for 1 sec to make sure the ion is fully recooled, then the beam is turned off for a variable delay time, the ion is heating up. Now the beam is unblocked and fluorescence counts are recorded for 4 ms during the recooling period. Data acquisition starts 1 ms before the beam is turned on to make sure none of the recooling fluorescence counts are missed.

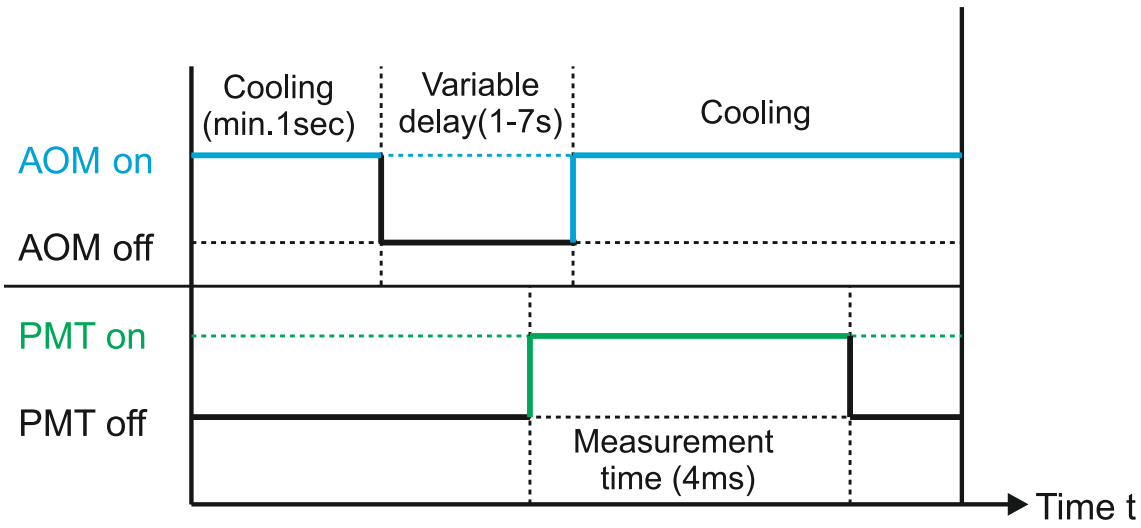


Figure 3.13: Time schematic illustrating the timings used to measure the gain in motional quanta of the ion after a certain delay. The measurement period starts 1ms earlier than the Doppler recooling to account for eventual delays in the data acquisition.

Delay times (when the cooling beam is blocked) were varied from 1-7 seconds and for each measurement 500 runs with identical parameters were recorded. Due to the thermal distribution of the mean starting energy and very low fluorescence count of detected photons many runs are required to achieve a good fluorescence curve.

After the runs were recorded a second linewidth measurement confirmed that there was no substantial increase in micromotion.

All fluorescence counts vs time are then added together and the count rate is normalized. By varying the mean energy in equation A.8 the recorded fluorescence rate is manually fitted with the curve predicted by the model. In Fig 3.14 the fluorescence counts evolution is plotted and fitted for a delay time of 5 seconds and a secular frequency of $\omega_z = 2\pi \times 178(1)$ kHz. The average degree of motional excitation at the start of the recooling cycle can then be directly calculated from the mean energy $\bar{E} = \hbar\omega\bar{n}$ and is equal to $\bar{n} = 61(5) \times 10^4$ quanta for the present case in Fig. 3.14.

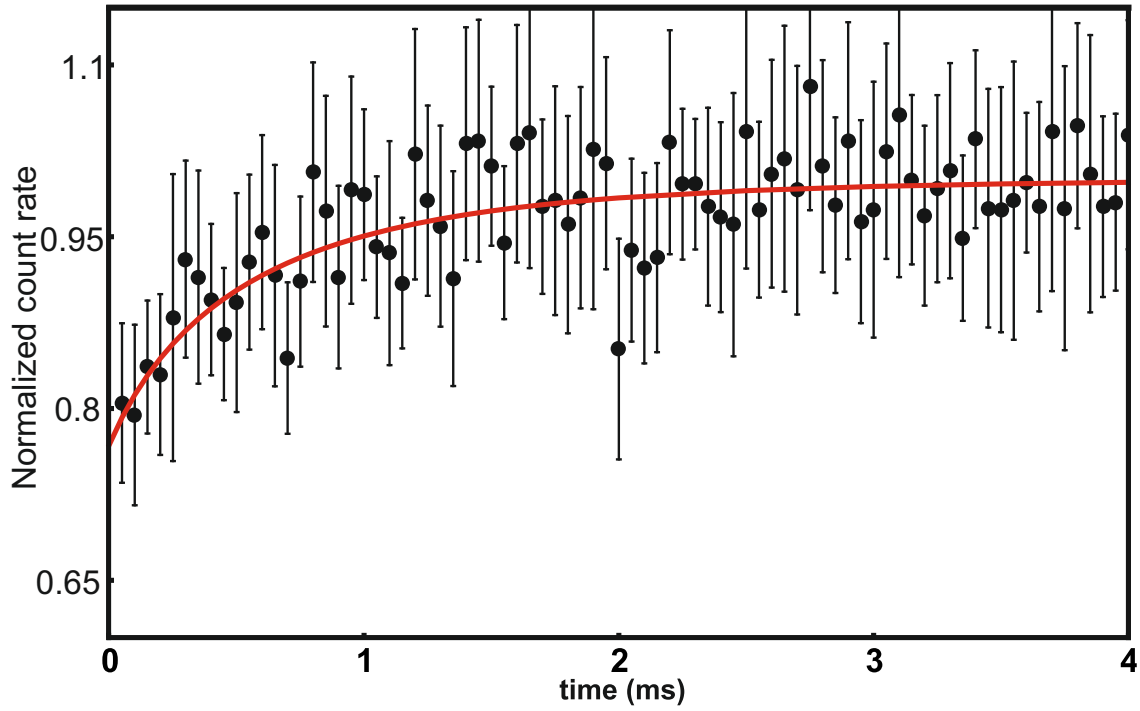


Figure 3.14: Normalized count rates summed up from 500 runs for $\omega_z = 178(1)$ kHz with a delay time of 5 sec. The average amount of quanta before recooling was determined to be $\bar{n} = 600,000$.

Standard deviations for each 50 μs bin were calculated and used as basis for the error analysis of the initial mean energy $\bar{E}$. This error was used for the rest of the calculations and is propagated through the rest of the fits and calculations.

Repeating the measurement for delay times of 1,3,7 sec allows us to plot the gained mo-

tional quanta vs time Fig. 3.15.

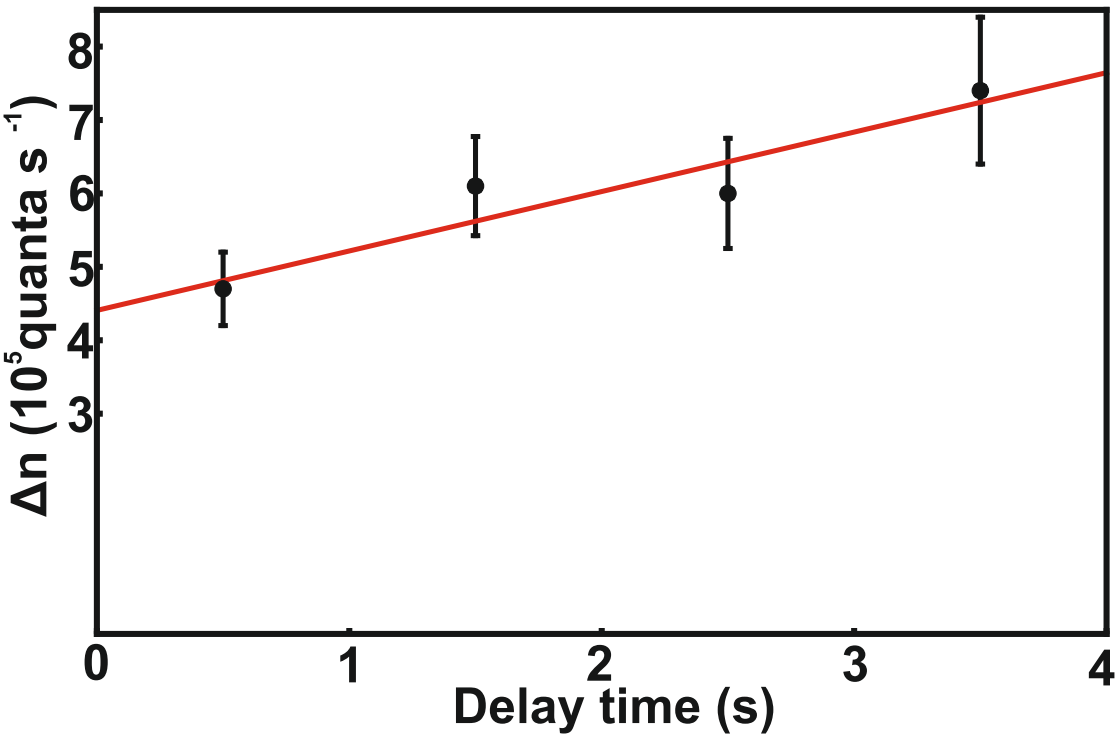


Figure 3.15: The gained motional quanta for $\omega_z = 2\pi \times 178(1)$kHz after a 1,3,5,7 sec delay time is plotted and fitted with a linear fit. Heating rate derived from the linear fit is equal to $dN/dt = 40.5(8) * 10^3$ quanta/sec. The offset of $\sim 440,000$ quanta will be discussed later.

The data points can be fitted and the heating rate dN/dt can be extracted. The offset of quanta will be discussed in detail in section 3.6.2 and will be ignored for the purpose of deriving the heating rate. From the gradient of the fit a heating rate of $dN/dt = 40.5(8) \times 10^3$ quanta/sec was derived with equation A.8.

The measurement was repeated for secular frequencies of $\omega_z = 2\pi \times 287(1)$ kHz and $\omega_z = 2\pi \times 355(1)$ kHz. Comparing results from different secular frequencies gives a good indication if the results follow the expected $1/\omega^2$ dependency. Heating rates corresponding to the three secular frequencies $\omega_z = 2\pi \times 178(1)$ kHz, $\omega_z = 2\pi \times 278(1)$ kHz and $\omega_z = 2\pi \times 355(1)$ kHz are plotted in a log-log graph and fitted in Fig. 3.16.

To compare this result with other ion traps and ion species we calculate the electric field noise density S, that would cause such heating and multiply it by the secular frequency and thereby scale out the ion mass m and secular frequency ω_z. A summary of heating rate results from various experiments [75] is shown in Fig. 3.17 and the result from the discussed heating measurement is highlighted.

It can be seen in Fig. 3.17 that the heating rate for a Yb ion traps with small ion electrode

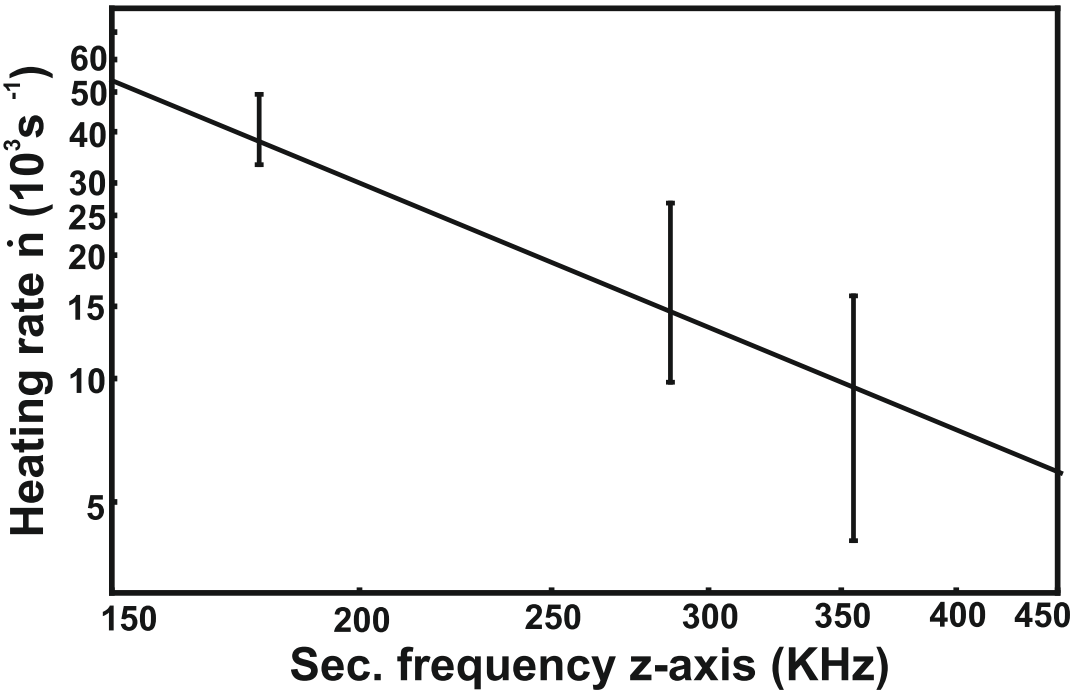


Figure 3.16: Plotting the heating rates for different secular frequencies $\omega_z = 2\pi \times 178(1)$ kHz, $\omega_z = 2\pi \times 287(1)$ kHz and $\omega_z = 2\pi \times 355(1)$ kHz vs ω with logarithmic scales illustrates the $1/\omega^2$ dependency of dN/dt.

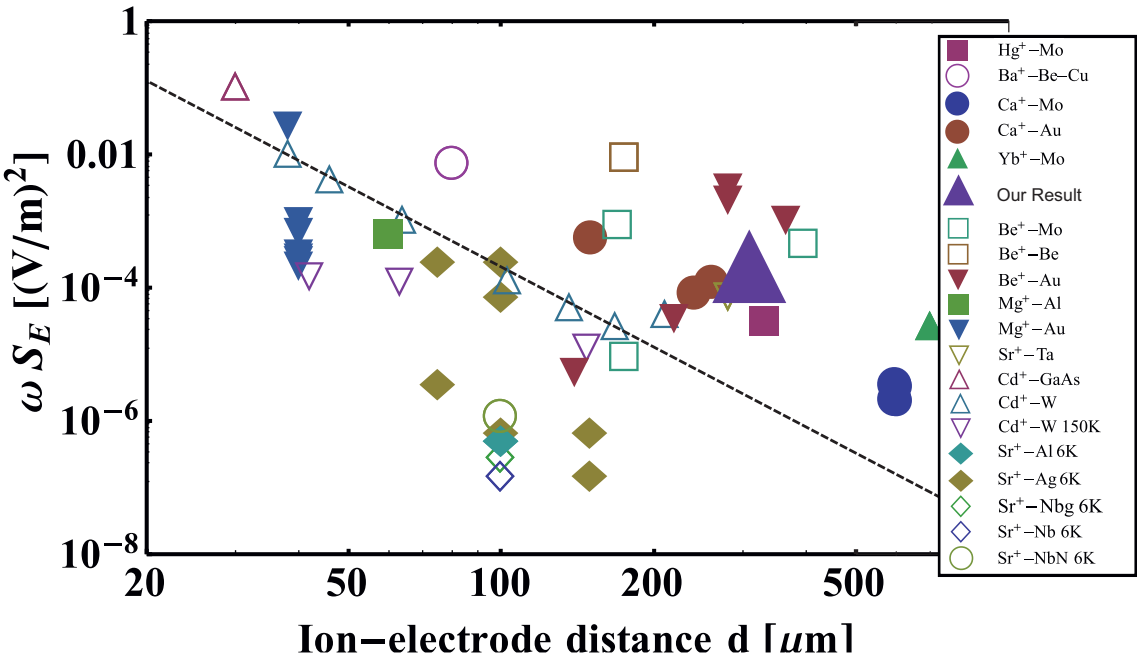


Figure 3.17: Heating rate vs ion electrode distance for different ion trap experiments marked according to ion species. Experiments performed at cryogenic temperatures show considerable lower heating rates.

distance is not significantly higher than for any other ion species.

3.6.3 Micromotion caused by RF Phase Mismatch

Coming back to the quanta offset in Fig. 3.15, after investigating possible causes for the offset it was concluded that the ion must experience micromotion that can not be compensated, also explaining the higher than expected linewidth L. One source of micromotion that can not be compensated is rf driven micromotion caused by a phase difference of electric potentials applied to the two rf electrodes. Phase differences are caused by different capacitances or path lengths of the connection from the helical resonator to rf electrodes. In the macroscopic blade trap the rf electrodes are connected to a single pin on the carrier mount using two wires. One of these wires was $\sim 2-3$ cm longer than then other one. This will lead to a phase mismatch of $\delta \sim 0.51°$ for 2 cm wire length difference and for a drive frequency $\Omega = 2\pi \times 21.48$ MHz. This rf phase mismatch has since been corrected by adjusting the wire lengths.

Following the work in [137, 138] we will investigate the effects of this phase mismatch on the transition linewidth and heating rate model. Instead of a zero electric field at the rf nil the phase difference δ will cause an electric field at the ion's trapping position of magnitude [138]:

$$\begin{aligned} E_{\mathrm{RFnil}} &= E_0 \cos \Omega t - E_0 \cos\left(\Omega t + \delta\right) \\ &\approx E_0 \delta \sin \Omega t \text{ for } \delta << 1 \end{aligned}$$

The non-vanishing oscillating electric field E_{RFnill} will exert a force $F = eE_{\mathrm{RFnill}} = m\ddot{x}$ onto the ion. The electric field E_0 can be determined by obtaining the basis function of one blade trap rf electrode, all dc electrodes and the second rf electrode are grounded. The basis function value at the trapping position will then be equal to E_0 and was determined to be $748,000$ V/m. Solving the equation of motion gives the micromotion amplitude x_{MM},

$$x_{\mathrm{MM}} = -\frac{qE_0\delta}{m\Omega^2} = 202 \times 10^{-9} \text{ m} \tag{3.5}$$

Assuming that the cooling beam enters the trap at a 27° angle to the micromotion axis which is additionally tilted by 59° with respect to the table, then the wavevector in direction of the micromotion will be $k_{\mathrm{MM}} \approx 0.46 \times 2\pi/\lambda$. The micromotion oscillation causes a Doppler shift equal to

$$k_{\mathrm{MM}} v_{\mathrm{MM}} = 0.46 \frac{2\pi}{\lambda} x_{\mathrm{MM}} \Omega \approx 940 \times 10^3 \text{ Hz} \tag{3.6}$$

which is of the same order as the shift created by 450,000 motional quanta for $\omega_z = 2\pi \times 178$ kHz and needs to be considered for the model.

Another process increasing the amplitude before recooling is a motional displacement inside the harmonic potential caused by radiation pressure. Implications on the Doppler recooling heating rate measurement are presented in [139]. Following this work we can approximate the radiation pressure onto the ion as:

$$F = \hbar k_z dN/dt(\Delta) = \hbar k_z \Gamma \frac{s/2}{1 + s + (2\Delta/\Gamma)} \tag{3.7}$$

After the cooling beam is turned off the radiation pressure vanishes and the displaced ion starts to oscillate in the harmonic potential. The amplitude of this oscillation will be on the order of $\sim$ 20nm as soon as the delay time period starts. In experiments without rf extrinsic micromotion this amplitude would be a dominant cause of a quanta offset when determining the heating rate. In the present experiment the rf phase mismatch amplitude is $\sim$ 10 higher and we do not investigate the radiation pressure further.

Using the approach in [114], the model can be extended for a three-dimensional case including micromotion. We will use the same approach but for a one-dimensional case. The micromotion happens in the radial direction and we're looking at heating in the axial direction. Nevertheless it will still affect the Doppler recooling beam and add a Doppler shift to the transition. The Lorentzian transition profile will have a different shape due to the micromotion Doppler shift. Following the work in [114] we can replace the transition $L(\Delta_{eff})$ with a different transition profile $R(\Delta_{eff})$, which includes the micromotion Doppler shift [140]:

$$R(\Delta_{eff}) = \sum_{n=-\infty}^{\infty} J_n^2(\beta) \frac{1}{1 + ((\hbar\Delta_{eff}/E_{0)} - n(\hbar\Omega/E_0))^2} \tag{3.8}$$

Where J_n is the n-th Bessel function, β is the so-called micromotion modulation index, equal to $\beta = | \ x_{MM} \cdot k_{MM} \ | = 1.58$. A comparison between the standard Lorentzian linewidth for 500,000 quanta and the micromotion transition linewidth is shown in Fig. 3.18.

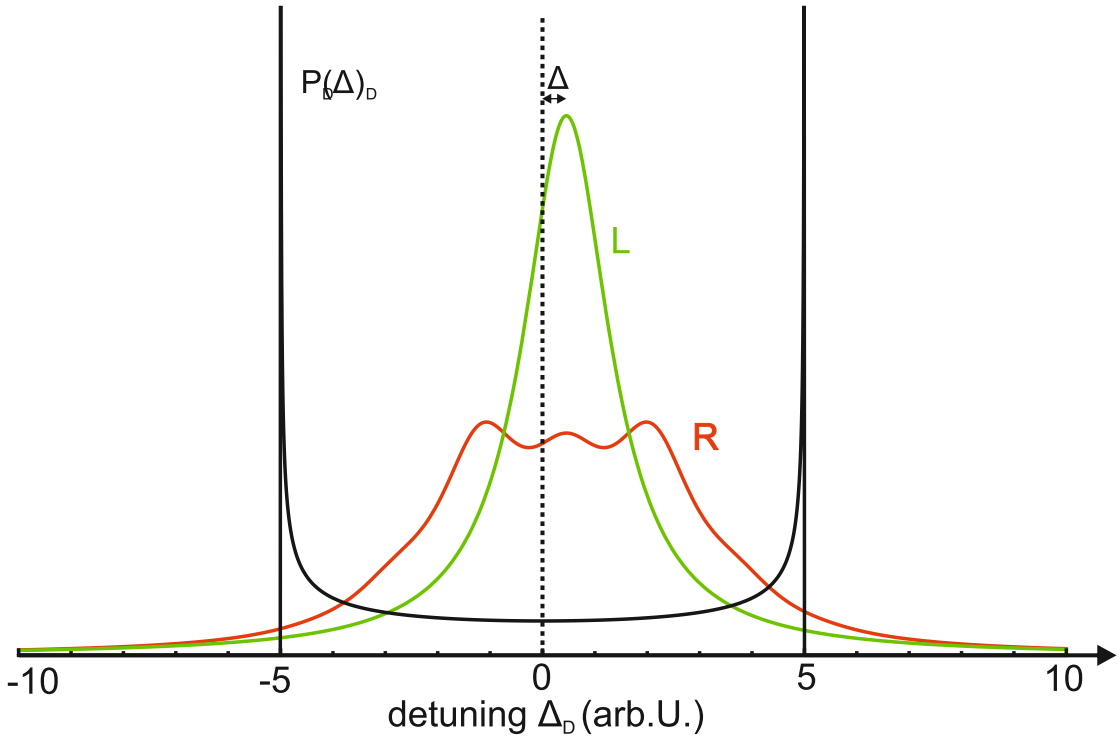


Figure 3.18: Power broadened transition linewidth L and micromotion modulated transition linewidth R are plotted with the probability density P.

Comparing the fluorescence rate f_{MM} of an ion with 10,000 quanta including micromotion sidebands and one f_{hot} with 450,000 quanta not including micromotion results in approximately the same scatter rate $\frac{f_{hot}}{f_{MM}} \sim 1.06$. We therefore assume that the offset in Fig. 3.15 is caused by the additional rf micromotion. More accurate calculations are not possible as the phase difference is only known with very large uncertainty.

Chapter 4

Microfabrication Techniques

Constructing a scalable ion quantum systems will require the individual traps to be microfabricated. Mechanically constructed and assembled traps are very useful for many quantum information experiments, but lack certain capabilities required for scalable systems. Small, precise and unlimitedly repeatable structures are essential for such a system and have been the basis for the tremendous success of computer chips, over one billion transistors can be fabricated and connected on an area of only 160 mm^2 [1].

When used for the construction of ion traps, it is possible to fabricate large numbers of trapping zones on a small area, including magnetic field gradients for microwave based entanglement. Trap electrodes, gaps, buried wires, vertical interconnect access (VIA) dimensions and dielectric thicknesses are of similar size as micro-electro-mechanical-systems (MEMS) features. Standard semiconductor technologies have been modified to create the larger MEMS structures, and can also be used to fabricate ion traps.

Successful operation and design of microfabricated ion traps requires certain additional issues to be addressed, when compared to macroscopic traps. As discussed in section 2.1.3, asymmetric designs cannot achieve trap depths as high as symmetric hyperbolic designs due to a geometric factor. To compensate, larger voltages must be applied to the asymmetric geometry. In addition, rf and dc electrodes are separated by only a few μm, which can ultimately result in voltage breakdown between electrodes [141].

When using conductive or semiconducting substrates, rf electrodes have to be electrically isolated from the substrates using a dielectric layer. Even when using a thick layer on the order of 10-15 μm the capacitance of the rf electrodes [142] can be strongly increased. This

[1] Intel Ivy Bridge 4C, 1.2B transistors on a 160 mm^2 chips

leads to additional rf losses in the substrate and increased power dissipation of the trap structure by adding an additional complex resistance to the resonant circuit. Additional trap resistances and large rf electrode capacitances will also decrease the quality factor Q of the resonator discussed in section 3.4.

Shrinking the trap dimensions can be useful when large oscillating magnetic field gradients are generated at the ions position [83], or strong motional coupling between ions in individual potential wells is desired [101]. On the other hand it will reduce the ion height, which is the distance of the trapped ion to the closest electrode and increases the motional heating in the trap due to the d^4 scaling of anomalous heating described in section 2.2.2. Designing structures with exposed dielectrics close to the ion can also lead to charge build-up, stray electric fields and even higher heating rates [143].

In the following chapter these issues will be addressed and solutions presented. Microfabrication techniques and processes successfully used to manufacture ion traps will be briefly outlined. The following discussion is largely based on work presented in [75].

4.1 Voltage Breakdown and Surface Flashover

High trap depths and secular frequencies can be achieved while maintaining a low q parameter, by applying very large rf voltages to an ion trap, see section 2.1.2. For initial trapping of ions high trap depths are essential and by using larger secular frequencies we can also achieve lower heating rates.

Small electrode-electrode gaps and thin dielectric layers separating electrodes will cause low breakdown voltages. Breakdown can occur either through a dielectric material (bulk breakdown), vacuum gaps between electrodes, or across an insulating surface between electrodes (surface flashover).

Commonly surface flashover occurs well before bulk breakdown and is the dominant factor limiting the amplitude of the applied rf voltage. The flashover can be explained with secondary electron emission avalanche effects [141]. Gas molecules on the surface desorb when electrons hop across the gap and lead to flashover in the desorbed gas layer. The initial electron emission starts at the interface of electrode, dielectric and vacuum, known as the triple point, shown in Fig. 4.1. Imperfections or spikes in the electrode structures at this point increase the electric field locally and will reduce the breakdown voltage. Further, the dielectric surface, over which flashover occurs, has a strong influence on the maximum

breakdown voltage. Recent investigations in our group showed that silicon nitride (Si_3N_4) deposited in a plasma-enhanced chemical vapor deposition (PECVD) reactor shows an increase in breakdown voltage of approximately 3.6, compared to a standard silicon dioxide (SiO_2) PECVD layer [141].

Bulk breakdown voltages are usually ∼2.5 times higher than surface breakdown voltages for the same dielectric material, electrode separation and deposition process [144]. When very thin dielectrics of ∼1-2 μm are used it can nevertheless become dominant. The maximum breakdown voltage V_{bulk} is related to the dielectric strength of an ideal capacitor by $V_{\text{bulk}} = dE$, where d is the thickness of the dielectric, illustrated in Fig. 4.1. There have been many studies into dielectric strengths and an inverse power law $E_c \propto d^{-n}$ was found [144–150]. Here n is the scaling parameter and was found to be on the order of $0.5 - 1$. Decreasing the dielectric layer thickness will increase the dielectric strength but ultimately not increase the breakdown voltage if the scaling parameter lies below one.

Before applying high voltages to a microfabricated trap it is recommended to carry out experimental tests on a similar structures to accurately determine the breakdown parameters. When designing traps it is important to avoid sharp corners that can give rise to large local electric fields, and to use Si_3N_4 as an insulating surface between rf and dc electrodes.

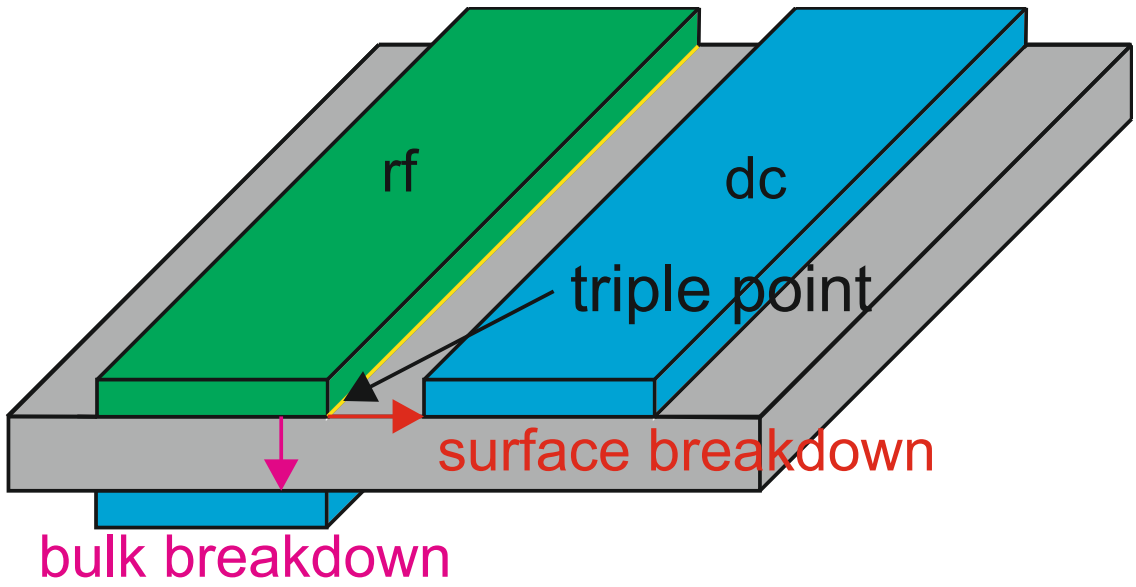


Figure 4.1: Schematic illustrating the paths for bulk and surface breakdown. Surface breakdown commonly originates from the marked triple Point.

4.2 RF Electrode Capacitance, Power Dissipation and Loss Tangent

When scaling up ion trap systems the increasing resistance R and capacitance C of the electrodes and rf losses in the dielectrics become more important. Also the inductance L of long on-chip rf electrode connections has to be evaluated. The power dissipation P_D of resistive electrode structures and lossy dielectrics can result in dramatic heating and even destruction of the trap. Large rf electrode capacitances and resistances will strongly affect the quality factor Q of the resonant circuit [104] (see section 3.4). Resonator size will increase with rf electrode capacitance and resistance to unpractical levels [104].

A simple linear trap, shown in Fig. 4.2, will be used to illustrate the following calculations for values of C, R, L and P_D. Two gold rf electrodes of width $w = 250$ μm, thickness $t = 5$ μm and length $l = 10$ mm are placed on a diamond layer with dielectric constant $\varepsilon_r = 5.7$. RF electrodes are separated from dc electrode by $s = 5$ μm on each side and from a ground plate by $h = 300$ μm. An rf potential of frequency $\omega = 2\pi \times 20$ MHz and amplitude V=200 V is applied to the rf electrodes.

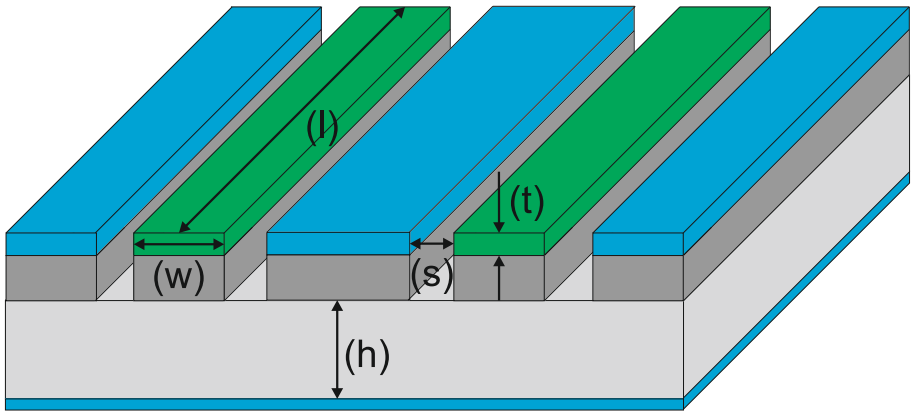


Figure 4.2: Example of an ion trap structure used to illustrate the calculations of C, R, L and P_D values.

4.2.1 Capacitance Calculation of RF Electrodes

To calculate the rf electrode capacitance of an ion trap we approximate the rf and dc electrode structure as a coplanar waveguide (CPW) with ground plate placed on the back of the trap substrates. The capacitance C of one rf electrode will consist of the capacitance to ground C_{GND} and capacitance C_{Strip} between rf and dc electrodes. Following the derivation in [151], capacitance C_{GND} between a metal strip and ground layer separated

by a dielectric is given by

$$C_{GND} = \frac{3\epsilon_0 l(\varepsilon_r + 1.41)}{\ln \frac{5.98h}{0.8w+t}} \tag{4.1}$$

where ϵ_0 is the vacuum permittivity constant. We can derive the capacitance C_{GND} for one rf electrode to $C_{GND} = 0.87$ pF. Capacitance between rf and dc electrodes will be approximated as the capacitance between two microstrips sitting on a dielectric with $\varepsilon_r = 1$. Based on the calculations in [152] we can write

$$C_{Strip} = \epsilon_0 \varepsilon_r \frac{K(k_1)}{K'(k_1)} l \tag{4.2}$$

the ratio between $K(k_1)$ and $K'(k_1)$ is equal to

$$\begin{aligned} \frac{K(k_1)}{K'(k_1)} &= \pi \ln \left(2 \frac{1 + (1-k^2)^{1/4}}{1 - (1-k^2)^{1/4}} \right)^{-1} && for\ 0 \leq k \leq \frac{1}{\sqrt{2}} \\ &= \frac{1}{\pi} \ln \left(2 \frac{1+k}{1-k} \right) && for\ \frac{1}{\sqrt{2}} \leq k \leq 1 \end{aligned}$$

where $k = \frac{w}{w+2S}$ [152]. Capacitance for the entire trap structure will be $C_{total} = 2 \times C_{GND} + 4 \times C_{Strip} \approx 2.34$ pF.

4.2.2 Inductance Calculation of RF Electrodes

In a similar way the inductance of the rf electrodes is approximated with the inductance between two plates representing the rf electrode and ground layer $L = (\mu_0 \mu_r l h)/w$ [153], where μ_0 is the vacuum permeability. The inductance between rf and dc electrodes is approximated with the inductance between two wires $L = \mu_0 l/(\pi \cosh[\frac{s}{w}])$ [154]. Assuming $\mu_r \approx 1$ we can calculate the total impedance for both rf electrodes to

$$L_{total} = \frac{\mu_0 \mu_r l h}{2w} + \frac{l \mu_0}{4\pi \cosh[\frac{s}{w}]} \approx 8.04 \text{ nH} \tag{4.3}$$

4.2.3 Resistance of RF Electrode

Before calculating the resistance R of the electrode we have to evaluate if the skin effect will be of importance as it would reduce the area of current flow. Skin depth δ for metals can be calculated according to

$$\delta = \sqrt{\frac{2\rho}{2\pi f \mu_0 \mu_r}} \tag{4.4}$$

Here ρ is the material specific resistance and equal to $\rho = 22.14$ nΩ·m for gold, $f = \Omega/(2\pi) = 20$ MHz and $\delta = 16.74$ μm. If the trap electrodes are made of gold and the trap is operated below 50 MHz, then the skin depth will be on the order of 10 μm and can therefore be ignored. Resistance R is then simply calculated to $R = 0.18\ \Omega$ with

$$R = \frac{\rho l}{wt} \tag{4.5}$$

4.2.4 Loss Tangent of the Dielectric Layer

The loss tangent $\tan\delta$ represents the ratio between lossy resistance and lossless reactance in a capacitor. Loss tangent resistance is fundamentally caused by changing the polarization of dielectrics in an oscillating field, which causes friction on a molecular level converting electrical energy into heat. The loss tangent will depend on the dielectric material used, frequency of the oscillating field [155–158] and temperature of the dielectric [157, 159]. Values are often studied in the GHz range for microwave integrated circuit applications [160], diode structures at kHz range [159, 161, 162] and sometimes in the MHz range [161–163]. The loss tangent for the diamond used in the trap structure is ~ 0.01 at room temperature [157, 158].

The loss tangent will also result in a serial equivalent conductance of the dielectric Layer. Before deriving the power dissipated in the trap P_D, this conductance of the dielectric needs to be calculated. To account for the loss tangent dielectric losses, a complex permittivity ε, with $\varepsilon = \varepsilon' + i\varepsilon''$ is used. Lossless parts are represented by ε' and lossy parts by ε''. By substituting this into Ampere's circuital law and rearranging we obtain [164]

$$\boldsymbol{\nabla} \times \mathbf{H} = \left[\left(\sigma + \Omega\epsilon''\right) - i\Omega\epsilon'\right] \mathbf{E} \tag{4.6}$$

where σ is the conductivity of the dielectric for an applied alternating current and Ω is

the drive frequency. The effective conductance is represented by $\sigma' = \sigma + \Omega\epsilon''$. The ratio of the conduction to displacement current densities is equal to the loss tangent $\tan\delta$

$$\tan\delta = \frac{\sigma + \Omega\epsilon''}{\Omega\epsilon'} \tag{4.7}$$

For a good dielectric the conductivity σ is much smaller then $\Omega\epsilon''$ and we can then make the following approximation: $\tan\delta = \epsilon''/\epsilon'$. For a parallel plate capacitor the real and imaginary parts of the permittivity can be expressed as [161]

$$\varepsilon' = \frac{Cd}{\varepsilon_0 A}, \qquad \varepsilon'' = \frac{Gd}{\varepsilon_0 \Omega A} \tag{4.8}$$

Substituting this into the approximated loss tangent expression, the conductance can be expressed as

$$G = \Omega C \tan\delta \tag{4.9}$$

4.2.5 Power Dissipation in Ion Trap Structures

Now that we have derived and acquired values for capacitance C, inductance L, resistance R and dielectric conductance G, the power dissipation in the trap P_D can be calculated using a simple lumped circuit model, as shown in Fig. 4.3.

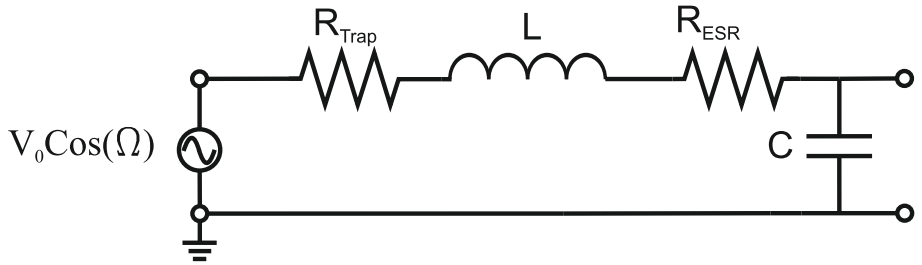


Figure 4.3: The rf electrode modelled with electrode resistance R_{Trap}, capacitance C, inductance L and equivalent series resistance R_{ESR} resulting from the dielectric conductance G.

Based on the lumped circuit we can write the complex impedance of the trap structure as a combination of the real electrode resistance R_{Trap} and equivalent series resistance of the dielectric $R_{\text{ESR}} = \frac{G}{\Omega^2 C^2}$ [165] and the complex impedances of capacitive $\chi_C = \frac{1}{\Omega C}$ and inductive reactance $\chi_L = \Omega L$.

$$Z_{\text{total}} = R_{\text{Trap}} + \frac{G}{\Omega^2 C^2} + i\left(\frac{1}{\Omega C} - \Omega L\right) \tag{4.10}$$

The real resistances R_{Trap} and R_{ESR} will lead to power dissipation in the trap. The reactance χ_C and χ_L do not dissipate power but result in charge accumulation in the trap structure. For the previously calculated capacitance and inductance values ($C \approx 2.34$ pF, $L \approx 8.04$ nH) and drive frequency $\Omega = 2\pi \times 20$ MHz, the capacitive reactance $\chi_C = 3392.3\ \Omega$ will be much higher than the inductive reactance $= 0.1\ \Omega$ and we can simplify the impedance with $Z_{\text{total}} = R + ESR + i\chi_C$. The power dissipated in the trap structure can then be derived by multiplying the real resistance of the trap $Re(Z_{\text{total}})$ with the square of the RMS[2] current in the system $P_D = I_{rms}^2 \times Re(Z)$ [166]. The RMS current in system is equal to the rms voltage divided by the magnitude of the impedance.

$$\begin{aligned} P_d &= Re(\frac{V_{rms}^2}{Z_{\text{total}}}) \\ &= V_{rms}^2(\frac{\Omega^2 C^2}{R_{\text{Trap}}\Omega^2 C^2 + G + \Omega C})^2(R_{\text{Trap}} + \frac{G}{\Omega^2 C^2}) \end{aligned}$$

In the discussed trap structure, shown in Fig. 4.2, the power dissipated by the two rf electrodes for an applied rf voltage of $V = 200$ V is then equal to 57.95 mW. We can simplify the equation for the common case of $R_{\text{Trap}} << \chi_C$ and $R_{\text{ESR}} << \chi_C$, which will be the case for a dielectric with $\tan\delta \leq 0.01$ to:

$$P_d = V_{rms}^2 \Omega C(\Omega C R_{\text{Trap}} + \tan\delta) \tag{4.11}$$

In addition to the power dissipation, the loss tangent will also affect the Q of the resonator as it increases the series resistance of the entire resonant circuit, which reduces the Q as discussed in section 3.4.

4.3 Extrinsic Micromotion and Motional Heating

When operating microfabricated asymmetric traps, the heating rate ($\frac{dN}{dt} \propto d^{-4}$) and micromotion become more dominant factors with smaller ion height d. With increased heating and micromotion the Doppler cooling limit will be increased, quantum operation fidelities and ion lifetime will be reduced and in the worst case, trapping becomes impos-

[2] Root mean square

sible. When designing ion trap architectures for small ion heights (< 100 μm), one has to therefore take precautions to limit the impact of these factors and also consider extra measures to combat anomalous heating and micromotion.

4.3.1 Micromotion

Intrinsic micromotion (as discussed in section 2.1.2) is caused by the ion's secular oscillation in and out of the rf nil. If the ion is at a constant displacement from the rf nil, which can be caused by static stray fields, imperfect trap electrodes or rf phase mismatch, we speak of extrinsic micromotion. Extrinsic micromotion, if uncompensated, adds sidebands to the Doppler cooling transition, broadening the linewidth as observed in section 3.6.3. This will reduce the effectiveness of Doppler cooling and increase the Doppler cooling limit, potentially preventing sideband cooling and reducing lifetimes of trapped ions when not cooled [137].

Static stray fields are very common in any type of ion trap and extremely difficult to avoid entirely. Adding a sufficient number of dc electrodes and placing them correctly allows for the stray fields to be compensated. Before compensation can start an ion must first be trapped. In the case where stray fields are so strong that trapping becomes impossible, large voltage parameter spaces have to be tested, and the ion trap can become completely unusable until charges dissipated.

Stray fields can be caused by charges accumulating on dielectric surfaces, from ionized Yb atoms or other background gas particles. It has also been demonstrated that dielectrics exposed to laser light can either directly charge up [167, 168] or the adsorbents on the surface can be ionized. Another cause for strong stray fields can be loading flux atoms deposited on the metal electrodes, as illustrated in Fig. 4.4 (a). Thin insulating adsorbent layers or native oxides (for aluminium electrodes) reduce the charge flow to ground from deposited ionized Yb and charges caused by the photoelectric effect. Ytterbium has a workfunction of 2.51[3]/2.45[4] eV [169], which is lower than the cooling laser light photon energy of 3.36 eV for 369 nm. If large amounts of Yb are deposited on the electrodes over time, the trap can instantly charge up when the cooling beams are turned on and trapping becomes impossible [170].

The effects of charges on dielectrics can be reduced by shielding the insulating layers from

[3] (111)surface
[4] (110)surface

trapped ions via ground plates or high aspect ratio gaps between rf and dc electrodes. Deposits on electrode surfaces can be removed performing an *in situ* cleaning using a high power laser beam [121] or more efficiently a sputter gun [86, 87]. Additionally it is possible to use backside loading techniques [99, 171], which prevent the deposition of Yb on electrodes entirely.

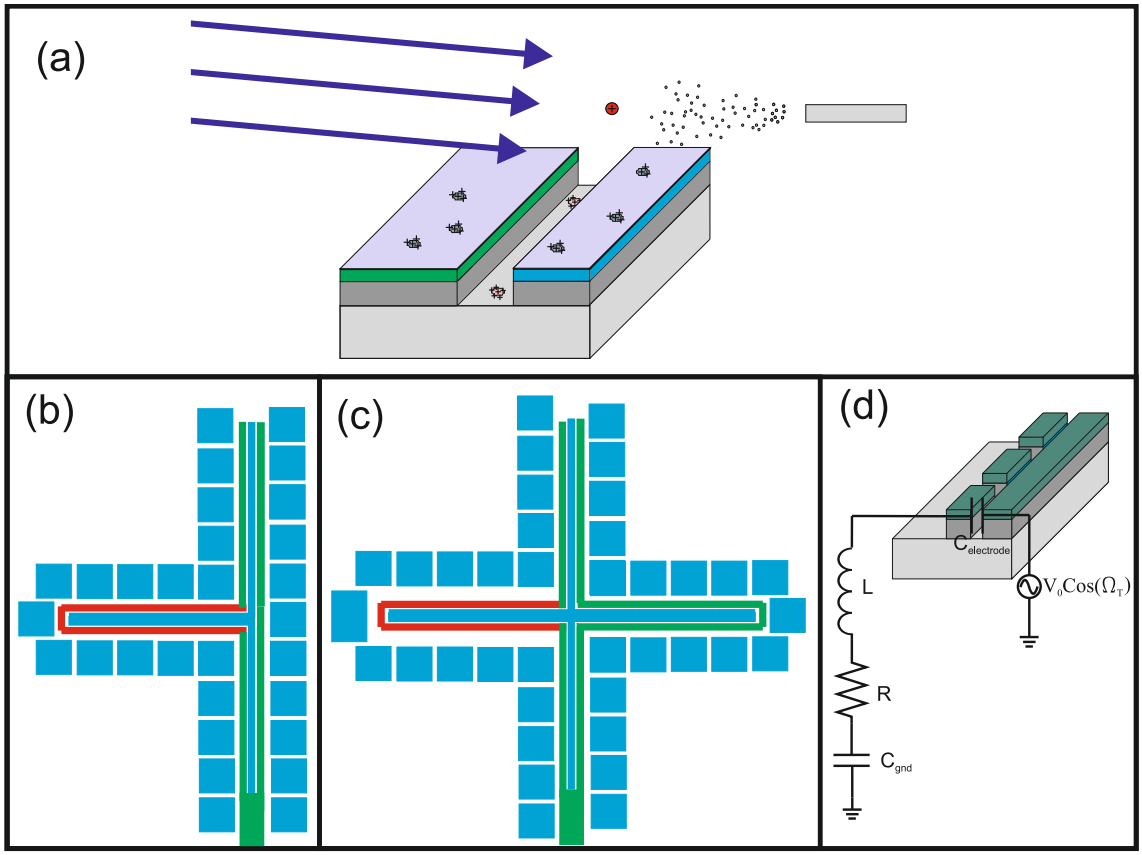


Figure 4.4: Schematic showing different causes of extrinsic micromotion. (a) Static micromotion caused by charging of deposited loading flux atoms and accumulation of charges on dielectrics. (b) shows electrodes with different rf path lengths (marked in red). In (c) electrodes with different rf path impedances. One arm of the junction (marked red) has a lower capacitance than the rest of the electrode structure. (d) Non-zero rf potential on dc electrodes resulting from high impedance to rf ground.

A different type of extrinsic micromotion is caused by a phase mismatch between the rf potential on the rf electrodes or a non zero rf potential on dc electrodes. This type of micromotion can not be compensated and will lead to the same detrimental effects as the previously discussed micromotion. RF phase mismatches, as discussed in section 3.6.3, are caused by different path lengths Δl or unequal complex impedances ΔZ of the transmission lines to the rf electrodes, see Fig. 4.4 (b),(c). A difference in path length of $\Delta l = 20$ mm will lead to a phase mismatch of $\delta \approx 1°$ for a drive frequency of $\Omega = 2\pi \times 40$ MHz.

An unequal complex impedance of the transmission lines $\Delta Z = \Omega\sqrt{L_1C_1 - L_2C_2}$ results

in different wave speeds $v = \Omega/Z$. As an example, for two transmission lines of length 5 mm, inductances $L_1 = L_2$ on the order of 10^{-8} H and a difference in capacitance of $\Delta C = (10 - 5)$ pF the phase mismatch would be equal to $\delta \approx 1.5°$.

Similar extrinsic micromotion can be caused by non-zero rf potentials on the dc electrodes. If the path to rf ground via dc electrodes has a significant inductance or resistance as shown in Fig. 4.4 (d), then the rf potential will be non-zero on the electrode. For the vacuum system described in section 3.3, dc electrodes are connected to rf ground via a $\sim$ 50 cm long, 0.3 mm diameter copper wire, which has an inductance of $\sim$ 800 nH. Assuming a drive frequency of 20 MHz, rf amplitude of 600 V and a capacitance between rf and dc electrode of $\sim$ 0.5 pF, the rf potential on the dc electrode will be on the order of 4 V. The wire resistance can be mostly ignored as the impedance resulting from the wire inductance is dominant ($Z \approx 100\ \Omega$) at the discussed frequency. Grounding the dc electrode as close as possible to the trap using a capacitor is therefore essential.

By keeping the sources of extrinsic micromotion in mind during the system and trap design, one can almost completely avoid the related issues. Dielectrics should be shielded from the rf nil, electrodes made of gold or other non oxidizing materials and *in situ* cleaned, and backside loading used for trapping. Additionally rf electrode path lengths and complex impedances should be equal, and dc electrodes grounded via capacitors close to the trap.

4.3.2 Anomalous heating

Microfabricating ion traps makes it possible to bring the rf nil very close to the surface, which can be beneficial for experiments requiring strong magnetic field gradients [83] or very small distances between individual trapping wells [101]. Smaller ion-electrode distances will also reduce the footprint of junctions for large scale systems. However, we must also consider that a lower ion-electrode distance will increase the heating rate according to the d^{-4} dependency of anomalous heating, see section 2.2.2.

If the ion height is reduced too much, motional heating rates will be on similar magnitude as the photon scattering rate, making laser cooling impossible. Depending on the particular application, there may be more stringent constraints. For example, in order to realize high fidelity quantum gates that rely on motional excitation for the entanglement of internal states [172, 173] of ions, motional heating should be negligible on the timescale of the quantum gate. This timescale is typically related to the secular period $1/\omega_m$ of the ion motion, however, can also be faster [174]. The heating rate has to be reduced by

increasing the ion height or other methods.

Scaling of heating rates was investigated using an ion trap with moveable needle electrodes and found to be $\dot{\bar{n}} \sim d^{-3.5\pm0.1}$ [118]. In this experiment it was also found that the heating rate can be suppressed by cooling the electrodes. After further investigations using a 4 K cryostat [120], a scaling law for the temperature dependence of the field noise density of $S_E(T) = 42(1 + (T/46K)^{4.1}) \times 10^{-15}$ V^{2}m^{-2}/Hz was determined. Superconducting ion traps with niobium and niobium nitride electrodes were also tested above and below the critical temperature T_c. The heating rate did not change significantly when the material went from normal states [175] to the superconducting state. Within the same study, heating rates were reported for gold and silver trap electrodes at the same temperature (6 K) showing no significant difference between the two and superconducting electrodes. This indicates that the heating rate is mostly independent of the bulk characteristics of the electrode materials and is dominated by the surface characteristics. Other experiments have also shown that coating of the electrode with an atom flux increases the heating rate [176].

Based on this experimentally gained knowledge, theoretical models where developed to describe observed anomalous heating. Different models were proposed, one based on small patches (on the order of 1 μm) of different potentials [177], based on surface adsorbents and changing crystal orientations. This model also explains the non-contact friction found in atomic force microscope (AFM) experiments between a surface and the AFM tip [178,179] and noise caused by surface patches in gravitational wave detectors [180]. Non-contact friction measurements also indicate a doubling of the heating rate if the closest surface is a dielectric [143]. Another theory explains anomalous heating with the fluctuating dipoles of adsorbed atoms on the electrode surfaces [181]. Cleaning of the electrodes [86, 87, 121] dramatically lowered measured heating rates, which supports this model but doesn't rule out the other one.

More detailed experimental analysis will be necessary to determine which model is more accurate and if it's possible to completely eliminate anomalous heating. Fig. 4.5 shows a collection of published motional heating results including results for *in situ* cleaned electrodes and cryogenically cooled traps. Instead of plotting the actual heating rate, the spectral noise density $S_E(\omega_m)$ is multiplied with the secular frequency in order to remove the dependence on ion mass or secular frequency.

We note that previous experiments [90,118] consistently showed $S_E(\omega_m) \sim 1/\omega_m$ allowing

the secular frequency to be scaled out by plotting $S_E(\omega_m) \times \omega_m$ rather than just $S_E(\omega_m)$.

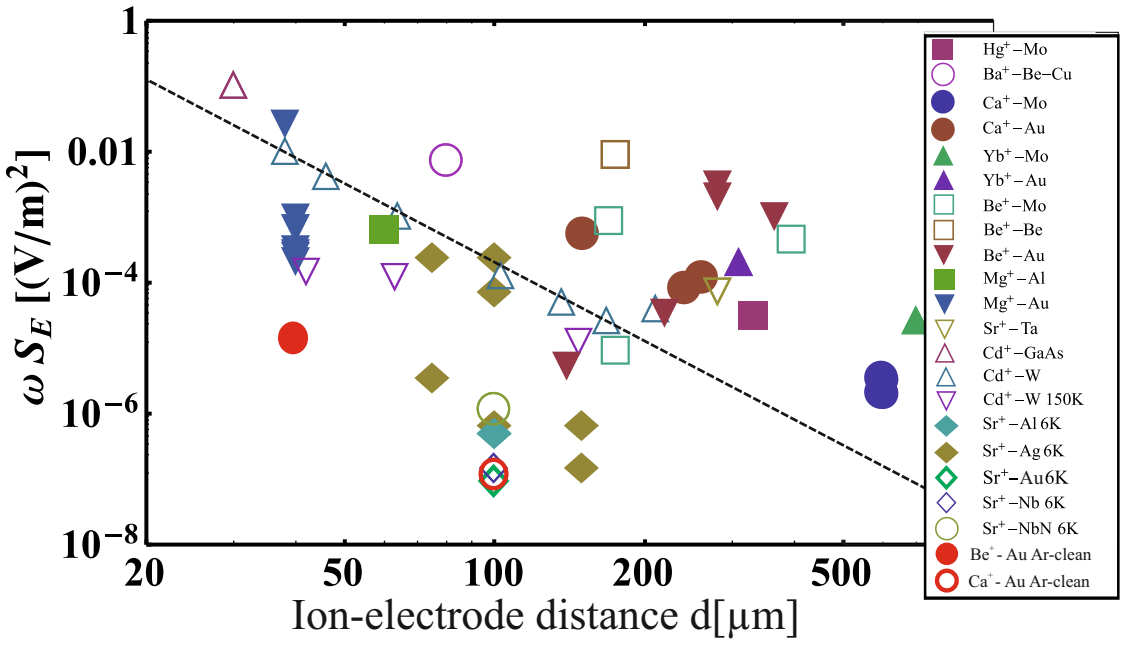


Figure 4.5: Published measurements of motional heating are compared by calculating the electric field noise spectral density $S_E(\omega)$ and multiplying it with the corresponding secular frequency ω. Resulting field noise densities, independent of experimental setup and ion species are plotted versus the ion-electrode distance d. Each label shows both the ion species and the electrode material used, the electrode temperature is also noted if the measurement is performed below room temperature and if the electrodes are sputter cleaned. Additionally a d^{-4} trend line is plotted for standard measurements. Data point are associated with the references: (Hg$^+$−Mo [182], Ba$^+$−Be-Cu [170], Ca$^+$−Mo [183], Ca$^+$−Au [100, 176, 184], Yb$^+$−Mo [185], Yb$^+$−Au [90], Be$^+$−Mo [117], Be$^+$−Be [117], Be$^+$−Au [117, 186], Mg$^+$−Al [138], Mg$^+$−Au [77, 99, 138, 187, 188], Cd$^+$−GaAs [76], Cd$^+$−W [118], Cd$^+$−W 150K [118], Sr$^+$−Al 6K [175], Sr$^+$−Ag 6K [119], Sr$^+$−Nb 6K, Sr$^+$−NbN 6K [175], Sr$^+$−Au 6K [120], Be$^+$−Au Ar-cleaned [86], Ca$^+$−Au Ar-cleaned [87]).

4.4 Microfabrication Technologies

Making use of MEMS fabrication techniques we can design a fabrication process most suitable for a particular trap design. Common techniques used to fabricate ion traps are outlined in this section and fabrication processes successfully used to manufacture asymmetric traps are discussed. Examples are presented for all fabrication processes, advantages and disadvantages are discussed.

4.4.1 Lithography

The most common technology used when creating MEMS structures is the photolithography. Photolithography allows structures on a photo mask to be transferred into a photoresist. Photoresist is a photosensitive chemical that either becomes soluble (positive resist) in a developer chemical after being exposed to ultra violet light or stays on the sample (negative resist). Independent of how the structures are created, by deposition of materials (Bottom Up) [77] or etching into materials deposited on a wafer (Top Down) [76], fabricating the structures starts with lithography. A different technique makes it possible to write designs directly into the resist using an electron-beam (e-beam). This lithography can create smaller features sizes but is much slower and more expensive. Ion trap structures usually have dimensions well above the minimum feature size of standard photolithography (on the order of 1 μm), therefore e-beam-lithography is not required and will not be discussed further here.

Photoresist

Two types of photoresists are commonly used in microfabrication, negative and positive resist. When negative photoresist is exposed, polymers in the resist cross-link with each other, which is further enhanced by a post exposure bake. The cross linked parts become insoluble to the photoresist developer, see Fig. 4.6 (g). Developers are aqueous alkaline solutions that dissolve non cross-linked parts of negative resist.

Negative resist is preferably used for lift-off processes, where material is deposited on top of the resist and in open areas of the substrate. If the entire negative resist layer is not fully exposed (underexposed), resist close to the sample surface is not fully cross-linked. During development underexposed resist is slowly dissolved by the developer depending on how many polymers are cross-linked. Underexposed parts dissolve quicker and an undercut is formed in the resist profile after development. This undercut prevents the coating of the resist sidewalls and no physical connection between material in trenches and on top of the resist is made as long as the resist thickness is about twice as thick as the deposited layer. After deposition, the sample is placed in a solvent, which creeps between resist layer and sample surface lifting off the resist from the substrate including the material deposited on top.

The chemical composition of positive resist changes when exposed and a developer can

dissolve the otherwise stable composition as shown in Fig. 4.6 (h). Besides the difference in polarity of the structure with respect to the mask, positive resist will also not cause an undercut when underexposed but rather show slanted sidewalls.

Spin Coating

Before the exposure step can start resist has to be applied to the substrate using a spin coater first. Wafers or substrate pieces are cleaned and dehydrated and then placed on chucks that can be accelerated to speeds of up to 6,000 revolutions per minute (rpm). A sufficient quantity of photoresist is applied to the substrate using a pipette or directly poured out of a bottle. The spin coater then evenly distributes the resist and thicker and thinner layers can be created, by varying the rotation speed of the chuck.

If rectangular wafer pieces are used with a spin coater, the resist will form an uneven coating and the thickness will be higher than intended in the corners, which is known as edge-beads formation (see Fig. 4.6 (b)). In addition to spinning the pieces at very high rpm (4,000-6,000) one can also carefully remove the thicker resist in these areas using a solvent. If thick edge-beads are left on the substrate then the resolution of the lithography will be reduced, as the minimum distance between resist and mask is increased.

After successful spin coating the resist needs to be softbaked on a hotplate, removing remaining solvents and increasing the stability of the resist.

Mask Alignment and Exposure

Next, a mask aligner is used to accurately position the photo mask with respect to the substrates. Designs are created using a special CAD mask software and send to a mask manufacturing company as GDSII file, where lasers or e-beam-lithography are used to pattern a chrome layer on a quartz or soda-lime glass plate. Multiple fabrication layers can be aligned to each other using alignment marks and the mask aligner. After successful alignment the mask is pressed against the substrate and light from a mercury lamp with emission lines at 365 nm, 405 nm and 436 nm exposes the resist. Negative resist is designed to have a maximum absorbtion at the I-line of Hg lamps (365.4 nm) and an optical I-line bandpass filter is used to filter all other wavelengths out. The required exposure dose will depend on the type and thickness of resist and desired structures. The photoresist manufacturer can supply the required dose and the exposure time can be calculated if the

tool is accurately calibrated.

Development

After exposure, negative resist is baked a second time, positive resist can be directly developed. If the resist is intended for a lift-off process then the developed structures should also be de-scummed. Descumming removes possible resist contaminants in trenches and other areas. Descumming is performed in a plasma ash step where an oxygen plasma slowly burns away $\sim 100 - 200$ nm of resist.

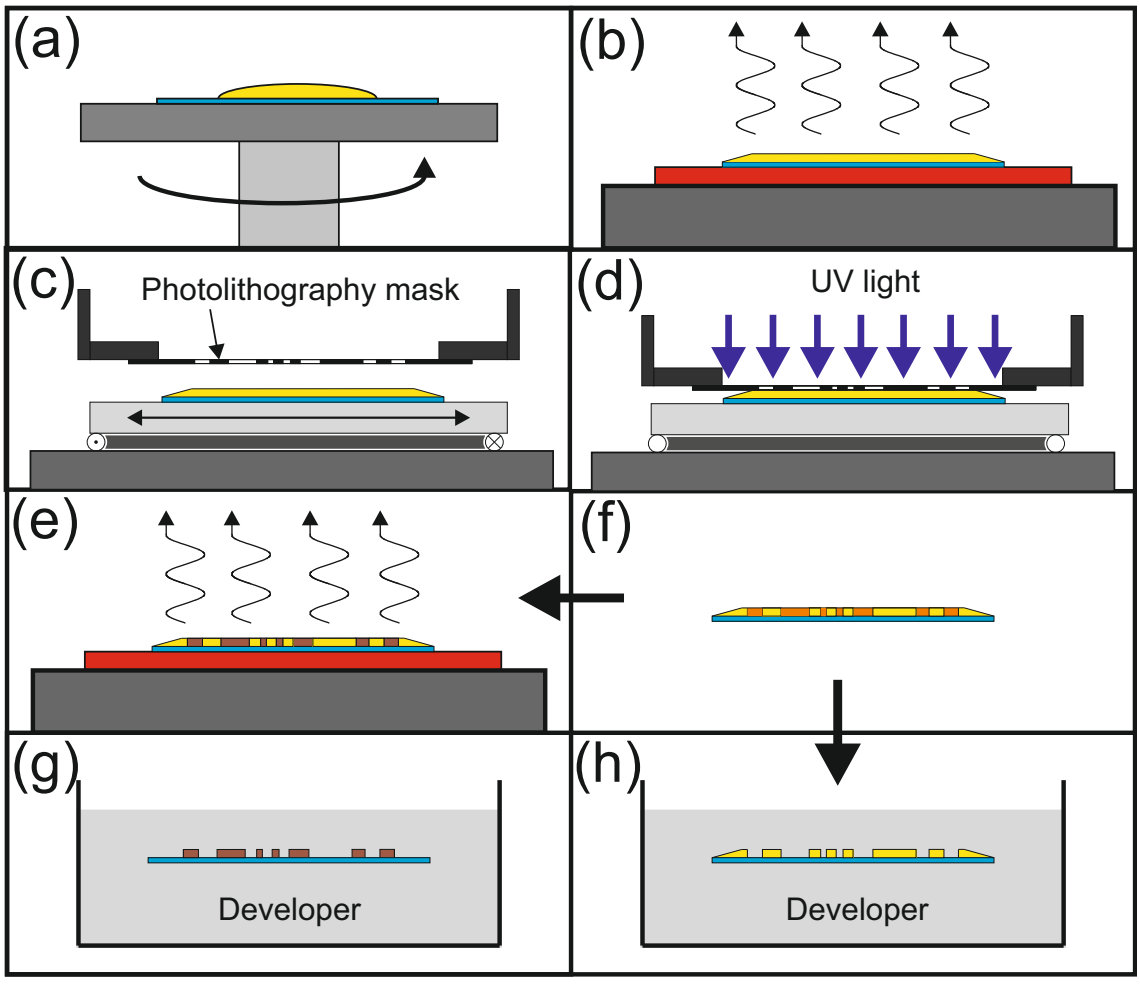


Figure 4.6: Schematic of the photolithography, starting with the spin coating of a substrate piece (blue) (a). (b) Followed by a soft bake on a hot plate. (c) The coated substrate and mask aligner are prepared for exposure. (d) After mask alignment the mask is pressed against the substrate and exposure starts. Schematic (f) shows the exposed photoresist (orange), which is either directly developed for positive resist (h) or post exposure baked (e) and developed if negative resist is used (g).

4.4.2 Deposition

Depending on the process, dielectric or metal layers can be deposited in a lift-off step or patterned afterwards using an etch step. Thick dielectric layers (> 500 nm of SiO_2 or Si_3N_4) can be deposited in a plasma-enhanced chemical vapor deposition (PECVD) reactor unsuitable for lift-off. Thinner dielectric and metal layers are deposited in physical vapour deposition (PVD) tools, where a directional atom flux coats the substrates.

Electron-beam Evaporation

Starting with PVD techniques, the most suitable processes for thick metal lift-off layers are electron-beam or thermal evaporation. Source material is placed in a special high temperature crucible and heated until the material sublimes. The chamber containing the material and substrates is evacuated to a pressure of $\sim 10^{-7}$ Torr, allowing evaporated atoms to reach the target. For thermal evaporation the entire crucible is heated up, leading to higher amounts of contaminants and less constant deposition rates. A cleaner and more constant evaporation is achieved by locally heating the material with a high energy electron-beam see Fig. 4.7 (b). Only the source material is evaporated, while the crucible is water cooled preventing contamination of the target.

To deposit exact film thicknesses a quartz crystal, shown in Fig. 4.7 (b), is placed next to the sample holder. When material is deposited on the crystal the mass of it changes and with it the oscillation frequency. A controller measures the oscillation frequency, determines the deposition rate, total deposition thickness and also blocks the atom flux with a shutter after the desired thickness is reached.

A large distance between evaporation source and substrate of up to one meter ensures a low incident angle of the flux onto the substrate. Additionally the sublimed atoms hit the sample with lower kinetic energy, when compared to a sputter deposition, resulting in a lower mobility on the surface, making this techniques preferable for lift-off processes.

Besides metals, dielectrics and semiconductors can also be deposited in an e-beam evaporator, including indium tin oxide (ITO), SiO_2, aluminium dioxide (Al_2O_3).

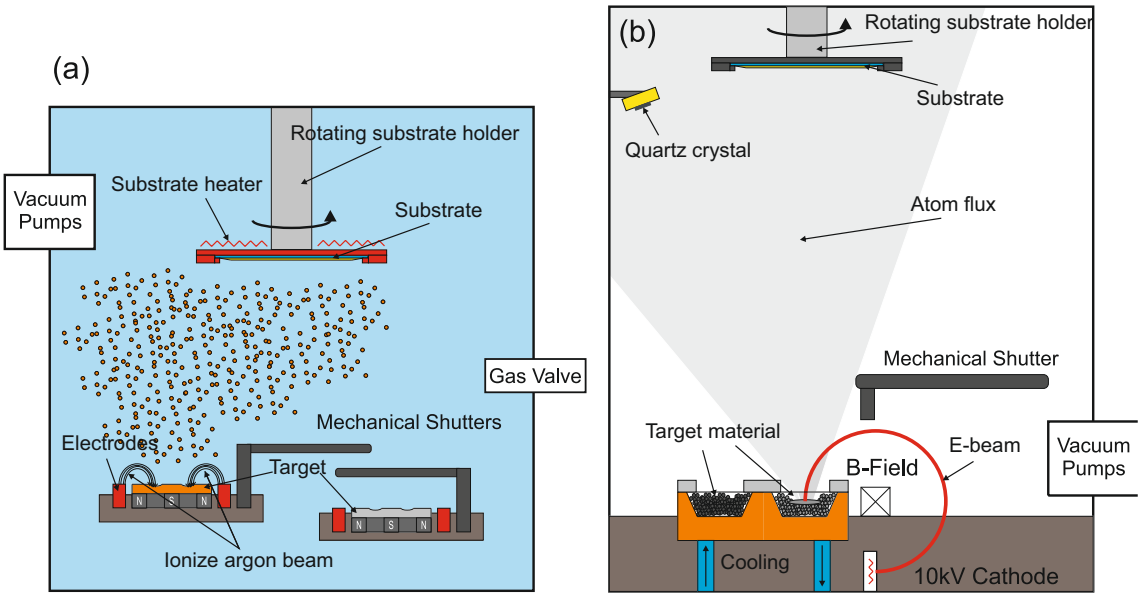


Figure 4.7: (a) Pictures showing a sputter deposition tool, with heated and rotating sample holder. Argon gas is led into the chamber, ionized and accelerated onto the deposition materials. Static magnetic fields are used to increase the plasma density. (b) Schematic of an E-beam deposition tool, showing crucibles filled with deposition materials. The beam is bent at 270 ° by a magnetic field onto the crucible. Next to the rotating substrate holder a quartz crystal is placed recording the thickness of deposited material.

Magnetron Sputtering

Sputtering is a different PVD method commonly used in MEMS fabrication. Argon gas is led into the chamber maintaining a pressure of ∼3-50 mTorr. The gas is then ionized using large dc or rf electric fields. A magnetron field compresses the plasma, which is accelerated onto metal or dielectric targets. In contrast to evaporation, the deposition material is bombarded by the plasma atoms and knocked out of the water cooled target. The flux atoms have a higher kinetic energy and higher mobility on the substrate surface. Also the distance between sample and deposited material is much smaller, which makes this method less suitable for lift-off processes. The deposition is more even and deposition rates are more constant then e-beam evaporation. This makes sputtering very suitable for highly uniform optical coatings and seed layer deposition for electroplating.

Plasma-enhanced Chemical Vapor Deposition (PECVD)

PECVD reactors are used for the deposition of thick dielectric or semiconducting layers. The substrate is placed inside a vacuum chamber (called reactor), shown in Fig. 4.8 (a), on a sample holder and heated to several hundred degree Celsius. Process gases are then led into the chamber via a so called shower head and an applied rf field (∼20 W of rf

power at 13.56 MHz) ionizes the gas atoms creating a plasma. A small static potential between the table and plasma pushes the ions to the sample surface and locally increases the plasma density. The ionized gases react with each other at the sample surface and form a dielectric layer. Due to the high sample temperature and ion bombardment of the surface the process is a constant deposition and desorption of material, with the ratio determined primarily by the substrate temperature. To deposit SiO_2 a silicon and oxygen precursor gas like silane SiH_4 and nitrous oxide N_2O are ionized in the chamber, to deposit Si_3N_4, SiH_4 and ammonia NH_3 are used.

Higher (13.56 MHz) and lower rf frequencies ($<$ 1 MHz) can be combined in a cyclic process to create denser layers. [189]. The higher frequency creates the plasma and the low frequency accelerates it onto the surface.

Electroplating

Electroplating is an electrochemical deposition technique and used to create very thick metal layers on top of a conductive seed layer, most commonly copper or gold. While e-beam deposition is limited to 5-10 μm thick layers, electroplating has the potential to create several hundred μm thick metal layers [190] and fill wafer through holes with very high aspect ratios. The required setup is very inexpensive, simple to use and achieves deposition rates much faster than with PVDs. A simple beaker or tank, see Fig. 4.8 (b), is filled with the plating solution, for example copper sulphate in sulfuric acid and additives. A copper anode and seed layer on the sample are electrically connected to a current supply and placed inside the solution. When a current is sent through the solution the anode material is oxidised and copper ions Cu^+ are reduced to copper at the sample surface.

4.4.3 Etching

Reactive Ion Beam Etching

Besides the discussed lift-off techniques, dry and wet etches are used to transfer structures of a photoresist onto dielectric, semiconductor or metal layers or substrates. If an anisotropic etch profile is required a dry etch is preferred. For isotropic etches, removals of sacrificial layers or cleaning substrates, wet etches are more suitable. Sacrificial layers can be used as support during fabrication of free standing structures.

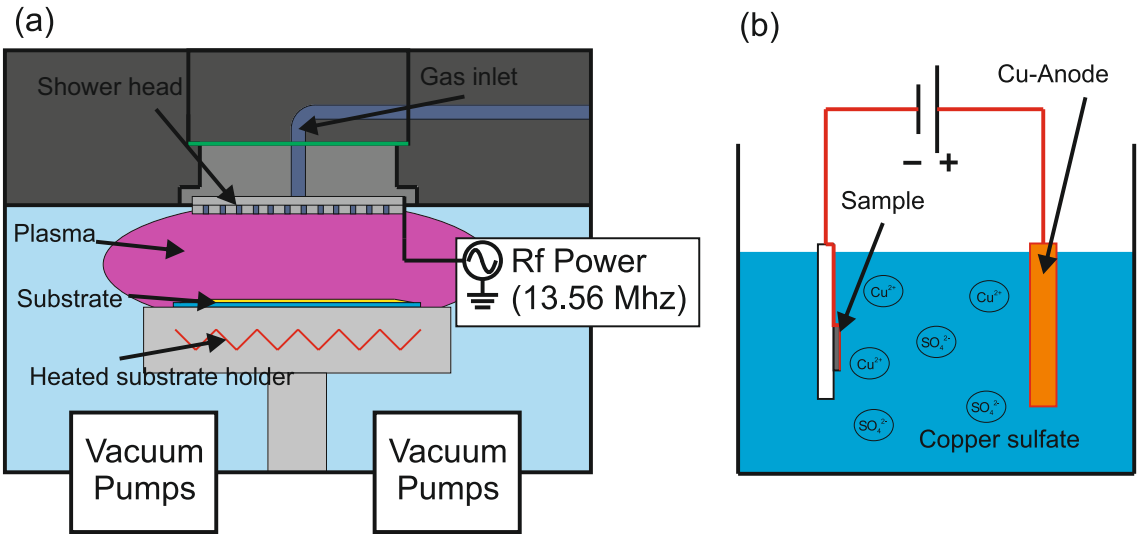


Figure 4.8: (a) PECVD reactor chamber with electrically grounded and heated substrate holder. Gas is led into the chamber via a shower head, and an rf potential between shower head and chamber excites the plasma. Schematic (b) shows a simple copper electroplating setup, with copper anode, and the substrate holder and sample connected to the negative output of a current source.

Dry etching is based on chemical reactions between targeted layers and gas plasma etchants with added physical sputtering and is known as reactive ion beam etching (RIE). Depending on the target material different gases are used - as an example diamond can be etched using an oxygen plasma, for SiO_2 a C_4F_8 and O_2 mixture can be used. All dry etch reactions have volatile end products that are transported away by the vacuum. In a simple RIE tool, see Fig. 4.9 (a), the plasma is excited using a standard capacitive coupled 13.56 MHz rf generator similar to a PECVD reactor but operated at lower pressures (∼20 mTorr) and higher power (∼1000 W). The combination of sputtering through accelerated ions and chemical etching creates much more anisotropic etch profiles than wet etching.

Deep Reactive-Ion Etching

If almost perfectly anisotropic profiles are required, deep reactive-ion etching (DRIE) techniques can be used. The most common method is based on the Bosch process[5]. This process makes use of two process cycles, which are alternated every few seconds. During the first cycle the intended material is etched using a standard RIE process, then during the second cycle a passivation layer that protects the target material from the chemical etch of the first cycle is deposited. The physical sputtering of the RIE etch is highly anisotropic and only breaks the passivation at the bottom of trenches. The etch continues

[5]named after the company (Robert Bosch GmbH) where the process was invented

there, while the sidewalls are still protected by the passivation layer.

Inductively Coupled Plasma Etching

To increase the anisotropy of the etch without relying on the Bosch process, a high energetic and very dense plasma can be used. Instead of capacitively coupling the rf power into the plasma, an rf generator is connected to a coil, which causes an alternating magnetic field inside the chamber. The alternating magnetic field ionizes the gas and creates the plasma. Inductive coupling of the rf power into the gas produces a very dense plasma and additionally makes it possible to apply an additional rf electric field to accelerate the plasma onto the substrate surface. A schematic of the chamber is shown in Fig. 4.9 (b). This so-called ICP etch allows for better control of the plasma and higher etch rates. The ratio between sputtering and chemical etching can be exactly adjusted by varying the strength of the applied rf electric field and a gas that forms a passivating layer on the sample surface can be permanently added to the etch mixture while avoiding low etch rates.

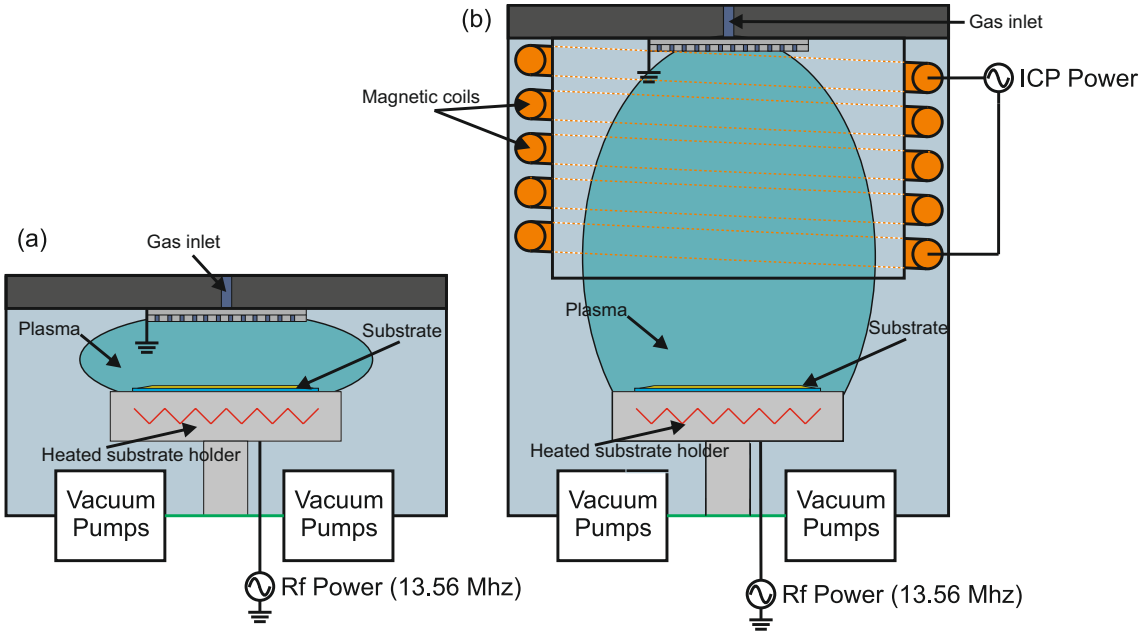


Figure 4.9: (a) Schematic showing a RIE chamber, gas is led into the system via a shower head similar to a PECVD reactor. The substrate holder is not isolated from the chamber and a high power rf generated is connected to the table and used to ionize the gas and accelerate it onto the substrate. The ICP tool, shown in (b), makes use of an inductively coupled rf generator to create a highly dense plasma. The plasma is accelerated onto the substrate using a second capacitively coupled generator.

Wet Etching

Wet etches are based on chemical reactions between target materials and strong acids or bases. The etches are usually highly material selective and can be used to completely remove sacrificial layers and also to remove organic contaminates on substrates. Hydrofluoric acid (HF), for example, strongly etches SiO_2 but doesn't attack silicon or gold. Elevated temperatures can increase etch rates and are used to adjust the etch parameters. Highly concentrated nitric acid (HNO_3, concentration $> 90\%$) oxidizes and removes most organic contaminants without attacking Si, Al, Au and many other substrate materials. The etch profile of a standard isotropic wet etch is shown in Fig. 4.10 (a).

Some material and wet etchant combinations also show a preference of certain crystal axes during the etch. Potassium hydroxide (KOH) etches preferably along the $\langle 100 \rangle$ crystal axis compared to the $\langle 111 \rangle$ axis. The resulting etch profile, see Fig. 4.9 (b), will be aligned with the $\langle 111 \rangle$ planes.

Removing SiO_2 sacrificial layers deeply buried underneath the supported structures can be a challenging and slow process. A vapour of highly concentrated HF acid ($\sim$48%) is suitable for very large undercuts as illustrate in Fig. 4.10 (c), [102] and etches SiO_2 at high speed. This technique was used to fabricate ion traps with 2.4 μm thick aluminium electrodes overhanging the supporting dielectric by 5 μm [167].

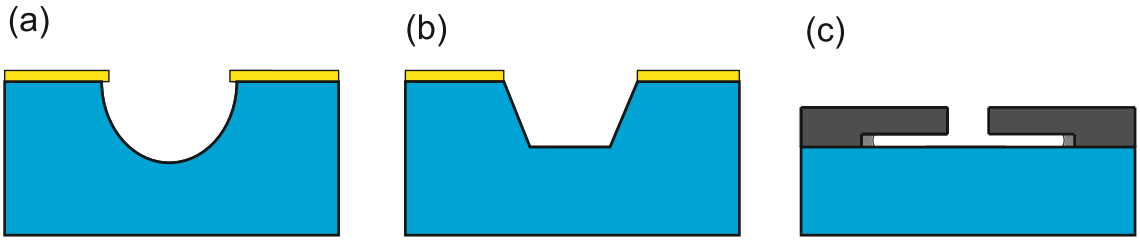


Figure 4.10: Schematic showing different wet etch profiles, including an isotropic etch (a), anisotropic wet etch along crystal axis (b) and a highly material selective sacrificial layer etch (c).

4.5 Fabrication Processes

Based on the outlined fabrication techniques and characteristics of microfabricated ion traps, successfully used fabrication processes are discussed. Based on examples, structural characteristics and limitations of processes are explained and solutions presented. As the exact fabrication steps depend on materials used and available equipment, the process

sequences are discussed as general as possible. However, to give a guideline of possible choices, material and process step details of published ion traps are given in brackets. The discussion will start with a simple process that can be performed in a wide variety of laboratories and is also offered by many commercial suppliers.

4.5.1 Printed Circuit Board (PCB)

The first discussed fabrication technique used for ion trap microfabrication is the widely available Printed Circuit Boards (PCB) process. This technology is commonly used to create electrical circuits for a wide variety of devices and does not require cleanroom technology. For ion traps generally a monolithic single or two layer PCB process is used. Monolithic processes rely on the fabrication of ion trap structures by adding to or subtracting material from one component. In contrast to this, wafer bonding, mechanical mounting or other assembly techniques are used to fabricate traps from pre-structured, potentially monolithic parts in a non-monolithic process. When combined with cleanroom fabrication such a process can be used for very precise and large scale structures, however, mechanical alignment remains an issue.

PCB processes commonly allow for minimal structure sizes of approximately 100 μm [191] and slots milled into the substrate of 500 μm width. This limits the uses of this technique for large and complex designs but also results in a less complex and more easily accessible process. The following section will give a general introduction into the PCB processes used to manufacture ion traps.

This process is based on removing material instead of depositing materials as used in most cleanroom processes. Therefore the actual process sequence starts by selecting a suitable metal coated PCB substrate. The substrate has to exhibit the characteristics needed for ion trapping; ultra high vacuum (UHV) compatibility, low rf loss tangent and high breakdown voltage (commercially available high-frequency (hf) Rogers 4350B used in ref. [191]). One side of the PCB substrates is generally pre-coated with a copper layer by the manufacturer, which is partially removed in the process to form the trap structures as shown in Fig. 4.11 (c). Possible techniques to do this are mechanical milling shown in Fig. 4.11 (b) or chemically wet etching using a patterned mask. The mask can either be printed directly onto the copper layer or photolithography can be used to pattern photoresist as shown in Fig. 4.11 (a). To reduce exposed dielectrics and prevent shorting from material deposited in the trapping process, slots can be milled into the substrate underneath the

trapping zones as shown in Fig. 4.11 (d).

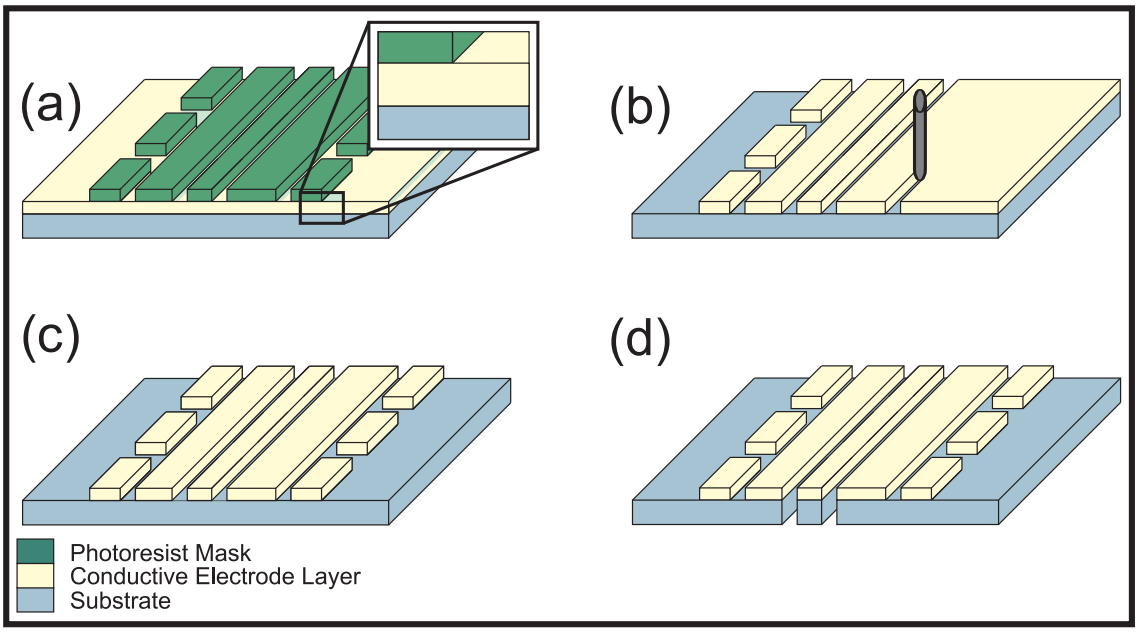


Figure 4.11: Overview of several PCB fabrication processes. (a) Deposition and exposure of the resist used as a mask in later etch steps. (b) Removal of the top copper layer using mechanical milling. (c) Removal of the copper layer using a chemical wet etch and later removal of the deposited mask. (d) Mechanical removal of the substrate underneath the trapping zone [192].

The fabricated electrodes form one plane and make the process unusable for symmetric ion traps (SIT). Not only are the electrodes located in one plane they also sit directly on the substrate, which makes a low rf loss tangent substrate necessary to minimize energy dissipation from the rf rails into the substrate. As explained in Section 4.2 high power dissipation leads to an increase of the temperature of the ion trap structure and also reduces the quality factor of the loaded resonator. PCB substrates intended for hf devices generally exhibit a low rf loss tangent (values of $\tan\delta = 0.0031$ are typical [193]), and if UHV compatible can be used for ion traps. Other factors reducing the quality factor are the resistances and capacitances of the electrodes. When slots are milled into the substrate exposed dielectrics underneath the ion can be avoided despite the electrode structures being formed directly on the substrate. The otherwise exposed dielectrics would lead to charge built up underneath the ion, resulting in stray fields pushing the ion away from the rf nil and leading to micromotion. By relying on widely available fabrication equipment, this technique has enabled the realization of several ion trap designs with micrometer-scale structures, published in [168,191,192,194,195], without the need for cleanroom techniques.

Single layer PCB processes can be used for electrode geometries including y-junctions and linear sections. More complex topologies with isolated electrodes and buried wires require

a more complex two-layer process. To address the limitations caused by the minimum structure separations and sizes allowing for ion traps with higher electrode and trapping-zone densities a process based on common cleanroom technology is discussed next.

4.5.2 Conductive Structures on Substrate (CSS)

Common cleanroom fabrication techniques like high resolution photolithography, isotropic and anisotropic etching, deposition, electroplating and epitaxial growth allow a very precise fabrication of large scale structures. The monolithic technique we discuss here is based on a "conductive structures on substrate" process and was used to fabricate the first microfabricated asymmetric ion trap (AIT) [77]. Electrode structures separated by only 5 μm [100] can be achieved with this process and smaller structures are not limited by the process but flashover and bulk breakdown voltage of the used materials. The structures are formed by means of deposition and electroplating of conductive material onto a substrate instead of removing precoated material. This makes it possible to use a much wider variety of materials in a low number of process steps. Several variations or additions were published [77, 119, 175, 196, 197] to adjust the process for optimal results with desired materials and structures.

First the standard process is presented, which starts by coating the entire substrate (for example polished fused quartz as used in [77]) with a metal layer (0.1 μm copper) that functions as a seed layer, necessary for a following electroplating step. Commonly an adhesion layer (0.03 μm titanium) is evaporated first, as most seed layer materials [77, 119] have a low adhesion on common substrates, see Fig. 4.12 (a). Then a patterned mask (photolithographic structured photoresist) with a negative of the electrode structures is formed on the seed layer. The structures are then formed by electroplating (6 μm gold) metal onto the seed layer, see Fig. 4.12 (b). Afterwards the patterned mask is no longer needed and is removed. The seed layer, providing electrical contact between the structures during electroplating, also needs to be removed to allow trapping operations. This can be done using the electroplated electrodes as a mask and an isotropic chemical wet etch process to remove the material, see Fig. 4.12 (c). Then the adhesion layer is removed in a similar etch process (for example using hydrofluoric acid) and the completed trapping structure is shown in Fig. 4.12 (d).

Depending on the available equipment additional or different steps can be performed, which also allow special features to be included on the chip. One variation was published

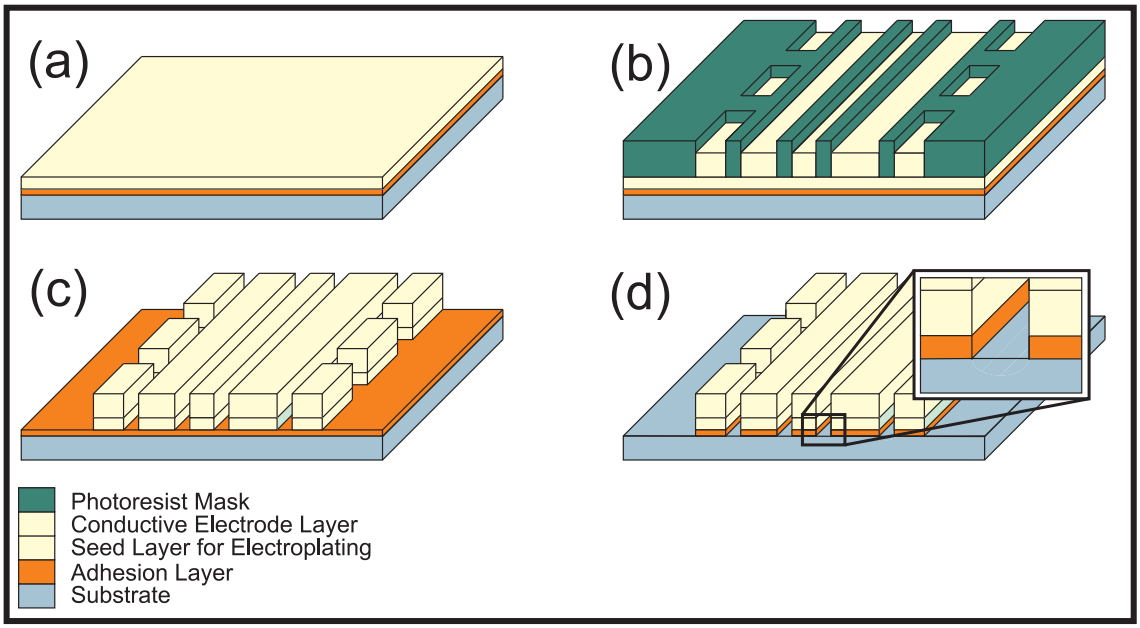


Figure 4.12: Fabrication sequence of the standard "Conductive Structures on Substrate" process. (a) The sequence starts with the deposition of an adhesion and seed layer. (b) An electroplating step creating the electrodes using a patterned mask. (c) Removal of the mask followed by a first etch step removing the seed layer. d) Second etch step removing the adhesion layer.

in [119] replacing the seed layer with a thicker metal layer (1 μm silver used in [119]) and forming the patterned mask on top of that, as shown in Fig. 4.13 (a). The electrode structures are then formed by using this mask to wet etch through the thick silver layer (NH3OH: H2O2 silver etch) and the adhesion layer (hydrofluoric acid) Fig. 4.13 (b). To counter potentially sharp electrode edges resulting from the wet etch process an annealing step (720°C to 760°C for 1 h) was performed to reflux the material and flatten the sharp edges. An ion trap with superconductive electrodes was fabricated using a similar process [175]. Low temperature superconductors Nb and NbN were grown onto the substrate in a sputtering step. Then the electrodes were defined using a mask and an anisotropic etch step. An annealing step was not performed after this etch step. With this variation of the standard process electroplating equipment and compatible materials are not required to fabricate an ion trap.

A possible addition to the process was presented in [77], incorporating on-chip meander line resistors onto the trap as part of the static voltage electrode filters. Bringing filters closer to the electrodes can reduce the noise induced in connecting wires as the filters are typically located outside the vacuum system or on the chip carrier. On-chip integration of trap features is essential for the future development of very large scale ion trap arrays with controls for thousands of electrodes needed for quantum computing.

In order to allow for appropriate resistance values for the resistors, processing of the chip occurs in two stages. Within the first stage only the electrode geometry is patterned with regions where resistors are to be fabricated entirely coated in photoresist. This step consists of patterning photoresist on the substrate (for example polished fused quartz [77]) to shape the electrodes followed by the deposition of the standard adhesion (0.030 μm titanium) and seed layers (0.100 μm copper) on the substrate (thicknesses stated correspond to the values used by Seidelin et al. [77]). After the electrodes have been patterned, the first mask is removed. In the next step, only the on-chip resistors are patterned allowing for different thickness of conducting layers used for resistors. A second mask is patterned on the substrate parts reserved for the on-chip resistors. Then an adhesion layer (0.013 μm titanium) and metal layer (0.030 μm gold) is deposited forming the meander lines as shown in Fig. 4.13 (c). The mask is removed and the rest of the sequence follows the standard process steps. This process illustrates one example of on-chip features integrated into an ion trap. Another process was published in [196], which integrates on chip magnetic field coils to generate a magnetic field gradient at the trapping zone. It was fabricated using the standard process and a specific mask to form the electrodes incorporating the coils.

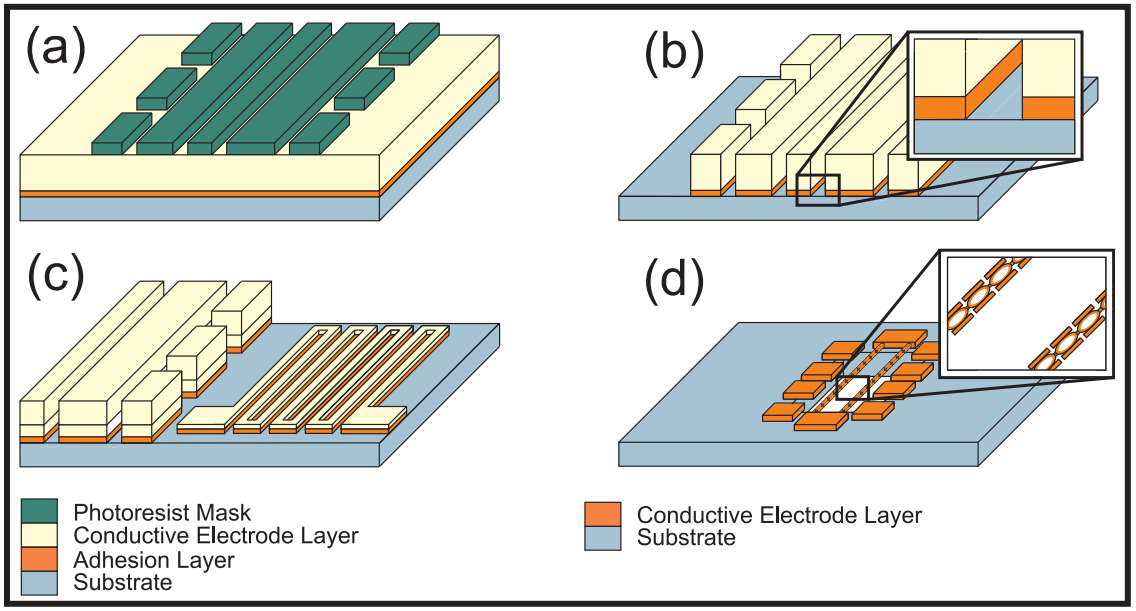


Figure 4.13: Different variations of the standard CSS process are shown. (a) Conductive material is deposited on the entire substrate and a resist mask is structured. (b) Structured electrodes after the etch step. (c) On chip resistor meander line, reported in ref. [77]. (d) Variation without exposed dielectrics underneath the trapping zone with free hanging rf rails [197] .

Most published variations [77, 100, 119, 120, 175, 196–198] of this process feature structure sizes much smaller than achievable with the PCB process, but similar to the PCB, elec-

trodes sit directly on the substrate resulting in the same rf loss tangent requirements. It also makes the process incompatible with symmetric ion traps. As a result of the smaller structure separations, high flash over and bulk breakdown voltages also become more important. Because no slots are milled into the substrate electric charges can accumulate on the dielectrics beneath the trapping zones, which can result in stray fields and additional micromotion. To reduce this effect a high aspect ratio of electrode height to electrode-electrode distance is desirable.

Similar to the one-layer PCB process, topologies including junctions are possible but isolated electrodes are prohibited by the lack of buried wires. By moving towards cleanroom fabrication techniques it is possible with this process to reduce the electrode-electrode distance and increase the trapping zone density. Scalability is still limited and the exposed dielectrics can lead to unwanted stray fields. To counter the exposed dielectrics another variation and a different process featuring "patterned silicon on insulator (SOI) layers" can be used and is explained in Section 4.5.3.

One variation of this process that prevents exposed dielectrics was fabricated by Sandia National Laboratory [197] featuring free standing rf rails with a large section of the substrate underneath the trapping region being removed. Electrodes consist of free standing wires held in place by anchor-like structures fabricated on the ends of the slot in the substrate, as shown in Fig. 4.13 (d). To prevent snapping under stress the wires are made from connected circles increasing the flexibility. While no dielectrics are exposed underneath the designs, scalability and compatibility with different electrode geometries is limited as the rf rails are suspended between the anchors in a straight line.

4.5.3 Patterned Silicon on Insulator Layers (SOI)

The "Patterned Silicon on Insulator Layers" process makes use of commercially available silicon-on-insulator (SOI) substrates and was first reported by Britton et al. [188]. Similarly to the PCB process this technique removes parts of a substrate instead of adding material to form the ion trap structures. Using the selective etch characteristics of the oxide layer between the two conductive silicon layers of the substrate, it is also possible to create an undercut of the dielectric to shield the ion from it, without introducing extra process steps. A metal deposition step performed at the end of the process to lower the electrode resistance does not require an additional mask, keeping the number of process steps low. Therefore this process allows for much more advanced trap structures without

increasing the number of process steps by making clever use of a substrate.

The substrates are available with insulator thicknesses of up to 10 μm and different Si doping grades resulting in different resistances. After a substrate with desired characteristics (100 μm Si, 3 μm SiO_2, 540 μm Si in ref. [188]) is found, the process sequence starts with photolithographic patterning of a mask on the top SOI silicon layer as shown in Fig. 4.14 (a). The mask is used to etch through the top Si layer, see Fig. 4.14 (b) by means of an anisotropic process (Deep Reactive Ion Etching (DRIE)). Using a wet etch process, the exposed SiO_2 layer parts are removed and an undercut is formed to further reduce exposed dielectrics as shown in Fig. 4.14 (c). If the doping grade of the top Si layer is high enough the created structure can already be used to trap ions.

To reduce the resistance of the trap electrodes resulting from the use of bare Si, a deposition step can be used to apply an additional metal coating onto the electrodes. No mask is required for this deposition step, the adhesion layer (Chromium or Titanium) and metal layer (1 μm Gold, in [188]) can be deposited directly onto the silicon structures as shown in Fig. 4.14 (d). This way the electrodes and the exposed parts of the second Si layer are coated. This has the benefit that possible oxidization of the lower silicon layer is also avoided. A slot can be fabricated into the substrate underneath the trapping zone, which allows backside loading in these traps [188]. This slot is microfabricated by means of anisotropic etching using a patterned mask from the backside. The benefit of such a slot is that the atom flux needed to ionize atoms in the trapping region can be created at the backside and guided perpendicular to the trap surface away from the electrodes. Therefore coating of the electrodes as a result of the atom flux can be minimized.

An ion trap based on the SOI process was fabricated with shielded dielectrics by Britton et al. [188]. A similar approach is used by Sterling et al. [102] to create 2-D ion trap arrays. Similar to the standard CSS process, discussed in the previous section, y-junctions and other complex topologies are possible, but buried wires are prohibited. The process design incorporates a limited material choice for substrate and insulator layer. Only the doping grade of the upper and lower conductive layers can be varied not the material. The insulator layer separating the Si layers must be compatible with the SOI fabrication technique and commercially available materials are SiO_2 and Al_2O_3 (Sapphire). Adjustments of electrical characteristics, like rf loss tangent and electrode capacitances are therefore limited to the two insulator materials and geometrical variations.

To further increase the scalability and trapping zone density of ion traps, process tech-

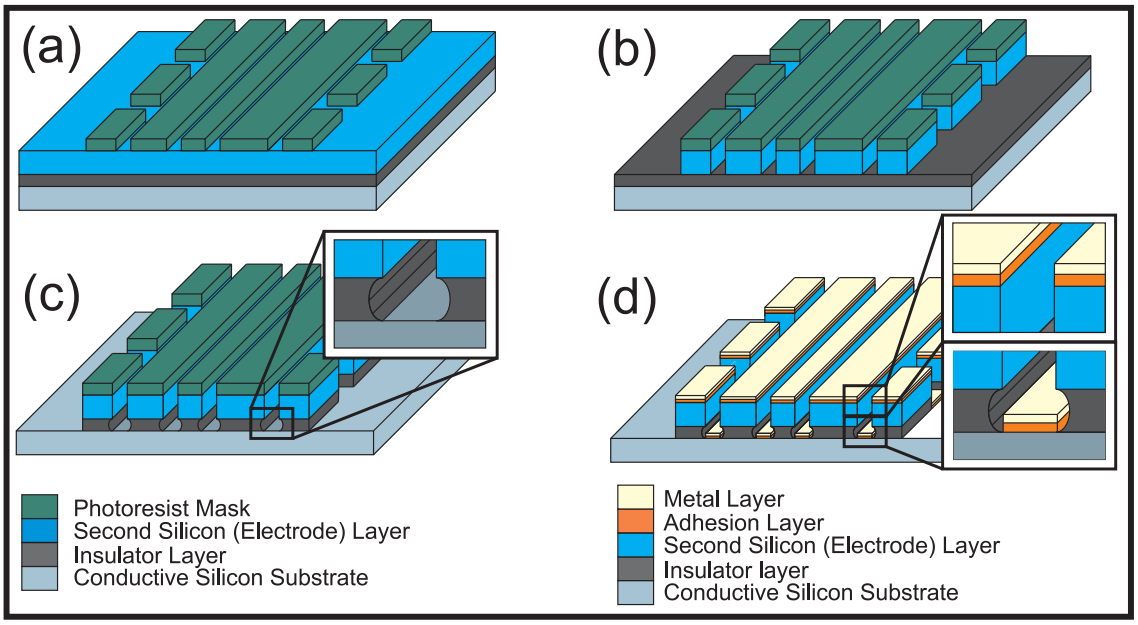


Figure 4.14: Fabrication sequence of the SOI process. (a) Resist mask is directly deposited on the substrate. (b) First silicon layer is etched in an anisotropic step. (c) Isotropic selective wet etch step removing the SiO_2 layer and creating an undercut. (d) Exposed Si layers coated with adhesion and conductive layer to reduce overall resistance.

niques should incorporate buried wires to allow isolated static voltage and rf electrodes. Examples of such monolithic processes are discussed next, first a process incorporating buried wires but exhibiting exposed dielectrics is presented, followed by a process allowing for buried wires and shielding of dielectrics.

4.5.4 Conductive Structures on Insulator with Buried Wires (CSW)

The process to be discussed here is a further development of the CSS process discussed in section 4.5.2, which adds two more layers to incorporate buried wires. With these wires it is possible to connect isolated static voltage and rf electrodes, and this method was used to fabricate an ion trap with six junctions arranged in a hexagonal shape [99], see Fig. 4.15 (a). The capability of buried wires is essential for more complex ion trapping arrays that could be used to trap hundreds or thousands of ions necessary for advanced quantum computing.

The process starts with the deposition of the buried conductor layer (0.300 μm gold layer [99]) sandwiched between two adhesion layers (0.02 μm titanium) on the substrate (380 μm quartz) and a patterned mask is deposited on these layers. Conductor and adhesion layers are then patterned in an isotropic etch step, see Fig. 4.15 (b) and then buried with an insulator material (1 μm SiO_2 deposited by means of chemical vapor

deposition (CVD)). To establish contact between electrodes and the buried conductor, windows are formed in the insulator layer (plasma etching) as shown in Fig. 4.15 (c). Then another patterned mask is used to deposit an adhesion and conductor layer forming the electrodes (0.020 μm titanium and 1 μm gold). In this deposition step the windows in the insulator are also filled and connection between buried conductor and electrodes is established as shown in Fig. 4.15 (d). For this ion trap a backside loading slot was also fabricated using a combination of mechanical drilling and focused ion beam milling to achieve a precise slot in the substrate [99]. As demonstrated by Amini et al. [99] this process allows for large scale ion trap arrays with many electrodes and trapping zones. While the scalability is further increased, this particular process design results in exposed dielectrics. The next process improves this further by shielding the electrodes and the substrate.

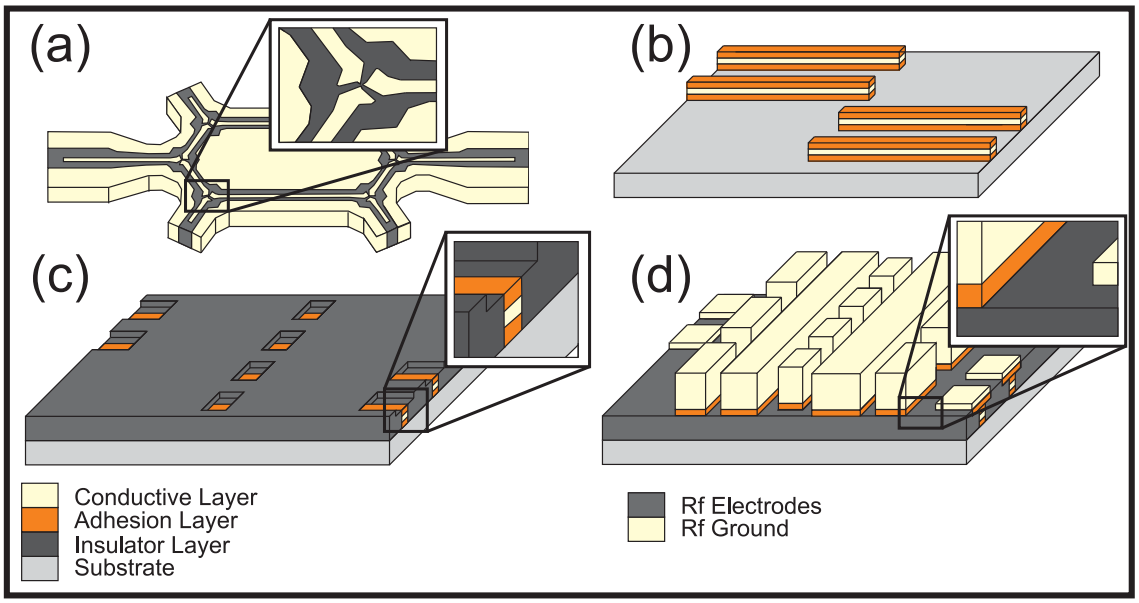


Figure 4.15: Process sequence for the buried wire process. (a) Hexagonal shaped six junction ion trap array [99]. (b) A structured resist mask is deposited and the mask is used to form wires in a following wet etch step. (c) The wires are then buried with an oxide layer and windows are formed in the oxide. (d) With another mask the electrodes are deposited on top of the wires and oxide layer.

4.5.5 Conductive Structures on Insulator with Ground Layer (CSL)

To achieve buried wires or in this case vertical interconnect access (vias) and shielding of dielectrics a monolithic process including a ground layer and overhanging electrodes can be carried out. Several structured and deposited layers are necessary for this process and while providing the greatest flexibility of all processes it also results in a complicated

process sequence. Therefore these processes are commonly performed using Very-Large-Scale Integration (VLSI) facilities that are capable of performing many process steps with high reliability.

A process design, which makes use of vias, was presented by Stick et al. [142]. In this process design the substrate (SOI in ref. [142]) is coated with an insulator and a structured conductive ground layer (1 μm Al) as shown in Fig. 4.16 (a). This is followed by a thick structured insulator (9-14 μm). The trapping electrodes are then placed in a plane above the thick insulator. The electrodes overhang the thick insulator layer and in combination with the conductive ground layer shield the trapping zone from dielectrics. Vias are used to connect static electrodes to the conductive layer beneath the thick insulator as shown in Fig. 4.16 (b). The process also includes creation of a backside loading slot.

A variation from the discussed process making use of a ground plate without vias is described by Leibrandt et al. [199] and more detailed process steps are given in ref. [197].

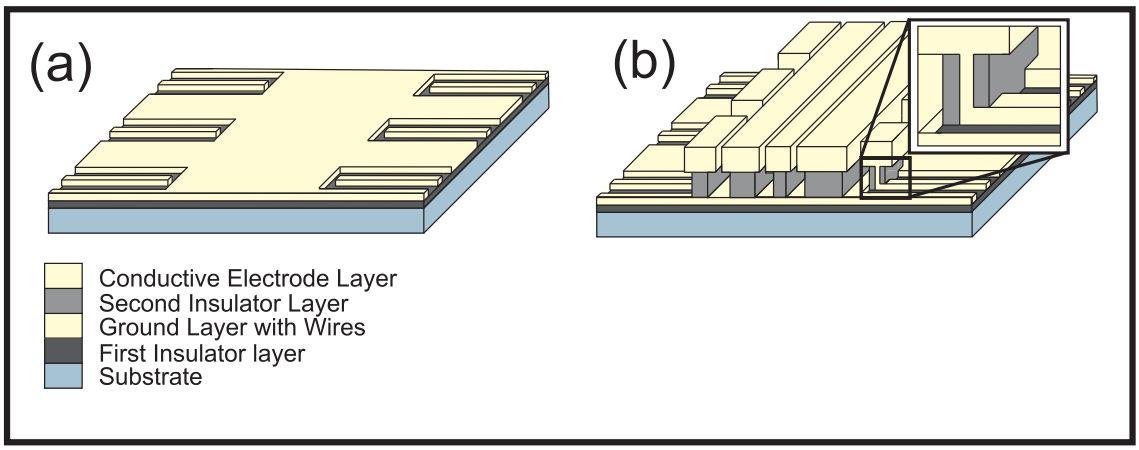


Figure 4.16: Two variations of the CSL process sequence. (a) In the process sequence published in [142] an insulating layer and a structured metal ground layer are deposited on the substrate. (b) Electrodes fabricated in one plane, with outer static voltage electrodes connected through via's [142].

The described process design [142] combines vias with shielded dielectrics and also makes the trap structures independent from the substrate. Therefore the same level of scalability as the CSW process, discussed in the previous section, can be achieved while dielectrics are shielded similar to the SOI process, described in section 4.5.3. The process uses aluminium to form the electrodes which can lead to oxidisation and unwanted charge build up. To avoid this the electrodes could be coated with gold or other non-oxidizing conductors in an additional step. Easier choice of substrate, isolator and electrode materials combined with vias and shielded dielectrics make this process well suited for very large scale asymmetric

ion traps with high trapping zone densities and low stray fields. With electrodes in one plane and another conductive layer above the substrate this structure could also be used to fabricate a symmetric ion traps (SIT).

4.5.6 Optimized Structures for Large Scale Ion Traps with Magnetic Field Gradients(OLM)

Traps fabricated using the CSL process can suffer from large trap capacitances due to the small gap between rf electrode and ground plate. Additionally if large currents should be applied to the trap one has to use a substrate with very high thermal conductivity. A new process was therefore developed by the author based on diamond substrate. The ground layer was removed and incorporated into the buried wire layer, see Fig. 4.17 (a). Ground plates are only placed on top of otherwise exposed dielectrics, reducing the trap capacitance and also the required process steps.

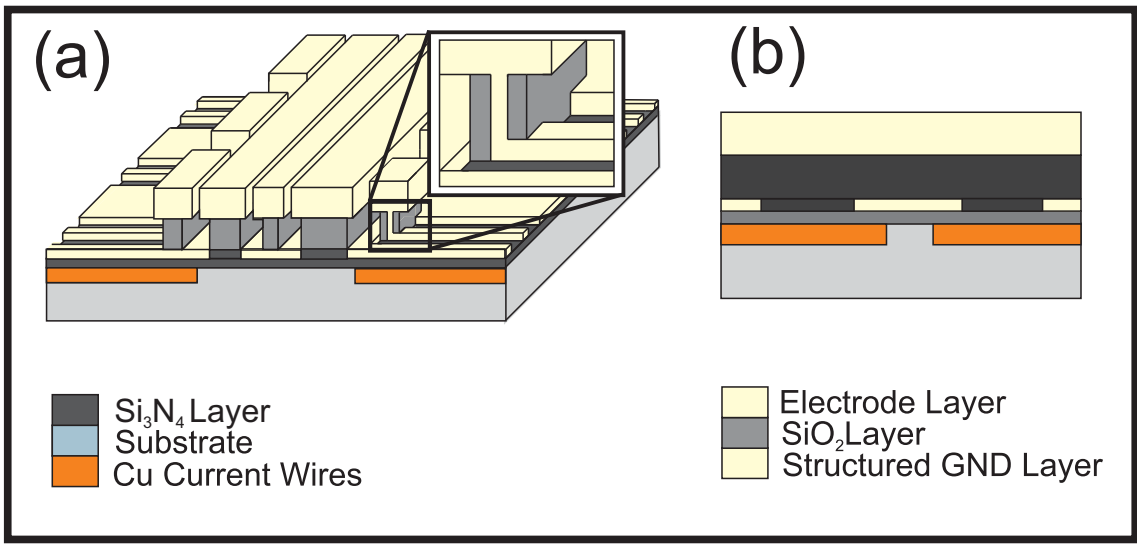


Figure 4.17: The OLM process makes use of the high thermal conductivity of CVD diamond substrate in which current carrying wires are embedded. The actual trap structure (a) features a buried wire/structured ground layer, VIAs and a thick aluminium/titanium/gold electrode layer. A layer schematic of the process is shown in (b).

Deep trenches are etched into the diamond substrate ($\sim$30 μm) and filled with copper using a seed layer and electroplating as shown in Fig. 4.17 (a). The surface is polished and any copper on the substrate surface, not inside trenches, is removed. The diamond substrate and copper tracks are then coated with a dielectric Si_3N_4 layer, followed by an aluminium deposition to create the buried wires including structured ground plates. Buried wires and structured grounds are separated form the electrode layer by a $\sim$3 μm

thick dielectric layer (SiO_2). Vertical interconnect access holes are etched into the SiO_2 and filled with aluminium. Lastly a ca. 5 μm thick aluminium/titanium/gold layer is deposited forming the electrodes. The vertical layer structure of the process is shown in Fig. 4.17.

Chapter 5

Concept for Scalable Ion Trap Quantum Computing

Designing and building a large scale ion quantum computer is an extremely challenging task requiring a physically scalable system. Capabilities that are usually achieved in individual systems such as robust, high fidelity state preparation [52] and detection [53–55], fast universal gate operations [45,51,57,58] and long qubit decoherence times [56] have to be combined into one scalable system.

Possible concepts including all necessary capabilities were proposed, ranging from large arrays of memory and entanglement zones [48] to ion-photon entanglement hybrid systems [49]. All of these systems will need to execute a suitable error correction code (ECC) that reduces errors of quantum operations. ECC make it possible to form logical qubits, which are capable of performing $\sim 10^{16}$ error protected quantum operations, enough for any quantum algorithm or simulation proposed so far [85].

ECC will impose requirements on the physical qubit systems and more importantly require certain qubit interaction capabilities. Some codes are based on interactions between completely arbitrary qubits in a vast system, illustrated in Fig. 5.1 (a) others on interactions only between nearest neighbours in a two-dimensional grid, see Fig. 5.1 (b) or one dimensional alignment, shown in Fig. 5.1 (c). Depending on which error correction scheme is used, the physical architectures will be completely different.

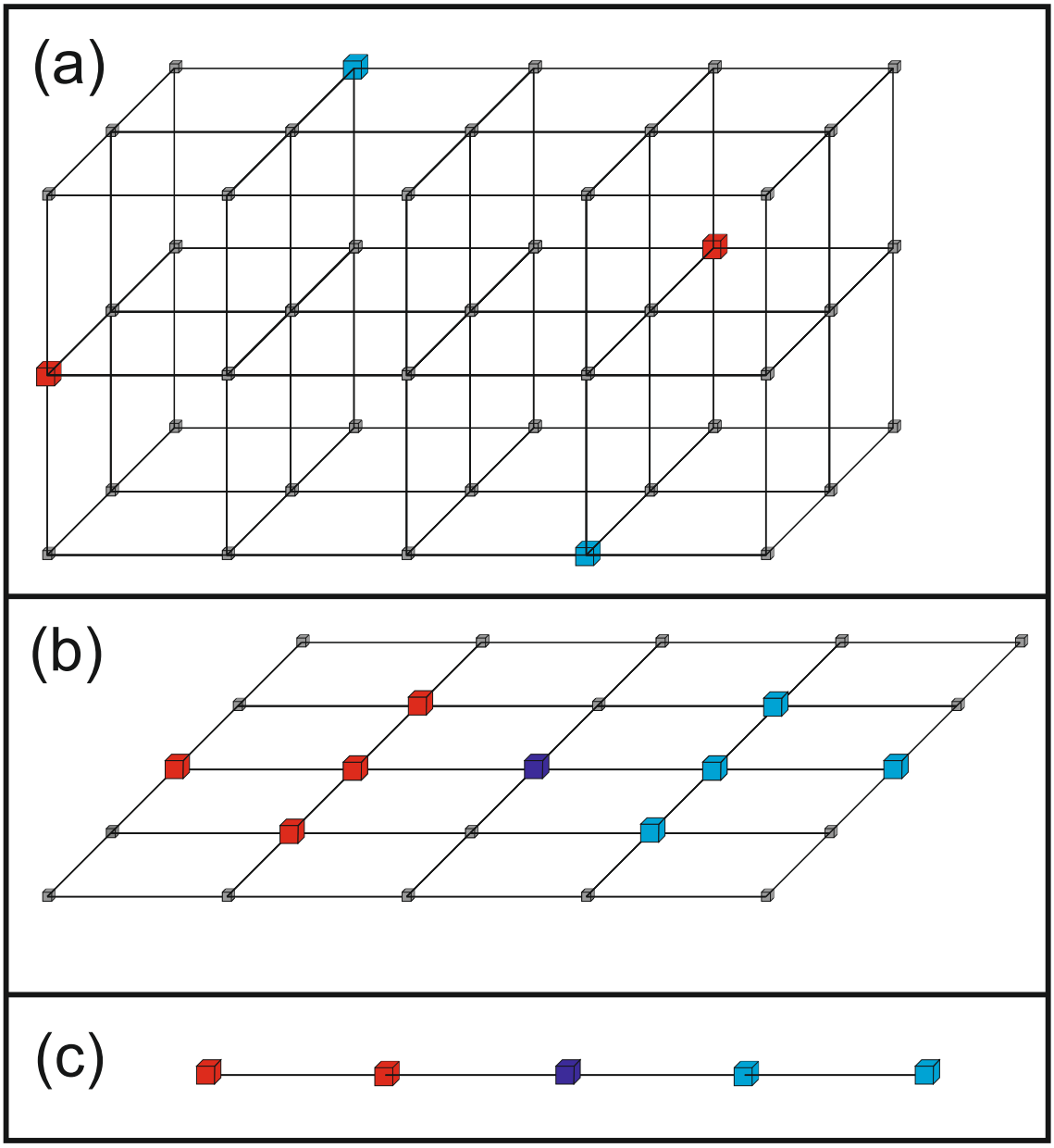


Figure 5.1: Schematic showing the required interactions for different error correction codes, large cubes of the same colour represent qubits that will interact with each other. (a) completely arbitrary interactions in a vast array, (b) nearest neighbour interactions in a 2D grid and (c) in a string of ions.

5.1 Error Correction Scheme

For any correction scheme to work, the physical qubit operations will require a certain fidelity. If the error rates of the operations are above a certain threshold, the correction scheme will fail.

One scheme requiring interactions between any arbitrary qubits, known as Knill's post-selection scheme, has the highest error threshold of over 3% [61]. Realizing an ion trap architecture that allows for interactions between completely arbitrary qubits requires either qubit interfaces based on optical fibres and cavities or unreasonable amounts of shuttling operations. Optical interactions between ion qubits are currently limited to very low success probabilities of $\sim 8.5 \times 10^{-8}$ [29]. Achieving very high probability rates requires almost perfect detection rates, optical switches and fibres with close to 100% transmission rates. A system based on elementary logic units connected via optical links is discussed in [49].

ECC making only use of interactions between nearest neighbours in a two-dimensional array tolerate qubit operation errors of up to 1% [62]. Allowing nearest neighbour interactions only in a string of ions dramatically lowers the error threshold to 0.001% [200] and will not be considered further here. The two-dimensional array ECC [62] is a surface error correction code, which is considered among the most suitable for nearest neighbour interactions in 2D arrays [201]. Other famous error correction codes [35], like the Steane [63] or Bacon-Shor [64] code have significantly lower error thresholds, currently out of reach of ion quantum systems.

Exact working principles of the error correction code used will not have a determining impact on the general concept of the scalable system as long as only nearest neighbour interactions and two-qubit gates are required. The proposed system can therefore also be used for other correction schemes based on these requirements.

5.2 Scalable Ion Trap Architecture and Entanglement Schemes

When creating a scalable 2D trap architecture, capable of executing surface error correction codes, one can make use of the vast amount of work performed by the ion trapping community. Ion trap experiments have reached entanglement gate fidelities of 99.3(1)% [60] and single qubit rotations [202, 203], addressing and readout [55] well below the 1% error

threshold. Scalable microfabricated ion traps were developed, fabricated and successfully tested [75–77] and adiabatic shuttling through junctions has been demonstrated [81].

Basing the architecture only on nearest neighbour interactions in a 2D array suggests using microfabricated asymmetric X-junction traps with entanglement zones. In each junction one ion will be trapped, laser cooled and shuttled to one of the four arms of the junction to be entangled with a nearest neighbour ion. All of these operations can be performed on the time scale of 10s of μs. Each junction will also need the capability to read out the qubit state of the ion with high fidelity. An illustration showing a potential architecture is shown in Fig. 5.2.

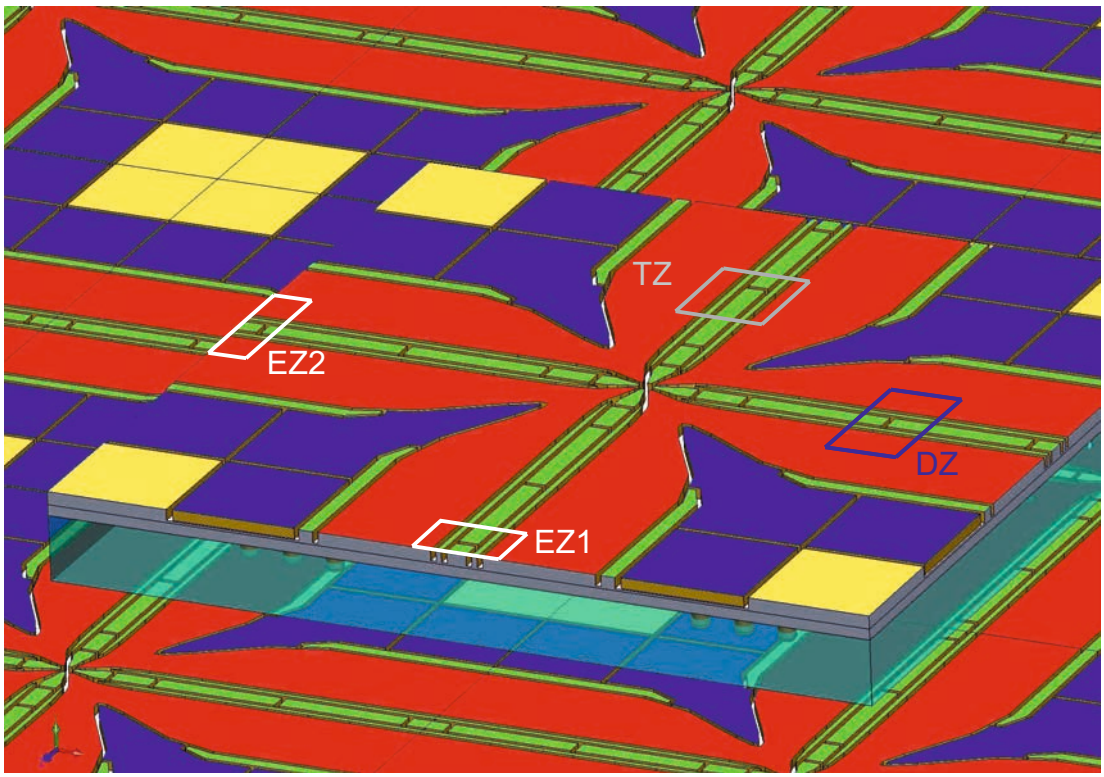


Figure 5.2: Illustration showing an individual junction section as part of a large two-dimensional array, rf electrodes are marked red, centre segmented and principal axes rotation dc electrodes green, outer dc electrodes blue and unsegmented ground sections yellow. Zones for entanglement (EZ1, EZ2), detection (DZ) and trapping (TZ) are highlighted and will be discussed in the following sections.

To extend this structure vastly in both dimensions, connections for electrodes have to be supplied and connected from the back of the trap. Detection devices and laser beams or current wires for entanglement zones need to be incorporate into the structure. All required connections must take up less area then occupied by the X-junction, which would otherwise limit the maximum size of the array. It should only be limited by the maximum

size of the UHV chamber. X-junctions placed close to a wall of the UHV chamber will also be equipped with a loading zone from where trapped ions are shuttled to the other X-junctions. Doppler cooling light sheets will need to be placed above all traps at rf nil height and ionization laser sheets will be placed above junctions with loading zones.

5.3 Junction Design and Fabrication

We start with the X-junction, which is the core structure of the scalable design. When shuttling through the centre of a junction, one has to overcome the unavoidable rf barrier which occurs due to the merging of several linear sections [78–81,97]. To allow for adiabatic shuttling through the junction, electrode geometries have to be optimized for minimal rf barrier height and gradient of the barrier [80]. Additionally several dc electrodes will be necessary for efficient shuttling. We propose to use a design similar to the one shown in Fig. 5.3 (a) with an optimized electrode layout. The electrode structure will be placed on a dielectric substrate and consist of three conductive and two insulating layers, as shown in Fig. 5.3 (b), avoiding exposed dielectrics and incorporating buried wires to contact all electrodes.

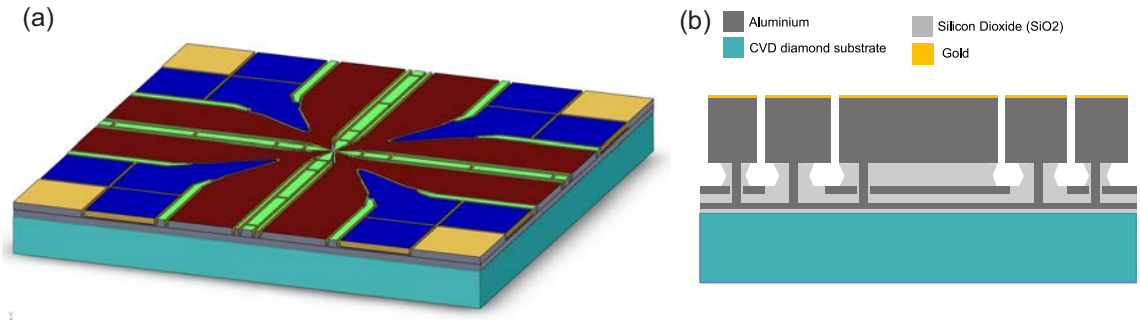


Figure 5.3: (a) shows an optimized junction electrode geometry on top of a diamond substrate (blue) and SiO_2 dielectric layer (grey). (b) shows the layer structure of the trap in more detail.

The junction presented in Fig. 5.3 (a) occupies an area of $\sim 5 \times 5\text{mm}^2$ and features 36 static voltage (dc) electrodes. As mentioned before connections to rf and dc electrodes have to be made from the back of the substrate, which can be achieved by etching holes with a diameter of ~ 100 μm through the entire substrate and filling them with a metal layer, as shown in Fig. 5.4 (a). Such structures are commonly referred to as a through-wafer vertical interconnects (TWVI). The 36 dc electrodes will be connected to the TWVI using buried wires and vertical interconnect accesses (VIAs) of the trap structure shown

in Fig. 5.3 (b). If too many junction sections are electrically connected, the rf electrode capacitance becomes so large that Q factor of the resonator will be drastically reduced or the resonator becomes extremely large. To keep the total rf electrode capacitance below 25 pF, a maximum of 6×6 junctions are connected together to form one section and driven by an in-vacuum discrete component resonant circuit similar to the one described in [204]. Using ultra low loss ferrite cores [1] a quality factors of > 100 should be achievable without cooling to cryogenic cooling.

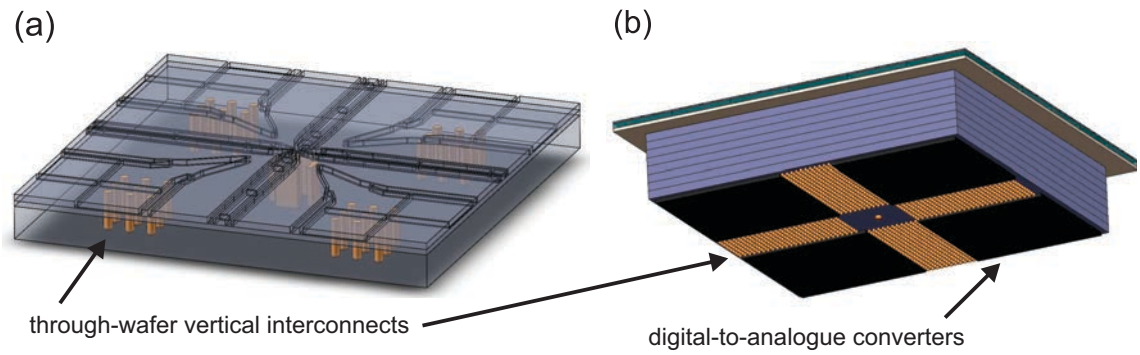


Figure 5.4: (a) illustrates through-wafer vertical interconnects for rf and dc electrodes. Buried wires are used to route the VIAs of individual electrodes to the through-wafer vertical interconnects. Rf interconnects also include 4 rf ground shields. A backside view of an array of 6x6 junctions including wafer-stacked DACs and a Si distribution wafer is shown in (b).

Several sections consisting of 36 junctions can be fabricated on one substrate as long as no electrical connection between rf electrodes of different sections is made. With standard 4" wafer technology a total of 144 junctions on an area of 60×60 mm^2 could be microfabricated. The 144 junctions require $>$ 5000 dc and 9 rf connections on an area of 60×60 mm^2. We propose to wafer bond the substrate on a silicon wafer where connections are rerouted and rc filters are incorporated based on deep trench capacitors [206] and on chip resistors [77]. The dc electrodes are controlled via on chip digital-to-analogue converters (DACs) with 40 outputs occupying an area of $\sim 6 \times 6$ mm^2 each. Four DACs can be placed on an area of 20×20 mm^2 as shown in Fig. 5.5, occupied by 36 junctions, including the routing of connections using TWVI. To reach the amount of outputs required for 36 junctions on an area of 20×20 mm^2, 8 layers with 4 DACs on each are physically and electrically connected together, commonly known as wafer-stacking [207]. Wafer-stacking has not been used for this specific application before, but has already reached commercial mass production[2] and with some development time the design should be realizable.

[1] Yttrium iron garnet ferrites [205]

[2] Samsung Starts Mass Producing Industrys First 3D Vertical NAND Flash; Seoul, Korea on Aug. 6. 2013

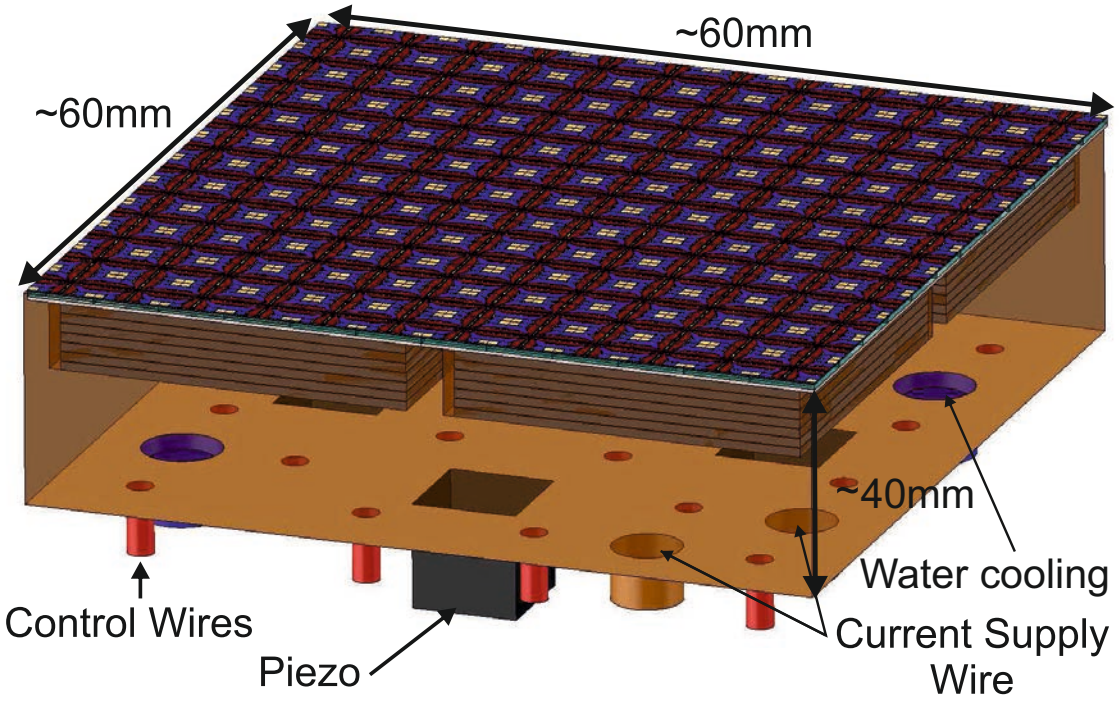


Figure 5.5: A large 12x12 array of junction sections including wafer stacked DACs is shown, embedded in a copper heat management socket. X-Y-Z piezo actuators are marked black, connection wires in red and tubing for the cooling blue.

Four sections with $4 \times 4 \times 8$ DACs are embedded in $\sim$ 30 mm thick copper heat sinks, which transport the heat created by DACs and entanglement regions out of the system. Additionally the 60×60 mm^2 parts need to be mechanically aligned with a precision on the order of ± 5 μm, so that ions can be shuttled from one part to another without encountering a large rf barrier. To achieve that, X-Y-Z piezo actuators [3] are mounted to the bottom of each 60×60 mm^2 part and supported by a stainless steel frame attached to the vacuum system. Individual parts are accurately aligned to each other using microscopes and laser measurement systems. The rf resonators required for each 60×60 mm^2 section are attached to the same steel frame beneath the piezos.

5.4 Entanglement Zone

To perform gates with the highest fidelity [60] or speed [174] two laser beams need to be guided to the trapped ions at a certain angle making optical fibre access essential. Besides requiring two large optical fibres per entanglement zones which also have to be inserted at an angle, laser setups used for optical entanglement are very complex and costly. Faultless operation of large numbers of these laser system will be extremely challenging.

[3] for example piezo actuator P-153.10 from Physik Instrumente (PI)

Recently developed schemes [82, 83] are based on magnetic field gradients and microwave radiation, see section 2.3.3. Although these gates have not yet achieved the high fidelities required for the surface error correction code to work, they hold tremendous potential for scalable systems.

Microwave gates based on static magnetic field gradients can be realized using a combination of current carrying wires or permanent magnets embedded in the trap structure shown in Fig. 5.6 and microwave horns driving necessary qubit transition for many ions in parallel. Large static magnetic field gradients (>100 T/m) will be generated using current carrying wires embedded in a diamond substrate and passing currents on the order of 10-20 A through them. To avoid melting the structures due to high currents, diamond substrates with extremely high thermal conductivity ($\kappa > 2000\, W/(m \cdot K)$) are used. Wires of all entanglement zones fabricated on the same wafer can be connected together requiring a total of only four connections per 60×60 mm chip.

Required microwave frequencies can be dialed into a frequency generator, mixers modulate all necessary frequencies onto one signal and amplifiers supply the signal with sufficient amplitude to horns for the entire system. No additional stabilization techniques are required, commercially available generators deliver microwave signals sufficiently clean and stable for this purpose. To individually address certain ions each entanglement zone is fitted with additional small coils as shown in Fig. 5.6. These make it possible to measure, stabilize and control the exact B-field at the ion's position and only the desired ions can be brought into resonance with the applied microwaves. The entire entanglement zone is controlled via currents and microwaves instead of laser light. An additional layer of high current DACs supplies currents to the small coils and can be used to electronically control the entire entanglement zone.

Issues arising from using magnetic field sensitive states and fluctuations of the B-field during quantum operations or shuttling can be addressed making use of microwave dressed states [208,209]. Adding two zones per junction reduces shuttling times significantly, while only increasing the requirement on the system minimally. In addition, ions will be shuttled together and separated again, making use of the centre segmented DC electrodes with optimal width and length [103] placed underneath the entanglement zone, see Fig. 5.6.

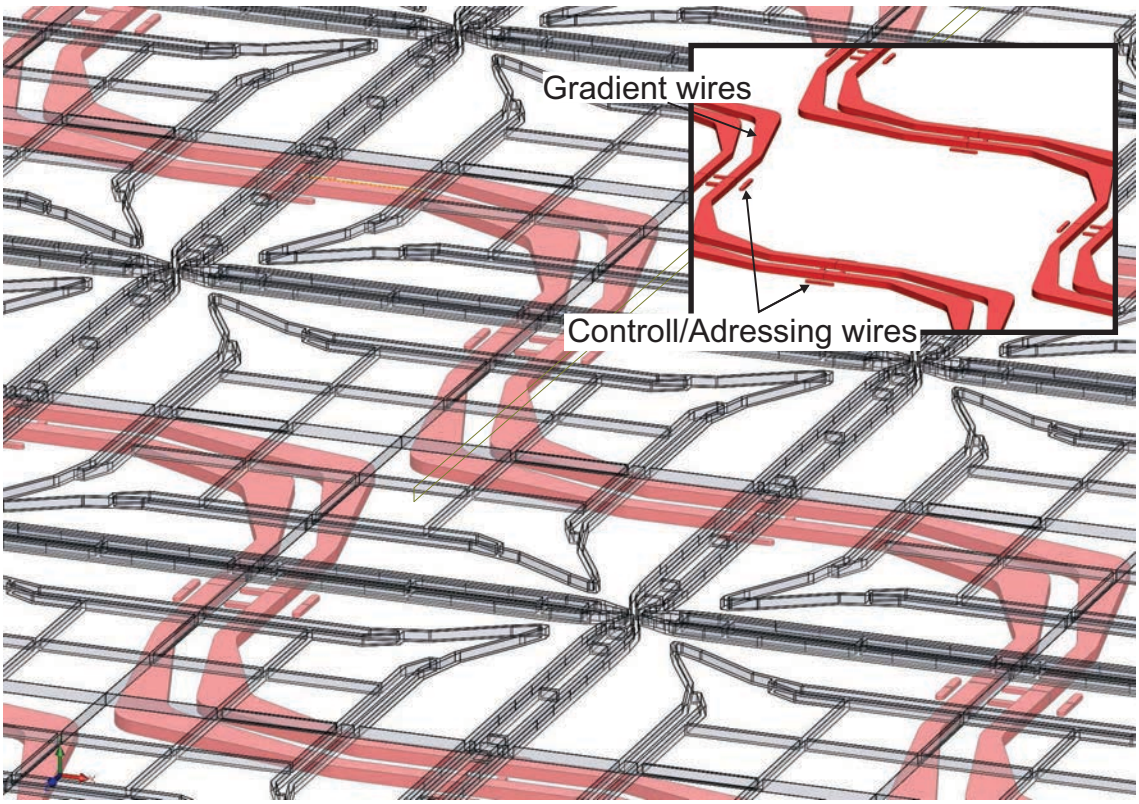


Figure 5.6: Inset shows the current carrying wires separated from the trap structure. Main picture shows an isometric view of the gradient wires placed underneath the trap structure.

5.5 Power Dissipation and Cooling

Current-carrying wires and the DACs will dissipate a substantial amount of heat that needs to be removed from the system. If we assume that ∼13 A of current [4] is passed through the wire structures shown in Fig. 5.6 then the current-carrying wires in each junction section will dissipate ∼ 9 W of heat. On one 60 × 60 mm^2 section the current-carrying wires will dissipate ∼1300 W. The power dissipation of the 128 DACs placed underneath each 60 × 60 mm^2 section is approximately 64 W [5]. The total power dissipation will be ∼0.4 W/mm^2, which is similar to that of a modern computer chip [6].

As the system does not need to be cooled to cryogenic temperatures we propose to incorporate a liquid cooler with microchannels fabricated into the copper heat sink to remove the dissipated heat from the system. Microchannel liquid coolers are commonly used to cool high power electronics and the design presented in [210] achieves a heat transfer coefficient of >0.15 W/(mm^2·K).

[4] resulting in a gradient of ∼100 T/m
[5] DAC of comparable size (AD5370, Analogue Devices)dissipates ∼0.5W
[6] Intel Ivy Bridge E, power dissipation ∼0.5 W/mm^2

Assuming that a microchannel cooler built into the heat sink reaches a heat transfer coefficients of at least 0.1 W/(mm^2·K) we can approximate the temperature of the ion trap chip by calculating the thermal resistance between water which is chilled to (5°C) and the chip. Taking into consideration the thermal resistance of the diamond wafer, silicon based DACs, the silicon distribution board, the 30 mm copper heat sink and a 25 μm thick hard solder attachment, [7] the temperature of the ion trap chip will be $\sim$ 35°C. The water will be supplied via UHV tight flexible steel tubing and will not hinder the alignment capabilities of the 60×60mm^2 sections.

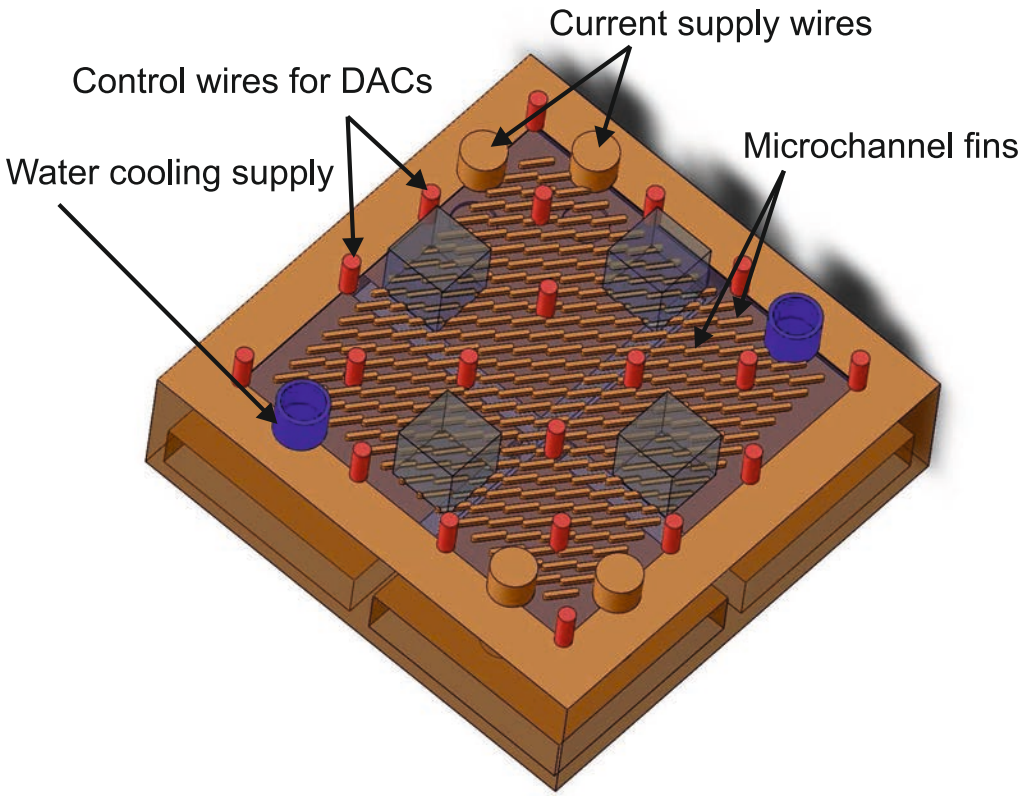


Figure 5.7: Picture of the copper heat sink with microchannel cooler. For illustration purposes the bottom plate of the heat sink is not included.

5.6 State Detection and Loading Zone

After performing ion addressing and one and two qubit gates, the qubit states will also have to be read out. Special detection regions will be placed in one arm of each junction shown in Fig. 5.8 allowing simultaneous detection of all qubit states in the entire system. The proposed diamond substrate is highly UV transparent and allows emitted light to

[7] Gold-tin solder, $T_c \sim 57$ W/(m· K), Indium Corporation

reach the back of the substrate if a gap is fabricated into the dc electrodes underneath the detection zone. Similar to the junction zone, the electrode geometry is optimized for minimal rf barrier height. To avoid exposing dielectrics a thin layer of UV transparent indium tin oxide (ITO) is evaporated onto the dielectric after the electrodes are formed and underlying dielectrics removed.

The detection itself is achieved using ultra-violet (UV) sensitive silicon avalanche diodes fabricated onto the back of the diamond, similar to the devices presented in [211, 212]. Diodes presented in [212] reach single-photon detection efficiencies (SPDE) of 30%, much higher than the PMT [8] described in section 3.2. Detection angles will also be comparable or higher than the imaging system described in section 3.2. Detection efficiency of this system should be comparable or higher than of the one described in section 3.4.

Loading zones, shown in Fig. 5.8, can be placed in the free remaining arm of junctions close to the edge of the two-dimensional array. These are to be used for initial loading of the entire system and to replace lost ions in the array. Sheets of ionizing laser light placed above the electrodes will intersect with an atom flux guided from the back through a slot in the substrate away from the electrodes to load ions. This type of loading is commonly known as backside loading [99,171] and can be further optimized for fully scalable systems making use of an atom guiding hollow core fibre [213]. The fibres collimate the flux into the trapping zones, and occupy a much smaller area than atomic ovens below the trap structures.

5.7 Vacuum System

Individual 60×60 mm^2 parts will be placed on a 600×600 mm^2 steel frame, shown in Fig. 5.9 (b), each holding 14400 X-junctions. Electrical connections and water cooling tubes are rerouted and connected to vacuum feedthroughs underneath the steel frame. Vacuum pumps and other required vacuum equipment can be placed underneath and above the trap structures.

We propose to place the steel frames inside large octagonal shaped UHV chambers ($\sim 2.5 \times 2.5$ m^2 large) that are connected together using airlocks. At the airlock fewer junction sections are placed and moved out of the lock section using rails underneath the steel carrier frame if the lock is closed. Individual parts are not physically connected and the junctions

[8] $\sim$15% for the H8259-01 PMT, Hamamatsu

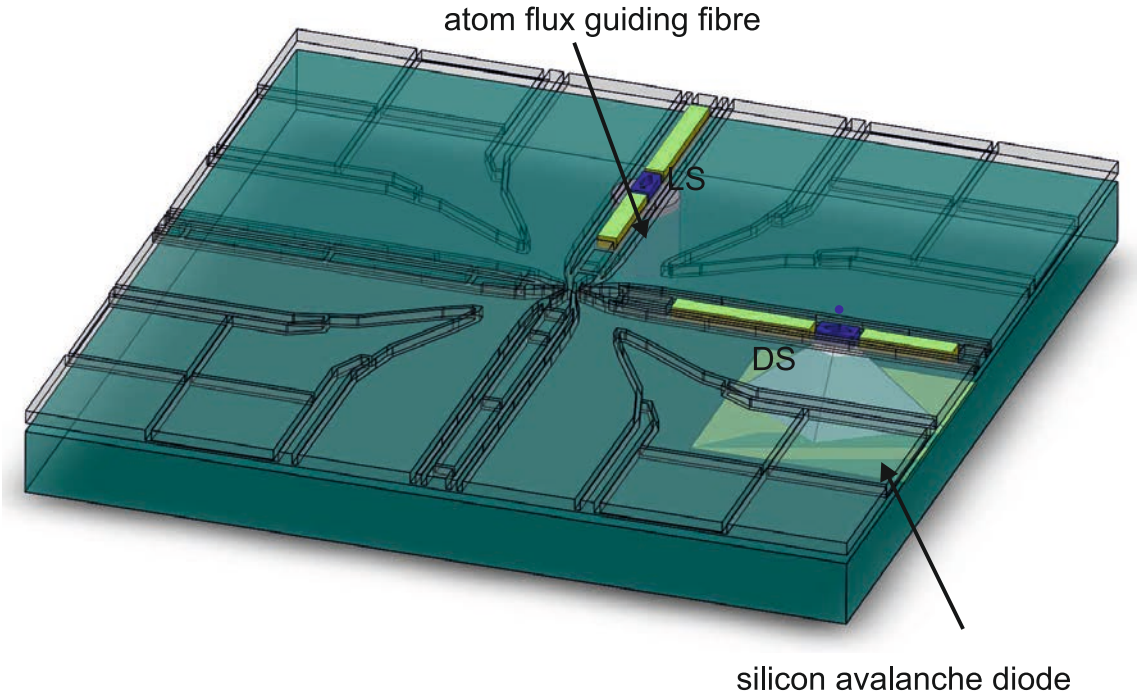


Figure 5.8: Showing an optimized X-junction with a loading (LS) and a detection slot (DS). Underneath the loading slot an atom flux guiding fibre is placed. A silicon avalanche diode is placed underneath the detection slot.

only have to be realigned to each other after the lock is opened again using the piezo actuators. Each chamber should be able to hold at least 17 600×600 mm^2 steel frames, which equals to over 244,800 individual junctions.

Viewports allow for optical access from the sides and top, see Fig. 5.9 (a) and are used for imaging, and to bring laser beams into the system. Imaging, shaping and guiding the laser light sheets above the trap surfaces will require in vacuum optics.

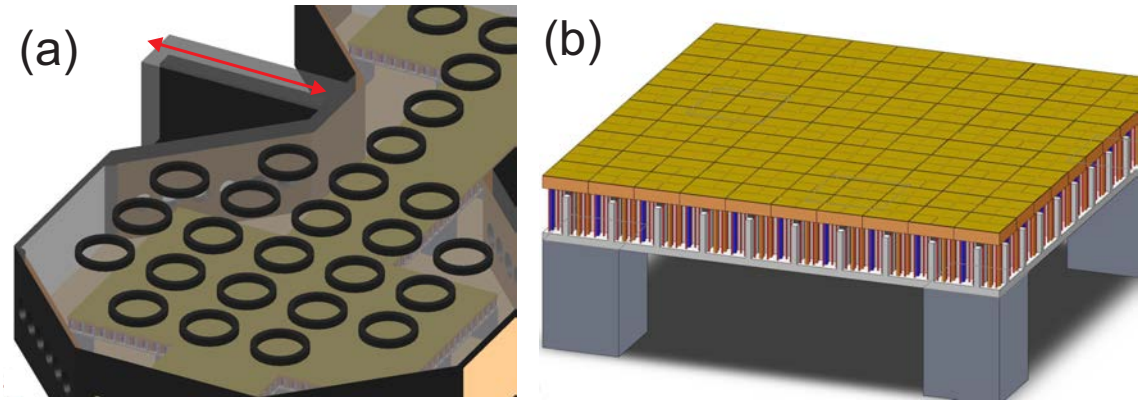


Figure 5.9: (a) shows a schematic of one octagonal UHV chamber connected to a second chamber via an air lock, each chamber can hold over 244,000 individual junctions. Trap sections and parts are placed on steel frames (b). As many chambers as required can be connected together to form an extremely large system.

5.8 Conclusion

We have presented a basic concept for a scalable ion trap quantum system based on requirements to perform the surface error correction code. Proposed technologies were chosen with the highest scalability potential in mind and a scalable asymmetric ion trap design was presented. Some of the technologies have not been fully developed for the exact use and the entanglement method has not reached the required fidelity yet, but no major obstacles that are extremely challenging to overcome were identified. The proposed design could serve as a guideline of what tasks and issues have to be solved in future works towards a large scale ion quantum system. The scalable quantum system concept was also used as motivation for most of the ion trap designs presented in the next chapter 6.

Chapter 6

Asymmetric Ion Trap Designs

After performing a detailed study of different microfabrication processes presented in [75] and developing new fabrication processes discussed in section 4.5.6, new ion trap designs were developed. Motivated by the idea of scalable ion trap systems, discussed in the previous chapter 5 a new optimized X-junction geometry with minimal rf barrier height was designed first. After a barrier reduction of a factor of > 100 was achieved, development of current-carrying wires that can be placed underneath ion trap structures started. The current-carrying wires will be used to generate very high static magnetic field gradients at the ions position required for microwave based quantum gates. The wire structures are embedded in the substrate and can be combined with almost any ion trap design which is fabricated on top. In addition, ion trap designs intended for the experimental demonstration of shuttling between electrically and physically separated rf rails of two linear trap sections were created. Further, designs to investigate backside loading and on-chip detection were developed. Based on the work towards optimization of two-dimensional ion trap arrays for quantum simulations [101], a 3×3 ion trap array was also created.

The design process starting from fabrication process design and electrode optimization via numerical simulations to the final mask layout will be presented. Limitations related to the use of certain fabrication techniques and processes will be discussed. Several ion trap designs will be discussed in detail and lastly the final mask designs for my microfabrication at the Southampton Nanofabrication Centre [1] will be presented.

[1] http://www.southampton-nanofab.com/

6.1 Trap Design, Electric Field Modelling and Mask design

Creating a new ion trap design requires a core electrode geometry, which includes the electrodes that determine the traps capabilities. The centre geometry of a junction trap is essential for adiabatic shuttling capabilities. Structured electrodes with a slot in central dc electrodes can be used for detection or loading and the rf and dc electrodes of 2D ion trap arrays determine if the design can be used for quantum simulations. Bond pads or buried wire structures are essential for the operation of traps but commonly do not affect the pseudopotential and are therefore not simulated.

6.1.1 AutoCAD Model

Designing three-dimensional electronic models of core electrode geometries is accomplished using a computer assisted drawing tool (CAD), like AutoCAD[2] and a design is shown in Fig. 6.1 (a). Models are made up of four-sided 3D polygons and exported as .dxf files[3]. The BEMSolver discussed in section 2.1.4 has an import module that can directly read-in .dxf models and an example is shown in Fig. 6.1 (b).

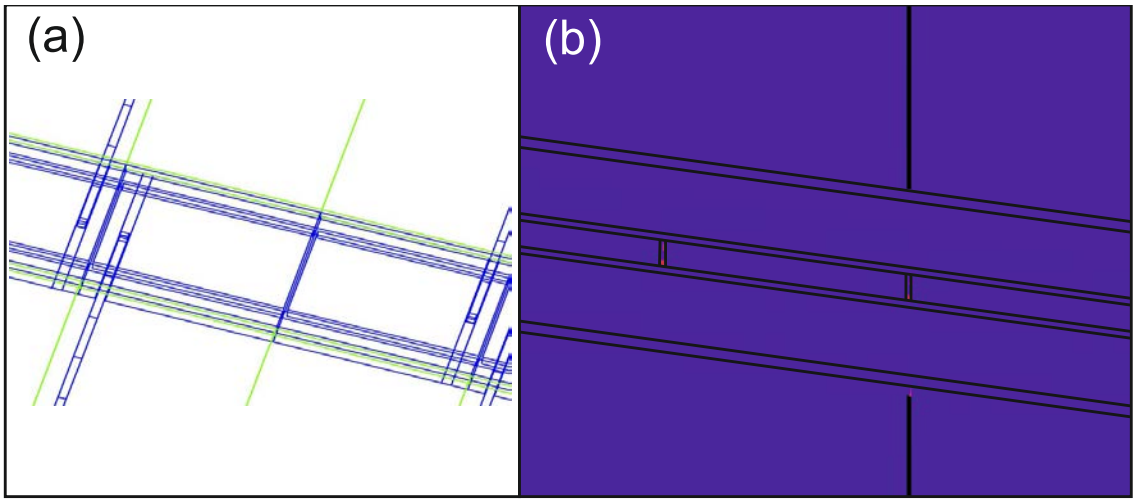


Figure 6.1: (a) Showing a design created in AutoCAD, for illustration purposes only the surface of the electrode layer is shown here, not the full 3D model. (b) The same electrode geometry is imported by the BEMSolver, blue parts correspond to the top of the electrodes, red to the ground plate underneath.

[2] AutoCAD software, by Autodesk
[3] Drawing Exchange Format

6.1.2 BEMSolver

Before simulating the trap geometry rf and dc/ground electrode structures need to be assigned to AutoCAD layers that can be imported by the BEMSolver, for example rf electrodes are assigned to layer rf, dc electrodes to dc1, dc2 and ground to gnd. The BEMSolver recognizes the layers and outputs an electric field function, generated by the electrode geometry. For the simulation a potential of 1 V is applied to the electrode structures in layer rf, while electrodes in all other layers are kept at 0 V.

6.1.3 Calculation of Pseudopotential and Trap Parameters

The BEMSolver outputs .dat files containing space coordinates for data points in a predefined volume and corresponding electric field values, based on the simulated electric field functions. A computational program like Mathematica is used to import the .dat files and interpolate individual data points with a function. The Pseudopotential of rf and dc electrodes can then be derived and visualized, as in Fig. 6.2. As discussed in chapter 2, the pseudopotential can also be used to calculate trap depth, secular frequencies, stability parameter q, residual rf potential at the rf nil, also known as rf barrier and principal axis rotation.

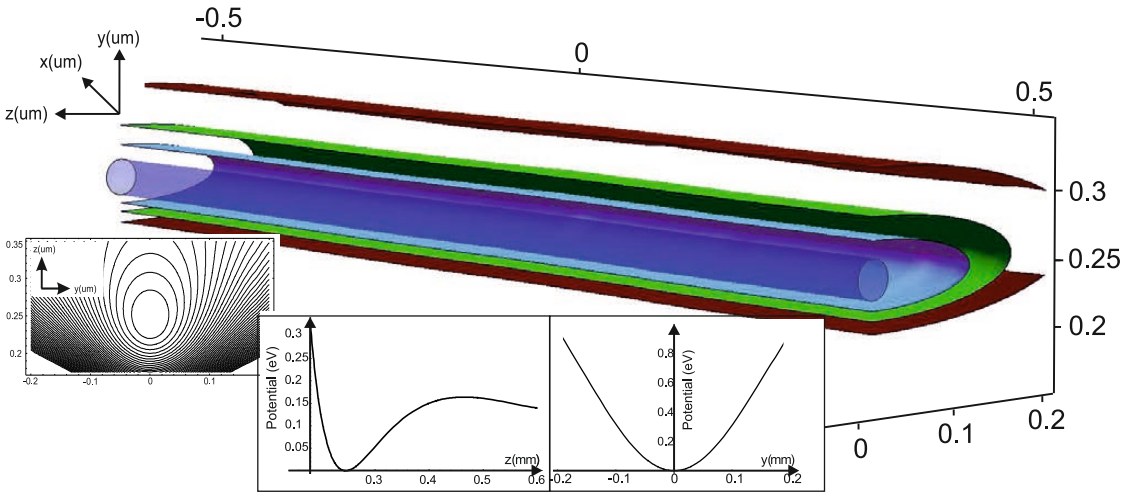


Figure 6.2: Pseudopotential of simulated electrode geometries are visualized using Mathematica. The main picture shows four boundaries of different potential heights in the geometry. Insets show pseudopotential in z and y direction as well as a 2D contour plot of the potential.

After the core electrode geometry is optimized for the intended purpose, the entire trap structure is designed in 2D. Additional structures for buried wires (BW), vertical inter-

connect access (VIA) between electrodes and buried wires and current-carrying wires are added. Also the top electrode layer is extended to a size of $\sim 10 \times 12$ mm^2, bond pads are added to the design. Wire or ribbon bond connections are made between the bond pads of the chip and pads of the chip carrier. After all geometries are finalized, a photolithography mask can be created from the individual designs. Photolithography masks are manufactured by a commercial supplier and the required data has to be supplied in GDSII format [4]. Compiling the mask and creating the GDSII file is done with a special mask software, which in our case is LayoutEditor[5]. Designs will be repeated several times on the mask and are imported to cells which are then repeatedly placed in the main mask design. In addition, alignment marks are added to the mask allowing the alignment of a mask layers with structures fabricated on the chips.

6.2 Process Limitations

Depending on the cleanroom where the trap design will be fabricated, the process described in section 4.5.6 will have to be adjusted according to the available machines and process step limitations. Besides minimum feature size and thickness of layers, the Southampton cleanroom does not allow the use of certain metals like gold or copper in several machines, as these can contaminate the tool chamber and destroy the samples of other users. Buried wires and the majority of the electrodes will be made by depositing aluminium. The electrode surface will be coated with a gold layer, which prevents the electrode surface from oxidising. Certain ion trap designs can also require different process steps, for example an ion trap with integrated ultra-high quality factor microwave resonator will require the electrodes to be made of a superconducting material.

Also the previously discussed electrical limitations (see chapter 4), large rf capacitance and resistance, loss tangent of dielectrics, power dissipation, voltage breakdown, non oxidizing electrode surfaces will have an impact on the trap design.

To cater for the different trap designs a versatile microfabrication process that consists of two independent process parts was developed in collaboration with Ibrahim Sari[6]. The first part of the process makes use of chemical vapour deposited (CVD) diamond substrates. Metal tracks are embedded in the substrate and covered with an insulating layer.

[4] Graphic Database System II stream format
[5] LayoutEditor software by juspertor
[6] Research staff member in the Nanoresearch group, University Southampton

The second part of the process can either be used to fabricate traps on quartz or alumina (Al_2O_3) substrates without current-carrying wires or used after the first process to create trap structures on top of diamond substrates including the current-carrying wires. Simplified layer structures for both processes are shown in Fig. 6.3.

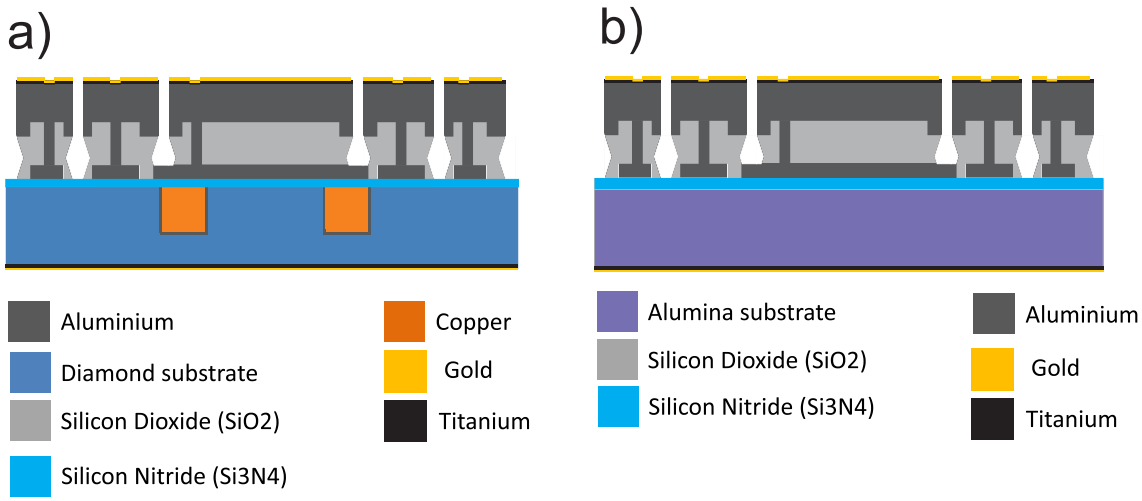


Figure 6.3: (a) Vertical structure of an ion trap fabricated on a diamond substrate with current-carrying wires and buried wires to connected isolated electrodes. (b) Layer structure of alumina substrate based ion traps, buried wires are connected to the top electrodes using vertical interconnect access holes. A gold metallization is deposited on the back of both substrates.

The minimum trap feature size is ~ 2 μm, limited by the photolithography used in the process, electrode layer thickness is limited to ~ 5 μm due to the e-beam evaporator used, dielectric layers can also be made ~ 5 μm thick. Deposited gold layers are limited to ~ 200 nm due to the financial cost of the deposition.

To keep capacitances of rf electrodes low, only dielectric substrates were considered and structured ground plates are placed on top of exposed dielectrics close to the rf nil and not extended underneath rf electrodes. Electrode-electrode gaps were kept at a minimum of 3 μm for 2D array traps with an ion-electrode distance of ~ 30 μm and ≥ 5 μm for all other designs to prevent surface breakdown at voltages above 250 V [141]. The number of dc electrodes is limited to 90 by the number of accessible chip carrier bond pads.

6.3 X-Junction Trap Design

Motivated by the idea of a two-dimensional junction array I started working on an optimized X-junction geometry. X-junctions connect four rf nils perpendicularly and make it possible to form a two-dimensional grid of rf nils, through which ions can be shuttled. Ions

can be shuttled around corners, which was first demonstrated in [78] using a symmetric trap, moving ions from one section to another and to rearrange ions. The geometry of the electrodes forming such an intersection has to be highly optimized to prevent the forming of rf barriers close to the nil intersections (junction centres), which can prevent adiabatic shuttling through the junction. Adiabatic shuttling through a junction has only been demonstrated using a symmetric X-junction [81] and has not been achieved in asymmetric ion trap junctions yet. Therefore the optimization was also intended to produce traps for future experiments demonstrating this.

For the optimization process a simple X-junction structure without any optimization, shown in Fig. 6.4 (a), is used for comparison. The 430 μm wide rf electrodes are separated by 170 μm from each other with a 150 μm wide centre dc electrode. Electrode-electrode gaps are 10 μm and a ground plate shown in Fig. 6.3, which has a significant influence on the pseudopotential and ion height at the junction centre, was included and placed 10 μm below the electrode surface. In a junction arm 1.5 mm away from the centre, the electrode geometry creates an rf minimum $\sim$ 216 μm above the surface. The ion height will change when coming closer to the junction centre. After the junction geometry was optimized, dc electrode rails for principal axis rotation will be added, the rf rails are of identical width.

Residual pseudopotential values at the rf minimum position are commonly referred to as rf barrier, which has to be overcome when shuttling through the junction. If one wants to shuttle adiabatically through the junction, the barrier has to be as small as possible to avoid motional excitations [79] of the shuttled ions. The barrier height was determined by finding the exact rf minimum for several data points (> 50) between x =400 μm and x = 0 μm. The data points are then interpolated and corresponding pseudopotential values are plotted. All X-junction designs are perfectly symmetric in x and y direction and therefore only the barrier from one arm towards the centre was investigated.

All X-junction designs were simulated with an rf potential amplitude of 400 V and frequency of $2\pi \times 20$ MHz applied to the rf electrodes. For a better comparison between different designs the barrier height was also normalized with the trap depth of the corresponding design at an rf minima in one of the arms 1.5 mm away from the trap centre, where the pseudopotential is unaffected by the junction centre geometry.

In Fig. 6.4 (b) the ion height along the x-axis of one junction arm from -400 μm to 0 μm at $y = 0$ is plotted together with a contour plot of the corresponding pseudopotential, showing a large ion height increase from $\sim$ 235 μm to $\sim$ 355 μm. The normalized residual

pseudopotential values at the rf minima positions are shown in Fig. 6.4 (c). The maximum value was determined to be 28% of the trap depth.

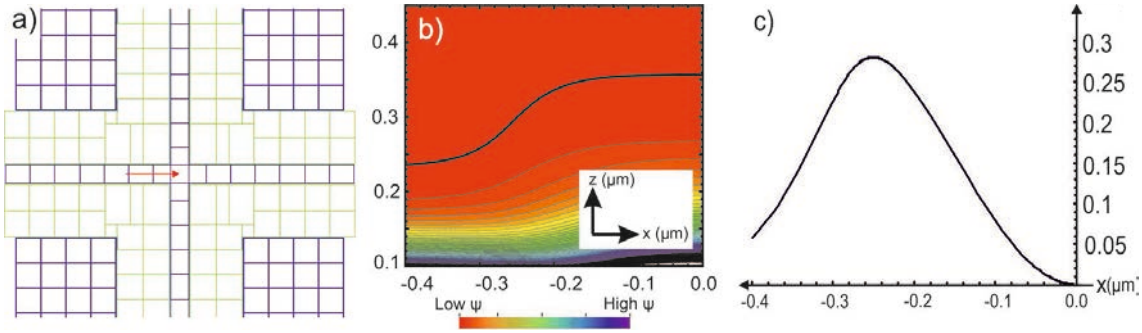


Figure 6.4: (a) Unoptimized junction section, with blue marked dc electrodes and green rf rails. Ion height graphs and barrier height are plotted for data points along the red line. (b) shows the height of the rf nil towards the junction centre and corresponding pseudopotential. The normalized barrier height, with a maximum of 28% the trap depth is shown in (c).

6.3.1 First Optimization of X-Junction

Following the Y-junction design by Robin Sterling presented in [113], the optimization started by narrowing the width of the inner dc electrodes towards the centre, while pulling the rf electrodes closer to the junction centre. In addition, part of the outer dc rails are moved towards the centre, reducing the rf rail width. The first optimization result is shown in Fig. 6.5 (a) and the corresponding normalized rf barrier is plotted in Fig. 6.5 (c). Compared with the example case the barrier was reduced by a factor of ∼2.5 to 11% of the trap depth. The ion height along the x-axis from $x = 400$ μm to $x = 0$ μm at y= 0 in this design is shown in Fig. 6.5 (b).

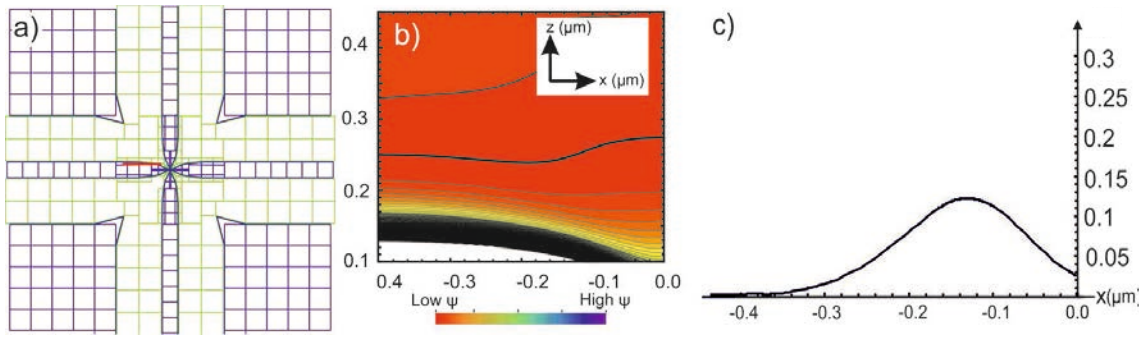


Figure 6.5: (a) First optimization of junction section, with blue marked dc electrodes and green rf rails. (b) Shows the height of the rf nil with corresponding pseudopotential along the red marked line. Normalized barrier height is equal to 11% of the trap depth and shown in (c).

6.3.2 Further Optimization of X-Junction

The previously presented geometry was optimized further by refining the inner dc electrode geometries. Outer dc electrodes are pulled much further towards the centre, significantly reducing the width of the rf rails. The optimized geometry is shown in Fig. 6.6 (a), and an rf barrier height suppression by a factor of ∼15 to 1.9% of the trap depth was achieved, see Fig. 6.6 (c). Fig. 6.6 (b) shows the ion height of the rf minimum at $x = 400$ μm to $x = 0$ μm and $y = 0$. No further reduction of the rf barrier was achieved by continued refining of rf and dc electrodes.

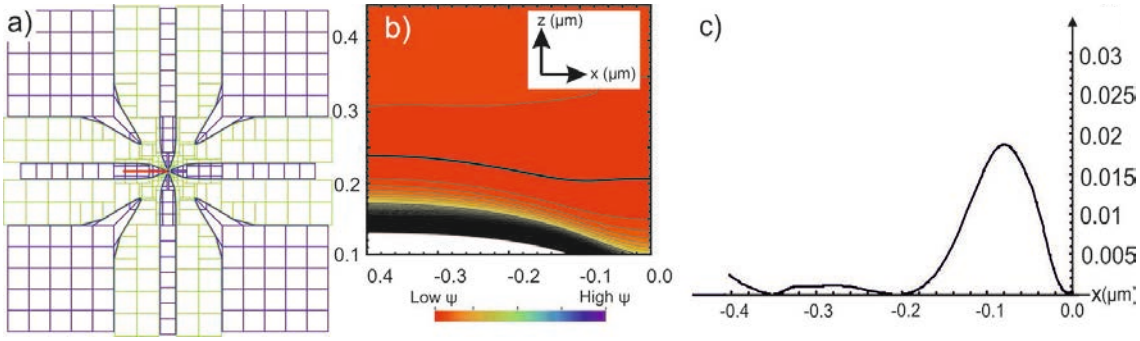


Figure 6.6: (a) Shows refined X-junction geometry with blue marked dc electrodes and green rf rails. In (b) the ion height along the red marked line in (a) is shown together with the corresponding pseudopotential. (c) Shows the normalized rf barrier height with a maximum at 1.9% of the trap depth.

6.3.3 Octupole X-Junction

A different concept based on the work presented in [214] using an octupole pseudopotential was therefore tested and initial optimization resulted in the geometry shown in Fig. 6.7 (a). The normalized barrier was suppressed further to 1.2% of the trap and is plotted in Fig. 6.7 (c) together with the ion height in Fig. 6.7 (b). Although the initial suppression resulted in promising results the octupole geometry was not considered further as it resulted in a much lower trap depth (∼3 times lower) compared to a standard quadrupole design with the same rf potential applied.

6.3.4 Final X-Junction Design

Instead the octupole geometry was combined with the optimized quadrupole junction, previously presented. The rf rails are interrupted close to the centre by small rf ground patches, which reduce the barrier at the junction centre, see Fig. 6.7 (a). This will reduce

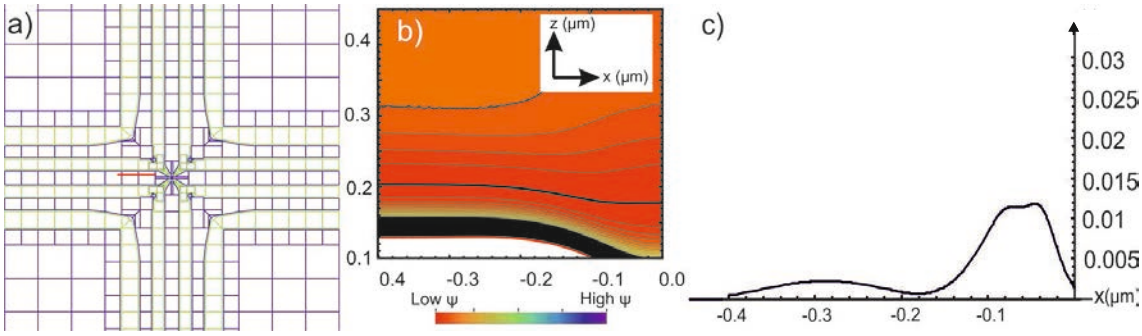


Figure 6.7: (a) Shows the octupole X-junction design, with 4 rf rails (green) separated by 3 dc rails (blue). Pseudopotential and ion height along the red marked line are shown in (b). The corresponding normalized barrier shown in (c) has a maximum at 1.2% of the trap depth.

the trap depth of the design close to the centre, while the trap depth in junction arms, where the ions are trapped and most experiments are performed, is unaffected. After several additional optimizations a barrier suppression of > 110 to 0.25% of the trap depth was achieved, as shown in Fig. 6.7 (c). The ion height is strongly reduced close to the centre from ~ 200 μm to ~ 100 μm, see Fig. 6.7 (b). This is caused by the missing dc electrode in the centre combined with the ground plate underneath, pulling the rf minima closer to the surface. Simulations of the rf pseudopotential showed that static voltages applied to the dc electrodes can be used to push the ion height to ~ 150 μm without increasing the barrier height above 0.25%, which would reduce the heating experienced by the ion while being shuttled through the centre. Further optimizations were not able to produce a lower barrier.

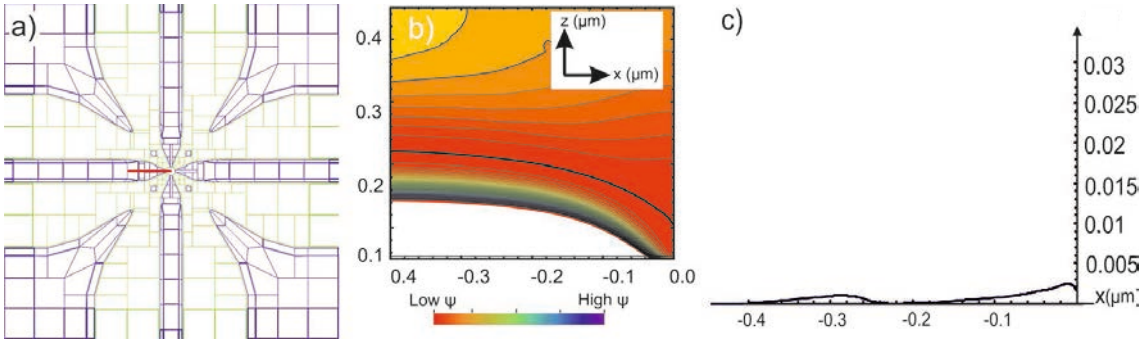


Figure 6.8: (a) Final design of the optimized X-junction geometry, combining quadrupole rf (green) and dc (blue) rails with small ground patches similar to an octupole design in the centre. The ion height towards the centre is shown in (b) with the corresponding pseudopotential. For this geometry an rf barrier suppression by a factor of > 110 was achieved. The normalized barrier is shown in (c) peaking at only 0.25% of the trap depth.

Fig. 6.9 shows a comparison of barrier heights for all discussed electrode structures. Starting with the unoptimized case at 28% of the trap depth, first optimization yielded

11% which was further improved to 1.9%. Using an octupole approach resulted in 1.2% and combining both designs it was possible to reduce the barrier to the final value of 0.25% of the trap depth.

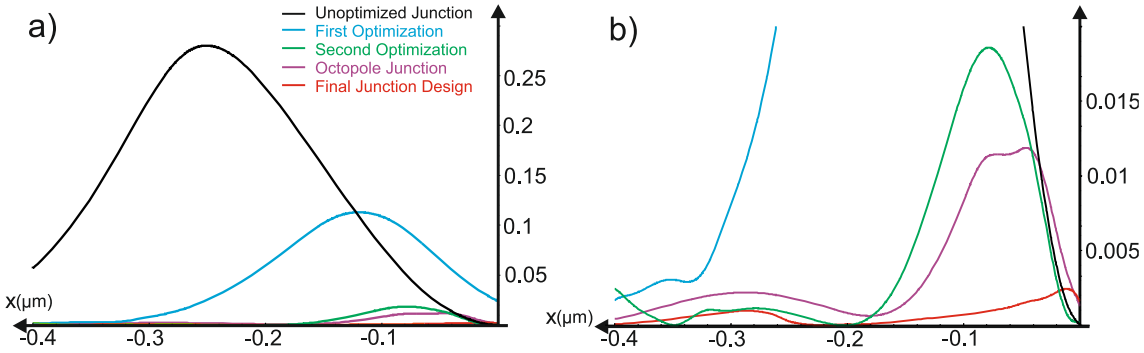


Figure 6.9: (a) showing a comparison of normalized barrier heights for all presented designs. (b) shows the same barrier heights plotted up to a value of 2% of the trap depth.

6.3.5 Ion Trap Design and Electrical Characteristics

After the optimization of the core geometry was completed, an ion trap design including all structures required to trap and shuttle ions was developed. First the inner dc electrodes of each arm were segmented into eight individual electrodes, the dimensions are optimized for fast ion separation and shuttling following the work presented in [103]. In addition, two dc rails were added, which are used to rotate the principal axes. Outer dc rails are also segmented into eight electrodes and two dc rails, required for the principal axis rotation. Fig. 6.10 shows the final top electrode layer, where the rf electrodes are connected from two sides to make sure no rf phase mismatch occurs due to different path lengths and then connected to a large bond pad. Also 88 bond pads are placed on the top and bottom of the ion trap design, where electrical connections between dc electrodes and the chip carrier are made.

The final ion trap design has a size of 12×10 mm^2, ideal for the used chip carrier (PN PGA10047002, Global Chip Materials). Smaller chips make wire bonding between bond pads on ion trap and chip carrier more challenging due to larger distance.

Connections between dc electrodes and bond pads are made using vertical interconnect access (VIAs) structures and buried wires (BW). The buried wire layer also includes a structured ground plate which shields otherwise exposed dielectrics close to the trapping regions, but does not extend underneath the rf electrodes, which would lead to an increase in the rf electrode capacitance. Buried wire structures are separated from the electrode

layer by a $\sim$ 3 μm thick SiO_2 layer. Fig. 6.11 shows the buried wire layer for the final X-junction trap. Where buried wires cross the rf electrode the width is reduced not to increase the capacitance more than necessary.

Vertical interconnect access holes are designed to be slightly smaller ($\sim$ 1 μm) than the buried wires underneath to prevent eventual shorting with the structured ground if the alignment of the two layers is not perfect. When depositing the electrode layer, VIA holes will be filled up with the electrode material and make an electrically connection between BWs and electrodes. Fig. 6.12 shows the VIA layer for the X-junction design.

In Fig. 6.13 all layers are overlaid with each other to illustrate how dc electrodes are connected with buried wires to the bond pads on the side.

Traps based on the X-junction design are intended to be operated with an rf potential of 400 V and $\Omega = 2\pi\times17$ MHz applied to the rf electrodes. Assuming the trap structure is fabricated on a 500 μm thick Al_2O_3 substrate with a ground plate on the back of the substrate and 3 μm thick aluminium electrodes that are separated from the buried wire layer by a 2.5 μm thick SiO_2 layer, the following trap characteristics were derived following the calculation in section 4.2.

Trap depth: 0.3 eV **Stability parameter** q**:** 0.29
Ion height: 210 μm
Radial secular Frequencies: 1.74 MHz in z direction and 1.60 MHz in y direction
RF electrode capacitance: 4.53 pF
RF electrode Resistance: 1 Ω
Power dissipation: 59 mW

6.3.6 Conclusion

An X-junction design with an rf barrier height suppression of > 110 was developed making use of a combination of quadrupole and octupole elements. The optimized geometry was used to design a complete ion trap chip and expected trap operation parameters are presented. After fabrication is completed, the measured electrode geometries and layer thicknesses will be used to make a realistic simulation of the junction design and to determine voltage functions for adiabatic shuttling through the junction.

Based on this design a second X-junction trap design with 100 μm ion height was developed

and the design is presented in App. D. The 100 μm ion height junction architecture is identical to the presented design but scaled down by a factor of 1/2 including the electrode-electrode gaps, which are now 5 μm wide. This design can also be combined with current-carrying wires presented in the next section. The lower ion height makes it possible to achieve larger gradients compared to the 200 μm version of the junction, which is more suitable for shuttling experiments.

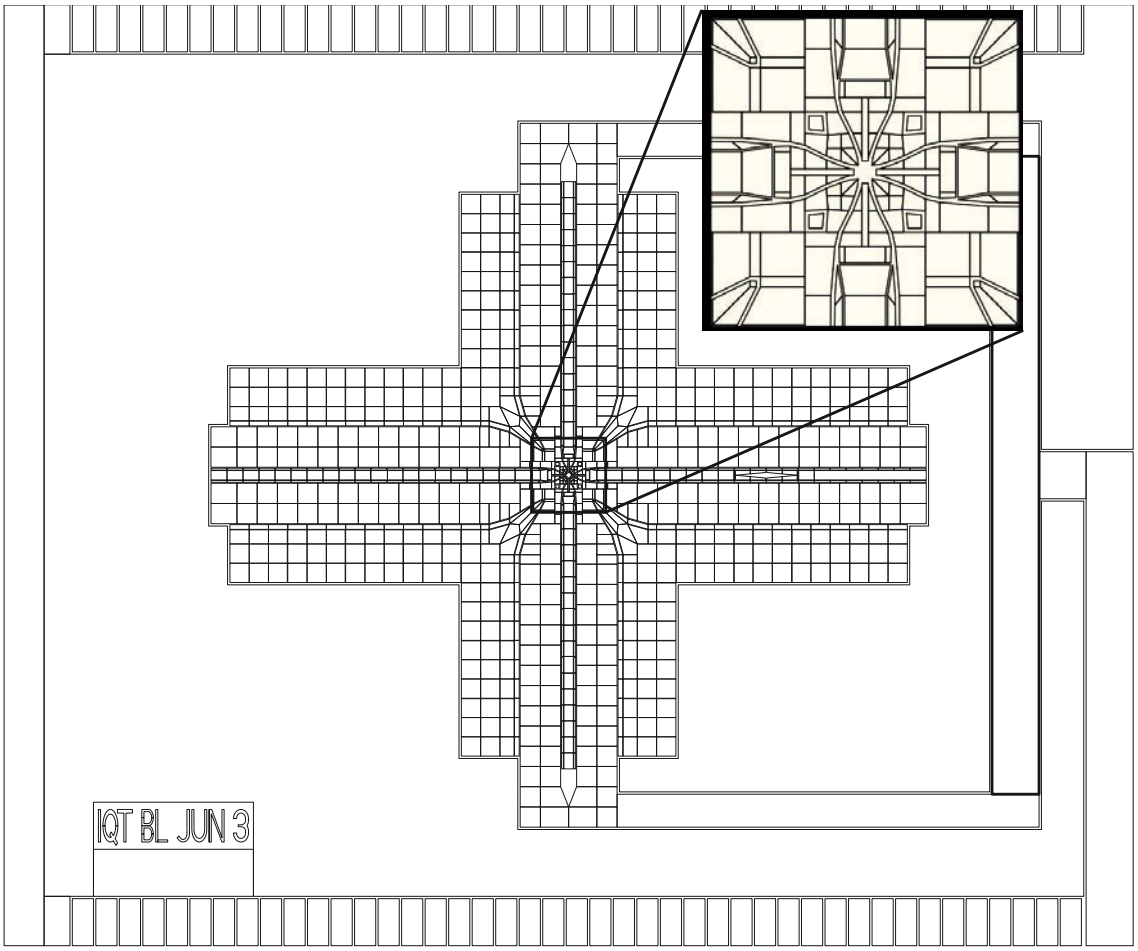


Figure 6.10: Showing the electrode layer of the X-junction chip design, including bond pads on top and bottom of the design. RF rails are connected from two sides to prevent an rf phase mismatch. Inset shows a magnification of the junction centre.

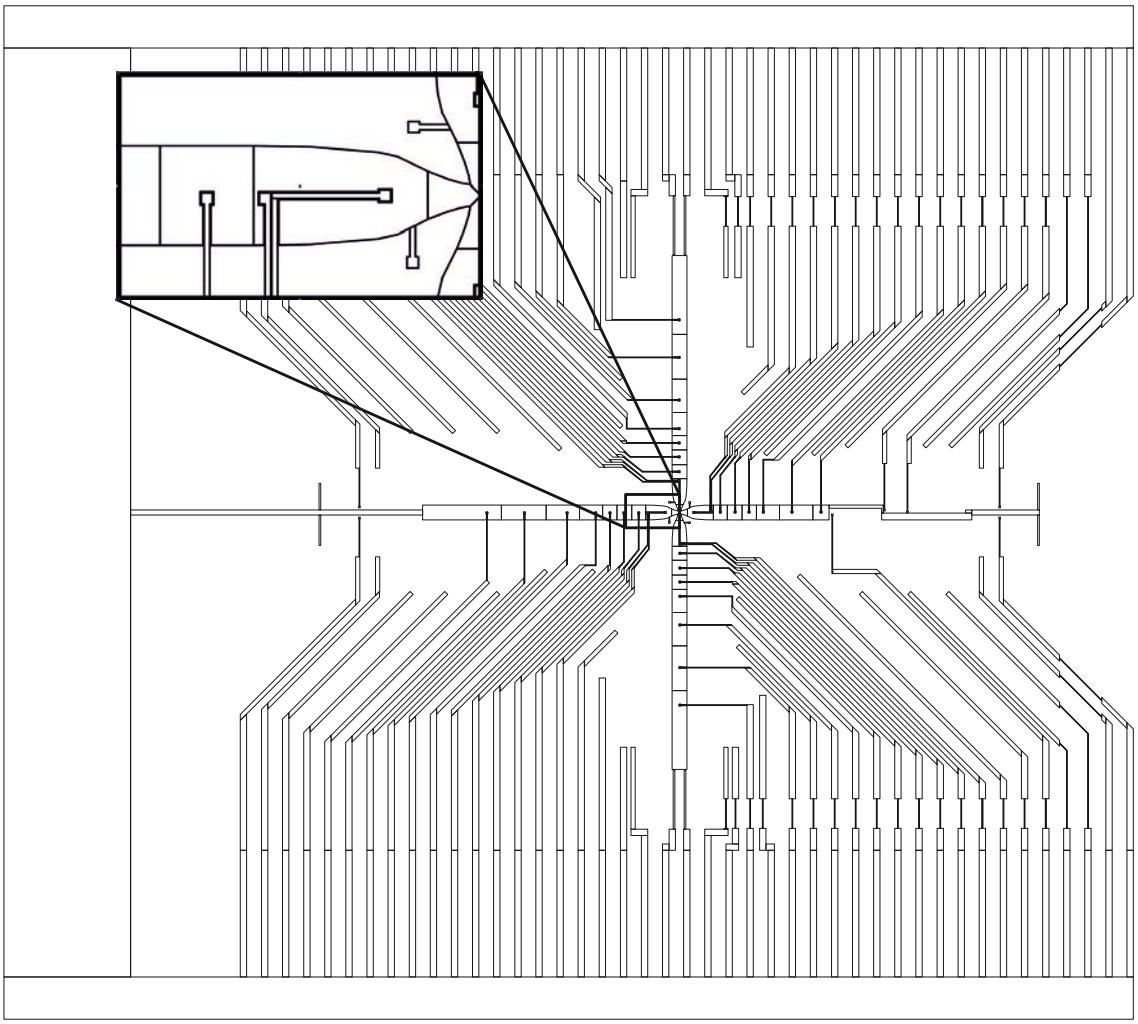


Figure 6.11: Shows the buried wire layer including the structured ground plate. All buried wires were connected together at the top and bottom, making the design compatible with potential electroplating steps for the following via layer. The connections will be removed by cutting the ion chip to the intended 12×10 mm^2 size after fabrication.

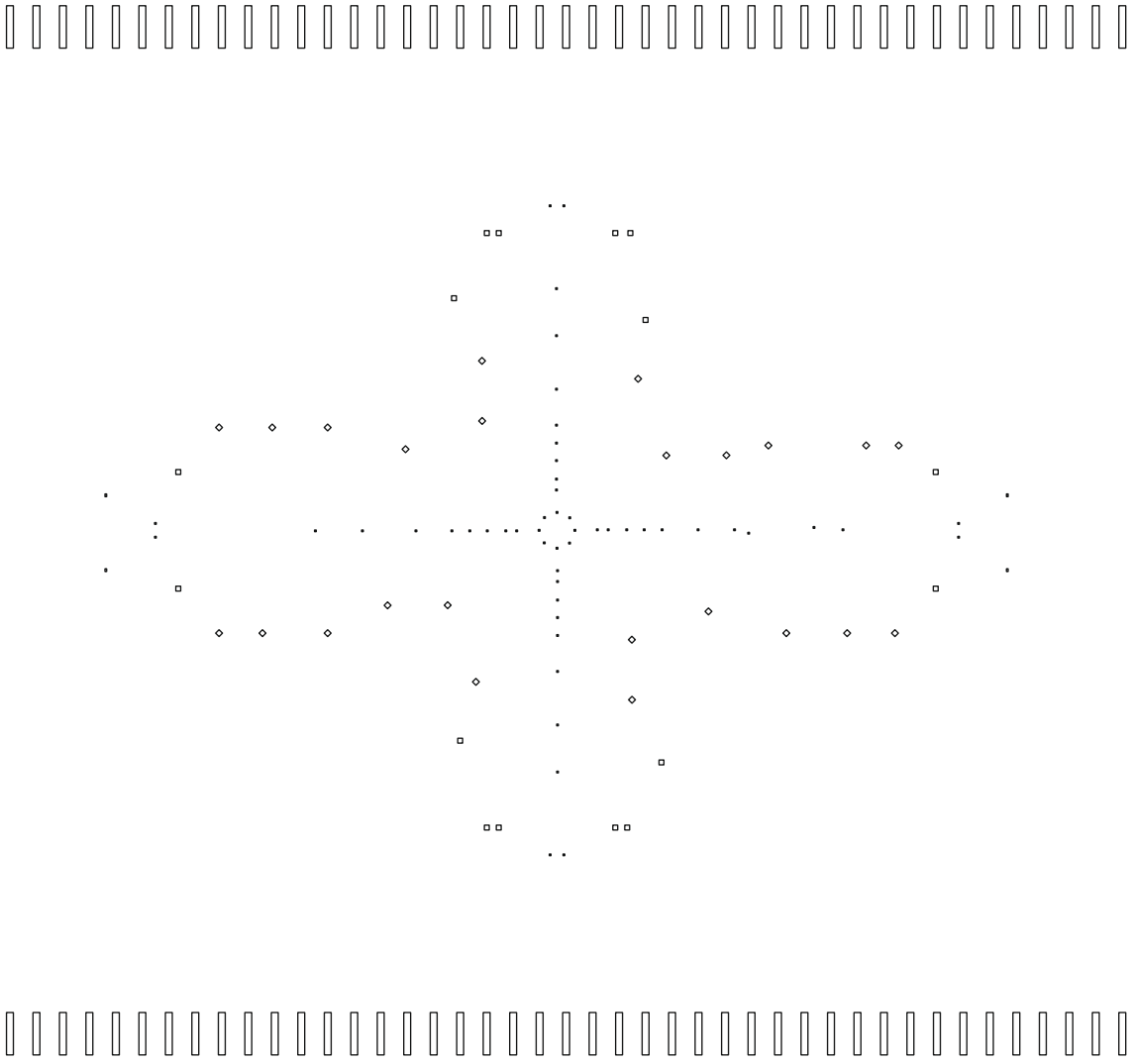


Figure 6.12: Shows the vertical interconnect access layer design used to etch holes into the SiO_2 layer separating electrodes and buried wires.

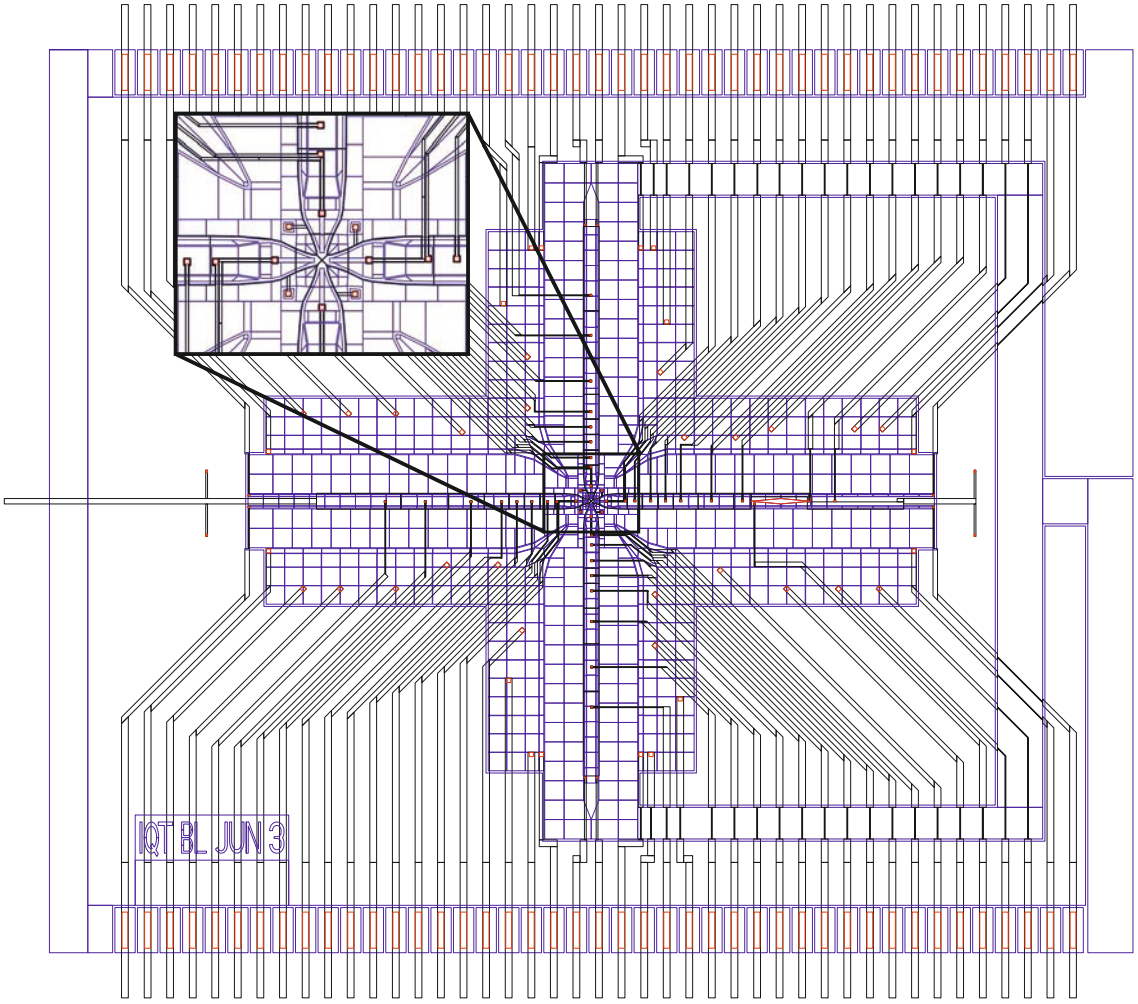


Figure 6.13: Shows all three layers overlapped with each other (electrode layer is blue, buried wire layer black and VIA layer red), illustrating how connections between buried wires, electrodes and bond pads are made. Inset shows a magnified view of junction centre.

6.4 Current-Carrying Wire Structures for Asymmetric Traps

The development of current-carrying wire structures intended to create large static magnetic field gradients at the ion position will be discussed next. Large magnetic field gradients will be used to perform microwave based quantum gates as outlined in section 2.3.3. Suitable gradients can either be generated by passing a current through wires close to the trapping position or using permanent magnets. Magnets have been successfully used to perform a microwave based quantum gate presented in [82] and can currently produce gradients on the order of $\sim 20 - 40$ T/m . Magnets will create a permanent magnetic field which requires careful alignment with the trapping position such that the magnetic field nil overlaps with the rf nil position. Otherwise this will cause a strong Zeeman shift, which can prevent Doppler cooling and make trapping of $^{171}Yb^{+}$ ions impossible.

Using current-carrying wires placed underneath the ion trap structure the magnetic field can be easily adjusted or completely turned off for trapping. In addition we hope to achieve much larger magnetic field gradients at the ions position on the order of 100-150 T/m. Current-carrying wires are placed underneath the actual trapping structure, which allows the wire positions and geometry to be freely chosen without having to take the electrode structures into consideration.

6.4.1 Challenges

When trying to apply very large currents to an ion trap structure several challenges arise that have to be overcome. To generate the largest possible gradients the wire diameter has to be as small as possible close to the trapping position, which results in very large current-densities that can locally produce so much heat that the wire structures melt even if the ion trap chip is kept at room temperature.

If the ion trap structure allows it to sufficiently cool the thin wire sections, the large current densities can still damage the structures due to electromigration. Electromigration occurs when very large current densities are applied to well cooled metal structures, commonly found in high power semiconductor devices. An atomic flux travels through the structure as a result of momentum transfers from electrons to the metal structures. If the atomic flux is too large, then the structures will be eroded at positions of highest current density destroying the wire structure. The atom flux caused by electromigration depends on the temperature of the metal, current density and a material specific activation energy for the

migration. In addition the wire structures have to be made of a very thick ($\sim 20-30$ μm) microfabricated conductive layer. Only electroplating is suitable for this process, which limits the choice of materials.

6.4.2 Wire Material Choice

When choosing the correct material to create the wires all of these factors have to be taken into consideration. Electroplating of superconducting materials is extremely challenging and it is not clear if a thick superconductor layer can withstand the applied current densities. Additionally the ion trap chips should be compatible with a room temperature vacuum system, ruling out superconducting materials.

The metals considered for the current-carrying wires include gold, silver, copper and aluminium. Silver has the highest thermal and electrical conductivity[7], but has a much lower electromigration activation energy of 0.67 eV [215] compared to copper with 1.2 eV [216]. Gold and aluminium have lower thermal and electrical conductivities than copper and lower electromigration activation energies of 0.92 eV [217] and 0.6 eV [216] respectively. Copper is the second best thermal and electrical conductor [8] and possess the highest electromigration activation energy (1.2 eV [216]) of the discussed metals. In addition copper is commonly used to produce thick electroplated wire structures, when making printed circuit boards. It was therefore decided that copper is the most suitable material for current-carrying wire structures.

6.4.3 Power Dissipation of Wire Structures

After we have chosen a suitable metal to fabricate the wire structures we can calculate the amount of power dissipated by the entire structure and the temperature gradient between the wire structures with smallest width (60 μm) and a heat sink. The wire structure presented in Fig. 6.14 is made of 30 μm thick copper embedded in the substrate. By increasing the wire width from the centre (60 μm) towards the outside (1500 μm) where electrical connections are made, the power dissipation can be reduced to a minimum. Wires structures also include 1 mm wide and 1.5 mm long contact pads, where electrical connections can be made.

[7] $T_c \sim 429$ W/(m· K) and $\rho = 15.9\ n\Omega \cdot m$
[8] $T_c \sim 400$ W/(m· K) and $\rho = 16.8\ n\Omega \cdot m$

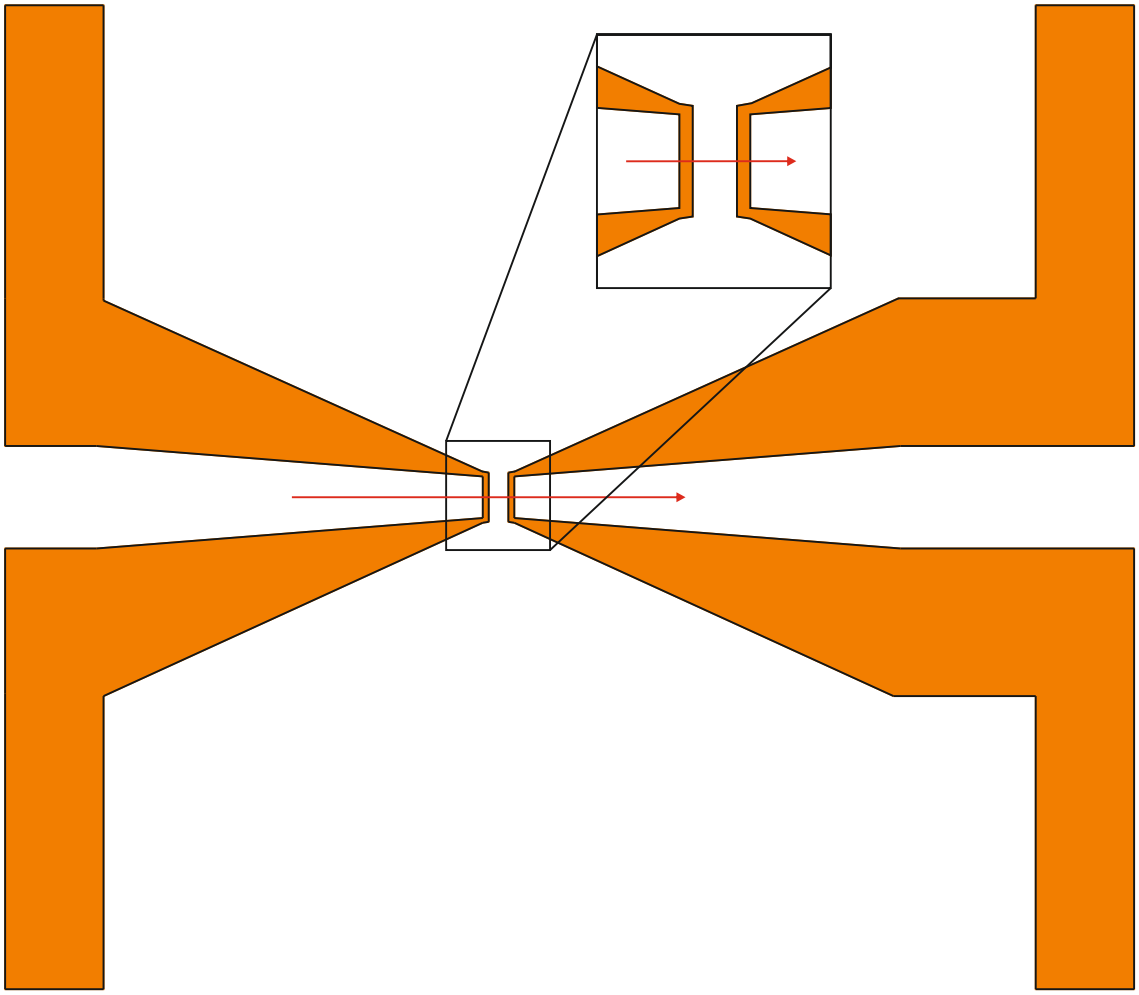


Figure 6.14: Shows the current-carrying wire structure, smallest wire width is 60 μm and size of the entire structure is $12 \times 10\text{mm}^2$. Gradients are plotted for positions along the red marked line at ion height.

The power dissipated by the discussed structure can be calculated using the equation

$$P_{\text{total}} = I^2 \frac{\rho l}{wt} \tag{6.1}$$

where ρ is equal to the resistivity of the metal used for the tracks, l the length of a section, w the width and t the thickness of the wire structure. If 12.5 A of current is sent through both wires the power dissipated in the structure shown in Fig. 6.14 will be equal to 5 W. For 25 A applied to both wires the power dissipation will go up by a factor of 4 (20 W).

To make sure the ion trap does not overheat a designated heat transfer system will be used, which is described in detail in section 7.1. For the following calculation we will assume that the chip is directly soldered onto a copper heat sink kept a room temperature, using a high performance gold-tin solder[9] .

6.4.4 Thermal Gradient Between Wire Structures and Heat Sink

Looking at the heat dissipation per area P/A= 23×10^6 W/m^2 in the wire section with smallest width (60 μm) it becomes clear that we also have to consider the temperature gradients between this wire section and the heat sink. Assuming that the wire structure is embedded in an Al_2O_3 substrate and taking the required adhesion and contact layers into consideration, shown in Fig. 6.15, we can calculate the temperature gradient by adding up contributions from individual layers derived with:

$$\Delta T = \frac{P_{\text{total}} t_{\text{Layer}}}{T_c(\text{Material}) wl} \tag{6.2}$$

In addition a thermal transport model based on a vertical heat spread, see Fig. 6.15, in the substrate and gold solder perpendicular to the transport direction will be considered. Commonly the heat spread angle is approximated to be 45°, but a more detailed analysis presented in [218] showed that for all the investigated materials the angle was close to ∼36.5, which will be used for the following calculations.

The electroplated copper layer is 30 μm thick and has a thermal conductivity of $T_c \sim$ 401 W/(m· K) [219]. Top and bottom titanium adhesion layers are 100 nm thick and have a thermal conductivity of $T_c \sim$ 22 W/(m· K) [219]. The bottom gold layer is 150 nm thick with a thermal conductivity of $T_c \sim$ 318 W/(m· K) [219]; the alumina substrate is

[9] 80Au/20Sn solder, Indium Corporation

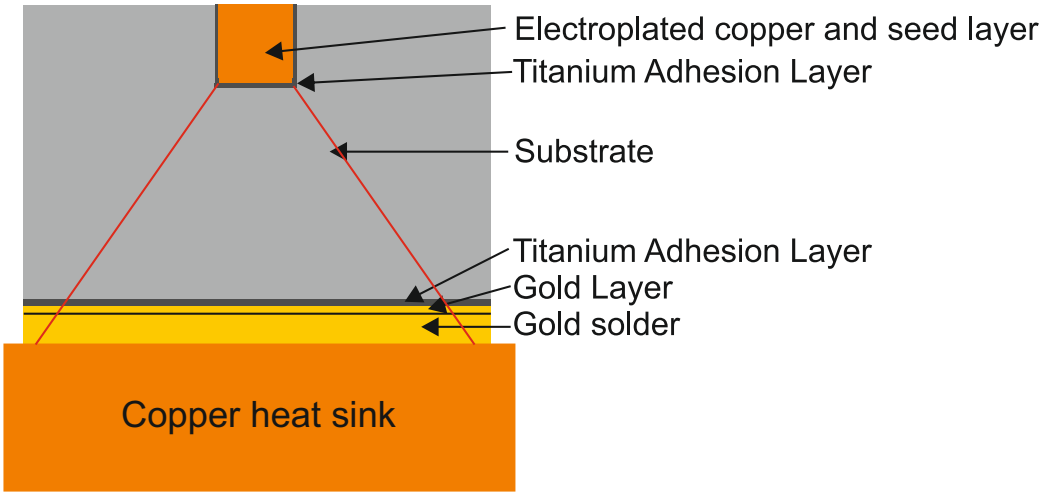


Figure 6.15: Schematic illustration of the layer structure of the ion trap involved in the transport of heat generated in current-carrying wires. Red lines indicate how the heat spreads in horizontal direction while traveling through the substrate and layer structure.

assumed to have a thermal conductivity of $T_c \sim 28$ W/(m· K)[10] and is 500 μm thick; the gold solder is 25 μm thick with a conductivity of $T_c \sim 57$ W/(m· K)[11].

For the described structure and a current of 12.5 A the temperature gradient between wire structure and heat sink was calculated to be $\sim$ 100 K, which increases to $\sim$ 400 K for 25 A of current. Increasing the temperature of the wires by $\sim$ 100 K will also increase of the copper resistance by 40% and increase the temperature gradient further. Passing 25 A of current through the wire structure will melt them. We therefore concluded that alumina substrate is unsuitable for current-carrying wire structures.

If we replace the alumina substrate with 300 μm thick diamond substrate, which has a thermal conductivity of $T_c \sim 1800$ W/(m· K)[12], then the temperature gradient between wires and copper heat sink is reduced to $\sim$ 3.7 k and $\sim$ 14.8 k for 12.5 A and 25 A of current respectively. The increase in electrical resistivity will be minimal. If the heat sink temperature can be kept close to room temperature we expect that even higher currents could potentially be applied to the wire structures.

If we look at the individual contributions for the thermal gradient we can see that the dominant contributors are the diamond substrate with $\sim$ 1.2 K and the solder attachment with $\sim$ 1.3 K. This emphasises the importance of a good connection to the heat sink. Indium based solder has an even higher thermal conductivity than gold-tin solder, but would melt during the 200°C vacuum system baking procedure. Highly thermally conduc-

[10] provided by Valley Design
[11] provided by Indium Corporation
[12] provided by Mintres BV

tive UHV glue (EPO-TEK H20E) possess a thermal conductivity of $T_c \sim 2.5$ W/(m· K) and would drastically limit the amount of current that can be applied.

6.4.5 Maximum Current Density

After determining the temperature gradient between the thinnest wire section, the current density in this section was also derived to 0.7×10^{10}A/m^2 and 1.4×10^{10}A/m^2 for 12.5 A and 25 A of current respectively. Measurements of the maximum copper current density limited by electromigration were presented in [220] and showed values of up to 8×10^{10}A/m^2. Exact values will have to be experimentally determined as they depend on the quality of the electroplated copper. Especially when using currents of 25 A the resistivity of the wires will have to be monitored constantly during the experiment to detect and prevent damage from electromigration to the wires.

6.4.6 Static Magnetic Field Strength and Gradient

To reduce the risk of electromigration damage a current of 12.5 A will be used for initial experiments. The corresponding magnetic field and magnitude of the gradients produced by this current were then derived.

The thinnest part of the current-carrying wire structure, shown in the inset of Fig. 6.14, is approximated as infinitely long wires with infinitely small diameter, allowing us to calculate the magnetic field and gradient analytically at the trapping position with,

$$B = \frac{\mu_0 I}{2\pi r} \tag{6.3}$$

where μ_0 is equal to the magnetic permeability in free space[13] and in our case r will be approximated as the distance between the centre of the wire structure and the trapping position. Other parts of the wire structure will not be considered for the calculation as the current flows parallel to the direction of the gradient produced by the thinnest wire section.

After initial development of the current-carrying wires we acquired the CST Studio suite FEM simulation tool, which allows us to numerically simulate the magnetic field and gradient produced by current-carrying wire structures. Magnetic field and gradient are

[13] metals used in the current-carrying wire and ion trap structure have a relative permeability of $\mu_r \sim 1$

plotted along the indicated red line, see Fig. 6.14, perpendicular to the thinnest wire section at a height of 85 μm above the centre of the copper tracks (assuming that the ion trap structure is no more than 10 μm thick and the ion is trapped 60 μm above the trap electrodes and that the copper tracks are 30 μm thick).

Eamon Standing simulated the magnetic field and gradient for the entire wire structure presented Fig. 6.14 and the results are plotted in Fig. 6.16 together with the analytically derived values for comparison.

The highest numerical gradient is equal to $\sim$ 155 T/m and the analytically derived gradient is $\sim$ 180 T/m. The difference of $\sim$16$\pm$20% is due to spikes in the numerical data and the fact that the numerically simulated structure varies greatly from the analytically approximate one.

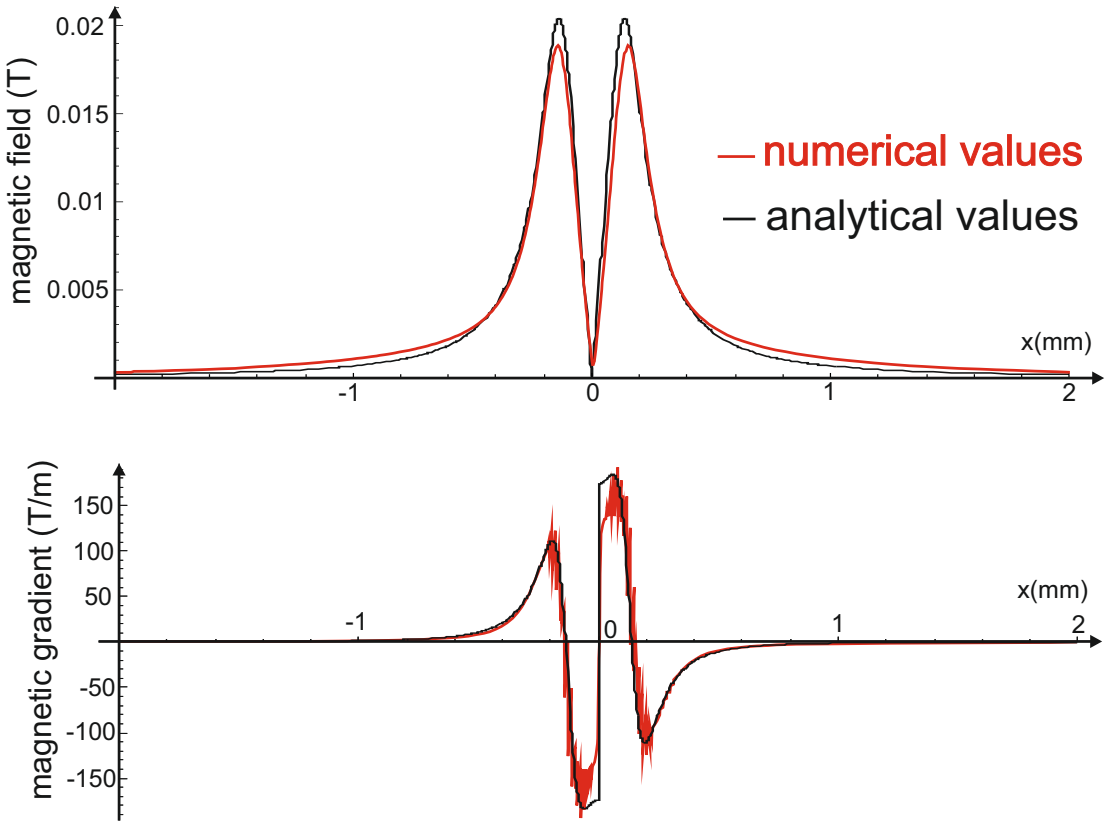


Figure 6.16: Comparison between gradients simulated by CST Studio suit FEM tool and analytically calculated for the wire structure presented in Fig. 6.14. A current of 12.5 is passed through both wire structures and the gradient is plotted for an ion height of 60 μm and along the red line shown in Fig. 6.14.

The analytical calculation produces results in a matter of second, while the numerical simulation can take hours. The analytical results are sufficiently accurate to optimize the

structure and were therefore used to optimize the width and separation of current-carrying wires for several different ion heights and ion trap structures. A linear ion trap design including the optimized wire structure will be presented in the next section. All ion trap designs with current-carrying wires can be found in App. D.

6.4.7 Conclusion

Assuming that a current of 12.5 A can be passed through the wire structures without causing thermal or electromigration damage, adjustable magnetic field gradients of > 150 T/m can be generated 60 μm above the ion trap electrodes based on the current-carrying wire design. Not only can the magnetic field be turned off and adjusted, it also provides much higher gradients than currently achievable in macroscopic ion traps with permanent magnets.

6.5 Trap Design for Current-Carrying Wire Structures

Current-carrying wires can be combined with any ion trap design, but will increase the rf electrode capacitance if large parts of the wire structures are placed underneath the rf electrodes. This will be the case if the gradient is generated in a radial direction of the pseudopotential and the wire structures are aligned parallel to the rf electrodes. The rf electrode capacitance can be increased by several picofarads, depending on the thickness of insulating layers and exact wire geometry.

A new linear ion trap geometry was therefore developed where the width of the rf rails is reduced and the inner dc electrode width increased, keeping the ion height constant. This design is also used for linear ion traps with loading and detection slots. Due to the large inner dc width the slots can be made wider, which is especially beneficial for traps with detection slots as it increases the collection angle of light passing through the slot.

Changing the rf electrode width will reduce the trap depth and cause a small rf barrier. Therefore the rf rail design was optimized and the normalized barrier was reduced to 0.6% of the trap depth as presented in Fig. 6.17. The barrier drops below 0.1% at the centre of the linear section, where the experiments will be performed. As the linear section will not be considered for adiabatic shuttling, the design was not optimized further.

The discussed linear trap design will be combined with current-carrying wire structures

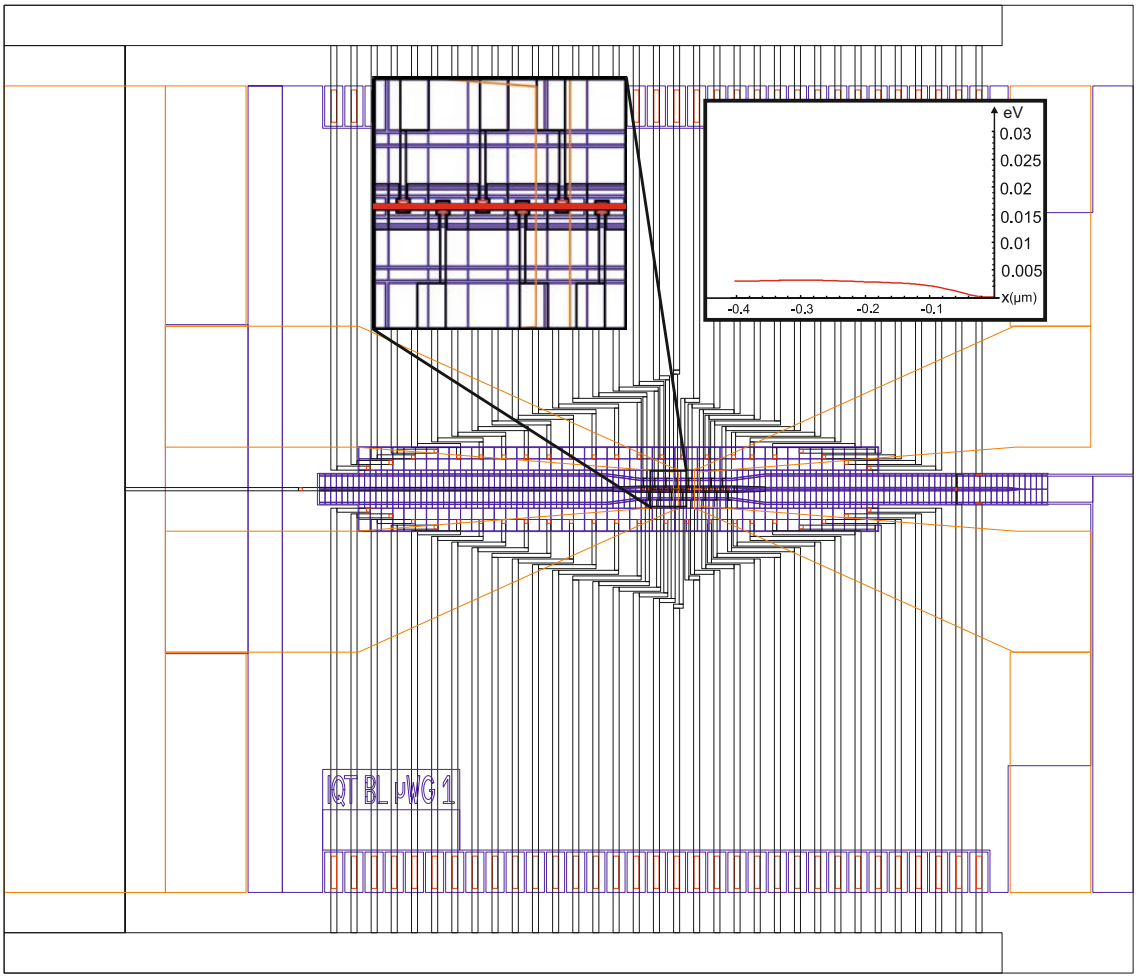


Figure 6.17: Linear ion trap section with narrowed rf electrodes to reduce the capacitance when current-carrying wires are placed underneath (electrode layer is blue, buried wire layer black and VIA layer red). Insets show magnified view of the centre of the trap and the normalized rf barrier along the red marked line at the rf nil positions.

and operated with an rf potential of 250 V and $\Omega = 2\pi \times 40$ MHz. For capacitance and resistance calculations a 300 μm thick diamond substrate was considered in combination with a 3 μm thick aluminium electrodes separated from the buried wires with a 2.5 μm thick SiO_2 layer. The copper wires underneath the trap structures are 60 μm wide when crossing the rf electrodes and the following trap characteristics were calculated.

Trap depth: 0.35 eV **Stability parameter** q**:** 0.39
Ion height: 58 μm
Radial secular Frequencies: 5.51 MHz in z direction and 5.26 MHz in y direction
RF electrode capacitance: 1.9 pF
RF electrode resistance: 1.7 Ω
Power dissipation: 9mW

6.6 Asymmetric Traps with Loading/Detection Zones and Disconnected RF Rails

Motivated by the scalable ion trap quantum system design presented in chapter 5 two linear ion trap designs were developed. One ion trap design is outfitted with a slot, placed in one of the centre segmented dc electrodes, which can be used for detection of light scattered from trapped ions or loading of ions from the backside of the chip. The second design is a linear ion trap consisting of electrically and physically disconnected rf rails, which are separated in x and y directions by 5 μm or 10 μm, respectively.

6.6.1 Loading and Detection Slot Designs

As discussed in the previous section, the rf rail width can be reduced and centre dc electrode width increased. This allows us to include a slot in the dc electrode design, which results in a larger detection angle. In addition to the barrier caused by the narrowing of the rf rails by placing a slot in one the dc electrodes will increase the barrier further. The slot geometry was therefore optimized and the normalized barrier could be suppressed to $\sim 1\%$ of the trap depth, shown in Fig. 6.18.

If the ion trap design is fabricated on an ultra-violet (UV) transparent substrate, like quartz glass, then light scattered by an ion trapped above the slot can be detected at

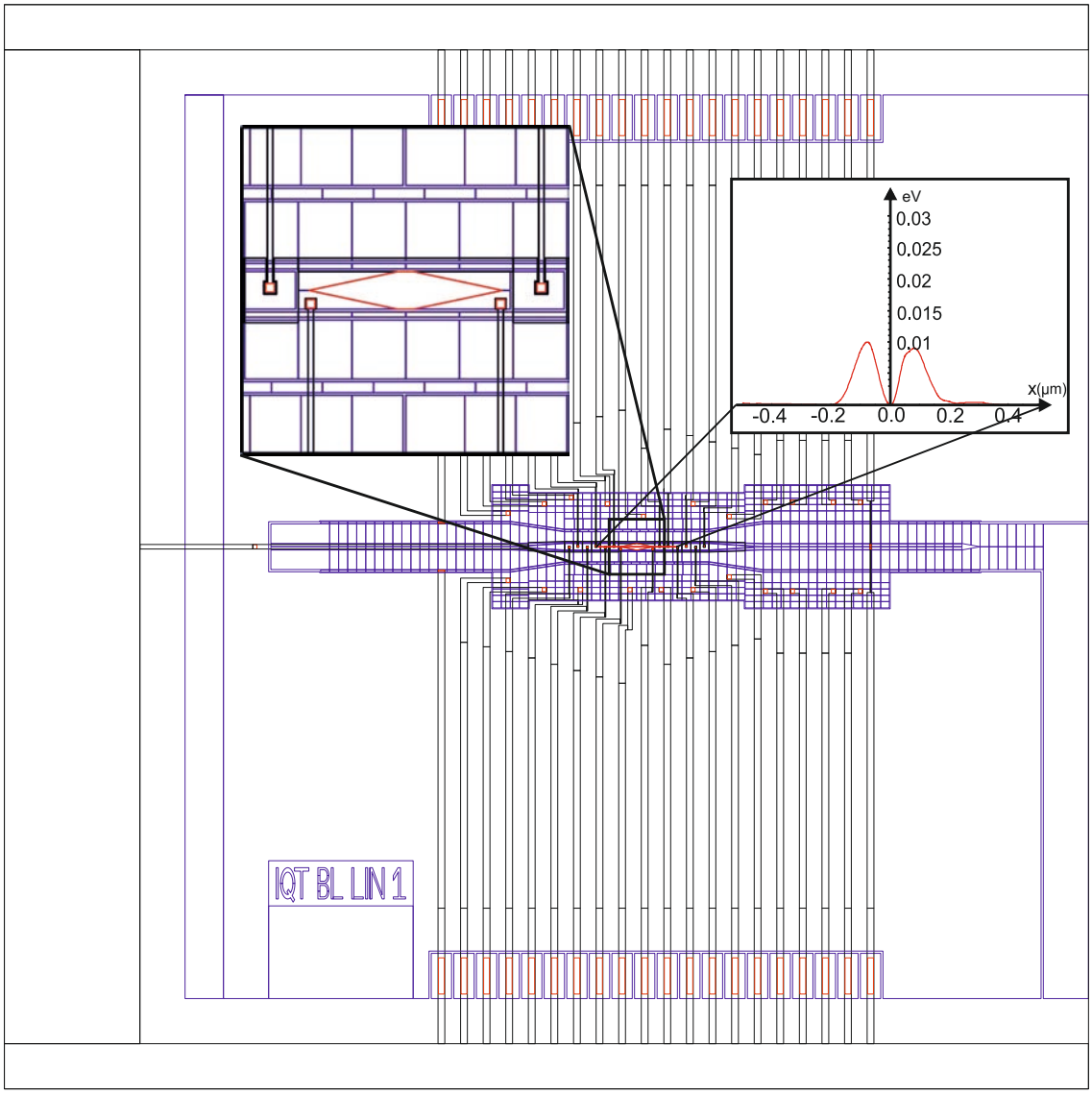


Figure 6.18: Linear Ion trap with detection slot for backside detection of scattered light from a trapped ion (electrode layer is blue, buried wire layer black and VIA layer red). The insets show the relevant dc electrodes and corresponding rf barrier.

the backside of the substrate. UV sensitive silicon avalanche diodes, similar to the devices presented in [211,212], can be attached to the back of the chips and used to detect photons without requiring any additional optics. Coating the exposed dielectric with a conductive UV transparent indium tin oxide (ITO) layer will prevent charge build up at the slot position.

If the design is intended for backside loading then the trap will be fabricated on an alumina substrate. A hole has to be machined into the substrate allowing the neutral atom flux passing through it and reaching the trapping zone. Alumina is very difficult to machine, which combined with the small hole diameter (~ 80 μm), will make laser drilling necessary.

Trap characteristics of a design for backside detection were derived for an rf potential with an amplitude of 400 V and frequency of $\Omega = 2\pi \times 30$ MHz. Assuming a 500 μm thick quartz substrate and otherwise the same trap structure, 3 μm thick aluminium electrodes and a 2.5 μm thick SiO_2 separation layer, trap parameters will be:

Trap depth: 0.31 eV **Stability parameter** q**:** 0.39
Ion height: 95 μm
Radial secular Frequencies: 4.10 MHz in the z-direction and 3.74 MHz in y-direction
RF electrode capacitance: 2.7 pF
RF electrode resistance: 1.5Ω
Power dissipation: 13 mW

6.6.2 Asymmetric Ion Trap with Separated RF Rails

Designing an ion trap with axially separated rf rail pairs can be used to experimentally demonstrate shuttling between two independent ion traps. Building a large scale ion trap system based on shuttling ions from one junction to a neighbour junction will require the shuttling between physically disconnected section as the ion traps have to be fabricated on many substrates.

The linear ion trap designs presented in Fig. 6.19 can be used to demonstrate adiabatic shuttling between rf rails separated by 5 μm and 10 μm in x and y directions respectively. In addition different rf potentials can be applied to the rf electrodes of the two sections. The traps can also be laser cut into two completely independent sections and aligned using piezo actuators in another experiment.

Due to the small size of the traps, two different designs were fitted on the same chip. Fig.

6.19 shows the two linear traps including the simulated barrier where the two separate rails are joined.

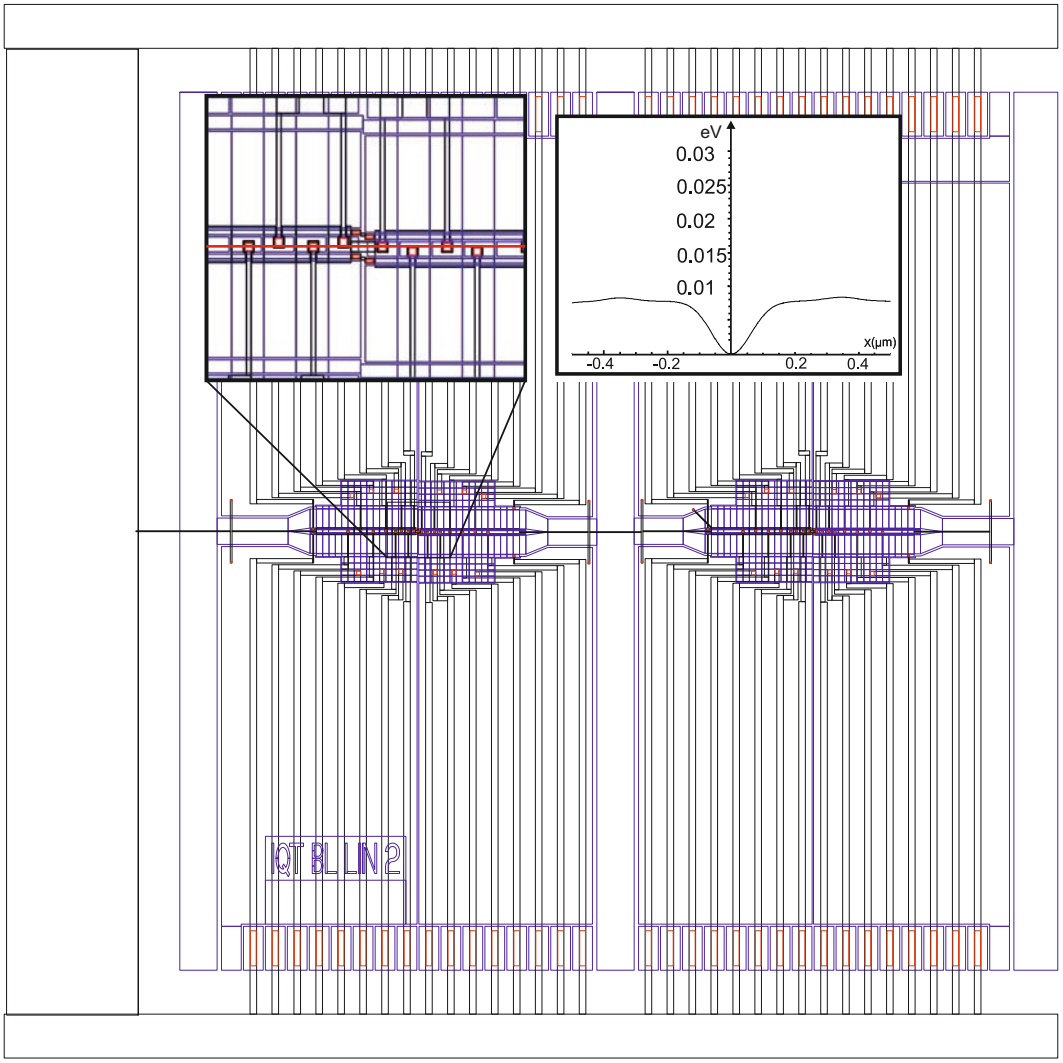


Figure 6.19: Showing the two ion trap designs intended for investigations of shuttling through separated and shifted rf rails (electrode layer is blue, buried wire layer black and VIA layer red). Insets show a magnified view of rf rails (left inset) and rf barrier at ion height when shuttling from one section to the other (right inset).

Applying an rf potential with an amplitude of 400 V and frequency of $\Omega = 2\pi \times 30$ MHz to one of the trap sections, placed on a 500 μm thick alumina substrate will results in the following trapping parameters:

Trap depth: 0.58 eV **Stability parameter** q**:** 0.39

Ion height: 101 μm

Radial secular frequencies: 4.13 MHz in z direction and 4.07 MHz in y direction

RF electrode capacitance: 2.33 pF

RF electrode resistance: 0.8 Ω

Power dissipation: 24 mW

6.7 Complete Mask Layout

In addition to the ion trap designs presented in this chapter, linear sections, junctions and 2D arrays were developed for various tasks. For the microfabrication at the Southampton Nanofabrication Centre a 6" diameter write field [14] mask was used and all of the developed 16 ion trap designs are placed four times on the mask. One quarter of the mask for the first three layers ('Electrode', 'VIA' and 'Buried Wire' layer) is shown in Fig. 6.20 and a summary for each trap design is given in the following sections. Additionally all mask designs, including the current-carrying wire layer, are shown in more detail in App. D.

Ion Trap Design 1

Trap Description: Linear ion trap
Approximate Ion Height: 250 μm
Number of DC Electrodes: 56
Substrate Material: Alumina
Design: Linear ion trap without CCWs. Large amount of dc electrodes allows for precise control of long chains of ions in the trap. The large ion height makes this the design with lowest expected heating rate.

Ion Trap Design 2

Trap Description: Linear ion trap with loading slot
Approximate Ion Height: 165 μm
Number of DC Electrodes: 34
Substrate Material: Alumina
Design: Linear ion trap fabricated with a loading slot placed in one of the dc electrodes. The neutral atom flux can be generated at the back of the trap and sent through a laser cut hole in the substrate to the loading zone.

Ion Trap Design 3

Trap Description: Linear ion trap with detection slot
Approximate Ion Height: 100 μm
Number of DC Electrodes: 36
Substrate Material: Quartz
Design: Linear ion trap fabricated on quartz substrate, with a detection slot replacing

[14] write field represents the part of the mask occupied by the designed structures

one of the centre dc electrodes. Scattered light from the ion can reach the back of the substrate, where a photo detector is placed. This design is described in more detail in section 6.6.1

Ion Trap Design 4

Trap Description: Linear ion trap with current-carrying wires and loading slot.
Approximate Ion Height: 170 μm
Number of DC Electrodes: 34
Substrate Material: Diamond
Design: Linear ion trap with CCWs and additional detection slot, otherwise similar to design 13.

Ion Trap Design 5

Trap Description: X-junction ion trap
Approximate Ion Height: 100 μm
Number of DC Electrodes: 88
Substrate Material: Alumina
Design: X-junction trap with optimized geometry and ion height of 100 μm. Trap design is intended for the demonstration of adiabatic shuttling.

Ion Trap Design 6

Trap Description: X-junction ion trap
Approximate Ion Height: 200 μm
Number of DC Electrodes: 88
Substrate Material: Alumina
Design: X-junction trap intended for initial shuttling experiments, design is presented in section 6.3.5.

Ion Trap Design 7

Trap Description: Linear ion trap with current-carrying wires
Approximate Ion Height: 120 μm
Number of DC Electrodes: 34
Substrate Material: Diamond
Design: Linear ion trap combined with CCWs, replaces design 12 if microfabrication of buried wires and VIAs is reliable.

Ion Trap Design 8

Trap Description: Linear ion trap with current-carrying wires and coplanar waveguide (CPW)
Approximate Ion Height: 60 μm
Number of DC Electrodes: 18
Substrate Material: Diamond
Design: This design was modified and placed on another mask. It is now being fabricated in a different cleanroom and will not be used for the fabrication described in this thesis.

Ion Trap Design 9

Trap Description: X-junction ion trap with current-carrying wires
Approximate Ion Height: 100 μm
Number of DC Electrodes: 72
Substrate Material: Diamond
Design: X-junction ion trap CCWs intended for advanced microwave quantum gate experiments, where several ions can be entangled in consecutive gate operations.

Ion Trap Design 10

Trap Description: Linear ion trap with current-carrying wires
Approximate Ion Height: 60 μm
Number of DC Electrodes: 66
Substrate Material: Diamond
Design: Linear ion trap including CCWs with the lowest ion height and largest expected gradients. The design is discussed in section 6.5

Ion Trap Design 11

Trap Description: Ion trap array
Approximate Ion Height: 100 μm
Number of DC Electrodes: 54
Substrate Material: Alumina
Design: Optimized 3×3 ion trap array intended for initial testing of the array design at higher ion height of 100 μm and rf nil separation of 184 μm.

Ion Trap Design 12

Trap Description: Linear trap with current-carrying wires
Approximate Ion Height: 120 μm
Number of DC Electrodes: 30
Substrate Material: Diamond
Design: Linear ion trap combined with CCWs without buried wires, intended for initial

experiments with CCW. Will be fabricate if the yield of the microfabrication is low.

Ion Trap Design 13

Trap Description: Linear ion trap with current-carrying wires
Approximate Ion Height: 170 μm
Number of DC Electrodes: 34
Substrate Material: Diamond
Design: Linear ion trap combined with CCWs, the ion height of 170 μm makes it suitable for experiments where low heating rates are important.

Ion Trap Design 14

Trap Description: Two linear ion traps with separated rf rails
Approximate Ion Height: 100 μm
Number of DC Electrodes: 2×36
Substrate Material: Alumina
Design: Linear ion trap sections with disconnected rf rails intended to demonstrate shuttling between physically and electrically separated rf rails, as discussed in section 6.6.2. In the left linear trap rf rails are separated by 10 μm in both x and y directions in the right trap by 5 μm in both directions.

Ion Trap Design 15

Trap Description: Ion trap array
Approximate Ion Height: 50 μm
Number of DC Electrodes: 54
Substrate Material: Alumina
Design: Optimized 3×3 ion trap array with 50 μm ion height and 87 μm separation between rf nils.

Ion Trap Design 16

Trap Description: Ion trap array
Approximate Ion Height: 30 μm
Number of DC Electrodes: 55
Substrate Material: Alumina
Design: Optimized 5×5 ion trap array based on the example case presented in [101].

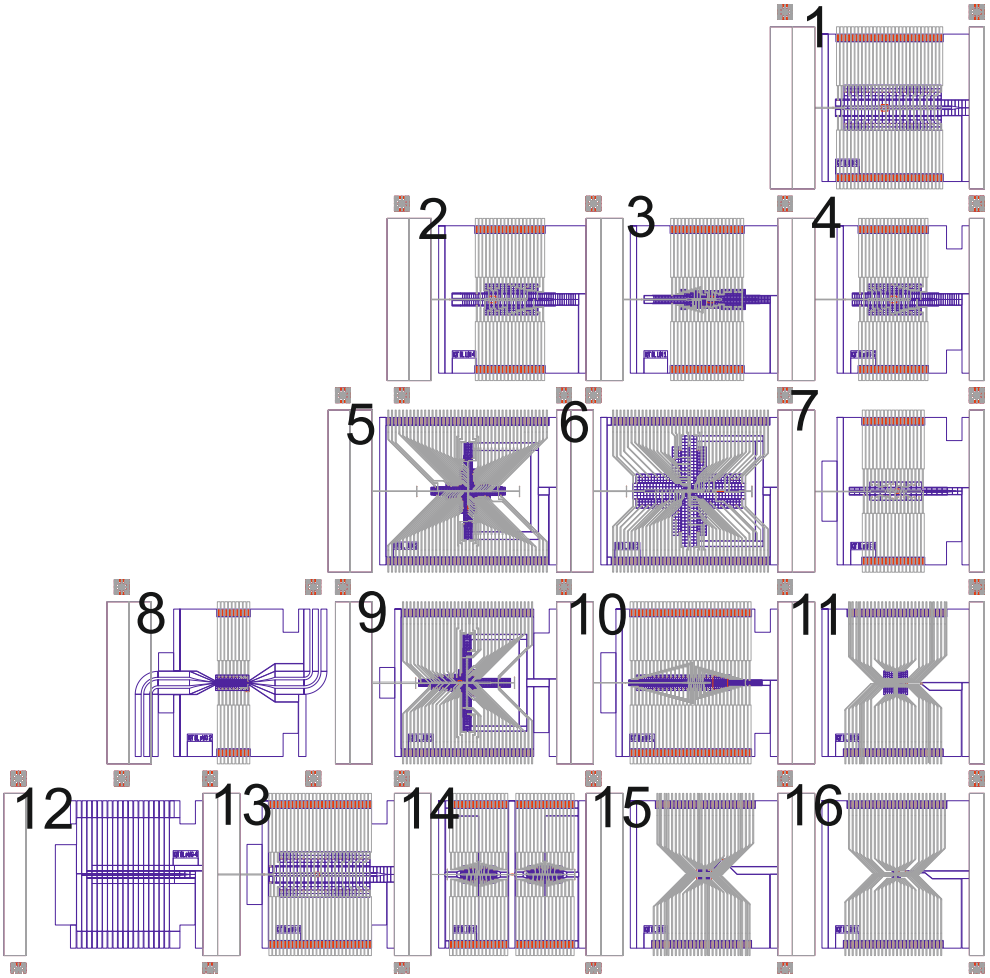


Figure 6.20: Picture of all ion trap designs and corresponding 'Electrode' (blue), 'VIA' (red) and 'Buried Wire' (black) layers placed in a quarter of the 6" diameter write field mask. Additionally alignment marks are placed around the individual designs, allowing the individual layers to be aligned with each other.

Chapter 7

Vacuum Chamber Modifications and Voltage Control System

Stable operation of ion traps with current-carrying wires (CCW) described in section 6.4 requires that the dissipated heat is efficiently removed from the ion trap chip. A novel thermal bridge system was therefore developed that is compatible with the vacuum system described in section 3.3.1 and also provides the possibility to cool the ion trap below room temperature.

Recent findings showed that an *in situ* clean of ion trap electrodes can dramatically reduce the heating rate by several orders of magnitude [86, 87]. Based on these results we decided to add a high voltage ion source to one of our vacuum systems, which required the development of a custom flange and redesign of the imaging window.

In addition a novel multichannel high speed voltage control system was designed that can be used for trapping and shuttling of ions. The system is based on low-noise components and can generate high speed, high voltage, arbitrary waveforms ideal for these tasks.

7.1 Thermal Transport System

Ion traps with current wires will generate up to 20 W of heat, which if not efficiently removed will heat up the ion traps and increase electromigration in the CCW and ultimately reduce the amount of current that can be applied to the wire structures. It will also increase the temperature of the trap electrodes and thereby the heating rate in the trap, as discussed in section 4.3.2. Individual temperature gradients of wire sections, dis-

cussed in section 6.4 will not be considered further here, as the heat spread perpendicular to the transport direction will lead to an even distribution of the heat dissipated by all wire sections. We will assume that the heat is dissipated over the entire chip area.

7.1.1 Chip Holder

Instead of placing the ion trap chip on the 2 mm thick alumina chip carrier cavity plate, which has a low thermal conductivity of $T_c \sim 28\ W/(m \cdot K)$) and would require a second solder attachment at the back, slots are laser cut into the chip carrier, as illustrated in Fig. 7.1. The ion chip is directly soldered onto a custom designed gold plated copper chip holder, shown in Fig. 7.2. The laser cutting of the chip carrier was done by Laser Cutting Ceramics Ltd.

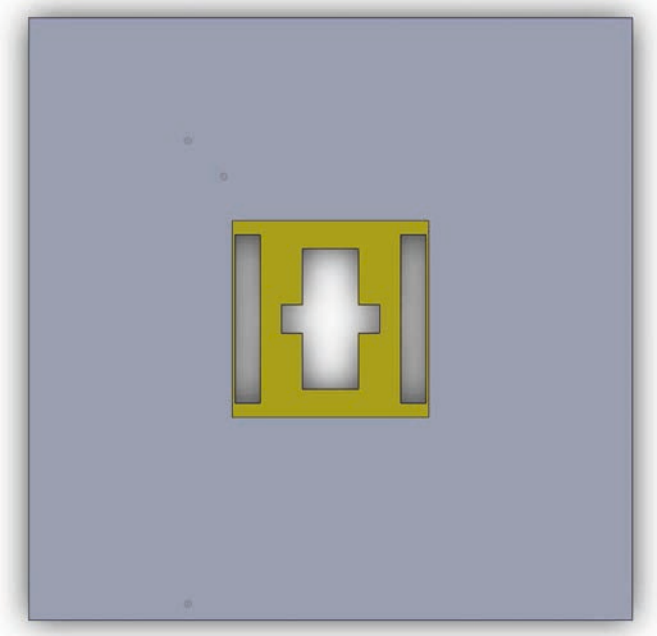


Figure 7.1: Picture showing the modified chip carrier, slots are laser cut into the central cavity plate.

The 23 mm long copper chip holder, which is designed to fit through the centre slot of the chip carrier, was fabricated by our workshop according to the drawings shown in App. C. After fabrication the surface of the copper holder is polished and electroplated with 2 μm of nickel and 200 nm of gold by CIR Electroplating.

The backside of the microfabricated ion traps will be coated with a $\sim$ 150 nm thick gold layer, which makes it possible to solder them directly onto the chip holder using $10 \times 10\ mm^2$ large and 25 μm thick gold-tin (80Au20Sn) solder sheets from Indium Corporation.

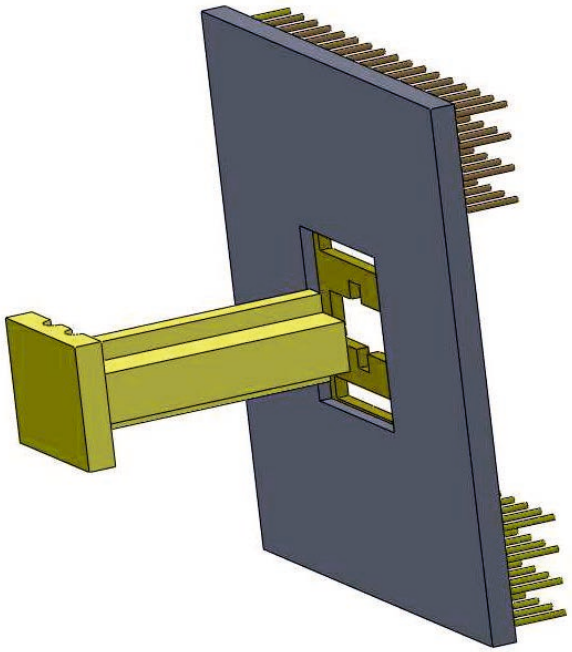


Figure 7.2: Gold platted copper chip holder and chip carrier with laser cut slots. The main part of chip holder is designed to fit through the slot. Ion traps are soldered onto the polished front plate, which is placed on top of the remaining chip carrier plate structure.

The sheet is placed between ion trap chip and chip holder and heated on a hot plate in an inert argon atmosphere to >280°C for a minimum of 4 min soldering the chip to the chip holder. If necessary a small weight can be placed on the chip to improve the solder process. The argon atmosphere protects the heated chip surface from contamination and enhances the solder process. The 25 μm thick solder layer will be able to compensate thermal expansion mismatches between ion trap chip and chip holder[1].

The ion chip soldered onto the copper holder is compatible with the standard baking procedure of the vacuum system at 200°C, as outlined in section 3.3.

7.1.2 Thermal Bridge and Current Supply Structures

To transport the heat from the chip holder to the outside, without changing the current vacuum system design, a thermal bridge was designed to fit through the chip bracket cavity illustrated in Fig. 7.3. The thermal bridge consists of two independent copper parts, shown in Fig. 7.4, which are pressed against the chip holder and each other using two 4 mm diameter screws, providing a good thermal contact. Four threaded screw holes

[1]Information provided by Indium Corporation

are used to attach the thermal bridge to a custom copper adapter using Allen head screws that can be tightened from side windows of the vacuum.

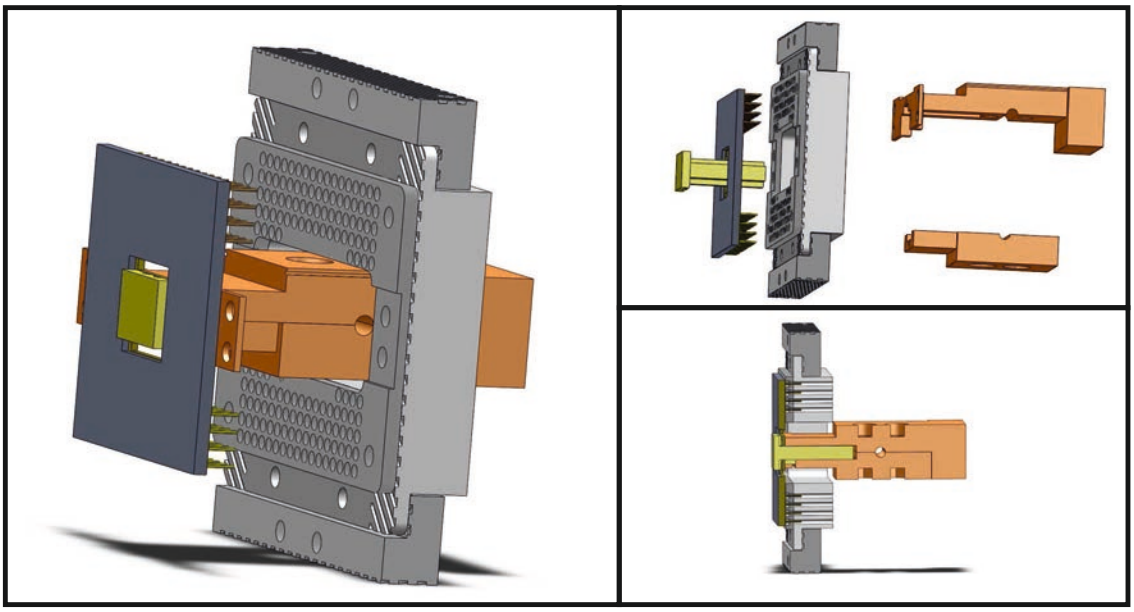


Figure 7.3: Showing the chip carrier and copper chip holder attached to the thermal bridge. The chip bracket of the vacuum system is included to illustrate the size of the thermal bridge with respect to the chip bracket cavity. Exploded and cutaway views demonstrate how the individual parts are assembled.

The centre 4 mm hole machined into both parts of the thermal bridge, see Fig. 7.4, is used to clamp four current supply structures onto the side of the heat transport system. The current supply structures, shown in Fig. 7.4, are made of copper and electroplated with 2 μm of nickel and 200 nm of gold as well. Peek spacers are used to the separate the four current delivery structures on each side, which are also placed on a 1 mm thick ceramic BNP2 plate. BNP2 is a machinable aluminium nitride ceramic with a high thermal conductivity of $T_c \sim 92$ W/$(m \cdot K)$[2] acquired from Ceramic Substrates and Components Ltd [3]. The BNP2 plates help transport heat dissipated in the current supply structures to the main transport system. The structures are designed to fit through the additional slots cut into the chip carrier and can be fixed in place using PEEK clamps. Current feedthroughs are placed on a 2 3/4" flange of the vacuum system and connected to the current supply structures using ceramic bead insulated copper wires crimped to a silver plated high current receptacle (PN 09 33 000 6204 AWG 16 receptacle, suitable for >15A of current), which fits onto the pin of the current supply structures.

Connections between current supply structures and current-carrying wire pads on the ion

[2]Value for T_c provided by Ceramic Substrates and Components Ltd
[3]http://www.ceramic-substrates.co.uk/

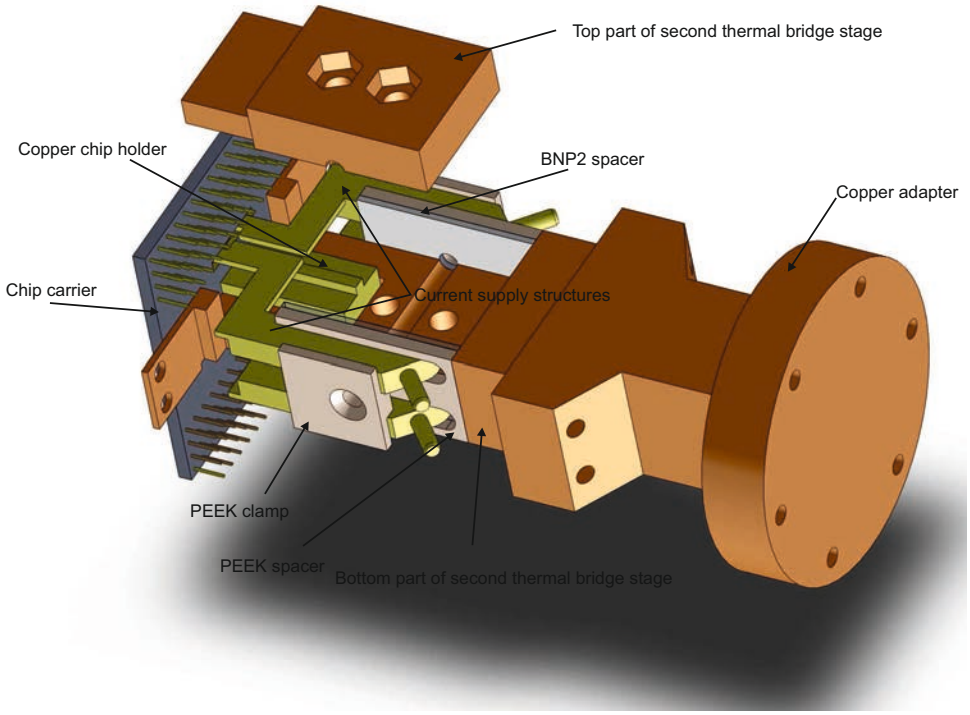


Figure 7.4: Assembled thermal bridge, including chip carrier, chip holder, both parts of the thermal bridge, current supply structure and corresponding mounts and copper adapter.

trap will be made using several gold ribbon bonds (125×25 μm). Five ribbons are expected to withstand a minimum of 20 A of current. Current supply structure and current bond pads on the chip are large enough to place more than 10 ribbon bonds if required.

The complete thermal bridge can be fully assembled outside the vacuum system and pushed through the chip bracket together with the chip holder and chip carrier afterwards. Fig. 7.5 shows a picture of the assembled thermal bridge attached to the copper adapter and mounted to the chip bracket.

7.1.3 Copper Adapters and custom Steel-Copper Flange

The copper adapters will be attached to a custom copper-steel flange at the back of the vacuum chamber, see Fig. 7.6. The custom flange is supplied by Allectra GmbH and is made up of a steel blank flange into which thick-walled copper tube is welded in. The thick-walled copper tube has a large copper plate welded to the end facing into the vacuum system, where the copper adapter can be screwed on. A short 4 1/2" stainless steel extension, shown in Fig. 7.6, thermally isolates the 4 1/2" steel-copper custom flange from the main vacuum chamber. Stainless steel[4] has a low thermal conductivity of

[4] 304 stainless steel

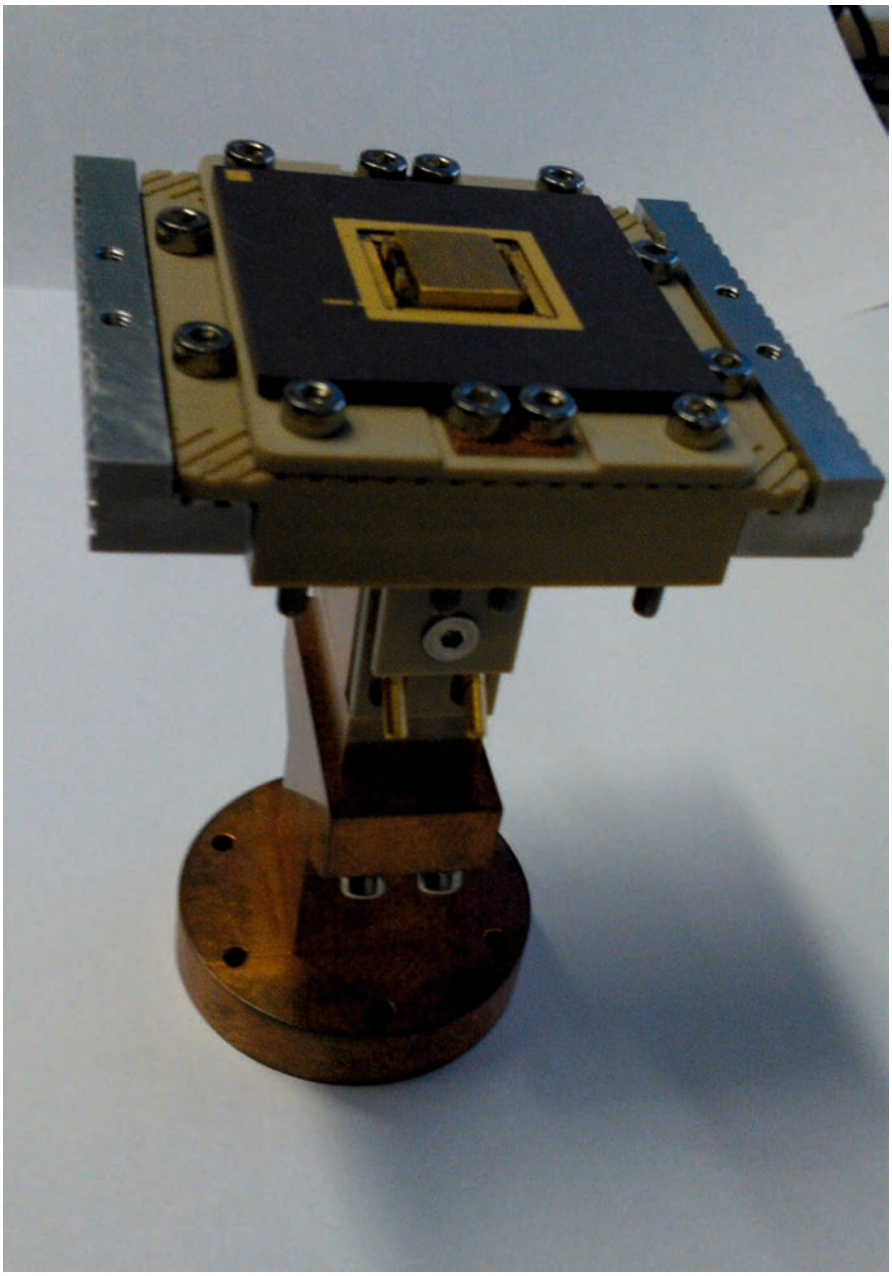


Figure 7.5: Picture of the assembled thermal bridge, chip bracket and copper adapter. Used stainless steel screws are not cut to the correct length yet.

$T_c \sim 16$ W/$(m \cdot K)$ [219] and combined with the thin walled tube (1.65 mm wall thickness) will thermally isolate the copper flange from the rest of the system.

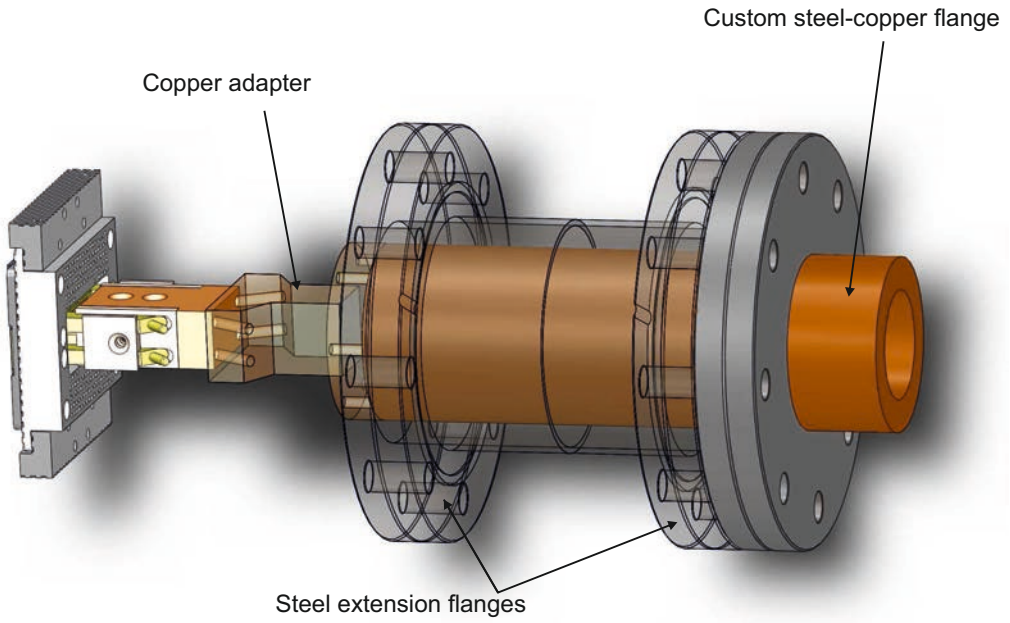


Figure 7.6: Showing the entire thermal bridge, copper adapter, steel-copper flange and steel extension flanges.

Under normal operation the thick-walled copper tube will provide a thermal conduction from the copper adapter to the outside of the vacuum system. A heat sink can be mounted on the part of the thick-walled copper tube, which is outside the vacuum system for further cooling. The thermal gradient between copper chip holder and the end of the thick-walled copper tube of the custom flange was derived to be approximately ΔT=2 K/W. Main contributors are the chip holder with ΔT$\sim$0.8 K/W and the thermal bridge stage with ΔT$\sim$0.6 K/W, other parts of the system have a much larger cross section and therefore much lower ΔT.

In addition we hope that by filling the copper tube with liquid nitrogen using an angled flange we will be able to cool the ion trap chip below 0°C. The liquid nitrogen will cool the heat transport system while slowly evaporating. A continuous flow of liquid nitrogen will not be required. The stainless steel extension separating the steel-copper flange from the vacuum system will be heated on the side attached to the main chamber to prevent condensation on the vacuum system. This cooling design is not fully scalable and is

intended for experiments towards the highest possible gate fidelities.

Fig. 7.7 shows a picture of the thermal bridge attached to the custom flange and an ion source attached to the system, which will be discussed in section 7.2.

7.1.4 Conclusion

A novel UHV compatible thermal transport system was designed that can be used to remove the heat dissipated in ion traps with current-carrying wires with a modest temperature gradient of 2 K/W. The thermal transport system also provides the possibility to cool any ion trap below 0°C, when filled with liquid nitrogen.

Drawings for all parts manufactured in our workshop can be found in App. C.

7.2 Plasma Source for *in situ* Ion Trap Cleaning

In recent experiments it was demonstrated that *in situ* cleaning of ion trap electrodes with a high energy argon plasma beam (2 kV in [86]) can result in a reduction of the heating rate by several orders of magnitude [86, 87].

Bombarding the ion traps electrodes with an argon beam can lead to implantation of argon atoms and surface contaminants into the surface and generally increase the surface roughness. Commonly after an argon plasma clean is performed the surface will be annealed at temperature > 300°C which is not possible for ion traps. To reduce the argon implantation and surface damage we decided to reduce the angle between argon beam and surface to a minimum where we can still achieve a sufficient cleaning effect [221]. This will help reduce the discussed issues and also less material of the trap electrodes will be milled away.

Following the work presented in [222] on the removal of adsorbents on a surface we decided that an angle of $\sim 15°$ between the sputter beam and surface will provide sufficient cleaning of our ion trap electrodes. By using a side window of the vacuum system, see Fig. 7.7 to mount the sputter gun with a custom flange an angle between beam and surface of 14° can be achieved. To achieve a higher angle we would have to completely redesign the vacuum chamber.

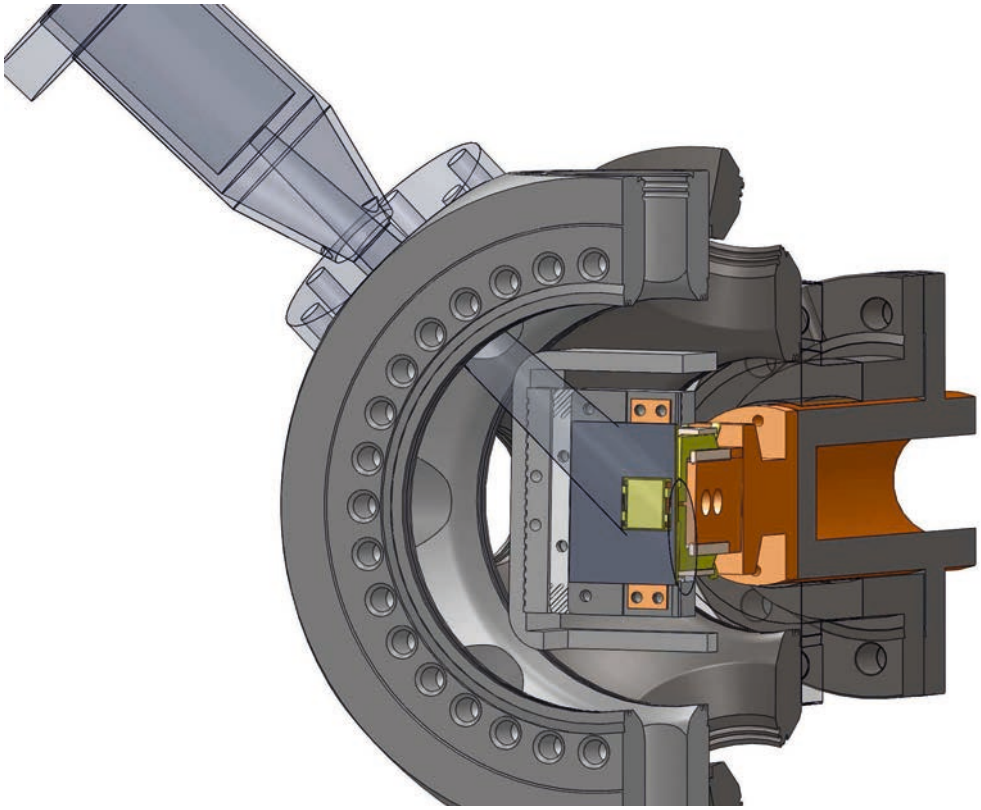


Figure 7.7: Cutaway view of the vacuum system, custom flange, ion beam (transparent conus) and thermal transport system.

7.2.1 Ion Source

After investigating several possible ion sources we acquired the IQE 11/35 from SPECS GmbH. The ion source is very compact (63.5 mm long, diameter of ∼30 mm inside the vacuum), has a high acceleration voltage 5 kV, and is compatible with reactive gases, which will allow us to perform a lower energy oxygen plasma etch clean in addition to an argon sputter clean. A digital controller (PU IQE 11/35 digital power supply, by SPECS GmbH) supplies the required high voltage and the gas flow is manually regulated using a high precision leak valve (Model 1000, Brechtel manufacturing Inc.)

7.2.2 Custom Flange

A custom flange, shown in Fig. 7.9, had to be designed to attach the plasma source to the chamber and allow the ion beam to enter the system through one of the side 2 3/4" flanges. The flange houses the 63.5 mm long ∼30 mm diameter ion source and is then conically reduced to fit onto the 2 3/4" flange at the discussed 14° angle. A small fraction of the ion beam (FWHM diameter of the beam is ∼5 mm when exiting the flange) will hit the

sidewalls of the conical flange and material of flange will be sputtered off and potentially redeposited on the ion trap electrodes. To prevent contamination of the electrode surfaces with steel, all exposed parts of the flange are gold coated with a 2 μm thick layer by CIR Electroplating.

In addition to the custom flange the recessed imaging window of the vacuum system presented in section 3.7 was redesigned to make sure the plasma beam is not obstructed on the way to the trap. A drawing of the new window can be found in App. C.

7.2.3 Operation

When performing an *in situ* clean of an ion trap chip, argon or oxygen gas is let into the vacuum system. To keep a stable pressure and to remove the gas from the chamber after cleaning the turbomolecular pump discussed in section 3.3 is attached to the system. The digital controller is connected to the high voltage feedthroughs of the ion source, shown in Fig. 7.8. Next, an argon or oxygen gas cylinder is attached to the leak valve via a flexible stainless steel tube (PN SS-FJ4RF4RF4-40, Swagelok). The stainless steel tube is evacuated using the turbomolecular pump and can also be baked to remove residual water. Afterwards, the gas line is filled with either argon for physical sputtering or oxygen to perform a dry etch clean of the surface. Then, the leak valve is slowly opened until the pressure in the vacuum chamber, monitored using an ion gauge, reaches $\sim 10^{-7}$ Torr. To start the plasma cleaning the ion source voltage is turned on, for argon based cleaning a voltage on the order of 2 kV [86] will be used, for oxygen dry etch cleans different voltages will be tested.

7.3 Voltage Control System

Trapping and especially shuttling of ions require a highly advanced multichannel high-speed voltage control system, that can supply low-noise arbitrary waveforms with update rates on the order of MHz and voltages of up to $\pm$100 V. Such a voltage control system was used to shuttle ions though a T-junction described in [78].

Before the development of our system started we compiled a list of minimal requirements

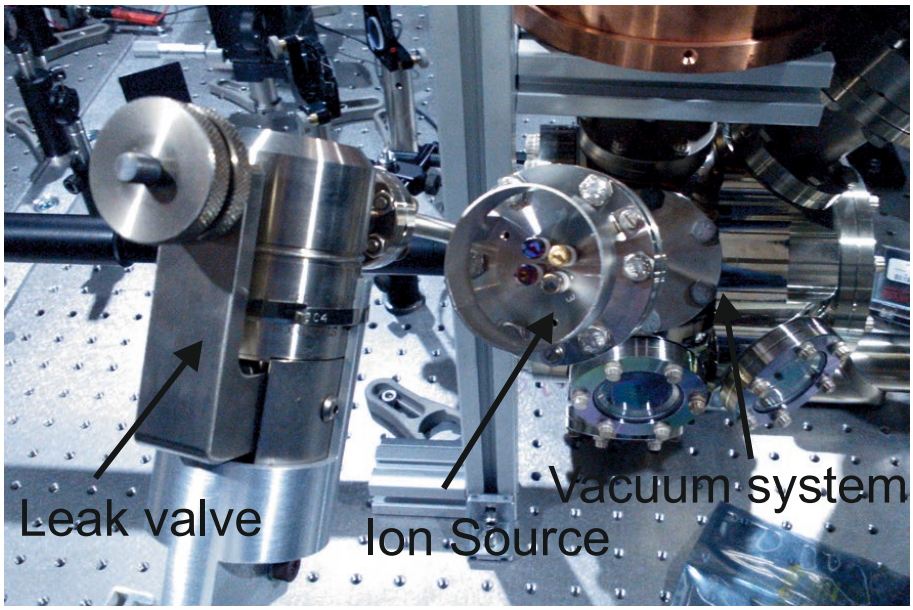


Figure 7.8: Picture of ion source and leak valve attached to a vacuum system. Gas line and high voltage connections are not attached in this picture.

on the system based on prior shuttling experiments and future ion trap designs in our group. The digital-to-analogue converter (DAC) of the system will have to have at least 16 bit and an update rate of >>1 mega sample per second (1 MSPS equals to a voltages update rate of 1 MHz). Output voltage span of the system has to be $\sim \pm 100\ V$, and it has to have on the order of 88 channels and the best possible noise performance.

7.3.1 Digital-to-Analogue Converters

The essential part of any voltage control system is the DAC, which determines the bit rate and update rate and has a strong impact on the noise performance. The type of DAC also determines in which format the digital information of the waveforms has to be supplied. Two different types of DACs are commercially available, which differ greatly in update rate and format of the digital data. Serial DACs require one data channel per DAC, the data bits are supplied to the DAC one at a time, where they are transferred to a circuit latch[5] by a supplied clock signal. After 16 bits are clocked into the latch a second clock transfers the data to the output stage of the DAC and the voltage is changed. Commonly serial DACs with update rates of up to 3 MSPS are commercially available.

Parallel DACs clock in all required 16 bits at the same time supplied by 16 digital data channels and update the output voltage with every clock cycle. Parallel DACs are com-

[5]Simple transistor based memory

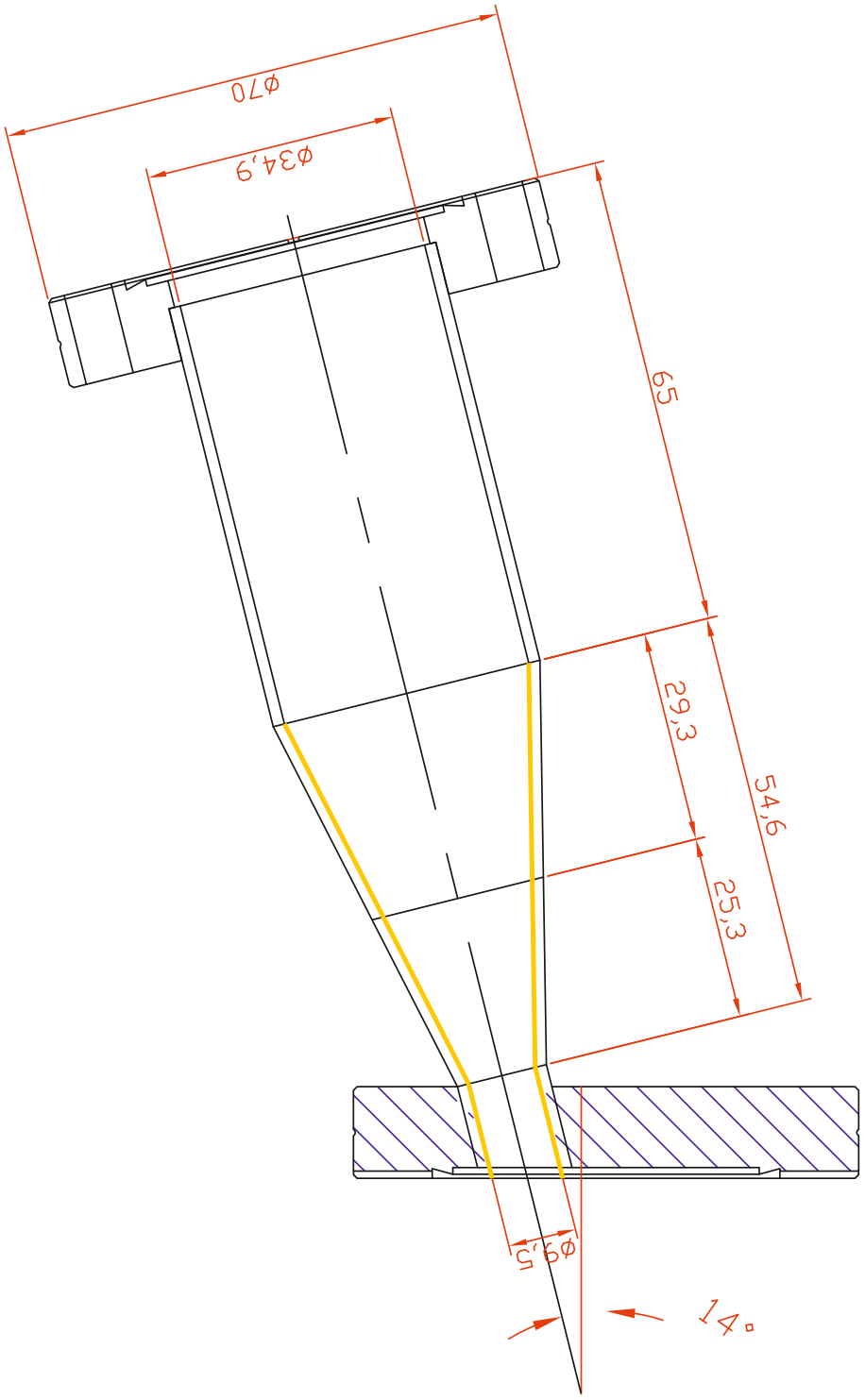


Figure 7.9: Custom designed flange used to attach the ion source to the vacuum system. Gold coated parts of the flange are marked yellow.

monly used if update rates on the order of fifty to several thousand MSPS are required. The Parallel DACs require data to be sent on 16 digital channels at rate of $\sim 20-50$ MHz, which equals to >56 gigabytes of data per second for a 90 channel system updated at a rate of 20 MSPS. Voltage control systems making use of these DACs [223, 224] make use of large numbers of field programable gate arrays (FPGA) which supply the required data for limited amount of waveforms. When the system is triggered a short outburst of data is sent to the parallel DACs until the memory of the FPGA is depleted.

Using FPGAs to supply the digital data to DACs in our 90 channel system would limit the length of arbitrary wave functions and require on the order of 45 FPGAs, which all have to be connected to a control computer via a universal serial bus (USB) connection. This would dramatically complicate our 90 channel system, limit its speed when outputting many different arbitrary waveforms and make it more susceptible to system errors due to the very large number of USB connections.

Serial DACs put less constraint on the digital data supply and can be connected to commercially available Digital I/O cards (for example M2I.7011-EXP from Spectrum GmbH), which can provide enough digital data for 30 DACs. Most serial DACs are limited to 3 MSPS, which is sufficient for shuttling operations in our traps [98], but leads to additional switching noise at a frequency of 3 MHz. The noise can dramatically increase the heating rate in the ion trap, when on resonance with a secular frequency of the trap, see section 2.2.2.

7.3.2 Voltage Generation and Active Filtering

Digital-to-Analogue Converter

One serial DAC was found that operates at an update rate of 16 MSPS by using a unique digital interpolation filter built into the DAC (PN DAC8580, by Texas Instruments) and was chosen for this system. Data bits are supplied at a rate of 16 MHz by three 32-channel M2I.7011-EXP digital I/O cards (by Spectrum GmbH) to a total of 90 DACs, which results in an interpolated update rate of 16 MSPS. The interpolation filters will also help smoothing out the arbitrary waveforms used for shuttling.

The 16 bit DAC can output ± 5 V with an update rate of 16 MSPS, has a more than sufficient slew rate[6] of 35 V/μs and a low output noise of 25 nV/$\sqrt{Hz}$ at 10 kHz and

[6] Slew rate defines the maximum voltage change the DAC can output in the give time span

20 nV/$\sqrt{Hz}$ at 100 kHz[7]. The DAC has three digital inputs, one for the waveform data, one for the latch clock and an additional clock controlling the voltage update.

Each of the digital data lines is galvanically isolated from the inputs of the DAC and the voltage grounds of the system using high speed optical isolators (PN HCPL-0723, by Avago Technologies) to reduce noise pick-up from the digital data supply lines.

Voltage Reference

A reference voltage V_{REF} has to be supplied to the DAC, which will determine the maximum output voltage span ($\pm V_{REF}$). The ADR443B V_{REF} =3 V voltage reference (by Analogue Devices) is designed for extremely low noise (1.4 μV peak-peak) applications and has a high initial voltage accuracy of (1 mV)[8]. Each DAC has its own voltage reference and the voltage reference output is also heavily filtered with a 33 μF capacitor.

Active Filter

To reduce the switching noise of the DAC at 16 MHz an active operational amplifier based low-pass filter with a cut-off at 500 kHz is placed after the DAC voltage output. The filter circuit consists of a low input noise (1 nV/$\sqrt{Hz}$ at 100 kHz)[9] operational amplifier (PN ADA 4899, by Analogue Devices), two 220 Ω resistors, a 2.2 μF and 680 pF capacitor.

Bypass Capacitors and Resistors

In addition to the discussed components three bypass capacitors (4.7 μF, 100 nF and 1 nF) are placed close to all voltage supply pins, to reduce high frequency noise entering the components. All bypass capacitors are either high quality ceramic (C0G dielectric) or tantalum capacitors, which exhibit the lowest possible impedance for the noise to ground. Three different capacitor values were chosen to efficiently remove a larger frequency bandwidth of noise, capacitors with lower values commonly have a lower impedance for noise at higher frequency.

All resistors used for the voltage control system are wirewound high power resistors, which induce the lowest noise [225] and the resistance value is largely unaffect by the power dissipated in the resistor.

[7] http://www.ti.com/lit/ds/symlink/dac8580.pdf
[8] http://www.analog.com/static/imported-files/data_sheets/ADR440_441_443_444_445.pdf
[9] http://www.analog.com/static/imported-files/data_sheets/ADA4899-1.pdf

7.3.3 Printed Circuit Boards

All components used to generate and filter the waveforms are placed in one section of a six layer printed circuit board fabricated by Rush PCB Inc, shown in Fig. 7.10.

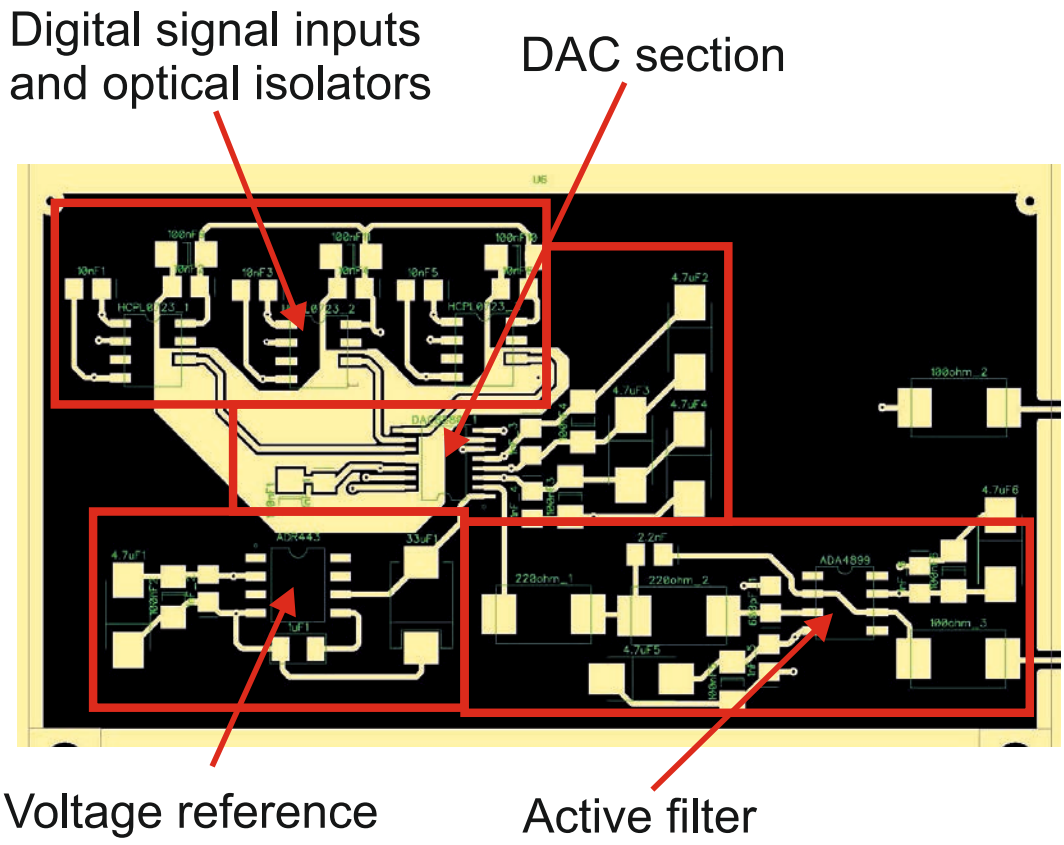


Figure 7.10: Voltage generation and active filter section for one channel.

The section shown in Fig. 7.10 has a small digital ground plate on the top layer (layer 1) covering the optical-isolators and digital input pins of the DAC. An analogue ground plate (layer 2) is placed directly underneath the top layer and the wide copper tracks surrounding the section on the top layer are also connected to analogue ground. These tracks will be electrically connected to nickel plated copper plates placed around each section for electromagnetic interference (EMI) shielding. On top of the plates a tin plated copper clad steel (TCS) wire mesh is placed that allows fan cooling of the components and also provides EMI shielding.

A second digital ground plate (layer 5) shields the analogue supply tracks (layer 3) and digital control lines (layer 4) from noise on digital data supply lines (layer 6) placed on the back of the six layer printed circuit board (PCB).

7.3.4 Voltage Amplification

In addition a voltage amplification section, which is placed on the same PCBs and shown in Fig. 7.11 is used to increase the voltage output span to ±9 V and ±90 V. By changing the amplifier circuits the output voltage spans can also be adjusted if required. A variable two-stage amplification was chosen to increase the voltage accuracy and reduce the noise on voltages below ±9 V.

The voltage amplification section has its own analogue ground plates preventing potential noise on the ground of the voltage generation section to the reach the amplifiers.

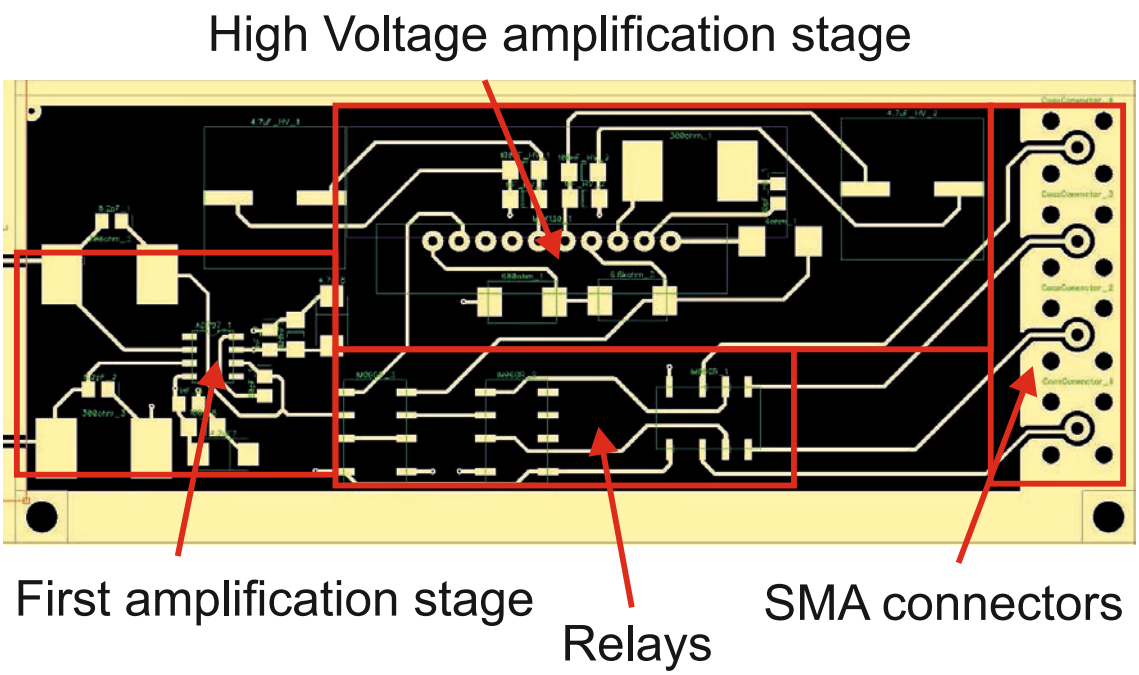


Figure 7.11: Amplification section of one channel including relays and SMA connectors.

First Amplification Stage

The main voltage amplification stage is made up of an ultra low input noise (0.9 nV/$\sqrt{Hz}$ at 1 kHz)[10] operational amplifier (PN AD797, by Analogue Devices) in a differential amplification circuit. A differential amplification circuit was chosen to reduce noise on the voltage generated in the first section of the system. Two 100 Ω and two 300 Ω resistors result in a voltage amplification of a factor of ∼ 3 and a maximum output voltage of ±9 V. Bypass capacitors identical to the ones used in the voltage generation section are placed at the analogue supply pins.

[10] http://www.analog.com/static/imported-files/data_sheets/AD797.pdf

High Voltage Amplification Stage

The amplified voltage can then be distributed to four different output SMA connectors via telecommunication relays (PN IM06GR, by TE connectivity) or send to a second voltage amplification stage if voltages above ±9 V are required. The second amplification stage consists of a MSK130 (by MS Kennedy) high slew rate (300 V/μS), high voltage (±195) and low input noise (∼5 nV/$\sqrt{Hz}$ at 100 kHz)[11] voltage amplifier. Special bypass capacitors compatible with the high voltages are used. One 680 Ω and 6.8 $k\Omega$ wirewound resistor in a non-inverting amplification circuit result in a voltage amplification by a factor of 10, increasing the maximum output voltage span to ±90 V.

The voltage amplification section is also equipped with EMI shielding plates and a mesh. The large MSK130 operational amplifier is placed on the backside of the PCB and a large aluminium heat sink (PN SK 04/50 SA, Fischer Elektronik) is screwed to the back of it for cooling.

7.3.5 Voltage Supplies

For the voltage generation and first amplification stage ±5 V and ±15 V voltages are supplied by two linear voltage supplies (HCC5-6/OVP-AG by Power-One, for ±5 V and 32212D by Calex Electronics Limited for ±15 V). Two SM120-13(by Delta Electronika) switched-mode power supplies are used to supply 120 V to the high voltage amplification stage. Switched-mode power supplies inherently have more high frequency noise than linear power supplies due to their working principle (a transistor constantly switches the maximum supply voltage on and off, at a frequency on the order of $\sim 100 - 1000$ kHz, output voltages are rectified by capacitors). Linear power supplies that can output the same voltage and current will be much larger and heavier and were financially not viable.

7.3.6 Testing of the Voltage Control System

After initial tests on single and two layer PCBs a design was made for the final six layer PCBs holding nine of the discussed generation and amplification sections on a 424×200 mm PCB. Tracks on the top layer and tracks on the backside of the PCB are impedance matched with the underlying ground plates. The multilayered PCB was then fabricated by Rush PCB Inc according to our design submitted as gerber files.

[11] http://www.mskennedy.com/products/Amplifiers/MSK130.prod

Components on one channel of a nine channel board were then assembled, see Fig. 7.12 (a) and the system was tested using one M2I.7011-EXP digital I/O card. The card is placed in a computer system with an Intel Xeon server motherboard (PN X9SCM-F, by Supermicro). The data output of the card is controlled via a LabView program. The two clock signals and digital data required by the DAC is supplied by the card and connected to the 9-channel voltage control test board using a very-high-density cable interconnect (VHDCI) 50Ω cable.

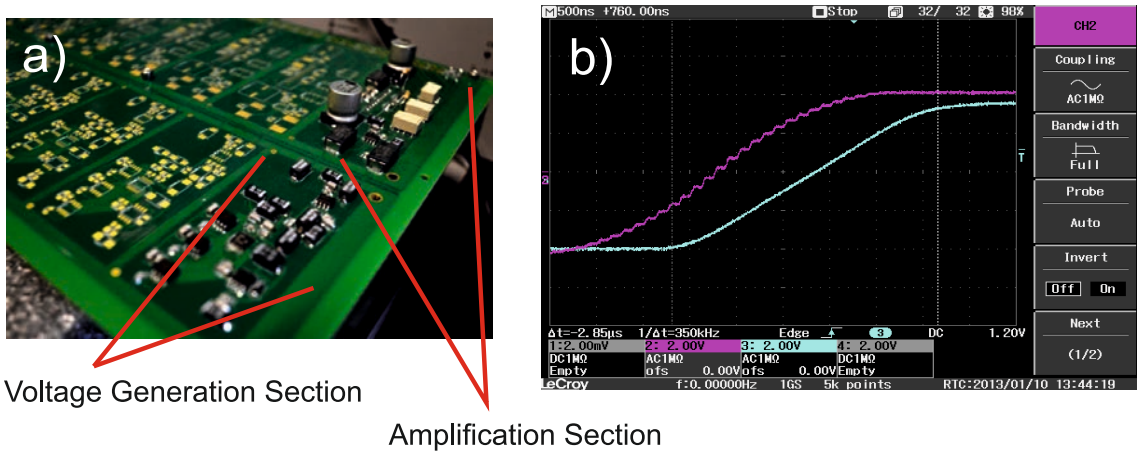


Figure 7.12: (a) Picture of the PCB with components assembled for one channel. (b) Waveform generated by the voltage control system, measured before (pink) and after the active filter (light blue).

Initial test were successful and a waveform generated by the system is shown before and after the active filtering circuit in Fig. 7.12 (b).

A preliminary noise measurement of the generated voltages was performed using a HP8562E spectrum analyser. Characterisation of the spectrum analyzer showed that at frequencies below 100 kHz an applied voltage amplitude was measured very inaccurately. After performing a crude calibration of the analyzer the output noise of the voltage control system was approximated for a static voltage output of 5 V. At 1 MHz the measured noise was on the order of 65 nV/$\sqrt{Hz}$, at 100 kHz we measured 190 nV/$\sqrt{Hz}$ and 230 nV/$\sqrt{Hz}$ at 10 kHz. A more detailed noise analysis will be performed after a 9-channel PCB is fully assembled and a suitable spectrum analyzer acquired.

7.3.7 Conclusion

A novel voltage control system was designed satisfying the goals outlined at the start of the development. The system is based on low-noise components, capable of producing

high-voltage, high-speed, arbitrary waveforms for 90 channels. Depending on the control computer used, several seconds or up to hours of completely arbitrary waveforms can be generated.

Chapter 8

Microfabrication of Ion Traps

The fabrication of ion trap designs that incorporate current-carrying wires (CCW) embedded in a diamond substrate requires the development of a highly advanced and versatile microfabrication process, based on the concepts described in section 4.5.6. Initial design and optimization of the process steps were supported by Ibrahim Sari and the fabrication was performed at the Southampton Nanofabrication Centre.

Several of the ion trap designs discussed in chapter 6 can be fabricated without current-carrying wires, and were fabricated on alumina (Al_2O_3) substrates. To minimize the process complexity, traps with and without CCW share most of the process steps. The first part of the process includes all of the steps required to fabricate copper tracks embedded in a diamond substrate. Advanced microfabricated ion trap structures including buried wires, shielding of exposed dielectrics and vertical interconnect access (VIA) for isolated electrodes are fabricated on top of the copper tracks based on the second part of the process.

Individual process steps of both processes will be briefly outlined first and then each step will be discussed in detail.

8.1 Process Overview

8.1.1 Current-Carrying Wire Structures

The first part of the microfabrication process used to create CCW embedded in diamond substrates is illustrated in Fig. 8.1. First the diamond substrates are cleaned from any

organic contaminates (a), followed by the deposition of a 4 μm silicon dioxide (SiO_2) layer (b), which will be used to create a hard mask. The SiO_2 is structured making use of a photoresist mask (c) and a dry etch. The hard mask (d) is then used to etch $\sim$30 μm deep trenches into the diamond substrates (e) with an oxygen plasma. Trenches are filled using a deposited copper seed layer (f) and a copper electroplating step (g), creating the current carrying wires. The uneven copper structures on the diamond substrate are afterwards polished by an external company leaving a flat surface with embedded copper tracks (h).

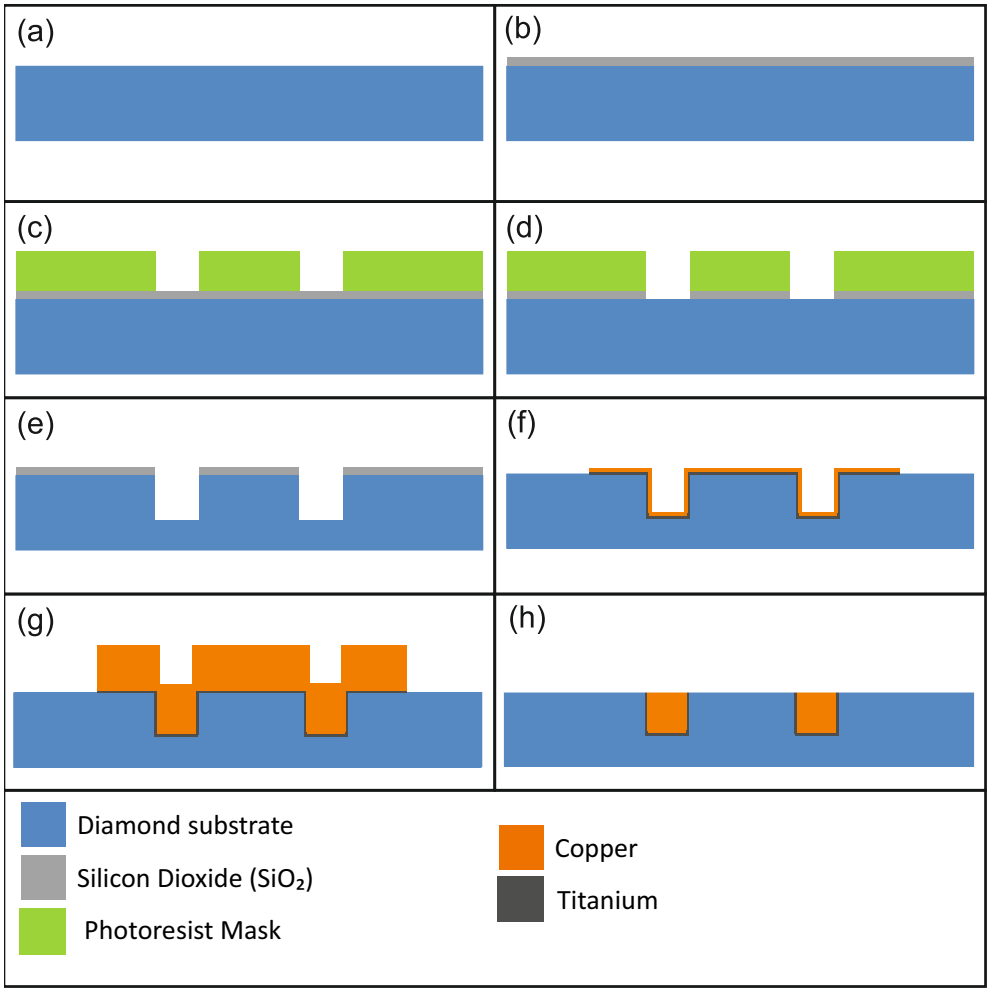


Figure 8.1: Schematic of the process used to fabricate current-carrying wires. (a) Wafers are cleaned first (a) followed by the deposition of SiO_2 layer (b), which is then structured using a photoresist mask (c) and a SiO_2 etch (d). The structured SiO_2 serves as a hard mask for the diamond dry etch (e). A seed layer is deposited (f) and used to electroplate copper into the trenches (g). The entire structure is then polished down to the level of the diamond substrate (h).

8.1.2 Ion Trap Structures

After the diamond substrates are polished a silicon dioxide (SiO_2) layer is deposited to prevent the underlying copper from diffusing out of the structures and contaminating the fabrication tools. To electrically isolate buried wires from the copper tracks and to increase the maximum breakdown voltage between rf electrodes and ground, an additional silicon nitride (Si_3N_4) layer is deposited. For traps without CCW, alumina substrates are cleaned and then a Si_3N_4 layer is deposited as well. Process steps are now identical for both substrate types as outlined in Fig. 8.2 and will be described next.

After the substrates were cleaned (a) and an insulating Si_3N_4 layer was deposited (b), the buried wire structures are created. The wires are used to connect isolated dc electrodes to bond pads and are fabricate in a lift-off step. First a negative photoresist mask is created (c), followed by an aluminium (Al) deposition step (d). After deposition, the substrates are placed in a solvent, which lifts off the resist mask from the substrate including metal deposited on top of it (e). The Al wires are buried underneath a SiO_2 layer in a PECVD process step (f) and vertical interconnect access (VIA) holes are etched into the SiO_2 layer (h) using a structured photoresist mask (g). Another photoresist mask is created (i) and aluminium (Al), chromium (Cr), nickel (Ni) and gold (Au) are deposited to form the electrodes (j). After a lift-off step is performed (k) the exposed SiO_2 located between electrodes is removed in a wet etch process (l), that also forms an undercut in the SiO_2 layer. Ion trap chips are soldered onto a heat sink, which requires the backside of the chips to have a gold metallization. Therefore a titanium (Ti) adhesion and gold (Au) contact layer is deposited onto the backside of the substrates. Lastly the individual chips have to be diced out of the larger substrate pieces, which is done by an external company using a laser cutter.

8.2 Fabrication of CCW Structures

Fabricating CCW structures embedded in a diamond substrate requires a completely novel fabrication process including the development of new process steps. The process steps will be discussed in detail in the following section, exact process parameters used for deposition and etch steps are summarized in App. B.

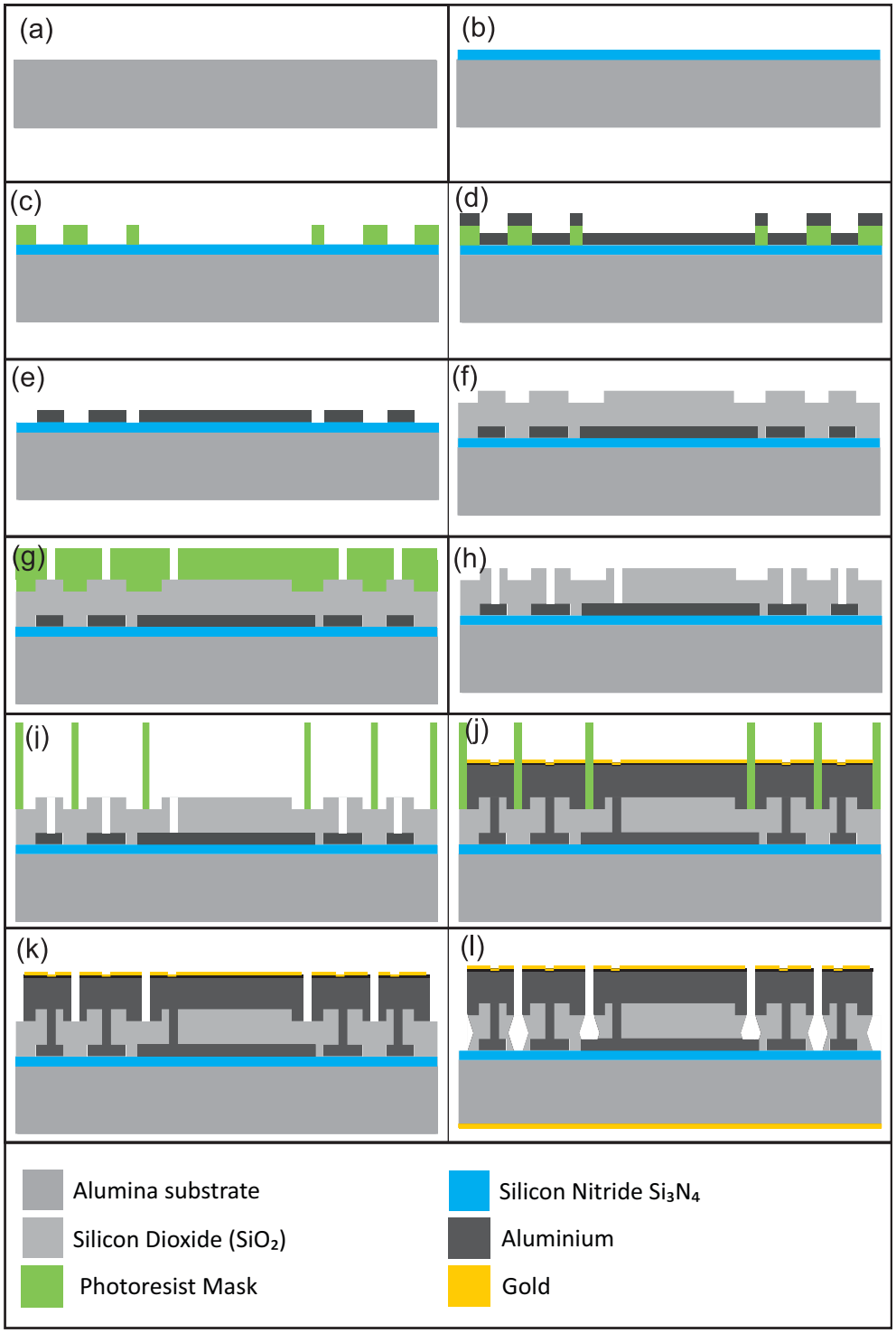


Figure 8.2: Fabrication of ion trap structures is illustrated for alumina based traps. The substrates are cleaned (a) and an insulating Si_3N_4 layer is deposited (b). Next a negative resist photo mask is created (c), followed by an Al deposition (d) and lift-off (e). Aluminium structures are buried underneath a SiO_2 layer (f) and holes are etched into this layer (g) using another photoresist mask (h) to create VIAs. Electrodes are fabricated on top of the SiO_2 layer, starting with a photoresist mask (i) followed by the deposition of Al, Cr, Ni and Au (j) and another lift-off process (k). Lastly exposed SiO_2 is etched away in an isotropic wet etch and a Ti and Au layer is deposited on the backside (l).

8.2.1 Substrate Preparation

During the design process of the CCW ion traps, it became clear that only diamond substrates would be suitable to prevent the copper tracks from melting. Prior ion trap experiments performed in our setup also showed that even traps with low power dissipation can heat up substantially if thermally isolated from the vacuum system. Therefore ion trap designs without CCWs are fabricated on alumina, which has a much higher thermal conductivity (Tc $\sim$ 20 W/m K) than quartz (Tc$\sim$ 3 W/m K).

Thermal grade diamond substrates, with a Tc of $>$ 1800 W/m K[1], at 300 °C, were acquired from Mintres b.v. The polymorph substrates are large enough (13×13 m^2) to hold one ion trap. Substrates are 300 μm thick and polished to a roughness average (RA) of $<$ 50 nm on the front side and to RA$<$ 250 nm on the back.

Alumina wafers (99.6% Al_2O_3) were acquired from Valley Design Corp. with a diameter of 150 mm, 500 μm thick and polished on one side to an RA of $<$ 50 nm. A total of 64 traps can be fabricated on a wafer of this size, unfortunately the wafers started to warp before fabrication started, which made it impossible to spin on photoresist or perform many other steps. This was most likely caused by the low thickness of the 150 mm wafer, which was chosen to allow easier machining of loading slots and dicing of the wafers. Also the material might not have been sintered perfectly, introducing stress and ultimately warping them. Dicing the wafers into smaller 32x32 mm^2 pieces solved this problem and was performed by Kian Shen Kiang using a Loadpoint Microace 3 dicing saw and diamond coated resin blades.

8.2.2 Substrate Cleaning

Before the microfabrication can start, substrates have to be thoroughly cleaned to remove organic contaminants on the surfaces. Especially when using the substrates in a PECVD process, where the wafers reach $>$350 °C, surfaces have to be extremely clean to avoid contaminating the tool. In the Southampton cleanroom wet etch cleans are preferred over solvent based cleaning processes.

Diamond substrates are chemically extremely inert and no extra precautions are necessary when performing a wet etch based cleaning. Alumina wafers will be attacked by hydrofluoric acid (HF), which is used for the standard semiconductor wet cleaning process

[1] Tc is expected to be even higher at liquid nitrogen temperatures [226]

RCA[2] and also dissolve in dilute nitric acid. It will not be attacked by highly concentrated fuming nitric acid (FNA) with a concentration > 90 %, which is also commonly used to wet etch clean wafers. FNA is an extremely strong oxidizer and very efficient in removing organic contaminates including developed photoresist.

Wet Etch Clean

Substrate pieces are placed in an acid proof plastic basket and dipped into a large tank ($\sim$ 60 l) with FNA for 10 min. Afterwards the acid has to be safely and thoroughly removed from the samples, which is done in a quick dump rinse (QDR) tank. Samples are placed with the basket inside the tank and a cleaning cycle is started. First deionized (DI) water is finely sprayed into the tank from several nozzles until the tank is full, followed by a quick dump of the entire water. This cycle is repeated twice and during the final third step water is sprayed into the tank until it overflows for $\sim$ 30 sec, then the water is dumped.

Wafer pieces are taken out of the QDR and blow dried with ultra pure nitrogen and placed in a transport box.

In addition, the substrates are cleaned in a 'PVA TePla 300' plasma asher using an oxygen plasma. The process is called ashing as it turns the organic contaminants into ash, which is removed by the vacuum. The exact process parameters are summarized in App. B.1. Diamond substrates were only ashed for 2 min as the process slowly attacks the diamond surface, Al_2O_3 substrates were ashed for 10 min. The microwave oxygen plasma strongly etches organic contaminates and is used directly prior to the following process.

When preparing diamond substrates for a deposition step, the oxygen ash is also used to break up and remove the hydrogen termination of the diamond surface [227]. Diamond grown in a chemical vapour deposition (CVD) process, which was used for the substrates described in this thesis, will always have a hydrogen terminated surface due to the hydrogen gas used in the growth process. Hydrogen terminated diamond surfaces can show reduced adhesion of photoresist, metals and dielectrics deposited [228–230].

[2] RCA stands for Radio Corporation of America, where the clean was developed by Werner Kern

8.2.3 Deposition of SiO_2 Hard Mask

After diamond substrates were cleaned and the hydrogen termination was removed the fabrication can start. As illustrated in Fig. 8.1 (e), etching deep trenches into diamond requires a hard mask, which is resilient against the dry etch. The diamond dry etch is oxygen based and will therefore not chemically attack SiO_2, only the sputter effect of the etch will mill away the mask.

Deposition

An 'OIPT SYS100' PECVD reactor was used for the mask deposition, shown in Fig. 8.1 (b). The reactor is configured for wafer and not chip level fabrication. Diamond pieces were therefore placed on a 6" Silicon (Si) carrier wafer and shuttled into the main chamber. An additional 2 min *in situ* plasma clean is performed using the plasma generator of the tool igniting a nitrous oxide (N_2O) plasma, exact process parameters are described in App. B.2. The deposition process is based on the reaction of silane (SiH_4) gas with nitrous oxide (N_2O) in a nitrogen diluted plasma. Silane and nitrous oxide are highly reactive and the dilution is required to achieve a stable and even deposition on the sample surface. With the deposition parameters presented in App. B.2 $\sim 4\mu$m of SiO_2 were deposited in 61 min.

Thickness Measurement

Thickness of a deposited transparent layer can be measured using the 'Woollam M2000D NIR' ellipsometer. This tool is capable of determining thicknesses of individual transparent layers in a multilayered structure. Polarized light of a broad spectrum (193-1700 nm) source is reflected by the sample layers and changes of the polarization of the reflected beams are recorded for different wavelengths. The ellipsometer then determines a Psi (Ψ) and Delta parameter (Δ), which are related to the reflected polarized light according to $e^{i\Delta}\tan\Psi = \frac{r_p}{r_s}$, where r_p is the amount of reflected p-polarized light and r_s is that of the s-polarized light. In Fig. 8.3 Psi and Delta are plotted vs the wavelengths.

With the analysis program 'CompleteEase' a model corresponding to the layer structure can be created and used to fit the plot of Psi and Delta. Data points are fitted by varying the thicknesses of the deposited layers. Fig. 8.3 shows the measured Psi and Delta for

the deposited layer fitted with the model of a $\sim$ 4 μm thick SiO_2 layer deposited on a diamond substrate.

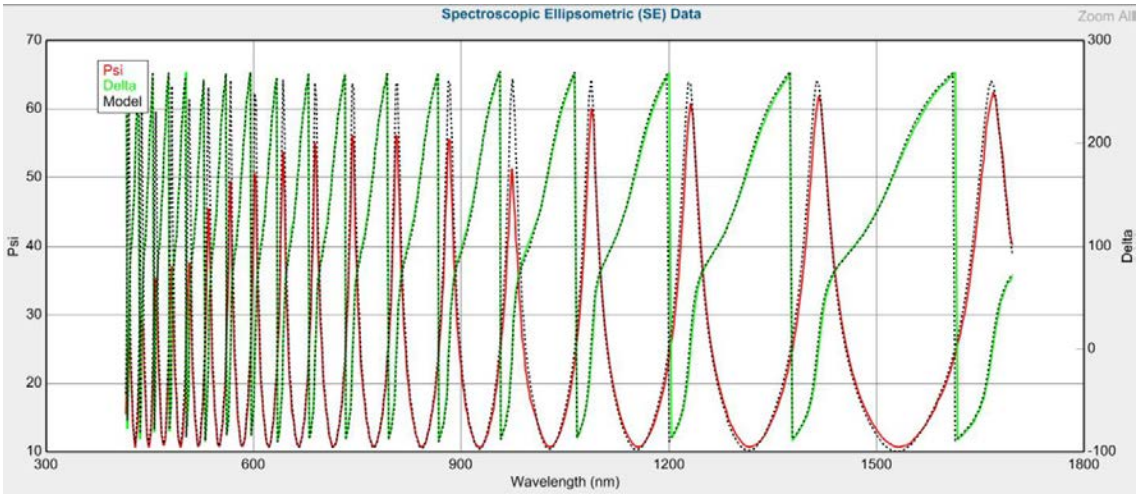


Figure 8.3: Graph showing the measured Psi (red) and Delta (green) parameter vs wavelength and a model of the layer structure fitted to the data (dashed).

8.2.4 Photoresist Mask to Structure the Hard Mask

To transfer the patterns of the photo mask, manufactured by Compugraphics Intl. Ltd onto the SiO_2 we need to perform a photolithography step, illustrated in Fig. 8.1 (c). Depending on the required polarity and thickness, different resists can be chosen. All masks were designed for negative resist, which is essential for reliable lift-off processes and due to its very high thermal stability also suitable for dry etches. For the structuring of the SiO_2 layer the resist should be at least 4 μm thick. Thinner resist can be completely etched away before patterns are etched through the entire SiO_2 layer.

Resist Coating

Before the resist was spun on, substrates are prepared by a 5 min oxygen plasma ash in the 'PVA Tepla 300' and a dehydration step is performed in an oven at 120 °C, for at least 30 min. Dehydration of the samples is important to achieve a good adhesion between resist and sample surface.

A 'Brewer Science CEE 200 Series' spin coater is used to apply $\sim$4 μm of 'AZ nLOF 2070' negative resist from MicroChemicals GmbH with a very high rotation speed of 6,000 rpm. Using rotation speeds above 4,000 rpm helps in reducing the edge bead effect described in section 4.4.1. The exact spin coating profile is outlined in App. B.3.

After successfully spinning on the resist, remaining solvents are removed during a soft-bake on a 'Sawatec HP-401-Z' hotplate at 110 °C for 2 min. The substrate pieces are now ready for the mask alignment and exposure step.

Resist Exposure

Mask aligners have a micrometer stage, that allows the alignment of the photo mask with the substrate pieces and are also equipped with a mercury (Hg) vapour lamp for exposure. Three different aligners were used during the fabrication of the ion traps, the 'EVG6200' automatic mask aligner, used in manual mode, and the two manual aligners 'EVG620T' and 'EVG620TB'[3]. All aligners are used in the same mode, manual front side alignment, with 6" masks and a 6" carrier wafer. Masks are pressed against the sample and no additional vacuum contact is used. Also an I-line optical bandpass filter is used removing all wavelengths but 365.4 nm light, corresponding to the Hg-vapour lamp I-line emission. Negative resist has a strong absorption peak at 365 nm and higher wavelengths from other emission lines could reduce the photolithography resolution. The three aligners are equipped with slightly different Hg-vapour lamps, which results in different exposure doses. Exposure doses of the I-line are well calibrated for all aligners in the cleanroom[4] and processing on different aligners is therefore no problem.

To align the 13x13 mm^2 diamond pieces with the intended trench design on the 6" mask a carrier wafer was used and the chips are manually aligned first. Fine alignment is performed using the mask aligner micrometer stage. Additional substrate pieces of the same thickness are placed on opposite sides of the carrier wafer to balance the force when the mask is pressed against the sample with $\sim$ 1bar pressure before the resist is exposed.

Post Exposure Bake and Development

Negative resist requires an additional post exposure bake (PEB) that helps cross-link exposed parts of the resist, which makes them insoluble for the 'AZ 726 MIF' developer from MicroChemicals GmbH as discussed in section 4.4.1. After several test runs an optimal exposure dose of $\sim$115 mJ/cm^2, PEB and development time of 1 1/2 min was found to produce the best results. Fig. 8.4 shows a trench pattern transferred into the photoresist, which is now ready for the dry step of the hard mask.

[3] 620TB is capable of backside alignment
[4] EVG 620TB 7.6 mW/cm^2, EVG6200 15 mW/cm^2, EVG620T 12.7 mW/cm^2

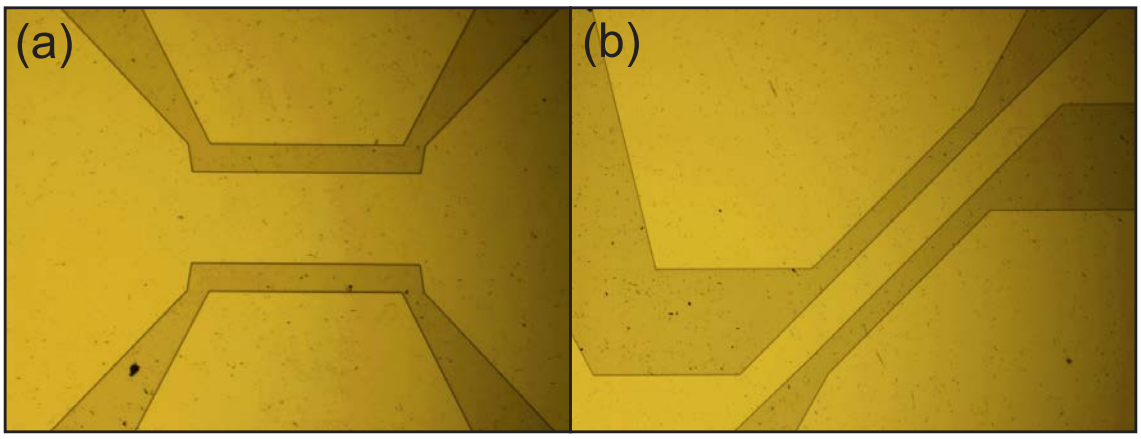


Figure 8.4: Pictures of trench patterns in a photoresist mask for a linear section (a) and a two-dimensional array (b).

8.2.5 Etching of SiO_2 Hard Mask and Diamond Substrates

Patterns in the photoresist mask can now be transferred into the SiO_2 layer making use of a fluorocarbon based SiO_2 dry etch, as illustrated in Fig. 8.1 (d). An inductively coupled plasma reactive ion beam etch (ICP RIE) is ideal to etch through such a thick oxide layer due to the very dense plasma it can create.

Silicon Dioxide Etch

Both the SiO_2 and diamond etch were performed in an 'OIPT SYS380 ICP RIE' tool with a 6" wafer holder. The high density plasma bombardment of the surface will significantly heat up the substrate surface and the photoresist could melt if the diamond samples are not cooled. To avoid this, sample pieces are placed on a carrier wafer cooled on the backside with a 10 °C helium flow. A small amount of vacuum oil is applied between wafer and sample to improve the thermal conductivity between them.

Process parameters described in App. B.1 were used for the etch and resulted in an etch rate of $\sim$ 300 nm/min. After 15 min of etching no SiO_2 was visible in the trenches anymore and the diamond etch step can start.

Diamond Etch

Diamond etches were never performed in the Southampton clean room before, but different recipes for diamond etching were found [231–233]. None of the etches was used to etch as deep as the anticipated $\sim 30\mu$m and most etches were performed using a metal mask,

which can not be used in the particular ICP. Several etch test runs were therefore performed starting with an oxygen/argon (O_2/Ar) plasma (50 ml/min O_2 and 10 ml/min Ar), an etch rate of $\sim$ 250 nm/min and etch selectivity of 7:1 between diamond and mask were achieved.

Etch depths were determined using a 'KLA-Tencor P-11' contact stylus profiler, which can measure step heights and surface roughnesses. A diamond stylus is moved along the surface following the contours and providing a 1D surface profile. In addition the 'Woollam ellipsometer' is used to determine the remaining thickness of the SiO_2 hard mask.

Diamond Etch Optimization

Observations of the plasma colour and dc bias between wafer holder and chamber indicated that the previous SiO_2 mask etch affected the diamond etch plasma. Fluorocarbon compositions were deposited on the chamber wall, carrier wafer and substrates during the SiO_2 etch and were now removed by the diamond etch. We assume that fluorocarbon molecules desorbed into the etch plasma adding a chemical SiO_2 etch component, which in turn reduced the selectivity between diamond and mask.

Based on this assumption a 10 min O_2/Ar plasma clean with only the carrier wafer present in the chamber was performed to remove most of the fluorocarbon contaminants, for exact parameters see App. B.1. Additionally the argon gas was removed from the etch process to increase the selectivity further, by reducing the sputter milling of the mask.

During the profiler measurement it was also found that the etched trenches showed a high surface roughness of $\sim \pm 2$ μm. It was assumed that sputtered SiO_2 mask parts were redeposited inside the trenches forming pillars [234] and that the polymorph nature of the substrate would in addition lead to locally uneven etch rates. To reduce the effects of redeposited SiO_2 on the roughness a cyclic etch was introduced with short 45 sec SiO_2 etch cycles, followed by a 5 min oxygen ash to remove the fluorocarbon contaminants and a 20 min oxygen diamond etch. Detailed parameters for the three etch cycle steps are presented in App. B.1. The etch cycle was repeated 5 times for a total etch depth of $\sim$ 29 μm with a selectivity of 15:1 and the surface roughness was reduced to $\sim \pm 1$ μm. As the trenches will be filled with electroplated copper, the roughness will not affect the performance of the ion traps and no further optimization was done.

8.2.6 Metallization of Current-Carrying Wires

The deep trenches in the diamond, shown in Fig. 8.1 (e), have to be filled with copper (Cu) in an electroplating process using a Cu seed layer. Copper was chosen for its high thermal and electrical conductivity and its ability to withstand very high current densities, which could lead to destruction of the wires due to electromigration as described in section 6.4.

Hard Mask Removal

Before depositing the seed layer the remaining SiO_2 mask is removed first using a wet etch based on 7:1 buffered hydrofluoric acid (BHF) [5] for 20 min. The etch rate of SiO_2 in 7:1 BHF is $\sim$ 400 nm/min [235], 20 min will be more than sufficient to remove any remaining SiO_2 parts. Afterwards the etched samples are cleaned in a QDR tank and dried using a nitrogen gun.

To make sure the diamond surface is clean and not hydrogen terminated a 2 min oxygen ash in the 'PVA Tepla 300' plasma tool is performed.

Seed Layer Deposition

Deposition of the Cu seed layer, shown in Fig. 8.1 (f), is performed in an 'AJA International, Inc. ORION' magnetron sputter system. First a 100 nm titanium (Ti) adhesion layer is deposited followed by a 1200 nm copper (Cu) seed layer. In the sputter process trench sidewalls are also covered making an electrical connection between trenches and top of the substrate. This makes sure that the applied current in the plating process has a low resistive path to every part of the trenches.

Detailed process parameters for the sputter deposition of Ti and Cu are presented in B.4. During the deposition step samples are attached to a carrier wafer using vacuum compatible Kapton polyimide tape, which will cover parts of the substrates.

Electroplating Setup

For the electroplating step illustrated in Fig. 8.1 (g) several copper plating solutions were investigated and the semiconductor grade 'OMNiCu TSV' copper plating solution was acquired from KMG Ultra Pure Chemicals. The plating system consists of a high copper

[5] 7:1 BHF consist of 7 parts 40% ammonium fluoride and 1 part 49% hydrofluoric acid [235]

electrolyte (OMNiCu HC Electrolyte), accelerator (OMNiCu TSV Accelerator), leveler (OMNiCu TSV Leveler) and suppressor (OMNiCu TSV Suppressor) solution. The plating solution is mixed in a glass beaker prior to the plating in a ratio of 500 ml electrolyte, 3 ml accelerator, 1.5 ml leveler and 5 ml suppressor and disposed afterwards, no additional substances have to be added.

A phosphorous de-oxidised copper[6] anode was acquired from Schloetter Co Ltd and cut into a suitable size for the plating setup. An 'Eco Chemie Autolab PGSTAT30' high current potentiostat/galvanostat operated in manual mode served as current supply.

Additionally a special teflon sample holder, shown in Fig. 8.5 (a) was designed allowing the diamond pieces to be clamped in place and making the electrical connection to the seed layer with a small copper plate. After the plating solution was mixed and the sample clamped to the holder, the copper anode is carefully placed inside the glass beaker. Both the sample holder and anode are electrically connected to the PGSTAT30 current supply and the electroplating can be started. Fig. 8.5 (b) shows the assembled plating setup.

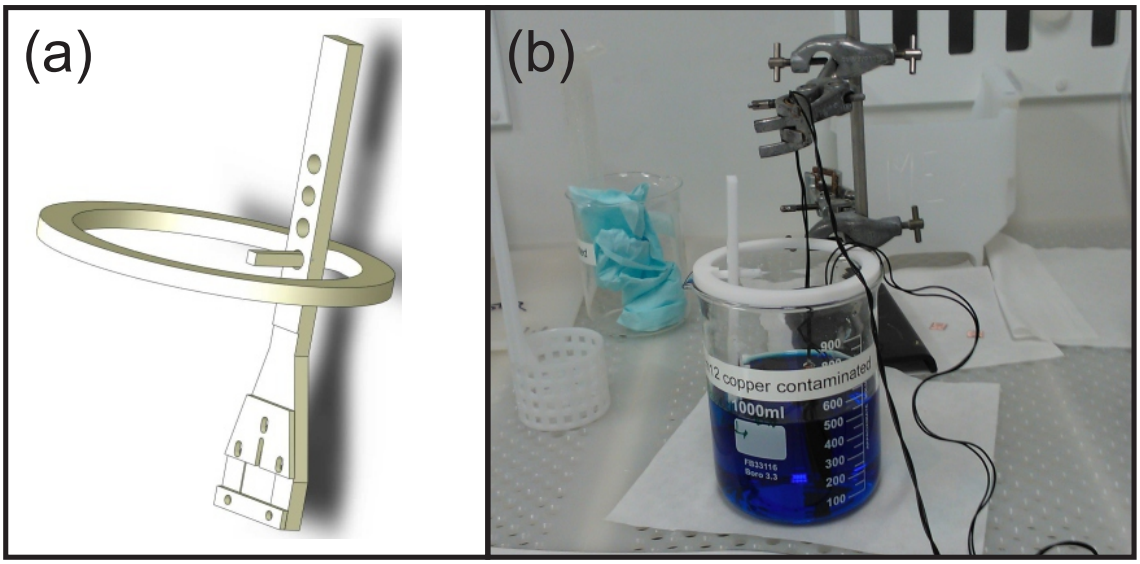


Figure 8.5: (a) Illustration showing the teflon sample holder and (b) picture of the assembled plating setup.

Copper Electroplating

Based on the measurements presented[7] in [236] a current density of ~ 5 A/dm^2 was chosen for the plating process which corresponds to a current of ~50mA. Several plating tests were performed and satisfying results were obtained for 60 min of plating with 50 mA.

[6] containing $\sim 0.05\%$ phosphorus
[7] OMNiCu TSV is the upgraded product of Cabas electrolyte

The profiler was used to determine the thickness of the plated copper by measuring height differences between uncoated parts of the substrate and the trench structures as shown in Fig. 8.6 (b). Copper inside the trenches was ~ 5 μm higher than the substrate surface.

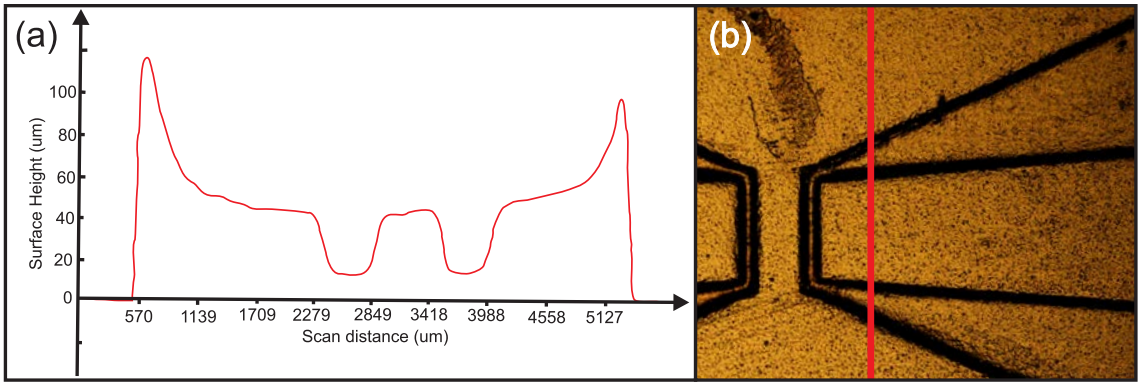


Figure 8.6: (a) Height profile of electroplated diamond sample vs scan distance. First ~ 500 μm of the scan shows the height of the uncoated substrate space (not shown in (b)), followed by the height of copper deposited on the top of the substrate ($\sim 40 - 120$ μm). The two sections at lower height (~ 15 μm) correspond to copper plated into the trenches. (b) Picture of the corresponding copper trenches, the path of the profiler stylus is marked in red. Not shown in this picture are parts of the substrate which are not coated with copper, but were measured by the stylus (the scan was leveled to the height of uncoated substrate sections).

Electroplated copper consists of many individual grains, their sizes determine the stress and electrical resistance of the layer. Performing an annealing step can change the grain size and lead to a lower resistivity. In [236] it was found that the annealing also happens at room temperature and the minimum resistivity is reached after 30 days, therefore no high temperature annealing step was performed.

After successful electroplating, the samples were sent to the diamond substrates supplier Mintres b.v for polishing, illustrated in Fig. 8.1 (h).

8.3 Fabrication of Ion Trap Structures

After polishing, CCW trap designs are coated with a 500 nm SiO_2 layer by an AJA Orion sputterer, sealing exposed copper and making it compatible with tools used in the following steps. Alumina based traps undergo the previously described FNA and oxygen plasma wafer clean. The following process steps are identical for both substrate types.

8.3.1 High Breakdown Voltage Insulating layer

In the first step, see Fig. 8.2 (a), a silicon nitride Si_3N_4 layer is deposited on the insulating substrate. Recent results [141] show that the maximum surface breakdown voltage over a Si_3N_4 surface is ~ 3 times higher when compared to standard SiO_2 layers. Additionally Si_3N_4 is an excellent etch barrier for an HF acid wet etch step, which will be performed at the end of the process sequence.

Silicon Nitride Deposition

By using a special cyclic low and high frequency deposition process in the 'OIPT SYS100 PECVD' reactor, a very dense Si_3N_4 layer can be created, which is ideal for etch stop layers. Deposition is based on the reaction of silane (SiH_4) with ammonia (NH_3) in a nitrogen diluted plasma. Before deposition starts the previously described nitrous oxide plasma clean is performed for 2 min followed by the deposition of $\sim$ 400nm Si_3N_4 in 37 min. Detailed process parameters can be found in App. B.2.

8.3.2 Buried Wire Steps

Next the substrates are prepared for the lift-off step used to create buried wires, which are used to electrically connect isolated electrodes.

Photoresist Coating, Exposure and Development

After dehydrating the samples for at least 30 min at 120 °C, 'AZ nLOF 2020' negative resist was spun on. 'AZ nLOF 2020' negative resist can be used to create thinner resist coatings of ~ 2 μm, which is ideal for the following 500 nm Al deposition and lift-off step.

Thicker resist would reduce the achievable minimum feature size and was not required. 'AZ nLOF 2020' resist is not readily available in the cleanroom and was mixed from 'AZ nLOF 2070' resist and 'AZ EBR solvent' in a 10:3 ratio. The resist is spun on at 4,000 rpm using the 'Brewer Science' spinner following the spin profile described in App. B.3 and baked on the 'Sawatec' hotplate at 110 °C for 2 min.

For the mask alignment and exposure step samples are again placed on a 6" carrier wafer and an exposure dose of 100 mJ/cm^2 was chosen. A post exposure bake at 110°C for

exactly 1 min was performed and the resist was developed in 'AZ 726 MIF' developer for 50 sec.

An optical microscope was used to inspect the resist structures and examples of successfully developed resist are shown in Fig. 8.7.

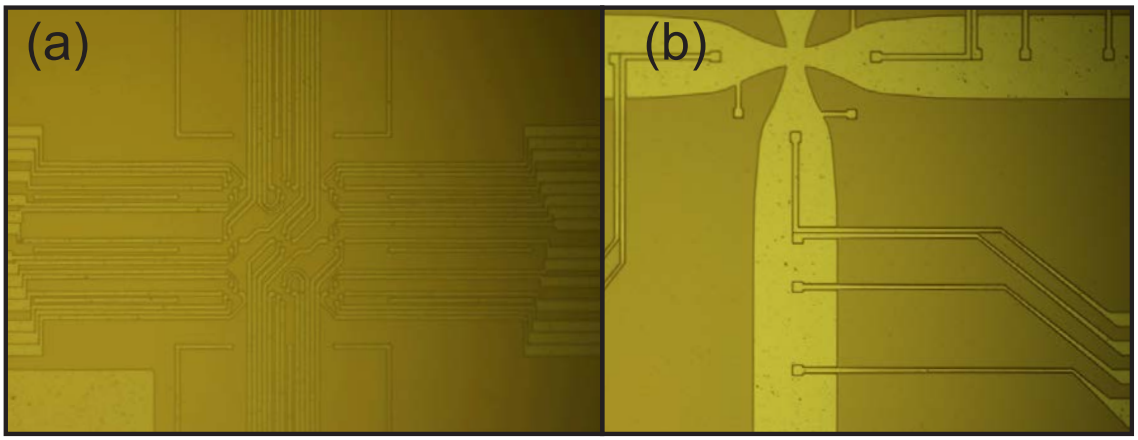


Figure 8.7: Pictures of developed resist structures for a two-dimensional array (a) and an X-junction in (b). Wires in the centre of (a) are taken with a 200× magnification and are ∼3 μm wide, picture (b) was taken with a 100× magnification and the wires are ∼10 μm wide.

Prior to the Al deposition, shown in Fig. 8.2 (d), an oxygen plasma descum is performed in a metal designated 'OIPT RIE80+' etch tool for 30 sec. The descum process parameters can be found in App. B.1. Performing a descum step helps remove residual photoresist in the developed trenches improving adhesion of the following metal deposition.

Aluminium Deposition and Lift-Off

After creating the photoresist mask, 500 nm of aluminium are deposited using the Leybold LAB700EB evaporator following the process parameters described in App. B.4. Deposition rate and total thickness is controlled by a deposition controller using a quartz crystal, which changes the vibration frequency with increased material deposition. Substrate pieces are placed on a Si carrier wafer and held in place by Kapton tape. To improve the uniformity of the deposition, the carrier wafer is placed 1 m above the evaporation material and rotated around its axis.

Directly following the deposition, samples are placed in N-Methyl-2-pyrrolidone (NMP) for at least 12 hours. NMP creeps underneath the resist and lifts it off the substrate, including metal deposited on top the resist. To completely remove the resist, samples are additionally placed in a second beaker with fresh NMP that is heated to 60°C and

ultrasonic force is applied. Afterwards, remaining metal parts are rinsed off the substrate with isopropyl alcohol (IPA) and dried with a nitrogen gun. Fig. 8.8 shows the structured Al layer inspected with an optical microscope.

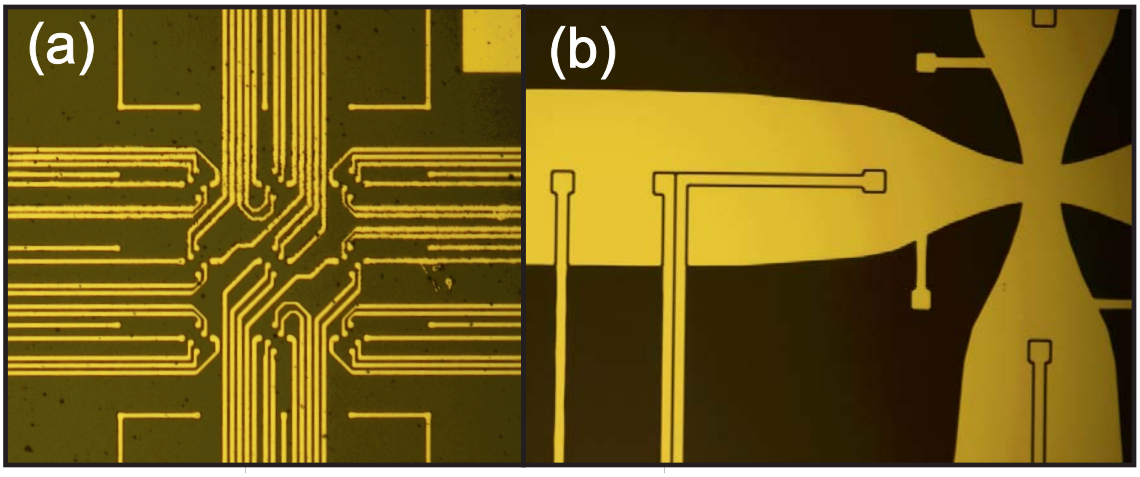


Figure 8.8: Pictures were taken with a 200× magnification showing Al buried wires of a 2D trapping array (a) and X-junction design (b).

8.3.3 Deposition and Structuring of Insulating Layer

Aluminium wire structures are buried under a 2.5 μm thick SiO_2 layer, which electrically isolates them from the trap electrodes.

Silicon Dioxide Deposition

The SiO_2 layer, shown in Fig. 8.2 (f), is deposited in the same 'OIPT SYS100' PECVD reactor and the same process parameters described in App. B.2 are used. Substrates can no longer be ashed in the 'PVA Tepla 300' system, therefore a 5 min *in situ* nitrous oxide clean is performed prior to deposition.

VIA Photoresist Mask

Next the VIA holes have to be etched into the insulating SiO_2 so that electrodes can be connected to the buried wires underneath. First the substrates are dehydrated and 4 μm of 'AZ nLOF 2070' resist is spun on, followed by a 2 min soft bake, identical to the steps used in section 8.2.4. The same exposure dose (∼115 mJ/cm^2), PEB and development time of 1 1/2 min is used. Unlike the lithography step in section 8.2.4 the mask has to be aligned precisely with the buried wire layer to make sure the VIA holes are exactly on

top of the metal structure underneath. Successful alignment of the two layers is shown in Fig. 8.9.

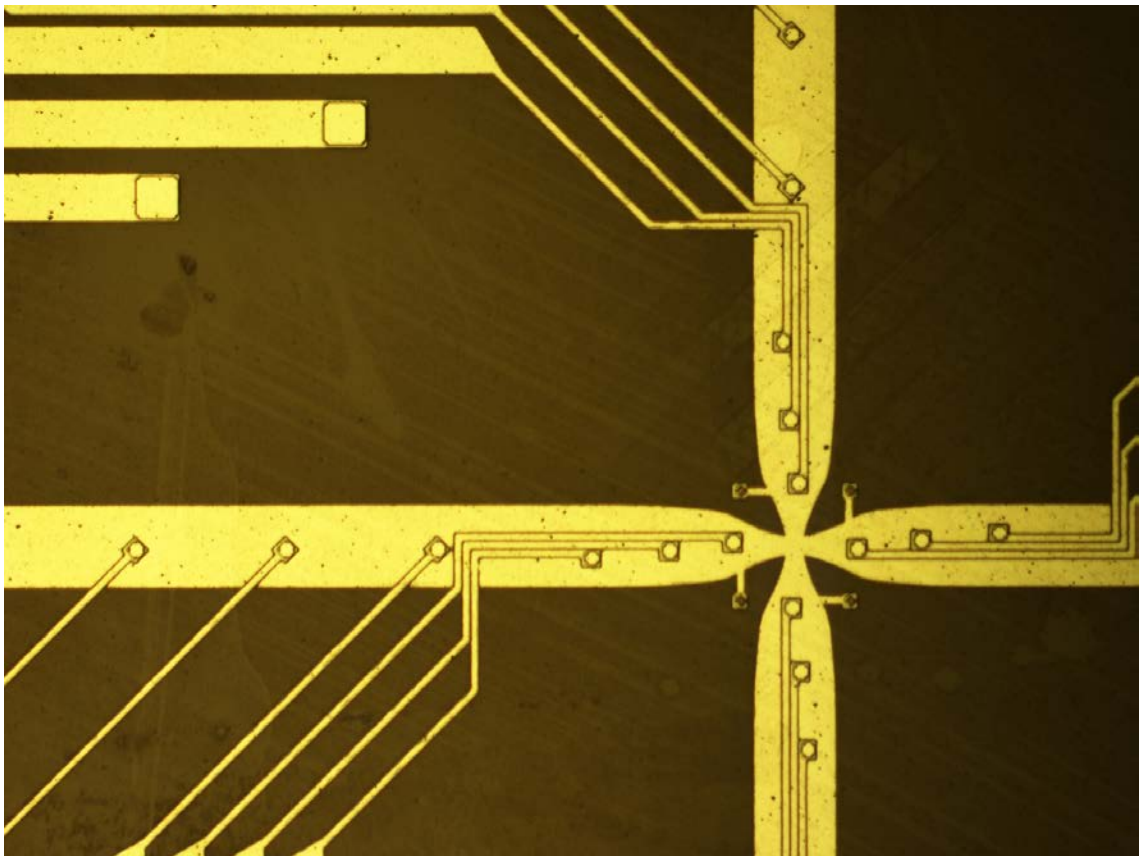


Figure 8.9: Showing the alignment of the VIA resist etch mask with the buried wires.

Silicon Dioxide VIA Etch

The structured photoresist mask is then used to etch holes into the SiO_2 with a second 'OIPT SYS380 ICP RIE' tool configured for metal etching, as illustrated in Fig. 8.2 (h). This tool has a different gas configuration and the previously used SiO_2 etch had to be adjusted. The new etch parameters can be found in App. B.1. Before the etch process starts, a 30 sec *in situ* oxygen ash is performed followed by a 12 min SiO_2 etch. Another 10 min oxygen ash is performed to remove the remaining photoresist.

8.3.4 Lithography and Deposition of Trap Electrodes

After the oxygen plasma ash, substrates are dehydrated for the following lithography step. Trap electrodes are created in metal deposition and lift-off step, shown in Fig. 8.2 (i-k).

Photoresist Mask for Electrode Lift-Off Step

As mentioned before photoresist structures should be at least twice the thickness of the deposited material, so for the intended electrode thickness of ∼3.5 μm, a 7μm thick 'AZ nLOF 2070' resist layer was chosen.

A different spin profile presented in App. B.3 with a maximum rotation of 2,750 rpm was used for this resist thickness. Due to the lower spin speed and rectangular substrates, large edge-beads form during the spinning and have to be removed using 'AZ EBR solvent' soaked cleanroom wipes. Afterwards, a 2 min soft bake is performed and the resist is ready for exposure.

Trap electrode structures on the photo mask are precisely positioned on top of the buried wire marks using the mask aligner microstage and resist is exposed with 140 mJ/cm^2. After a 2 min PEB was performed, the resist is developed for 1 min and 45 sec in 'AZ 726 MIF' developer. After successful development the resist is descumed for 30 sec using the 'OIPT RIE80+' etch tool.

Electrode Metal Deposition Step and Lift-Off

Trap electrodes consist of 3.5 μm aluminium, 50 nm chromium, 100 nm nickel and 150 nm gold deposited in the Leybold LAB700EB Evaporator. The thick Al was chosen to further improve the shielding of exposed dielectrics and to reduce the electrical resistance of the rf electrodes structures. A gold finish was deposited to prevent oxidisation of the electrode surface and the chromium/nickel layer promotes the adhesion between Al and Au and also acts as a diffusion barrier between them. Deposition parameters can be found in App. B.4.

To lift-off the resist after deposition the substrates are placed in a beaker with NMP for at least 12 hours, then moved to a second beaker with fresh NMP at 60 °C and ultrasonic force is applied. Several electrode layer structures are shown in Fig. 8.10 after lift-off.

Silicon Dioxide Wet Etch

Parts of the SiO_2 layer located between electrodes are still exposed, see Fig. 8.2 (k), and would lead to micromotion if charged particles are deposited or laser scattered on the layer as discussed in section 4.3.1. To prevent this the ground plate incorporated in the buried

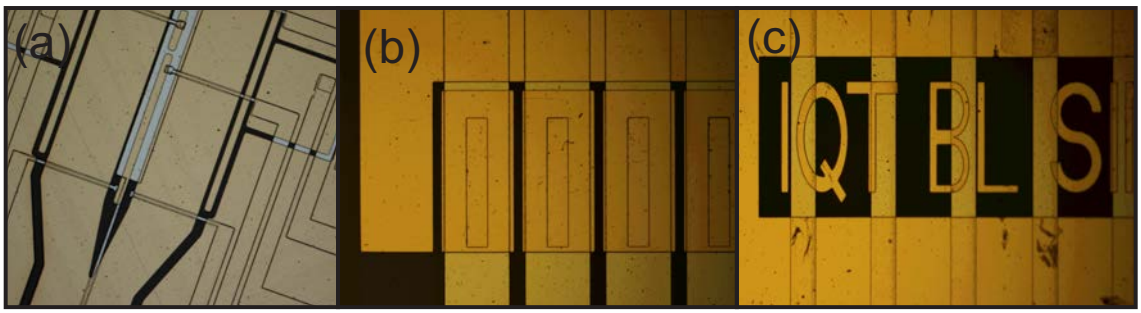


Figure 8.10: Electrode Layer structures after lift-off process, showing (a) linear section, (b) bond pads and (c) labelling of the trap.

wire layer is exposed by etching away the SiO_2 at these locations using an isotropic wet etch, shown in Fig. 8.2 (l).

Hydrofluoric acid only minimally attacks aluminium, chromium, or nickel and the top of the alumina substrate is protected from the etch by the Si_3N_4 etch stop layer, diamond is inert to any wet etch. Buffered HF acid strongly etches SiO_2 with an etch rate of $\sim$ 400 nm/min, making it ideal for this wet etch step. Dipping the substrates for 10 min in 7:1 BHF removes exposed parts of the 2.5 μm thick SiO_2 layer and also creates an undercut, which further reduces the possibility of exposed dielectrics further.

Backside Metallization

At the end of the process a 100 nm Ti layer and 200 nm Au layer is deposited on the backside of the substrates, which is required to attach the samples to a heat sink with gold-tin solder as intended. The deposition is carried out in the AJA Orion sputterer, exact process parameters are described in App. B.4.

After the fabrication substrate pieces have to be cut into 12×12 mm^2 pieces to fit onto the chip carriers. Wafer dicing of alumina can only be performed for entire wafers and not wafer pieces in the cleanroom. Diamond substrates can not be diced at all in the cleanroom and it was therefore decided that both substrate pieces will be cut into smaller pieces with a laser after initial tests confirm the functionality of the chips. Diamond pieces are cut by the substrate supplier Mintres b.v., Al_2O_3 substrates by Laser Cutting Ceramics Ltd.

8.4 Conclusion and outlook

A novel versatile fabrication process was developed in the Southampton Nanofabrication cleanroom and initial test samples were manufactured. More trap designs will be microfabricated in the following weeks and after the fabrication is completed the substrates will be laser cut and used for ion trap experiments.

Chapter 9

Conclusion and Outlook

My work towards scalable ion trap quantum technology presented in this thesis, is based on the comprehensive theory developed for ion traps, which I summarized first. In the following chapter I described the experimental setup used to successfully trap Yb^+ ions, discussed the heating rate measurement performed in this setup and presented a detailed analysis of the results.

Then I gave an overview of possible microfabrication techniques and challenges one faces when fabricating and operating asymmetric ion traps. After comparing a variety of previously used fabrication processes, I presented a new process suitable for scalable asymmetric ion traps with current-carrying wire structures. These wire structures are intended to produce large static magnetic field gradients at the ions position, which can be used to perform the microwave based quantum gates proposed by Mintert et al.

Next I discussed error correction schemes, which are required to perform large numbers of quantum operations without decoherence of the quantum states. Based on the requirements of a surface error correction code I presented a potential concept for a scalable ion trap quantum system based on microwave entanglement and shuttling of ions through X-junctions.

Motivated by the requirements of such a system I developed a range of asymmetric ion trap designs. The designs include an optimized X-junction geometry with an rf barrier suppression of >110, followed by the development and design of current-carrying wire structures embedded in the substrate, that are compatible with almost any asymmetric ion trap design. In addition, designs with loading and detection slots, traps with electrically and physically separated rf rails in axial direction were developed.

The heat dissipated in ion traps with current-carrying wires needs to be transported out of the vacuum system and a novel thermal transport system was developed and is described in the next chapter. I also presented modifications of the vacuum system to add a high energy ion source for *in situ* cleaning. Performing *in situ* cleaning of the trap electrodes has shown to reduce the heating rate in ion traps [86,87] and will be experimentally tested in one of our vacuum systems in the future. Lastly I described the successful development of a novel high-speed, multichannel, high-voltage and low-noise voltage control system. The system will be used to perform shuttling operations in linear and X-junction traps.

In the last chapter I described the development of a novel fabrication process capable of producing extremely thick copper wires embedded in a diamond substrate. New process steps for the fabrication of current carrying wires were developed and tested. In addition, asymmetric ion traps without current-carrying wires were also fabricated.

Future Work

I intend to complete the microfabrication of ion traps with current-carrying wires in the next weeks and the traps will be tested shortly after. After successful trapping of ions, currents will be applied to the chips and the exact gradients will be measured using the ion. Extensive work towards microwave based quantum gates has been done in our group, using permanent magnets attached to a macroscopic trap. Asymmetric traps with current-carrying wires will allow us to generate larger adjustable gradients, which will help our work towards a high fidelity quantum gate.

Bibliography

[1] R. P. Feynman. Simulating physics with computers. *Int. J. Th. Phys.*, 21(6/7):467–488, 1982. 1

[2] D. Greif, T. Uehlinger, G. Jotzu, L. Tarruell, and T. Esslinger. Short-range quantum magnetism of ultracold fermions in an optical lattice. *Science*, 340(6138):1307–1310, May 2013. 1

[3] J. W. Britton, B. C. Sawyer, A. C. Keith, C.-C. J. Wang, J. K. Freericks, H. Uys, M. J. Biercuk, and J. J. Bollinger. Engineered two-dimensional Ising interactions in a trapped-ion quantum simulator with hundreds of spins. *Nature*, 484:489 to 492, Apr. 2012. 1

[4] M. Pons, V. Ahufinger, C. Wunderlich, A. Sanpera, S. Braungardt, A. Sen(De), U. Sen, and M. Lewenstein. Trapped ion chain as a neural network: Fault-tolerant quantum computation. *Phys. Rev. Lett.*, 98, July 2006. 1

[5] A. Friedenauer, H. Schmitz, J. T. Glueckert, D. Porras, and T. Schaetz. Simulating a quantum magnet with trapped ions. *Nat. Phys.*, 4:757 to 761, Oct. 2008. 1

[6] M. Johanning, A. F. Varón, and C. Wunderlich. Quantum simulations with cold trapped ions. *J. Phys. B: At., Mol. Opt. Phys.*, 42(15):154009, 2009. 1

[7] R. J. Clark, T. Lin, K. R. Brown, and I. Chuang. A two-dimensional lattice ion trap for quantum simulation. *J. Appl. Phys.*, 105(1):013114–013114–8, 2009. 1

[8] K. Kim, M.-S. Chang, S. Korenblit, R. Islam, E. E. Edwards, J. K. Freericks, G.-D. Lin, L.-M. Duan, and C. Monroe. Quantum simulation of frustrated Ising spins with trapped ions. *Nature*, 465:590–593, 2010. 1

[9] T. Li, Z.-X. Gong, Z.-Q. Yin, H. T. Quan, X. Yin, P. Zhang, L.-M. Duan, and X. Zhang. Space-time crystals of trapped ions. *Phys. Rev. Lett.*, 109, 2012. 1

[10] B. Horstmann, B. Reznik, S. Fagnocchi, and J. I. Cirac. Hawking radiation from an acoustic black hole on an ion ring. *Phys. Rev. Lett.*, 104:250403, June 2010. 1

[11] R. Schützhold, M. Uhlmann, L. Petersen, H. Schmitz, A. Friedenauer, and T. Schätz. Analogue of cosmological particle creation in an ion trap. *Phys. Rev. Lett.*, 99:201301, Nov. 2007. 1

[12] L. Lamata, J. León, T. Schätz, and E. Solano. Dirac equation and quantum relativistic effects in a single trapped ion. *Phys. Rev. Lett.*, 98:253005, June 2007. 1

[13] D. Deutsch. Quantum theory, the Church-Turing principle and the universal quantum computer. *Proc. R. Soc. Lond. A*, 400(1818):97–117, July 1985. 1

[14] A. M. Turing. On computable numbers, with an application to the Entscheidungsproblem. *Proc. London Math. Soc.*, 42:230–265, 1937. 1

[15] P. Shor. Algorithms for quantum computation: Discrete logarithms and factoring. *Ann. IEEE Symp. Found.*, 0:124–134, 1994. 1

[16] L. K. Grover. A fast quantum mechanical algorithm for database search. In *STOC*, pages 212–219. ACM, 1996. 1

[17] V. Subramaniam and P. Ramadevi. Quantum computation of Jones polynomials. *arXiv:quant-ph/0210095*, 2002. 1

[18] S. A. Fenner and Y. Zhang. Quantum algorithms for a set of group theoretic problems. In *P. 9^{th} ICTCS*, pages 215–227, 2005. 1

[19] A. Y. Kitaev. Quantum measurements and the Abelian stabilizer problem. In *ECCC*, volume 3, 1996. 1

[20] T. Szkopek, V. Roychowdhury, E. Yablonovitch, and D. S. Abrams. Eigenvalue estimation of differential operators with a quantum algorithm. *Phys. Rev. A*, 72:062318, Dec. 2005. 1

[21] L. M. K. Vandersypen, M. Steffen, G. Breyta, C. S. Yannoni, M. H. Sherwood, and I. L. Chuang. Experimental realization of Shor's quantum factoring algorithm using nuclear magnetic resonance. *Nature*, 414:883887, Dec. 2001. 1

[22] E. Martin-Lopez, A. Laing, T. Lawson, R. Alvarez, X.-Q. Zhou, and J. L. O'Brien. Experimental realization of Shor's quantum factoring algorithm using qubit recycling. *Nat. Photon.*, 6:773776, Nov. 2012. 1

[23] K.-A. Brickman, P. C. Haljan, P. J. Lee, M. Acton, L. Deslauriers, and C. Monroe. Implementation of Grover's quantum search algorithm in a scalable system. *Phys. Rev. A*, 72:050306, Nov. 2005. 1

[24] C. Zalka. Using Grover's quantum algorithm for searching actual databases. *Phys. Rev. A*, 62:052305, Oct. 2000. 2

[25] R. L. Rivest, A. Shamir, and L. M. Adleman. A method for obtaining digital signatures and public-key cryptosystems. *Commun. ACM*, 21(2):120–126, 1978. See also U.S. Patent 4,405,829. 2

[26] G. F. Viamontes, I. L. Markov, and J. P. Hayes. Is quantum search practical? *Comput. Sci. Eng.*, 7(3):62–70, May 2005. 2

[27] W. K. Wootters and W. H. Zurek. A single quantum cannot be cloned. *Nature*, 299:802 to 803, Oct. 1982. 2

[28] C. H. Bennett and G. Brassard. Quantum cryptography: Public key distribution and coin tossing. In *Proceedings of the IEEE International Conference on Computers, Systems and Signal Processing*, pages 175–179, 1984. 2

[29] S. Olmschenk, D. Hayes, D. Matsukevich, P. Maunz, D. Moehring, and C. Monroe. Quantum logic between distant trapped ions. *Int. J. Quantum Inf.*, 08:337–394, 2010. 2, 107

[30] D. Bouwmeester, J.-W. Pan, K. Mattle, M. Eibl, H. Weinfurter, and A. Zeilinger. Experimental quantum teleportation. *Nature*, 390:575 to 579, Dec. 1997. 2

[31] P. Maunz, D. L. Moehring, S. Olmschenk, K. C. Younge, D. N. Matsukevich, and C. Monroe. Quantum interference of photon pairs from two remote trapped atomic ions. *Nat. Phys.*, 03:538–541, 2007. 2

[32] J. Yin, Y. Cao, S.-B. Liu, G.-S. Pan, J.-H. Wang, T. Yang, Z.-P. Zhang, F.-M. Yang, Y.-A. Chen, C.-Z. Peng, and J.-W. Pan. Experimental single-photon transmission from satellite to earth. *arXiv:1306.0672v1*, 2013. 2

[33] D. P. Divincenzo. The physical implementation of quantum computation. *Fortschr. Phys.*, 48:2000, 2000. 2

[34] D. P. DiVincenzo. Two-bit gates are universal for quantum computation. *Phys. Rev. A*, 51:1015–1022, Feb. 1995. 2

[35] M. Suchara, A. Faruque, C.-Y. Lai, G. Paz, F. Chong, and J. D. Kubiatowicz. Estimating the resources for quantum computation with the QuRE toolbox. Technical Report UCB/EECS-2013-119, May 2013. 2, 107

[36] I. Bloch. Quantum coherence and entanglement with ultracold atoms in optical lattices. *Nature*, 453:1016 to 1022, June 2008. 2

[37] C. C. Nshii, M. Vangeleyn, J. P. Cotter, P. F. Griffin, E. A. Hinds, C. N. Ironside, A. G. See, P. Sinclair, E. Riis, and A. S. Arnold. A surface-patterned chip as a strong source of ultracold atoms for quantum technologies. *Nat. Nano.*, pages 1748–3395, Apr. 2013. 2

[38] S. Ritter, C. Nölleke, C. Hahn, A. Reiserer, A. Neuzner, M. Uphoff, M. Mücke, E. Figueroa, J. Bochmann, and G. Rempe. An elementary quantum network of single atoms in optical cavities. *Nature*, 484:195200, Apr. 2012. 2

[39] Y. Nakamura, Y. A. Pashkin, and J. S. Tsai. Coherent control of macroscopic quantum states in a single-Cooper-pair box. *Nature*, 398:786788, Apr. 1999. 2

[40] I. Chiorescu, Y. Nakamura, C. J. P. M. Harmans, and J. E. Mooij. Coherent quantum dynamics of a superconducting flux qubit. *Science*, 299(5614):1869–1871, 2003. 2

[41] J. Clarke and F. K. Wilhelm. Superconducting quantum bits. *Nature*, 453:10311042, June 2008. 2

[42] E. Knill, R. Laflamme, and G. J. Milburn. A scheme for efficient quantum computation with linear optics. *Nature*, 409:4652, Jan. 2001. 2

[43] H. J. Kimble. The quantum internet. *Nature*, 453:10231030, June 2008. 2

[44] W. J. Munro, K. Nemoto, T. P. Spiller, S. D. Barrett, P. Kok, and R. G. Beausoleil. Efficient optical quantum information processing. *J. Opt. B.*, 7(7):S135, 2005. 2

[45] C. Monroe, D. M. Meekhof, B. E. King, W. M. Itano, and D. J. Wineland. Demonstration of a fundamental quantum logic gate. *Phys. Rev. Lett.*, 75:4714–4717, Dec. 1995. 2, 3, 105

[46] R. Blatt and D. Wineland. Entangled states of trapped atomic ions. *Nature*, 453:10081015, June 2008. 2

[47] J. I. Cirac and P. Zoller. A scalable quantum computer with ions in an array of microtraps. *Nature*, 404, Apr. 2000. 2

[48] D. Kielpinski, C. Monroe, and D. Wineland. Architecture for a large-scale ion-trap quantum computer. *Nature*, 417:709–711, 2002. 3, 105

[49] C. Monroe and J. Kim. Scaling the ion trap quantum processor. *Science*, 339(6124):1164–1169, 2013. 3, 105, 107

[50] J. P. Home, D. Hanneke, J. D. Jost, J. M. Amini, D. Leibfried, and D. J. Wineland. Complete methods set for scalable ion trap quantum information processing. *Science*, 325(5945):1227–1230, 2009. 3

[51] D. Leibfried, B. DeMarco, V. Meyer, D. Lucas, M. Barrett, J. Britton, W. M. Itano, B. Jelenkovic, C. Langer, T. Rosenband, and D. J. Wineland. Experimental demonstration of a robust, high-fidelity geometric two ion-qubit phase gate. *Nature*, 422, Mar. 2003. 3, 105

[52] C. Wunderlich, T. Hannemann, T. Körber, H. Häffner, C. Roos, W. Hänsel, R. Blatt, and F. Schmidt-Kaler. Robust state preparation of a single trapped ion by adiabatic passage. *J. Mod. Opt.*, 54(11):1541–1549, 2007. 3, 105

[53] M. Acton, K.-A. Brickman, P. C. Haljan, P. J. Lee, L. Deslauriers, and C. Monroe. Near-perfect simultaneous measurement of a qubit register. *Quant. Inf. Comp.*, 6(6):465–482, Sept. 2006. 3, 105

[54] A. H. Burrell, D. J. Szwer, S. C. Webster, and D. M. Lucas. Scalable simultaneous multiqubit readout with 99.99% single-shot fidelity. *Phys. Rev. A*, 81:040302, Apr. 2010. 3, 105

[55] A. H. Myerson, D. J. Szwer, S. C. Webster, D. T. C. Allcock, M. J. Curtis, G. Imreh, J. A. Sherman, D. N. Stacey, A. M. Steane, and D. M. Lucas. High-fidelity readout of trapped-ion qubits. *Phys. Rev. Lett.*, 100:200502, May 2008. 3, 105, 107

[56] P. Fisk, M. Sellars, M. Lawn, and C. Coles. Accurate measurement of the 12.6 GHz "clock" transition in trapped $^{171}Yb^{+}$ ions. *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, 44(2):344–354, 1997. 3, 105

[57] T. Monz, P. Schindler, J. T. Barreiro, M. Chwalla, D. Nigg, W. A. Coish, M. Harlander, W. Hänsel, M. Hennrich, and R. Blatt. 14-qubit entanglement: Creation and coherence. *Phys. Rev. Lett.*, 106:130506, Mar. 2011. 3, 105

[58] C. A. Sackett, D. Kielpinski, B. E. King, C. Langer, V. Meyer, C. J. Myatt, M. Rowe, Q. A. Turchette, W. M. Itano, D. J. Wineland, and C. Monroe. Experimental entanglement of four particles. *Nature*, 404, Mar. 2000. 3, 105

[59] J. Chiaverini, D. Leibfried, T. Schaetz, M. D. Barrett, R. B. Blakestad, J. Britton, W. M. Itano, J. D. Jost, E. Knill, C. Langer, R. Ozeri, and D. J. Wineland. Realization of quantum error correction. *Nature*, 432, Dec. 2004. 3

[60] J. Benhelm, G. Kirchmair, C. F. Roos, and R. Blatt. Towards fault-tolerant quantum computing with trapped ions. *Nat. Phys.*, 4, June 2008. 3, 107, 111

[61] E. Knill. Quantum computing with realistically noisy devices. *Nature*, 434:39–44, Mar. 2005. 3, 107

[62] A. G. Fowler, A. M. Stephens, and P. Groszkowski. High-threshold universal quantum computation on the surface code. *Phys. Rev. A*, 80:052312, Nov. 2009. 3, 107

[63] A. M. Steane. Efficient fault-tolerant quantum computing. *Nature*, 399:124–126, Mai 1999. 3, 107

[64] D. Bacon. Operator quantum error-correcting subsystems for self-correcting quantum memories. *Phys. Rev. A*, 73:012340, Jan. 2006. 3, 107

[65] W. Paul and H. Steinwedel. Ein neues Massenspektrometer ohne Magnetfeld. *Z. Naturforsch., A*, 8:448, 1953. 3, 7, 12

[66] W. Paul. Electromagnetic traps for charged and neutral particles. *Rev. Mod. Phys.*, 62(3):531–540, July 1990. 3, 8, 11, 12

[67] W. Paul, O. Osberghaus, and E. Fischer. Ein Ionenkäfig. *Forschungsberichte des Wirtschafts- und Verkehrsministeriums Nordrhein-Westfalen*, 415, 1958. 3, 6, 7

[68] E. Fischer. Die dreidimensionale Stabilisierung von Ladungsträgern in einem Vierpolfeld. *Z. Phys.*, 156(1):1–26, 1959. 3

[69] H. G. Dehmelt. Spin resonance of free electrons. *Progr. Rep. NSF-G5955*, May 1962. 3

[70] H. G. Dehmelt. Radiofrequency spectroscopy of stored ions I: Storage. *Adv. At. Mol. Phys.*, 3:53, 1967. 3, 8, 11

[71] W. Neuhauser, M. Hohenstatt, P. Toschek, and H. Dehmelt. Optical-sideband cooling of visible atom cloud confined in parabolic well. *Phys. Rev. Lett.*, 41:233–236, July 1978. 3

[72] D. J. Wineland, R. E. Drullinger, and F. L. Walls. Radiation-pressure cooling of bound resonant absorbers. *Phys. Rev. Lett.*, 40:1639–1642, June 1978. 3

[73] J. I. Cirac and P. Zoller. Quantum computations with cold trapped ions. *Phys. Rev. Lett.*, 74(20):4091–4094, May 1995. 3

[74] M. Brownnutt, G. Wilpers, P. Gill, R. C. Thompson, and A. G. Sinclair. Monolithic microfabricated ion trap chip design for scaleable quantum processors. *New J. Phys.*, 8:232, 2006. 3

[75] M. D. Hughes, B. Lekitsch, J. A. Broersma, and W. K. Hensinger. Microfabricated ion traps. *Contemp.Phys.*, 52(6):505–529, 2011. 4, 6, 7, 13, 19, 33, 66, 72, 108, 118

[76] D. Stick, W. K. Hensinger, S. Olmschenk, M. J. Madsen, K. Schwab, and C. Monroe. Ion trap in a semiconductor chip. *Nat. Phys.*, 2:36–39, 2006. 4, 57, 83, 84, 108

[77] S. Seidelin, J. Chiaverini, R. Reichle, J. J. Bollinger, D. Leibfried, J. Britton, J. H. Wesenberg, R. B. Blakestad, R. J. Epstein, D. B. Hume, W. M. Itano, J. D. Jost, C. Langer, R. Ozeri, N. Shiga, and D. J. Wineland. Microfabricated surface-electrode ion trap for scalable quantum information processing. *Phys. Rev. Lett.*, 96(25):253003, June 2006. 4, 6, 19, 83, 84, 95, 96, 97, 108, 110

[78] W. K. Hensinger, S. Olmschenk, D. Stick, D. Hucul, M. Yeo, M. Acton, L. Deslauriers, C. Monroe, and J. Rabchuk. T-junction ion trap array for two-dimensional ion shuttling, storage, and manipulation. *Appl. Phys. Lett.*, 88(3):034101, 2006. 4, 109, 123, 160

[79] R. B. Blakestad, C. Ospelkaus, A. P. VanDevender, J. M. Amini, J. Britton, D. Leibfried, and D. J. Wineland. High-fidelity transport of trapped-ion qubits through an X-junction trap array. *Phys. Rev. Lett.*, 102:153002, Apr. 2009. 4, 109, 123

[80] R. B. Blakestad, C. Ospelkaus, A. P. VanDevender, J. H. Wesenberg, M. J. Biercuk, D. Leibfried, and D. J. Wineland. Near-ground-state transport of trapped-ion qubits through a multidimensional array. *Phys. Rev. A*, 84:032314, Sept. 2011. 4, 22, 109

[81] R. Bowler, J. Gaebler, Y. Lin, T. R. Tan, D. Hanneke, J. D. Jost, J. P. Home, D. Leibfried, and D. J. Wineland. Coherent diabatic ion transport and separation in a multizone trap array. *Phys. Rev. Lett.*, 109:080502, Aug. 2012. 4, 108, 109, 123

[82] A. Khromova, C. Piltz, B. Scharfenberger, T. F. Gloger, M. Johanning, A. F. Varón, and C. Wunderlich. Designer spin pseudomolecule implemented with trapped ions in a magnetic gradient. *Phys. Rev. Lett.*, 108:220502, June 2012. 4, 39, 112, 133

[83] C. Ospelkaus, U. Warring, Y. Colombe, K. R. Brown, J. M. Amini, D. Leibfried, and D. J. Wineland. Microwave quantum logic gates for trapped ions. *Nature*, 476, Aug. 2011. 4, 39, 72, 81, 112

[84] W. K. Hensinger. Quantum information: Microwave ion-trap quantum computing. *Nature*, 476, Aug. 2011. 4

[85] S. J. Devitt, W. J. Munro, and K. Nemoto. High performance quantum computing. *arXiv:0810.2444*, 2008. 4, 105

[86] D. A. Hite, Y. Colombe, A. C. Wilson, K. R. Brown, U. Warring, R. Jördens, J. D. Jost, K. S. McKay, D. P. Pappas, D. Leibfried, and D. J. Wineland. 100-fold reduction of electric-field noise in an ion trap cleaned with *In Situ* argon-ion-beam bombardment. *Phys. Rev. Lett.*, 109:103001, Sept. 2012. 5, 33, 80, 82, 83, 151, 158, 160, 192

[87] N. Daniilidis, S. Gerber, G. Bolloten, A. R. M. Ramm, E. Ulin-Avila, I. Talukdar, and H. Häffner. Probing surface electric field noise with a single ion. *arXiv:1307.7194*, 2013. 5, 33, 80, 82, 83, 151, 158, 192

[88] S. Earnshaw. On the nature of the molecular forces which regulate the constitution of the luminiferous ether. *Trans. Camb. Phil. Soc*, 7:97–112, 1842. 6

[89] D. J. Wineland, C. Monroe, W. M. Itano, D. Leibfried, B. E. King, and D. M. Meekhof. Experimental issues in coherent quantum-state manipulation of trapped atomic ions. *J. Res. Nat. Inst. Stand. Tech.*, 103(3):259–328, 1998. 7, 8, 13, 16

[90] J. J. McLoughlin, A. H. Nizamani, J. D. Siverns, R. C. Sterling, M. D. Hughes, B. Lekitsch, B. Stein, S. Weidt, and W. K. Hensinger. Versatile ytterbium ion trap experiment for operation of scalable ion-trap chips with motional heating and transition-frequency measurements. *Phys. Rev. A*, 83:013406, Jan. 2011. 7, 39, 40, 45, 48, 56, 61, 62, 82, 83

[91] D. Gerlich. *Inhomogeneous RF Fields: A Versatile Tool for the Study of Processes with Slow Ions*. John Wiley and Sons, Inc., 2007. 8, 25

[92] P. L. Kapitza. Dynamic stability of a pendulum with an oscillating point of suspension. *J. Exp. Theor. Phys.*, 21(5):588–597, 1951. 11

[93] L. Landau and E. Lifshitz. *Mechanics*. Pergamon Press Oxford, 1960. 11

[94] E. Mathieu. Mémoire sur le mouvement vibratoire d'une membrane de forme elliptique. *J. Math. Pures Appl.*, 13, 1868. 12

[95] M. Abramowitz and I. Stegun. *Handbook of Mathematical Functions*. Dover Publications, New York, NY), 1964. 12, 13

[96] M. G. House. Analytic model for electrostatic fields in surface-electrode ion traps. *Phys. Rev. A*, 78(3):033402, Sept. 2008. 16, 17

[97] J. H. Wesenberg. Electrostatics of surface-electrode ion traps. *Phys. Rev. A*, 78(6):063410, Dec. 2008. 16, 109

[98] D. Hucul, M. Yeo, W. K. Hensinger, J. Rabchuk, S. Olmschenk, and C. Monroe. On the transport of atomic ions in linear and multidimensional ion trap arrays. *Quant. Inf. Comp.*, 8(6&7):501–578, 2008. 18, 28, 163

[99] J. M. Amini, H. Uys, J. H. Wesenberg, S. Seidelin, J. Britton, J. J. Bollinger, D. Leibfried, C. Ospelkaus, A. P. VanDevender, and D. J. Wineland. Toward scalable ion traps for quantum information processing. *New J. Phys.*, 12:033031, 2010. 19, 80, 83, 100, 101, 115

[100] D. T. C. Allcock, J. A. Sherman, D. N. Stacey, A. H. Burrell, M. J. Curtis, G. Imreh, N. M. Linke, D. J. Szwer, S. C. Webster, A. M. Steane, and D. M. Lucas. Implementation of a symmetric surface-electrode ion trap with field compensation using a modulated Raman effect. *New J. Phys.*, 12:053026, 2010. 19, 21, 83, 95, 97

[101] J. D. Siverns, S. Weidt, K. Lake, B. Lekitsch, M. D. Hughes, and W. K. Hensinger. Optimization of two-dimensional ion trap arrays for quantum simulation. *New J. Phys.*, 14(8):085009, 2012. 19, 72, 81, 118, 149

[102] R. C. Sterling, H. Rattanasont, S. Weidt, K. Lake, P. Srinivasan, S. C. Webster, M. Kraft, and W. K. Hensinger. Two-dimensional ion trap lattice on a microchip. *arXiv:1302.3781*, Feb. 2013. 19, 53, 92, 99, 214

[103] A. Nizamani and W. Hensinger. Optimum electrode configurations for fast ion separation in microfabricated surface ion traps. *Appl. Phys. B*, 106(2):327–338, 2012. 20, 21, 112, 127

[104] J. Siverns, L. Simkins, S. Weidt, and W. Hensinger. On the application of radio frequency voltages to ion traps via helical resonators. *Appl. Phys. B*, 107(4):921–934, 2012. 21, 55, 56, 74

[105] P. Fitzpatrick. *Advanced Calculus: A Course in Mathematical Analysis*. PWS Publishing Company, 1996. 21

[106] M. Madsen, W. Hensinger, D. Stick, J. Rabchuk, and C. Monroe. Planar ion trap geometry for microfabrication. *Appl. Phys. B*, 78(5):639–651, 2004. 23

[107] F. G. Major and H. G. Dehmelt. Exchange-collision technique for the rf spectroscopy of stored ions. *Phys. Rev.*, 170:91–107, June 1968. 23

[108] A. Drakoudis, M. Söllner, and G. Werth. Instabilities of ion motion in a linear paul trap. *Int. J. Mass Spectrom.*, 252(1):61–68, 2006. 23, 24

[109] L. Peng, S. E. Parker, and J. J. Bollinger. Simulation of non-adiabaticity in surface electrode traps. In *Workshop on Ion Trap Technology, Boulder*, Feb. 2011. 24, 25

[110] J. Mikosch, U. Frühling, S. Trippel, D. Schwalm, M. Weidemüller, and R. Wester. Evaporation of buffer-gas-thermalized anions out of a multipole rf ion trap. *Phys. Rev. Lett.*, 98:223001, May 2007. 24, 25

[111] Y.-S. Liao, S.-W. Chyuan, and J.-T. Chen. FEM versus BEM. *IEEE Circuits Devices Mag.*, 20(5):25–34, 2004. 28

[112] K. Singer, U. Poschinger, M. Murphy, P. Ivanov, F. Ziesel, T. Calarco, and F. Schmidt-Kaler. Colloquium: Trapped ions as quantum bits: Essential numerical tools. *Rev. Mod. Phys.*, 82:2609–2632, Sept. 2010. 28

[113] R. C. Sterling. *Ytterbium ion trapping and microfabrication of ion trap arrays*. Ph.d. thesis, 2011. 28, 45, 53, 56, 124

[114] J. H. Wesenberg, R. J. Epstein, D. Leibfried, R. B. Blakestad, J. Britton, J. P. Home, W. M. Itano, J. D. Jost, E. Knill, C. Langer, R. Ozeri, S. Seidelin, and D. J. Wineland. Fluorescence during Doppler cooling of a single trapped atom. *Phys. Rev. A*, 76(5):053416, Nov. 2007. 30, 62, 63, 69, 214, 216

[115] D. J. Wineland and W. M. Itano. Laser cooling. *Physics Today*, 40(6):34–40, 1987. 31

[116] D. Wineland, C. Monroe, W. Itano, B. King, D. Leibfried, D. Meekhof, C. Myatt, and C. Wood. Experimental primer on the trapped ion quantum computer. *Fortschr. Phys.*, 46(4-5):363–390, 1998. 32, 33, 55

[117] Q. A. Turchette, D. Kielpinski, B. E. King, D. Leibfried, D. M. Meekhof, C. J. Myatt, M. A. Rowe, C. A. Sackett, C. S. Wood, W. M. Itano, C. Monroe, and D. J. Wineland. Heating of trapped ions from the quantum ground state. *Phys. Rev. A*, 61:063418, May 2000. 32, 55, 83

[118] L. Deslauriers, S. Olmschenk, D. Stick, W. K. Hensinger, J. Sterk, and C. Monroe. Scaling and suppression of anomalous heating in ion traps. *Phys. Rev. Lett.*, 97:103007, Sept. 2006. 33, 82, 83

[119] J. Labaziewicz, Y. Ge, P. Antohi, D. Leibrandt, K. R. Brown, and I. L. Chuang. Suppression of heating rates in cryogenic surface-electrode ion traps. *Phys. Rev. Lett.*, 100:013001, Jan. 2008. 33, 83, 95, 96, 97

[120] J. Labaziewicz, Y. Ge, D. R. Leibrandt, S. X. Wang, R. Shewmon, and I. L. Chuang. Temperature dependence of electric field noise above gold surfaces. *Phys. Rev. Lett.*, 101:180602, Oct. 2008. 33, 82, 83, 97

[121] D. T. C. Allcock, L. Guidoni, T. P. Harty, C. J. Ballance, M. G. Blain, A. M. Steane, and D. M. Lucas. Reduction of heating rate in a microfabricated ion trap by pulsed-laser cleaning. *New J. Phys.*, 13(12):123023, 2011. 33, 80, 82

[122] J. R. de Laeter, J. K. Böhlke, P. D. Bièvre, H. Hidaka, H. S. Peiser, K. J. R. Rosman, and P. D. P. Taylor. Atomic weights of the elements: Review 2000. *Pure Appl. Chem.*, 75:683–800, 2000. 33

[123] A. H. Nizamani, J. J. McLoughlin, and W. K. Hensinger. Doppler-free Yb spectroscopy with the fluorescence spot technique. *Phys. Rev. A*, 82:043408, Oct. 2010. 34, 61

[124] S. Olmschenk. *Quantum teleportation between distant matter qubits.* Ph.d. thesis, 2009. 34, 36, 37

[125] P. J. Lee. *Quantum information processing with two trapped cadmium ions.* Ph.d. thesis, 2006. 38

[126] C. Monroe, D. M. Meekhof, B. E. King, S. R. Jefferts, W. M. Itano, D. J. Wineland, and P. Gould. Resolved-sideband Raman cooling of a bound atom to the 3D zero-point energy. *Phys. Rev. Lett.*, 75:4011–4014, Nov. 1995. 38

[127] F. Mintert and C. Wunderlich. Ion-trap quantum logic using long-wavelength radiation. *Phys. Rev. Lett.*, 87:257904, Nov. 2001. 38

[128] L. Ricci, M. Weidemüller, T. Esslinger, A. Hemmerich, C. Zimmermann, V. Vuletic, W. König, and T. W. Hänsch. A compact grating-stabilized diode laser system for atomic physics. *Opt. Commun.*, 117:541–549, Feb. 1995. 41

[129] J. McLoughlin. *Development and Implementation of an Yb+ Ion Trap Experiment Towards Coherent Manipulation and Entanglement.* Ph.d. thesis, 2011. 42

[130] S. Kraft, A. Deninger, C. Trück, J. Fortágh, F. Lison, and C. Zimmermann. Rubidium spectroscopy at 778-780 nm with a distributed feedback laser diode. *Laser Phys. Lett.*, 2(2):71, 2005. 45

[131] J. D. Siverns. *Yb ion trap experimental set-up and two-dimensional ion trap surface array design towards analogue quantum simulations.* Ph.d. thesis, 2011. 46

[132] K. Mathia. *Robotics for Electronics Manufacturing; Principles and Applications in Cleanroom Automation.* Cambridge University Press, 1995. 49

[133] K. Odaka and S. Ueda. Dependence of outgassing rate on surface oxide layer thickness in type 304 stainless steel before and after surface oxidation in air. *Vacuum*, 47(6-8):689–692, 1996. 49

[134] M. Audi. Pumping speed of sputter ion pumps. *Vacuum*, 38(8-10):669–671, 1988. 50

[135] A. H. Nizamani. *Yb+ ion trapping and optimum planar trap geometries for scalable quantum technology.* Ph.d. thesis, 2011. 53

[136] D. J. Berkeland and M. G. Boshier. Destabilization of dark states and optical spectroscopy in Zeeman-degenerate atomic systems. *Phys. Rev. A*, 65:033413, Feb. 2002. 61

[137] D. J. Berkeland, J. D. Miller, J. C. Bergquist, W. M. Itano, and D. J. Wineland. Minimization of ion micromotion in a Paul trap. *J. Appl. Phys.*, 83(10):5025–5033, 1998. 63, 68, 79

[138] J. Britton. *Microfabrication techniques for trapped ion quantum information processing.* Ph.d. thesis, Boulder, 2008. 68, 83

[139] E. Brama, A. Mortensen, M. Keller, and W. Lange. Heating rates in a thin ion trap for microcavity experiments. *Appl. Phys. B*, 107(4), 2012. 69

[140] R. G. DeVoe, J. Hoffnagle, and R. G. Brewer. Role of laser damping in trapped ion crystals. *Phys. Rev. A*, 39:4362–4365, May 1989. 69

[141] R. C. Sterling, M. D. Hughes, C. J. Mellor, and W. K. Hensinger. Increased surface flashover voltage in microfabricated devices. *Appl. Phys. Lett.*, 103(14):143504, 2013. 71, 72, 73, 122, 184

[142] D. Stick, K. M. Fortier, R. Haltli, C. Highstrete, D. L. Moehring, C. Tigges, and M. G. Blain. Demonstration of a microfabricated surface electrode ion trap. *arXiv:1008.0990v2*, Aug. 2010. 71, 102

[143] S. Kuehn, R. F. Loring, and J. A. Marohn. Dielectric fluctuations and the origins of noncontact friction. *Phys. Rev. Lett.*, 96:156103, Apr. 2006. 72, 82

[144] J. Mueller, D. Pyle, I. Chakraborty, R. Ruiz, W. Tang, and R. Lawton. Feasibility study of MEMS-based accelerator grid systems for micro-ion engines: Electric breakdown characteristics. *AIAA J. Propul. Power.*, 1999. 73

[145] V. K. Agarwal and V. K. Srivastava. Thickness dependence of breakdown field in thin films. *Thin Solid Films*, 8:377–381, 1971. 73

[146] V. K. Agarwal and V. K. Srivastava. Thickness dependent studies of dielectric breakdown in Langmuir thin molecular films. *Solid State Commun.*, 12:829–834, 1973. 73

[147] D. Mangalaraj, M. Radhakrishnan, and C. Balasubramanian. Electrical conduction and breakdown properties of silicon nitride films. *J. Mater. Sci.*, 17:1474–1478, 1982. 73

[148] H. K. Kim and F. G. Shi. Thickness dependent dielectric strength of a low-permittivity dielectric film. *IEEE Trans. Dielectr. Electr. Insul*, 8(2):248–252, 2001. 73

[149] H. Zhou, F. Shi, and B. Zhao. Thickness dependent dielectric breakdown of PECVD low-k carbon doped silicon dioxide dielectric thin films: Modeling and experiments. *Microelectron. J.*, 34:259–264, 2003. 73

[150] H. Bartzsch, D. Glöß, B. Böcher, P. Frach, and K. Goedicke. Properties of SiO_2 and Al_2O_3 films for electrical insulation applications deposited by reactive pulse magnetron sputtering. *Surf. Coat. Technol.*, 174-175:774–778, 2003. 73

[151] H. Johnson and M. Graham. *High Speed Signal Propagation: Advanced Black Magic.* Prentice Hall, 2003. 74

[152] K. C. Gupta, R. Garg, I. J. Bahl, and P. Bhartia. *Microstrip Lines and Slotlines.* Artech House Microwave Library, 1996. 75

[153] S. C. Thierauf. *High-speed circuit board signal integrity.* Artech House Publishers, 2004. 75

[154] F. W. Grover. *Inductance Calculations.* Dover Publications, 2009. 75

[155] S. Karataş. Studies on electrical and the dielectric properties in MS structures. *J. Non-Cryst. Solids*, 354:3606–3611, 2008. 76

[156] A. B. Selçuk. On the dielectric characteristics of Au/SnO_2/n-Si capacitors. *Physica B*, 396:181–186, 2007. 76

[157] Z. Heng-Da, C. Guang-Chao, L. Cheng-Ming, T. Wei-Zhong, and L. Fan-Xiu. Dielectric characterization of free-standing diamond films. *Chin. Phys. Lett.*, 19(11):1695, 2002. 76

[158] S. L. Heidger, N. J. Baraty, and J. A. Weimer. CVD diamond for high power and high temperature electronics. In *AFRL/PRPE*. Wright-Patterson, 2001. 76

[159] A. Tataroğlu. Electrical and dielectric properties of MIS Schottky diodes at low temperatures. *Microelectron. Eng.*, 83:2551–2557, Nov. 2006. 76

[160] J. Krupka, J. Breeze, A. Centeno, N. Alford, T. Claussen, and L. Jensen. Measurements of permittivity, dielectric loss tangent, and resistivity of float-zone silicon at microwave frequencies. *IEEE Trans. Microw. Theory Techn.*, 54(11), 2006. 76

[161] I. Dökme, c. Altindal, and M. Gökçen. Frequency and gate voltage effects on the dielectric properties of Au/SiO_2/n-Si structures. *Microelectron. Eng.*, 85:1910–1914, Sept. 2008. 76, 77

[162] M. M. Bülbül. Frequency and temperature dependent dielectric properties of Al/Si_3N_4/p-Si(100) MIS structure. *Microelectron. Eng.*, 84:124–128, Jan. 2007. 76

[163] N. Tomozeiu. Electrical conduction and dielectric relaxation of a-SiO_x (0 <x< 2) thin films deposited by reactive RF magnetron sputtering. *Thin Solid Films*, 516:8199–8204, 2008. 76

[164] J. D. Kraus and D. A. Fleisch. *Electromagnetics with Applications*. McGraw-Hill Science/Engineering/Math, 5th edition, 1999. 76

[165] S. Westerlund and L. Ekstam. Capacitor theory. *IEEE Trans. Dielectr. Electr. Insul*, 1(5):826–839, 1994. 77

[166] P. Horowitz and W. Hill. *The Art of Electronics*. Cambridge University Press, 1989. 78

[167] D. Allcock, T. Harty, H. Janacek, N. Linke, C. Ballance, A. Steane, D. Lucas, J. Jarecki, R.L., S. Habermehl, M. Blain, D. Stick, and D. Moehring. Heating rate and electrode charging measurements in a scalable, microfabricated, surface-electrode ion trap. *Appl. Phys. B*, 107(4):913–919, 2012. 79, 92

[168] M. Harlander, M. Brownnutt, W. Hänsel, and R. Blatt. Trapped-ion probing of light-induced charging effects on dielectrics. *New J. Phys.*, 12(9):093035, 2010. 79, 94

[169] H. L. Skriver and N. M. Rosengaard. Surface energy and work function of elemental metals. *Phys. Rev. B*, 46:7157–7168, Sept. 1992. 79

[170] R. G. DeVoe and C. Kurtsiefer. Experimental study of anomalous heating and trap instabilities in a microscopic ^{137}Ba ion trap. *Phys. Rev. A*, 65:063407, June 2002. 79, 83

[171] J. Britton, D. Leibfried, J. A. Beall, R. B. Blakestad, J. J. Bollinger, J. Chiaverini, R. J. Epstein, J. D. Jost, D. Kielpinski, C. Langer, R. Ozeri, R. Reichle, S. Seidelin, N. Shiga, J. H. Wesenberg, and D. J. Wineland. A microfabricated surface-electrode ion trap in silicon. *arXiv:quant-ph/0605170*, Feb. 2008. 80, 115

[172] K. Mølmer and A. Sørensen. Multiparticle entanglement of hot trapped ions. *Phys. Rev. Lett.*, 82(9):1835–1838, Mar. 1999. 81

[173] P. J. Lee, K.-A. Brickman, L. Deslauriers, P. C. Haljan, L.-M. Duan, and C. Monroe. Phase control of trapped ion quantum gates. *J. Opt. B.*, 7(10):S371–S383, 2005. 81

[174] J. J. Garcia-Ripoll, P. Zoller, and J. I. Cirac. Speed optimized two-qubit gates with laser coherent control techniques for ion trap quantum computing. *Phys. Rev. Lett.*, 91:157901, Oct. 2003. 81, 111

[175] S. X. Wang, Y. Ge, J. Labaziewicz, E. Dauler, K. Berggren, and I. L. Chuang. Superconducting microfabricated ion traps. *Appl. Phys. Lett.*, 97:244102, 2010. 82, 83, 95, 96, 97

[176] N. Daniilidis, S. Narayanan, S. A. Möller, R. Clark, T. E. Lee, P. J. Leek, A. Wallraff, S. Schulz, F. Schmidt-Kaler, and H. Häffner. Fabrication and heating rate study of microscopic surface electrode ion traps. *New J. Phys.*, 13(1):013032, 2011. 82, 83

[177] R. Dubessy, T. Coudreau, and L. Guidoni. Electric field noise above surfaces: A model for heating-rate scaling law in ion traps. *Phys. Rev. A*, 80:031402, Sept. 2009. 82

[178] B. C. Stipe, H. J. Mamin, T. D. Stowe, T. W. Kenny, and D. Rugar. Noncontact friction and force fluctuations between closely spaced bodies. *Phys. Rev. Lett.*, 87:096801, Aug. 2001. 82

[179] A. I. Volokitin, B. N. J. Persson, and H. Ueba. Enhancement of noncontact friction between closely spaced bodies by two-dimensional systems. *Phys. Rev. B*, 73:165423, Apr. 2006. 82

[180] N. A. Robertson, J. R. Blackwood, S. Buchman, R. L. Byer, J. Camp, D. Gill, J. Hanson, S. Williams, and P. Zhou. Kelvin probe measurements: Investigations of the patch effect with applications to ST-7 and LISA. *Classical. Quant. Grav.*, 23(7):2665, 2006. 82

[181] A. Safavi-Naini, P. Rabl, P. F. Weck, and H. R. Sadeghpour. Microscopic model of electric-field-noise heating in ion traps. *Phys. Rev. A*, 84:023412, Aug. 2011. 82

[182] F. Diedrich, J. C. Bergquist, W. M. Itano, and D. J. Wineland. Laser cooling to the Zero-Point Energy of motion. *Phys. Rev. Lett.*, 62(4):403–406, Jan. 1989. 83

[183] C. Roos, T. Zeiger, H. Rohde, H. C. Nägerl, J. Eschner, D. Leibfried, F. Schmidt-Kaler, and R. Blatt. Quantum state engineering on an optical transition and decoherence in a paul trap. *Phys. Rev. Lett.*, 83(23):4713–4716, Dec. 1999. 83

[184] S. A. Schulz, U. Poschinger, F. Ziesel, and F. Schmidt-Kaler. Sideband cooling and coherent dynamics in a microchip multi-segmented ion trap. *New J. Phys.*, 10(045007):15, 2008. 83

[185] C. Tamm, D. Engelke, and V. Bühner. Spectroscopy of the electric-quadrupole transition ${}^2S_{1/2}(f = 0)$-${}^2D_{3/2}(f = 2)$ in trapped ${}^{171}Yb^+$. *Phys. Rev. A*, 61:053405, Apr 2000. 83

[186] M. A. Rowej, A. Ben-Kish, B. Demarco, D. Leibfried, V. Meyer, J. Beall, J. Britton, J. Hughes, W. M. Itano, B. Jelenković, C. Langer, T. Rosenband, and D. J. Wineland. Transport of quantum states and separation of ions in a dual RF ion trap. *Quant. Inf. Comp.*, 2(4):257–271, June 2002. 83

[187] R. J. Epstein, S. Seidelin, D. Leibfried, J. H. Wesenberg, J. J. Bollinger, J. M. Amini, R. B. Blakestad, J. Britton, J. P. Home, W. M. Itano, J. D. Jost, E. Knill, C. Langer, R. Ozeri, N. Shiga, and D. J. Wineland. Simplified motional heating rate measurements of trapped ions. *Phys. Rev. A*, 76(3):033411, Sept. 2007. 83

[188] J. Britton, D. Leibfried, J. A. Beall, R. B. Blakestad, J. H. Wesenberg, and D. J. Wineland. Scalable arrays of rf paul traps in degenerate Si. *Appl. Phys. Lett.*, 95:173102, Oct. 2009. 83, 98, 99

[189] E. van de Ven, I.-W. Connick, and A. Harrus. Advantages of dual frequency PECVD for deposition of ILD and passivation films. In *VMIC, 1990. Proc., IEEE*, pages 194–201, 1990. 89

[190] P. Dixit and J. Miao. Aspect-ratio-dependent copper electrodeposition technique for very high aspect-ratio through-hole plating. *J. Electrochem. Soc.*, 153(6):G552–G559, 2006. 89

[191] K. R. Brown, R. J. Clark, J. Labaziewicz, P. Richerme, D. R. Leibrandt, and I. L. Chuang. Loading and characterization of a printed-circuit-board atomic ion trap. *Phys. Rev. A*, 75(1):015401, Jan. 2007. 93, 94

[192] C. E. Pearson, D. R. Leibrandt, W. S. Bakr, W. J. Mallard, K. R. Brown, and I. L. Chuang. Experimental investigation of planar ion traps. *Phys. Rev. A*, 73(3):032307, Mar. 2006. 94

[193] J.-S. Chenard, C. Y. Chu, Z. Žilić, and M. Popović. Design methodology for wireless nodes with printed antennas. *Des. Aut. Con. 2005. Proceedings. 42nd*, pages 291–

296, June 2005. 94

[194] F. Splatt, M. Harlander, M. Brownnutt, F. Zähringer, R. Blatt, and W. Hänsel. Deterministic reordering of 40Ca+ ions in a linear segmented paul trap. *New J. Phys.*, 11:103008, Oct. 2009. 94

[195] D. R. Leibrandt, R. J. Clark, J. Labaziewicz, P. Antohi, W. Bakr, K. R. Brown, and I. L. Chuang. Laser ablation loading of a surface-electrode ion trap. *Phys. Rev. A.*, 76:055403, Nov. 2007. 94

[196] S. X. Wang, J. Labaziewicz, Y. Ge, R. Shewmon, and I. L. Chuang. Individual addressing of ions using magnetic field gradients in a surface-electrode ion trap. *Appl. Phys. Lett.*, 94:094103, 2009. 95, 97

[197] D. Stick. *Fabrication and Characterization of Semiconductor Ion Traps for Quantum Information Processing.* Ph.d. thesis, 2007. 95, 97, 98, 102

[198] N. Daniilidis, T. Lee, R. Clark, S. Narayanan, and H. Häffner. Wiring up trapped ions to study aspects of quantum information. *J. Phys. B: At. Mol. Opt. Phys.*, 42(15):154012, 2009. 97

[199] D. Leibrandt, J. Labaziewicz, R. Clark, I. Chuang, R. Epstein, C. Ospelkaus, J. Wesenberg, J. Bollinger, D. Leibfried, D. Wineland, D. Stick, J. Stick, C. Monroe, C.-S. Pai, Y. Low, R. Frahm, and R. Slusher. Demonstration of a scalable, multiplexed ion trap for quantum information processing. *Quant. Inf. Comp.*, 9:0901–0919, Nov. 2009. 102

[200] A. M. Stephens, A. G. Fowler, and L. C. L. Hollenberg. Universal fault tolerant quantum computation on bilinear nearest neighbor arrays. *Quant. Inf. Comp.*, 8(3):330–344, Mar. 2008. 107

[201] A. G. Fowler and S. J. Devitt. A bridge to lower overhead quantum computation. *arXiv:1209.0510*, Sept. 2012. 107

[202] K. R. Brown, A. C. Wilson, Y. Colombe, C. Ospelkaus, A. M. Meier, E. Knill, D. Leibfried, and D. J. Wineland. Single-qubit-gate error below 10^{-4} in a trapped ion. *Phys. Rev. A*, 84:030303, Sept. 2011. 107

[203] D. T. C. Allcock, T. P. Harty, C. J. Ballance, B. C. Keitch, N. M. Linke, D. N. Stacey, and D. M. Lucas. A microfabricated ion trap with integrated microwave circuitry. *Appl. Phys. Lett.*, 102(4):044103, 2013. 107

[204] D. Gandolfi, M. Niedermayr, M. Kumph, M. Brownnutt, and R. Blatt. Compact radio-frequency resonator for cryogenic ion traps. *Rev. Sci. Instrum.*, 83(8):084705, 2012. 110

[205] G. G. Bush. The complex permeability of a high purity yttrium iron garnet (YIG) sputtered thin film. *J. Appl. Phys.*, 73(10):6310–6311, 1993. 110

[206] H. Johari and F. Ayazi. High-density embedded deep trench capacitors in silicon with enhanced breakdown voltage. *IEEE Trans. Compon. Packag. Manuf. Technol.*, 32(4):808–815, 2009. 110

[207] R. Patti. Three-dimensional integrated circuits and the future of system-on-chip designs. *Proc. IEEE*, 94(6):1214–1224, 2006. 110

[208] N. Timoney, I. Baumgart, M. Johanning, A. F. Varón, M. B. Plenio, A. Retzker, and C. Wunderlich. Quantum gates and memory using microwave-dressed states. *Nature*, 476, Aug. 2011. 112

[209] S. C. Webster, S. Weidt, K. Lake, J. J. McLoughlin, and W. K. Hensinger. Simple manipulation of a microwave dressed-state ion qubit. *Phys. Rev. Lett.*, 111:140501, Oct. 2013. 112

[210] E. Colgan, B. Furman, M. Gaynes, W. Graham, N. LaBianca, J. Magerlein, R. Polastre, M.-B. Rothwell, R. J. Bezama, R. Choudhary, K. Marston, H. Toy, J. Wakil, J. Zitz, and R. Schmidt. A practical implementation of silicon microchannel coolers for high power chips. *IEEE Trans. Compon. Packag. Manuf. Technol.*, 30(2):218–225, 2007. 113

[211] C. Piemonte, R. Battiston, M. Boscardin, G.-F. Dalla Betta, A. Del Guerra, N. Dinu, A. Pozza, and N. Zorzi. Characterization of the first prototypes of silicon photomultiplier fabricated at ITC-irst. *IEEE Trans. Nucl. Sci*, 54(1):236–244, 2007. 115, 144

[212] E. Cicek, Z. Vashaei, R. McClintock, C. Bayram, and M. Razeghi. Geiger-mode operation of ultraviolet avalanche photodiodes grown on sapphire and free-standing GaN substrates. *Appl. Phys. Lett.*, 96(26):261107, 2010. 115, 144

[213] F. Fatemi, M. Bashkansky, and S. Moore. Side-illuminated hollow-core optical fiber for atom guiding. *Opt. Express*, 13(13):4890–4895, June 2005. 115

[214] J. H. Wesenberg. Ideal intersections for radio-frequency trap networks. *Phys. Rev. A*, 79(1):013416, Jan. 2009. 125

[215] J. Dryzek. Migration of vacancies in deformed silver studied by positron annihilation. *Mater. Sci. Forum*, 255 - 257:533–535, 1997. 134

[216] J. Lloyd, J. Clemens, and R. Snede. Copper metallization reliability. *Microelectron. Reliab.*, 39(11):1595 – 1602, 1999. 134

[217] S. Kilgore, C. Gaw, H. Henry, D. Hill, and D. Schroder. Electromigration of electroplated gold interconnects. *MRS Proceedings*, 863, 1 2005. 134

[218] B. Vermeersch and G. D. Mey. Influence of substrate thickness on thermal impedance of microelectronic structures. *Microelectron. Reliab.*, 47(23):437 – 443, 2007. 136

[219] J. F. Shackelford and W. Alexander. *Materials Science and Engineering Handbook*. Taylor and Francis(CRC Press), 2000. 136, 157

[220] A. Roy and C. M. Tan. Very high current density package level electromigration test for copper interconnects. *J. Appl. Phys.*, 103(9), 2008. 138

[221] E. Taglauer. Surface cleaning using sputtering. *Appl. Phys. A*, 51(3):238–251, 1990. 158

[222] E. Taglauer, W. Heiland, and J. Onsgaard. Ion beam induced desorption of surface layers. *Nucl. Instr. Meth.*, 168(13):571 – 577, 1980. 158

[223] R. Bowler, U. Warring, J. W. Britton, B. C. Sawyer, and J. Amini. Arbitrary waveform generator for quantum information processing with trapped ions. *Rev. Sci. Instrum.*, 84(3), 2013. 163

[224] M. Tanveer Baig, M. Johanning, A. Wiese, S. Heidbrink, M. Ziolkowski, and C. Wunderlich. A scalable, fast and multichannel arbitrary waveform generator. *arXiv:1307.5672*, July 2013. 163

[225] S. P. Vaclav Papez. Low noise dc power supplies. In *XIX IMEKO*, pages 809–814, 2009. 164

[226] R. Berman, P. R. W. Hudson, and M. Martinez. Nitrogen in diamond: Evidence from thermal conductivity. *J. Phys. C: Solid State Physics*, 8(21):L430, 1975. 174

[227] S. Torrengo, A. Miotello, L. Minati, I. Bernagozzi, M. Ferrari, M. Dipalo, E. Kohn, and G. Speranza. The role of oxygen in the one step amination process of nanocrystalline diamond surface. *Diam. Relat. Mater.*, 20(7):990–994, 2011. 175

[228] H. Guo, Y. Qi, and X. Li. Adhesion at diamond/metal interfaces: A density functional theory study. *J. Appl. Phys.*, 107(3), 2010. 175

[229] Y. Qi and L. G. Hector. Hydrogen effect on adhesion and adhesive transfer at aluminum/diamond interfaces. *Phys. Rev. B*, 68:201403, Nov. 2003. 175

[230] X.-G. Wang and J. R. Smith. Copper/diamond adhesion and hydrogen termination. *Phys. Rev. Lett.*, 87:186103, Oct. 2001. 175

[231] G. Ding, H. Mao, Y. Cai, Y. Zhang, X. Yao, and X. Zhao. Micromachining of CVD diamond by RIE for MEMS applications. *Diam. Relat. Mater.*, 14(9):1543 – 1548, 2005. 179

[232] S. Kiyohara, Y. Yagi, and K. Mori. Plasma etching of CVD diamond films using an ECR-type oxygen source. *Nanotechnology*, 10(4):385, 1999. 179

[233] P. Leech, G. Reeves, and A. Holland. Reactive ion etching of diamond in CF_4, O_2, O_2 and Ar-based mixtures. *J. Mater. Sci.*, 36(14):3453–3459, 2001. 179

[234] T. Yamada, H. Yoshikawa, H. Uetsuka, S. Kumaragurubaran, N. Tokuda, and S. ichi Shikata. Cycle of two-step etching process using ICP for diamond MEMS applications. *Diam. Relat. Mater.*, 16(47):996 – 999, 2007. 180

[235] K. Williams, K. Gupta, and M. Wasilik. Etch rates for micromachining processing-part ii. *J. Microelectromech. S.*, 12(6):761–778, 2003. 181, 225

[236] L. Hamelin, S. Ledain, E. Dufour-Gergam, and C. Bunel. Copper electroplating process for passive Si-based system in package applications. In *IMAPS*, Nov. 2007. 182, 183

[237] R. W. Robinett. Quantum and classical probability distributions for position and momentum. *Am. J. Phys.*, 63(9):823–832, 1995. 215

Appendix A

Theoretical Description of Ion Fluorescence During Doppler Recooling

Based on the model developed in [114] and the Doppler cooling described in section 2.2.1 a theoretical description of the observed fluorescence changes during recooling will be given. Approximations can be made if the observed fluorescence change is dominated by recooling in one motional axis, which is the case if the secular frequency in one axis is much lower compared to the other two ($\omega_z << \omega_{x,y}$) as the heating in this axis will be much higher ($dN/dt \sim \omega^2$). In most ion traps the confinement in the axial direction is provided by static potentials and can therefore be adjusted appropriately.

In cases where all secular frequencies are very similar [102] one can still use this method if the 369nm laser beam is guided onto the ion almost parallel to one principal axis (x). As the model is based on changes of the Doppler shift ($\Delta_{Dop} = -k_x v_x - k_y v_y - k_z v_z$, $k_x >> k_y, k_z$), the other two wavevectors ($k_{y,z}$) will be minimal and the impact of the other axes on the detected fluorescence evolution will be small.

Following [114], the fluorescence rate dN/dt during Doppler cooling is given by

$$dN/dt(\Delta_{Dop}) = \Gamma \frac{s/2}{1 + s + (2\Delta_{eff}/\Gamma)} \tag{A.1}$$

We can average the fluorescence rate over one secular oscillation of the trapped ion as long as the change in Doppler shift Δ_{Dop} is small compared to the oscillation period. We

have to integrate $dN/dt(\Delta_{Dop})$ over one oscillation period, but also need to consider that the Doppler shift follows a probability density $P_{Doppler}(\Delta_{Dop})$ during the oscillation. The probability density $P_{Doppler}(\Delta_{Dop})$ depends on the maximal motional energy E and follows as [237],

$$\begin{aligned} P_{Doppler}(\Delta_{Dop}) &= \frac{N}{2\pi\sqrt{\sqrt{2E/m}k_z - \Delta_{Dop}}} \text{ for } \mid \Delta_{Dop} \mid < \sqrt{2E/m}k_z \\ &= 0 \text{ for } \mid \Delta_{Dop} \mid \geq \sqrt{2E/m}k_z \end{aligned}$$

Integrating the instantaneous scatter rate $dN/dt(\Delta_{Dop})$ over all possible Δ_{Dop} gives the average scatter rate for a certain energy E during one oscillation.

$$\langle dN/dt(\Delta_{Dop})\rangle = \int \Gamma P_{Doppler}(\Delta_{Dop})\rho_{excited}(\Delta + \Delta_{Dop})d\Delta_{Dop} \tag{A.2}$$

Looking at the momentum transfer on the ion resulting from one scattering event, $p = \hbar k_z$ we can write the energy change during one event as $dE/dN = \hbar k_z v_z = -\hbar\Delta_D$. The average energy can than be calculated in a similar way to the averaged scatter rate,

$$\langle dE/dt(\Delta_{Dop})\rangle = \int -\hbar\Delta_{Dop}\Gamma P_{Doppler}(\Delta_{Dop})\rho_{excited}(\Delta + \Delta_{Dop})d\Delta_{Dop} \tag{A.3}$$

Both integrals will be solved for the case where the overlap of probability density $P_{Doppler}(\Delta_{Dop})$ with Lorentzian linewidth L is low, see Fig. A.1 . This is the case for a 'hot' ion with high motional energy as illustrated in Fig. A.1 (a). The solutions for the integrals then take the form:

$$\langle dN/dt\rangle = \frac{1}{\sqrt{2E/m}k_z}\frac{s/2\Gamma^2\sqrt{1+s}}{1+s} \tag{A.4}$$

$$\langle dE/dt\rangle = \frac{\hbar\Delta}{\sqrt{2E/m}k_z}\frac{s/2\Gamma^2\sqrt{1+s}}{1+s} \tag{A.5}$$

This assumption is only valid if the ion has acquired a sufficient amount of motional energy before recooling starts. While the motional energy E was considered to be constant over one oscillation, the change of motional energy during the Doppler recooling is what

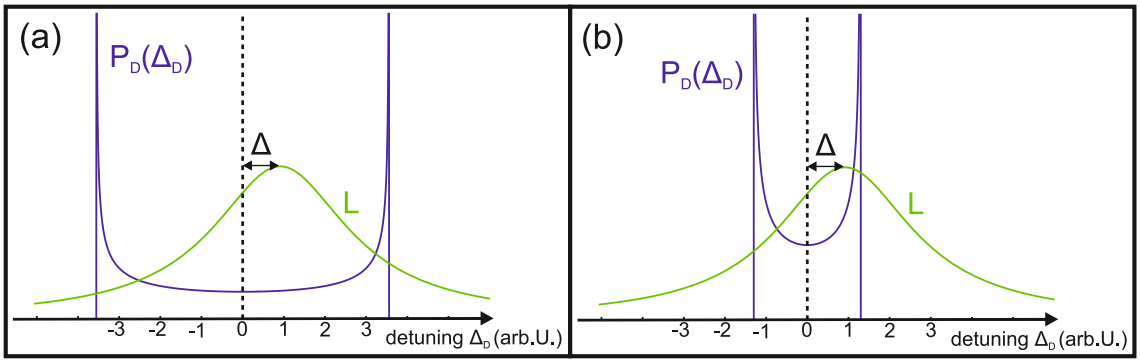


Figure A.1: Lorentzian line profile L shifted by Δ with respect to the laser wavelength and Doppler shift probability P_D are shown for a 'hot' ion with high motional quanta (a), where the approximations made are valid. For a 'cool' ion, shown in (b), the approximation is not valid anymore.

determines the observed fluorescence count evolution. Integrating $\langle dE/dt \rangle$ over time t results in [114],

$$E(E_0, t) = [E_0^{3/2} + \frac{3s\Gamma^2\hbar\Delta}{8\sqrt{1+s}\sqrt{2/mk_z}}]^{2/3} \tag{A.6}$$

Knowing the motional energy of the ion at any given time $E(E_0, t)$ allows us to express the scattering rate during the recooling process as:

$$\langle dN/dt(E(E_0, t)) \rangle = \frac{s\Gamma^2}{4\sqrt{(1+s)E(E_0, t)2/mk_z}} \tag{A.7}$$

Starting energy E_0 is equivalent to the energy acquired by the ion during the heating period. The process of motional heating is stochastic, so E_0 follows a Maxwell-Boltzmann distribution $P_B(E_0) = E_0/\bar{E}e^{-E_0/\bar{E}}$, where $\bar{E}$ is equal to the mean motional energy acquired after a certain delay time.

Fitting a fluorescence curve recorded over many recooling cycles therefore requires the scattering rate of equation A.7 to be weighted with the distribution $P_B(E_0)$:

$$\langle dN/dt(\bar{E}) \rangle = \int_0^\infty P_B(E_0) dN/dt(E(E_0, t)) dE_0 \tag{A.8}$$

From the fitted scatter rate we can extrapolate a mean motional energy $\bar{E}$ and the corresponding amount of motional quanta $\bar{n}$.

Appendix B

Detailed Microfabrication Processes

B.1 Plasma Etch and Ash Process Details

Oxygen Plasma Ash

Tool Description: PVA Tepla 300 Plasma Asher
Process Gases: Oxygen (O_2) 600 ml/min
Plasma Generator: 800 W (2.45 GHz), microwave plasma generation
Chamber Pressure: $\sim$ 750 mTorr
Sample Temperature: uncontrolled, on the order of 100-200°C
Process Characteristics: Microwave oxygen plasma with very high electron mobility with no dc bias on the sample. The etch characteristics are similar to an isotropic wet etch. The oxygen plasma burns organic contaminants and photoresist with minor impact to the sample surface.

ICP Chamber Clean

Tool Description: OIPT SYS380 (Dielectric/Metal) ICP RIE Tool
Process Gases: Oxygen (O_2) 50 ml/min, Argon (Ar) 50 ml/min
Plasma Generator: 2000 W ICP power (1.8-2.2 MHz), 100 W rf (13.56 MHz)
Chamber Pressure: 20 mTorr

Sample Temperature: Carrier wafer cooled with helium flow, helium chiller set to 10 °C
Process Characteristics: Oxygen/argon plasma chamber clean designed to remove contaminants from chamber walls and carrier wafers. The 2000 W ICP power generates a highly dense plasma, 100 W rf table bias accelerates the plasma onto the carrier wafer.

ICP Oxygen Ash

Tool Description: OIPT SYS380 (Dielectric/Metal) ICP RIE Tool
Process Gases: Oxygen (O_2) 50 ml/min
Plasma Generator: 1500 W ICP power (1.8-2.2 MHz), 0-50 W rf (13.56 MHz)
Chamber Pressure: 15 mTorr
Sample Temperature: Carrier wafer cooled with helium flow, helium chiller set to 10 °C
Process Characteristics: Mild oxygen plasma clean to remove remaining fluorocarbons or photoresist on the sample surface, carrier wafer and chamber walls. Plasma is ignited with an rf table bias of 50 W, which is turned of after 20 sec stabilization time. The plasma slowly diffuses to the sample instead of being accelerated by the rf bias. A 5 min clean is sufficient to remove most of remaining fluorocarbons as indicated by the stable plasma colour [1] and dc bias level on the sample table [2] during the following ICP diamond etch.

ICP Oxide Silicone Dioxide Etch

Tool Description: OIPT SYS380 (Dielectric) ICP RIE Tool
Process Gases: Octafluorocyclobutane (C_4F_8) 34 ml/min, Oxygen (O_2) 8.5 ml/min, Fluoroform (CHF_3) 37.4 ml/min
Plasma Generator: 1500 W ICP power (1.8-2.2 MHz), 100 W rf (13.56 MHz)
Chamber Pressure: 7 mTorr
Sample Temperature: Carrier wafer cooled with helium flow, helium chiller set to 10 °C
Process Characteristics: Fluorocarbon based SiO_2 etch with an etch rate of $\sim$ 300 nm/min. Smaller samples are placed on a 6" *Si* carrier wafer and thermal conductivity between wafer and sample is improved by applying a drop of vacuum oil on the carrier wafer. Ex-

[1] changes from blue/white to light purple without clean
[2] without clean the dc bias starts at $\sim$300 V and drops to $\sim$220 V

act recipe parameters were provided by Ibrahim Sari.

ICP Oxide CVD Diamond Etch

Tool Description: OIPT SYS380 (Dielectric) ICP RIE Tool
Process Gases: Oxygen (O_2) 50 ml/min
Plasma Generator: 2000 W ICP power (1.8-2.2 MHz), 200 W rf (13.56 MHz)
Chamber Pressure: 10 mTorr
Sample Temperature: Carrier wafer cooled with helium flow, helium chiller set to 10 °C
Process Characteristics: High density and high rf bias oxygen plasma optimized to etch diamond by breaking carbon bonds and oxidizing the free carbon achieving an etch rate of ~ 290 nm/min. The SiO_2 hard mask is only eroded by the oxygen ion bombardment, which results in a high selectivity between diamond and mask.

ICP Metal Silicone Dioxide Etch

Tool Description: OIPT SYS380 (Metal) ICP RIE Tool
Process Gases: Octafluorocyclobutane (C_4F_8) 40 ml/min, Oxygen (O_2) 15 ml/min,
Plasma Generator: 1500 W ICP power (1.8-2.2 MHz), 100 W rf (13.56 MHz)
Chamber Pressure: 10 mTorr
Sample Temperature: Carrier wafer cooled with helium flow, helium chiller set to 10 °C
Process Characteristics: Altered fluorocarbon based SiO_2 etch, compatible with the available (Metal) ICP process gases, achieving an etch rate of ~ 250 μm/min. The metal ICP has to be used for all metal contaminated samples, which are also placed on a carrier wafer with vacuum oil applied to it.

RIE Photoresist Descum

Tool Description: OIPT RIE80+ Tool
Process Gases: Oxygen (O_2) 50 ml/min
Plasma Generator: 100 W rf (13.56 MHz)
Chamber Pressure: 100 mTorr
Sample Temperature: Quartz table cooled to 20°C,
Process Characteristics: A low power 30 sec RIE oxygen plasma is used to remove

residual resist in trenches of negative resist structures intended for a lift-off process. This process is similar to the Tepla oxygen ash, but can also be used for samples with deposited metal.

B.2 Plasma Deposition (PECVD) Process Details

PECVD *in situ* Nitrous Oxide Clean

Tool Description: OIPT SYS100 PECVD reactor
Process Gases: Nitrous oxide (N_2O) 500 ml/min
Plasma Generator: 50 W rf gas inlet bias (13.56 MHz)
Chamber Pressure: 1000 mTorr
Sample Temperature: Sample table is heated to 350 °C, carrier wafer and samples are placed on table 5 min prior to the start of the process
Process Characteristics: The PECVD reactor is intended for SiO_2 and Si_3N_4 deposition but can also be used to perform *in situ* plasma cleans. Nitrous oxide plasma removes organic contaminants similar to an oxygen plasma, which is avoided due to its highly volatile reaction with silane gas.

PECVD of Silicon Dioxide

Tool Description: OIPT SYS100 PECVD reactor
Process Gases: Silane (SiH_4) 8.4 ml/min, Nitrous oxide (N_2O) 80 ml/min, Nitrogen (N_2) 700 ml/min
Plasma Generator: 20 W high frequency (HF) 13.56 MHz rf gas inlet bias
Chamber Pressure: 1000 mTorr
Sample Temperature: Sample table is heated to 350 °C, carrier wafer and samples are placed on table 5 min prior to process start
Process Characteristics: Silicon dioxide deposition based on highly reactive silane and nitrous oxide plasma diluted with nitrogen, recipe parameters provided by Owain Clark. The process is a constant absorbtion and desorption of material on the hot sample surface. Process parameters are optimized for low stress and film uniformity and allow the deposition of SiO_2 of over 5 μm thickness. Deposition rate was measured to be $\sim$ 65 nm/min.

PECVD of Silicon Nitride

Tool Description: OIPT SYS100 PECVD reactor

Process Gases: Silane (SiH_4) 20 ml/min, Ammonia (NH_3) 35 ml/min, Nitrogen (N_2) 500 ml/min

Plasma Generator: 30 W low frequency (LF) 50 kHz and 20 W high frequency (HF) 13.56 MHz rf gas inlet bias

Chamber Pressure: 875 mTorr

Process Characteristics: A cyclic LF and HF process used to deposit highly dense low stress silicon nitride, process parameters were optimized by Owain Clark. The process alternates between an HF and LF phase every 10 sec. During the LF cycle the deposited layer is densified, which is ideal if used as an etch stop layer. Deposition rates were much lower then SiO_2 with $\sim$ 11 nm/min.

B.3 Resist Coating Process Details

AZ nLOF 2020 2μ**m**

Tool Description: Brewer Science CEE 200 spin coater, Sawatec HP-401-Z hotplate

Dehydration: Minimum of 30 min at 120 °C in dehydration oven

Resist: AZ nLOF 2020 is mixed from MicroChemicals GmbH AZ nLOF 2070 and AZ EBR solvent in a 10:3 ratio.

Spin profile:

Step	Acceleration	Speed	Time
1	100rpm/s	500rpm	5s
2	1500rpm/s	4000rpm	2.5s
3	0rpm/s	4000rpm	30s
4	-2000rpm/s	100rpm	1s

Table B.1: AZ nLOF 2070 4μm spin profile

Soft-bake: 2 min at 110 °C on hotplate

Process details: High rotation speed (4,000 rpm) and thin resist lead to minimal edge-bead build-up and even coating of the sample surface. If the resist is unevenly distributed or particles are visible on the samples, an acetone and isopropyl alcohol (IPA) clean followed by nitrogen drying is performed and the spin coating repeated. The spin recipe

was provided by Kian Shen Kiang.

AZ nLOF 2070 4μm

Tool Description: Brewer Science CEE 200 spin coater, Sawatec HP-401-Z hotplate
Dehydration: Minimum of 30 min at 120 °C in dehydration oven
Resist: MicroChemicals GmbH AZ nLOF 2070 negative resist
Spin profile:

Step	Acceleration	Speed	Time
1	100rpm/s	500rpm	5s
2	1000rpm/s	6000rpm	30s
4	-1000rpm/s	100rpm	1s

Table B.2: AZ nLOF 2070 4μm spin profile

Soft-bake: 2 min at 110 °C on hotplate
Process details: Very high rotation speed (6,000 rpm) spin profile intended to reduce edge-beads of the thicker negative resist layer. After successful spin coating remaining solvents are evaporated during the soft-bake. Recipe is provided by Kian Shen Kiang.

AZ nLOF 2070 7μm

Tool Description: Brewer Science CEE 200 spin coater, Sawatec HP-401-Z hotplate
Dehydration: Minimum of 30 min at 120 °C in dehydration oven
Resist: MicroChemicals GmbH AZ nLOF 2070 negative resist
Spin profile:

Step	Acceleration	Speed	Time
1	500rpm/s	500	0.5s
2	0rpm/s	500rpm	3s
3	500rpm/s	2750rpm	0.5s
4	0rpm/s	2750rpm	6s
5	-5000rpm/s	500rpm	0.5s

Table B.3: AZ nLOF 2070 4μm spin profile

Soft-bake: 2 min at 110 °C on hotplate
Process details: Strong accelerations at the start and end of the spin profile are intended to reduce the edge-beads. Nevertheless when rectangular pieces are used significant edge-beads are still present after spinning, which are removed using AZ EBR solvent prior to the soft bake. The spin recipe was provided by Kian Shen Kiang.

B.4 Physical Vapour Deposition (PVD) Process Details

Sputter Deposition of Copper Seed Layer

Tool Description: AJA International, Inc. ORION magnetron sputter
Process Materials: Ar gas and Copper (Cu) target
Chamber Pressure: 3 mTorr
Plasma Generator: 400 W dc magnetron plasma directed onto Cu target.
Distance Between Target and Sample: $\sim$ 0.2 m
Process Characteristics: DC argon plasma directed onto Cu targets is slowly ramped up with closed shutters, to reduce thermal stress on the target. After the maximum power is reached shutters are opened, after the set deposition time, shutters are closed and plasma power ramped down. A prior characterisation was performed to determine the deposition rate. For the copper target and 400W a rate of $\sim$ 60 nm/min was measured.

Sputter Deposition of Titanium Adhesion Layer

Tool Description: AJA International, Inc. ORION magnetron sputter
Process Materials: Ar gas and Titanium (Ti) target
Chamber Pressure: 3 mTorr
Plasma Generator: 300 W dc magnetron plasma directed onto target.
Distance Between Target and Sample: $\sim$ 0.2 m
Process Characteristics: For the titanium deposition a dc plasma power of 300 W was chosen taking the lower thermal conductivity of Ti into consideration and the resulting deposition rate was $\sim$ 8 nm/min.

Sputter Deposition of Gold Layer

Tool Description: AJA International, Inc. ORION magnetron sputter
Process Materials: Ar gas and Gold (Au) target
Chamber Pressure: 3 mTorr
Plasma Generator: 300 W dc magnetron plasma directed onto target.
Distance Between Target and Sample: $\sim$ 0.2 m
Process Characteristics: Gold is deposited using the same dc plasma power of 300 W, deposition rates of $\sim$ 46 nm/min were measured.

Sputter Deposition of Silicon Dioxide Layer

Tool Description: AJA International, Inc. ORION magnetron sputter
Process Materials: Ar gas and Silicon dioxide SiO_2 target
Chamber Pressure: 3 mTorr
Plasma Generator: 200 W rf magnetron plasma directed onto target.
Distance Between Target and Sample: ~ 0.2 m
Process Characteristics: Silicon dioxide is sputtered using an rf magnetron plasma of 200 W, and very low deposition rates of only ~ 25 nm/h were achieved.

E-beam Evaporation of Aluminium Buried Wire Layer 500nm

Tool Description: Leybold LAB700EB Evaporator
Process Materials: Aluminium (Al) target, no process gases were used
Chamber Pressure: $< 5 \times 10^{-6}$ mbar
E-beam Power: 10 kV, ~ 340 mA
Distance Between Target and Sample: ~ 1 m
Set Deposition Rate: 2.5 Angstrom/s
Process Characteristics: Deposition in the LAB700EB is controlled using a quartz crystal, which directly measures the deposition rate. When the final thickness is reached the deposition control automatically closes the shutters and ramps down the e-beam power.

E-beam Evaporation of Aluminium Electrode Layer 3500nm

Tool Description: Leybold LAB700EB Evaporator
Process Materials: Aluminium (Al) target, no process gases were used
Chamber Pressure: $< 5 \times 10^{-6}$ mbar
E-beam Power: 10 kV, ~ 450 mA
Distance Between Target and Sample: ~ 1 m
Set Deposition Rate: 5 Angstrom/s
Process Characteristics: For the thicker electrode layer the deposition rate was increased to 5 A/s resulting in a total deposition time of just under 2 hours.

E-beam Evaporation of Chromium Adhesion Layer 50nm

Tool Description: Leybold LAB700EB Evaporator
Process Materials: Chromium (Cr) target, no process gases were used
Chamber Pressure: $< 5 \times 10^{-6}$ mbar
E-beam Power: 10 kV, $\sim$ 240 mA
Distance Between Target and Sample: $\sim$ 1 m
Set Deposition Rate: 1 Angstrom/s
Process Characteristics: A thin chromium layer was deposited to increase adhesion between aluminium and nickel layer. Chromium was chosen over titanium as it is not rapidly etched by hydrofluoric acid [235].

E-beam Evaporation of Nickel Barrier Layer 100nm

Tool Description: Leybold LAB700EB Evaporator
Process Materials: Nickel (Ni) target, no process gases were used
Chamber Pressure: $< 5 \times 10^{-6}$mbar
E-beam Power: 8 kV, $\sim$ 17.6 mA
Distance Between Target and Sample: $\sim$ 1 m
Set Deposition Rate: 1 Angstrom/s
Process Characteristics: The nickel layer serves as a barrier layer, preventing gold from diffusing into the aluminium layer at elevated temperatures.

E-beam Evaporation of Gold Top Electrode Layer 150nm

Tool Description: Leybold LAB700EB Evaporator
Process Materials: Gold (Au) target, no process gases were used
Chamber Pressure: $< 5 \times 10^{-6}$ mbar
E-beam Power: 10 kV, $\sim$ 230 mA
Distance Between Target and Sample: $\sim$ 1 m
Set Deposition Rate: 1 Angstrom/s
Process Characteristics: A final Au layer prevents oxidization of the electrode surface and was deposited in the same run as the Al layer without opening the chamber.

Appendix C

Heatbridge Designs

C.1 SolidWorks Drawings

Workshop design drawings for thermal bridge components and custom window.

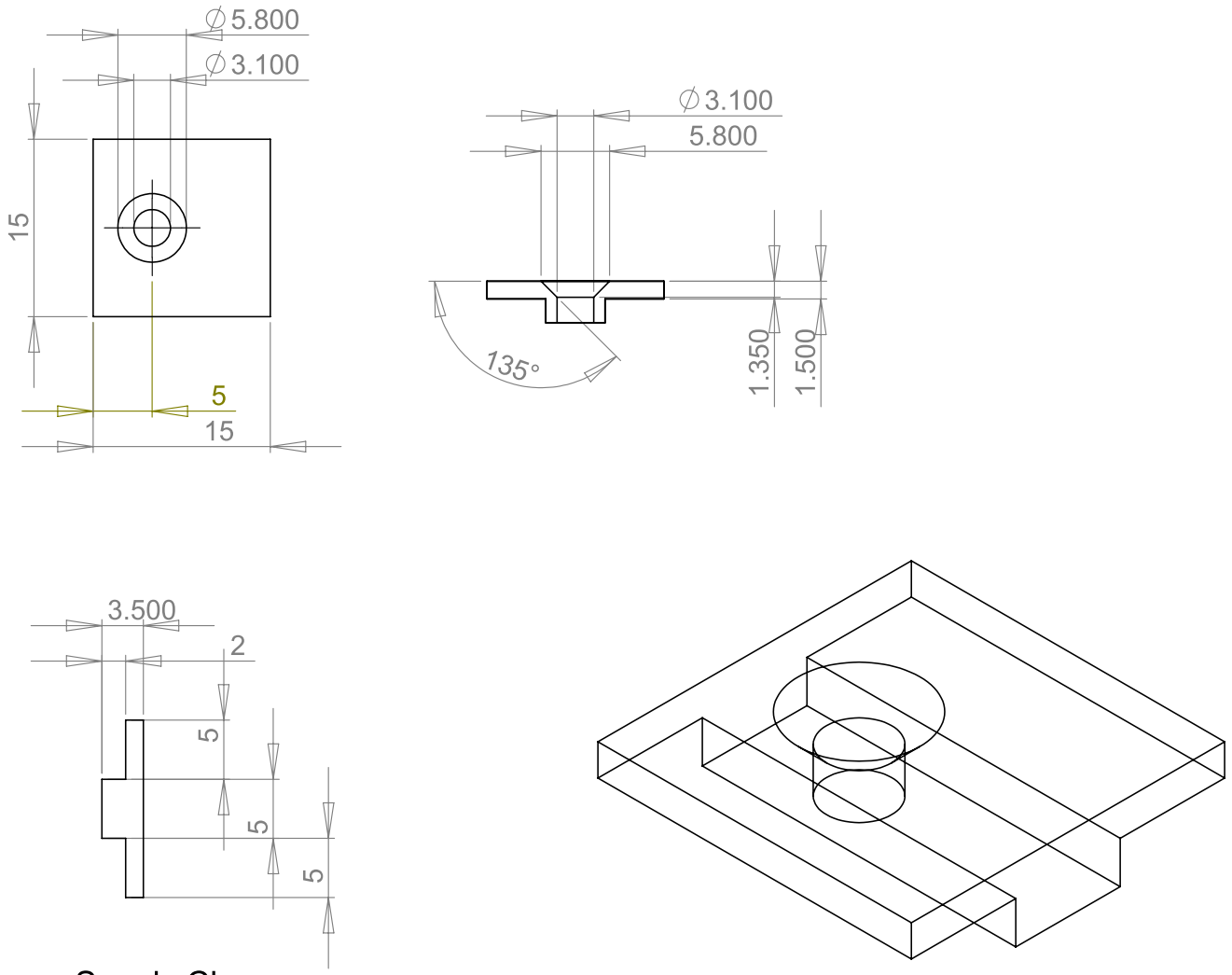


Figure C.1: A SolidWorks drawing for current supply clamps.

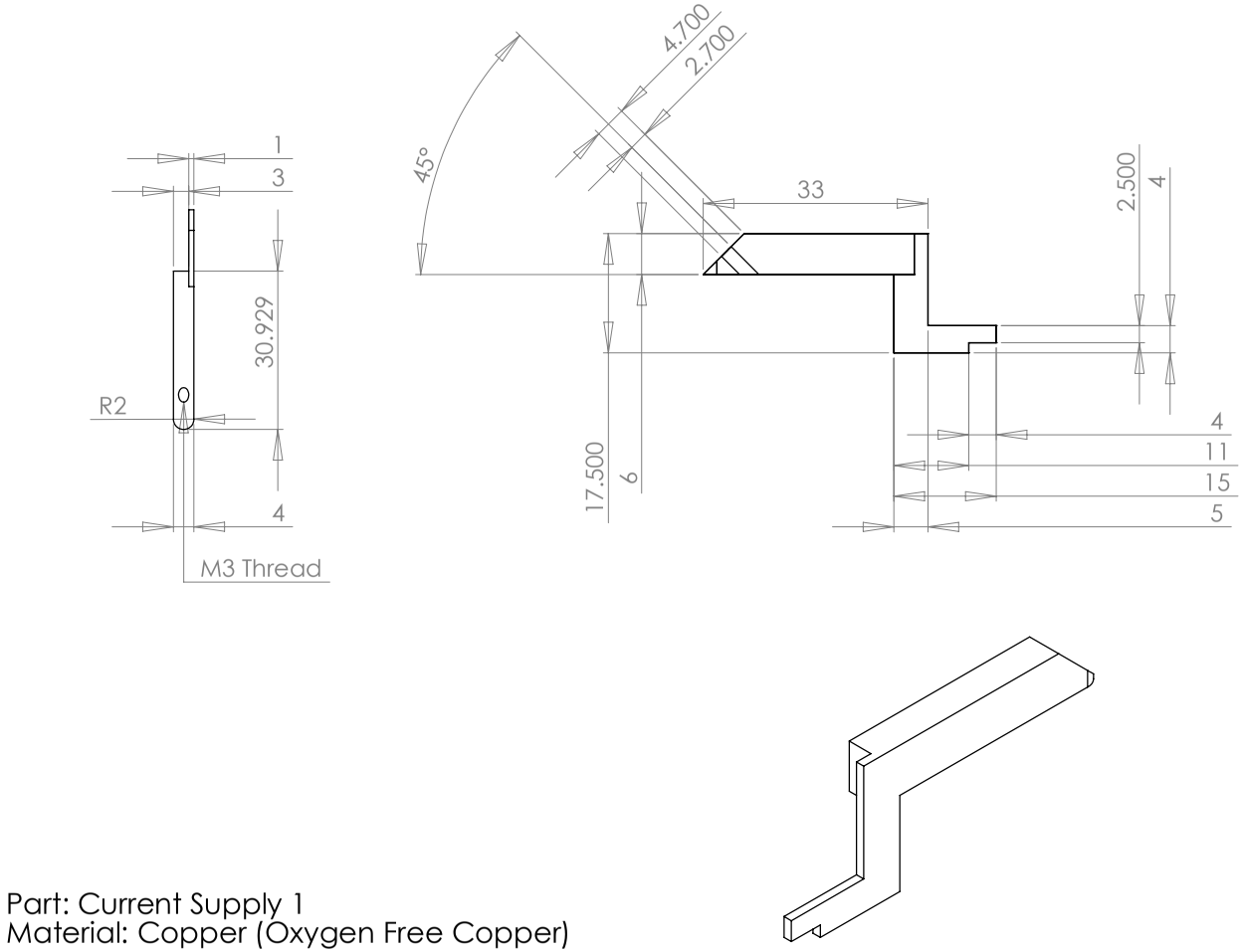
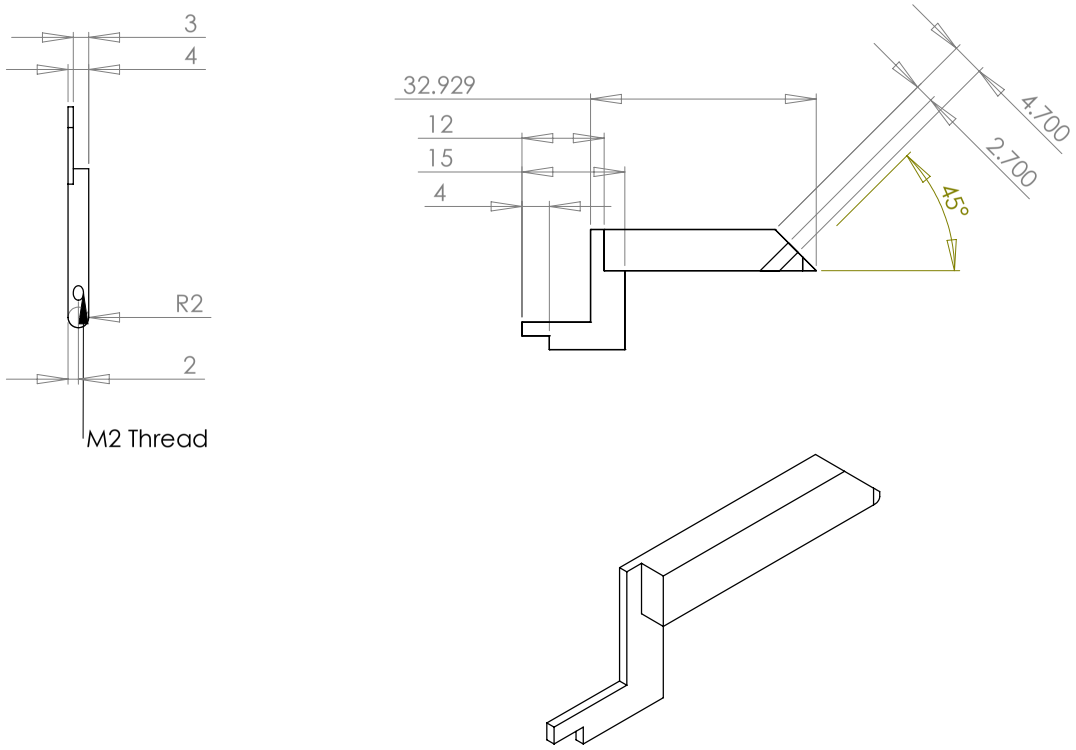
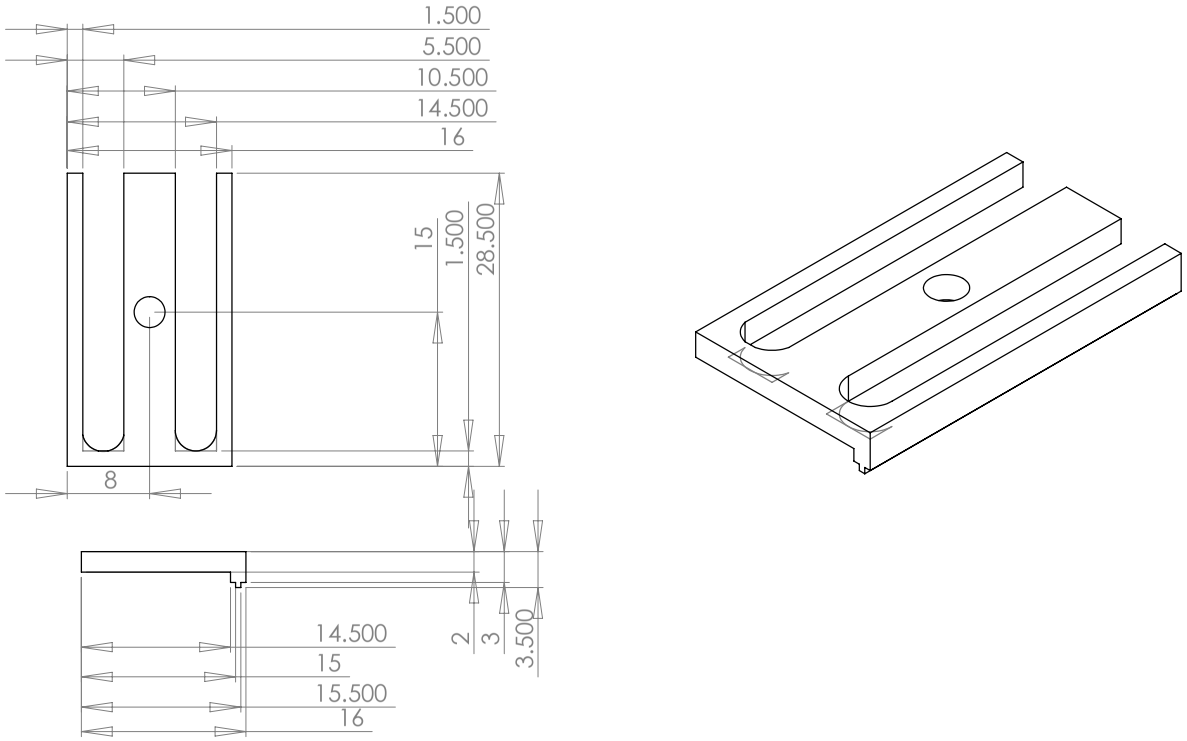


Figure C.2: A SolidWorks drawing for current supply structure (part 1).



Part: Current Supply 2
Material: Copper (Oxygen Free Copper)

Figure C.3: A SolidWorks drawing for current supply structure (part 2).



Part: Peek Guide 1
Material: Peek

Figure C.4: A SolidWorks drawing for peek spacer separating the two current supply structures (part 1).

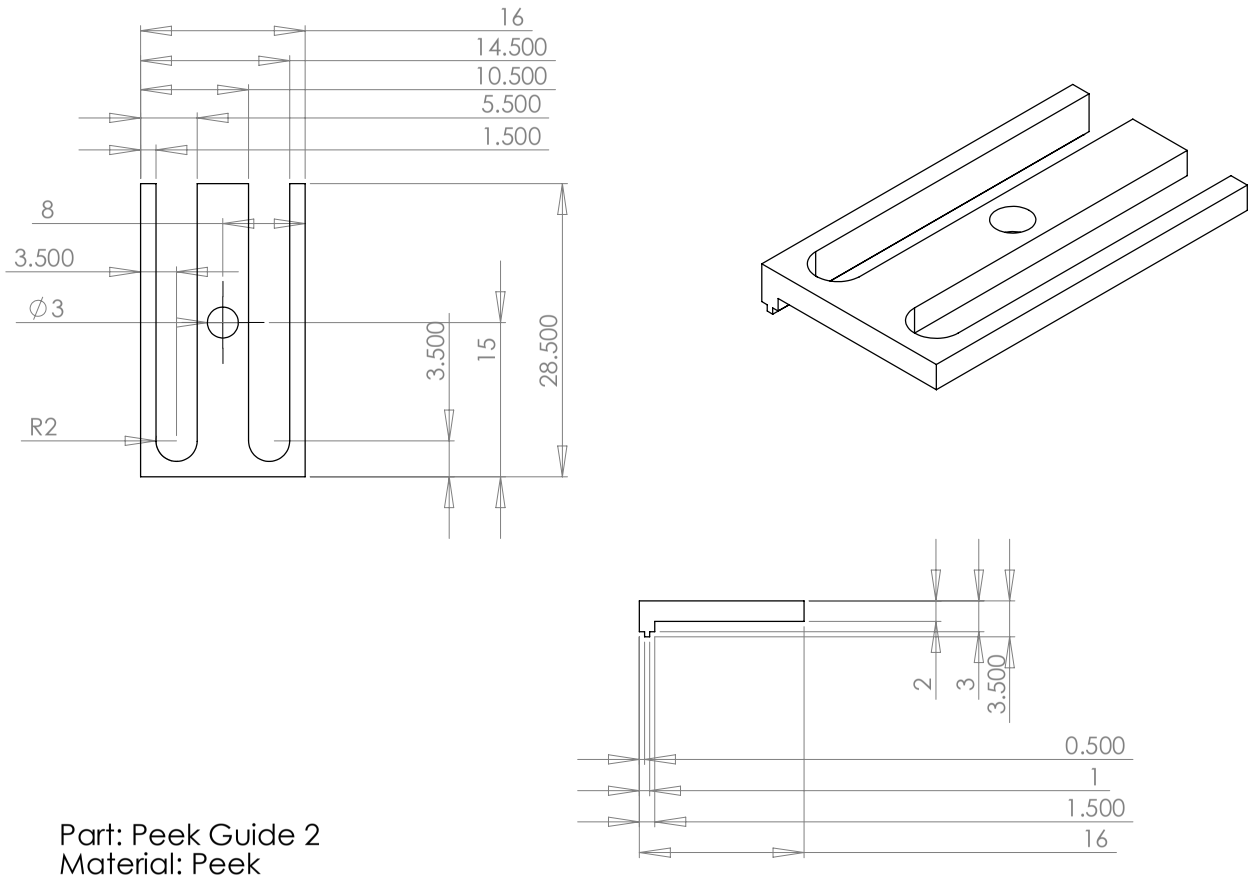
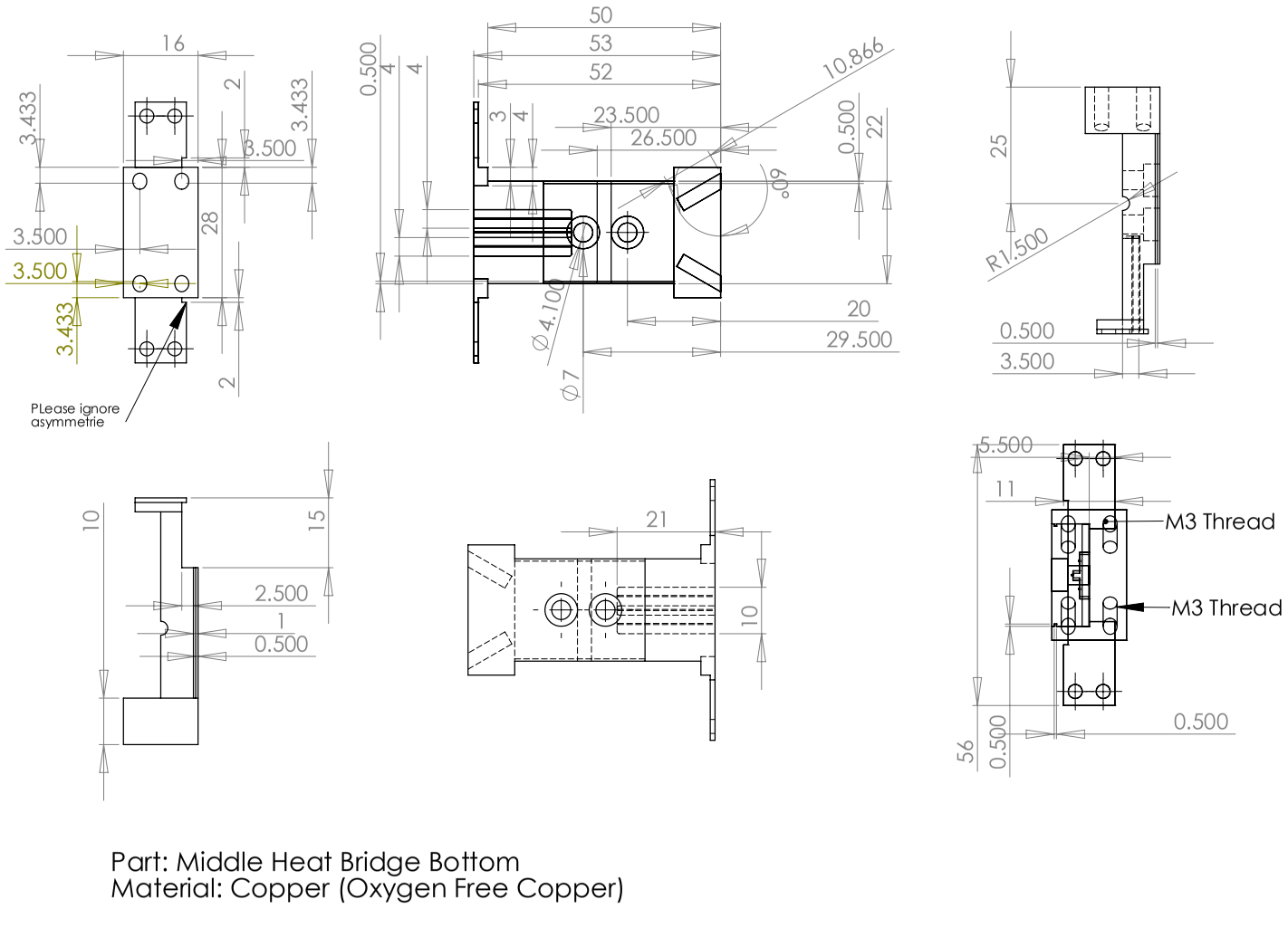


Figure C.5: A SolidWorks drawing for peek spacer separating the two current supply structures (part 2).



Part: Middle Heat Bridge Bottom
Material: Copper (Oxygen Free Copper)

Figure C.6: A SolidWorks drawing for the bottom part of the thermal bridge.

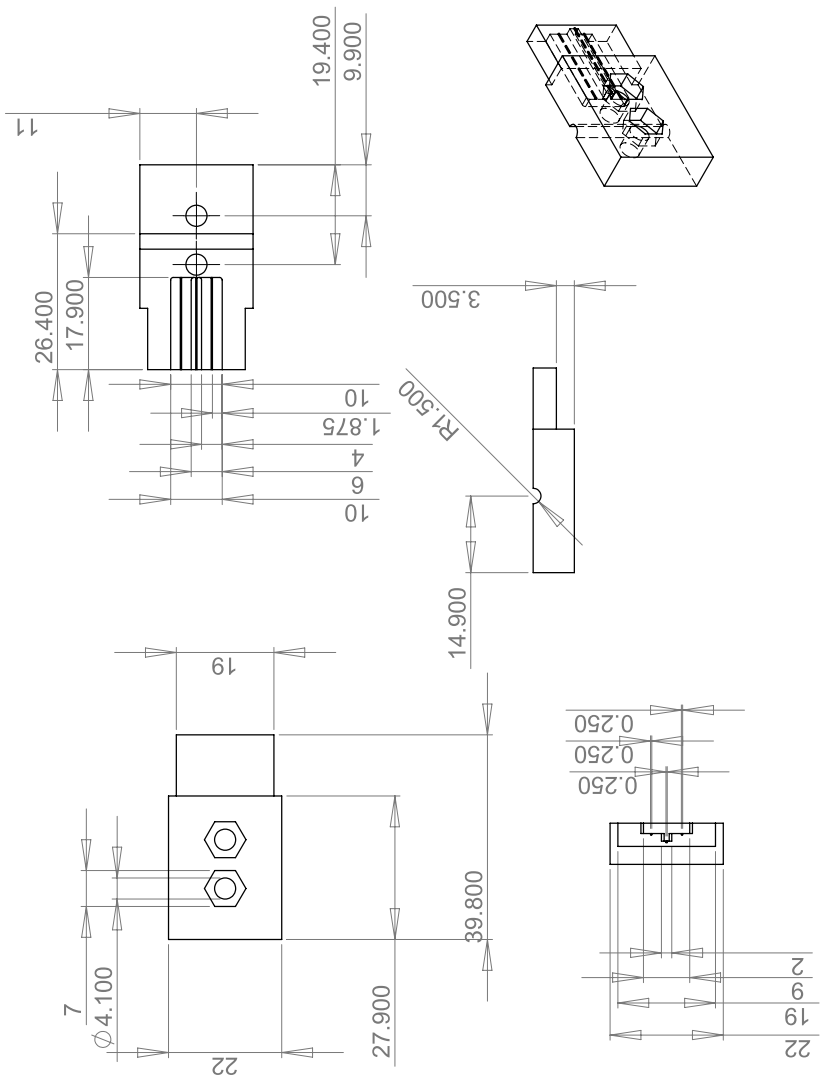
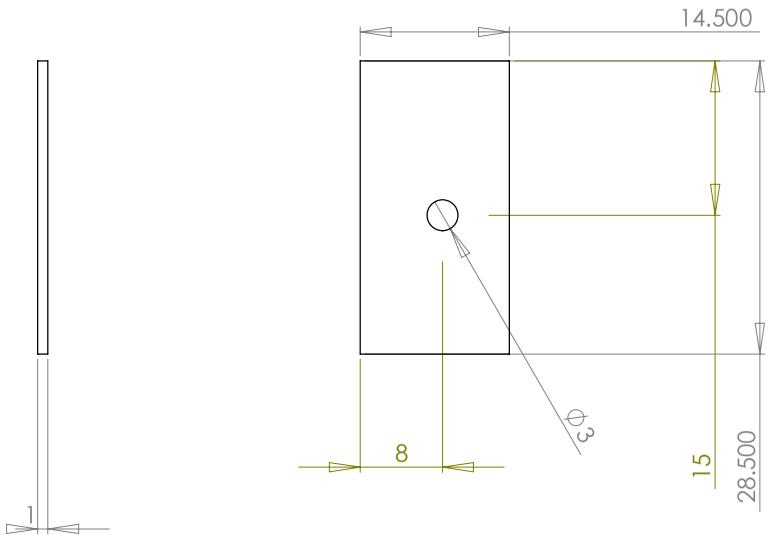
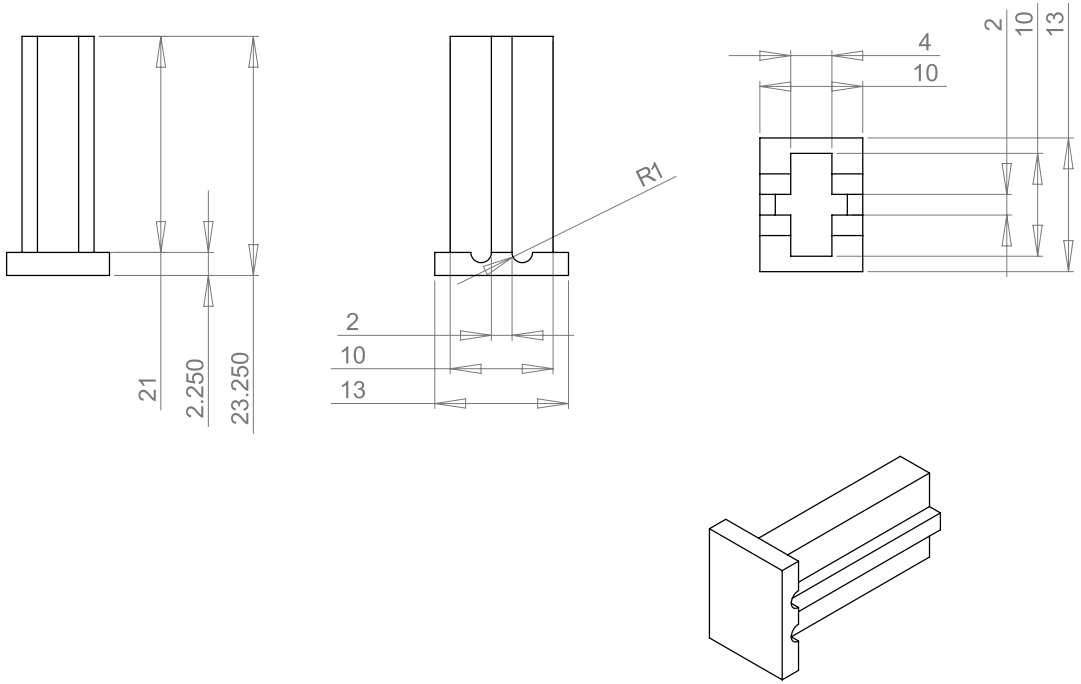


Figure C.7: A SolidWorks drawing for the top part of the thermal bridge.



Part: Heat Transfer Plate
Material: BNP2

Figure C.8: A SolidWorks drawing of BNP2 spacers.



Part: Front Bridge
Material: Copper (Oxygen Free Copper)

Figure C.9: A SolidWorks drawing of the copper chip holder.

Figure C.10: A SolidWorks drawing for the connection pin, (part of the current supply structures).

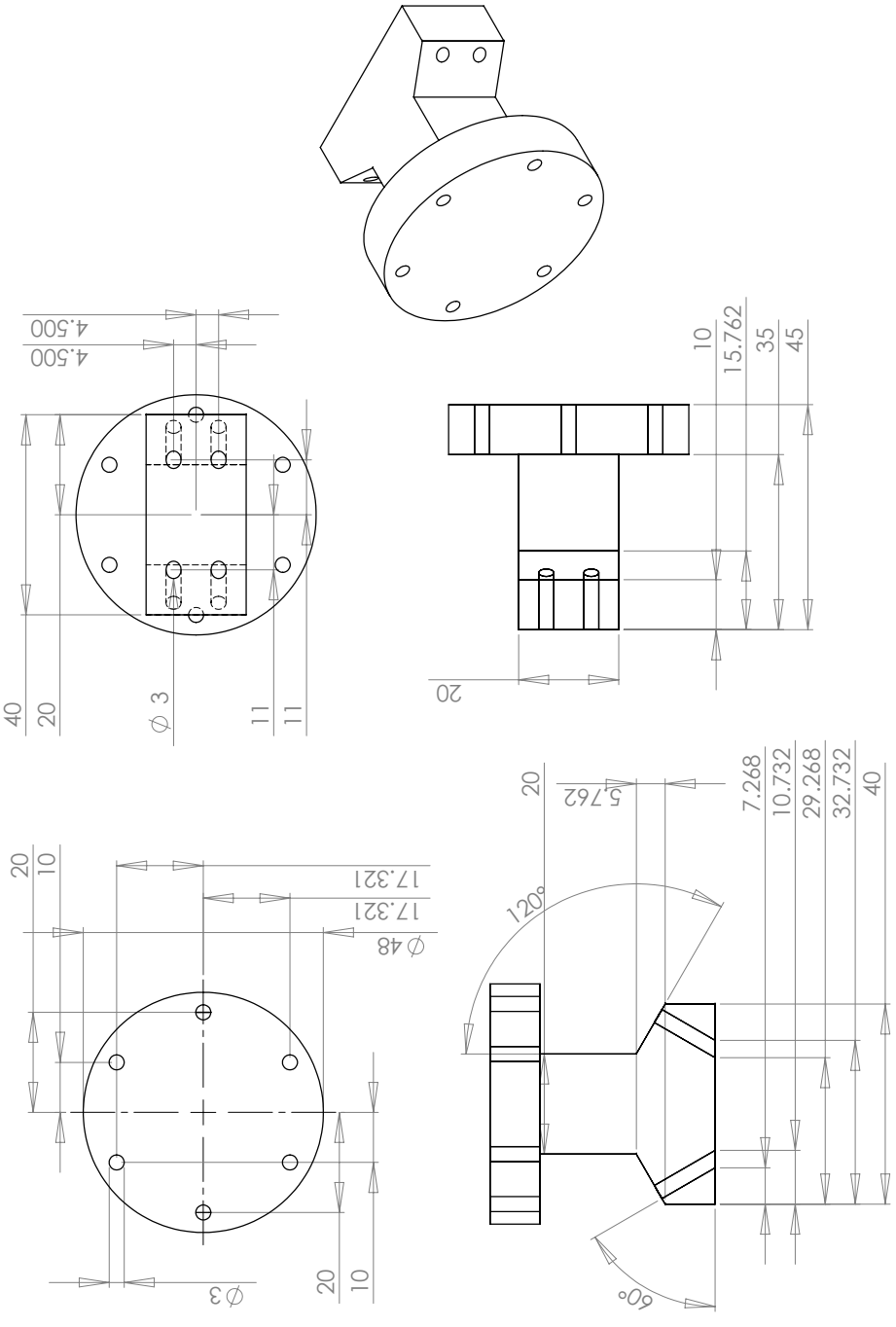


Figure C.11: A SolidWorks drawing of the copper adapter.

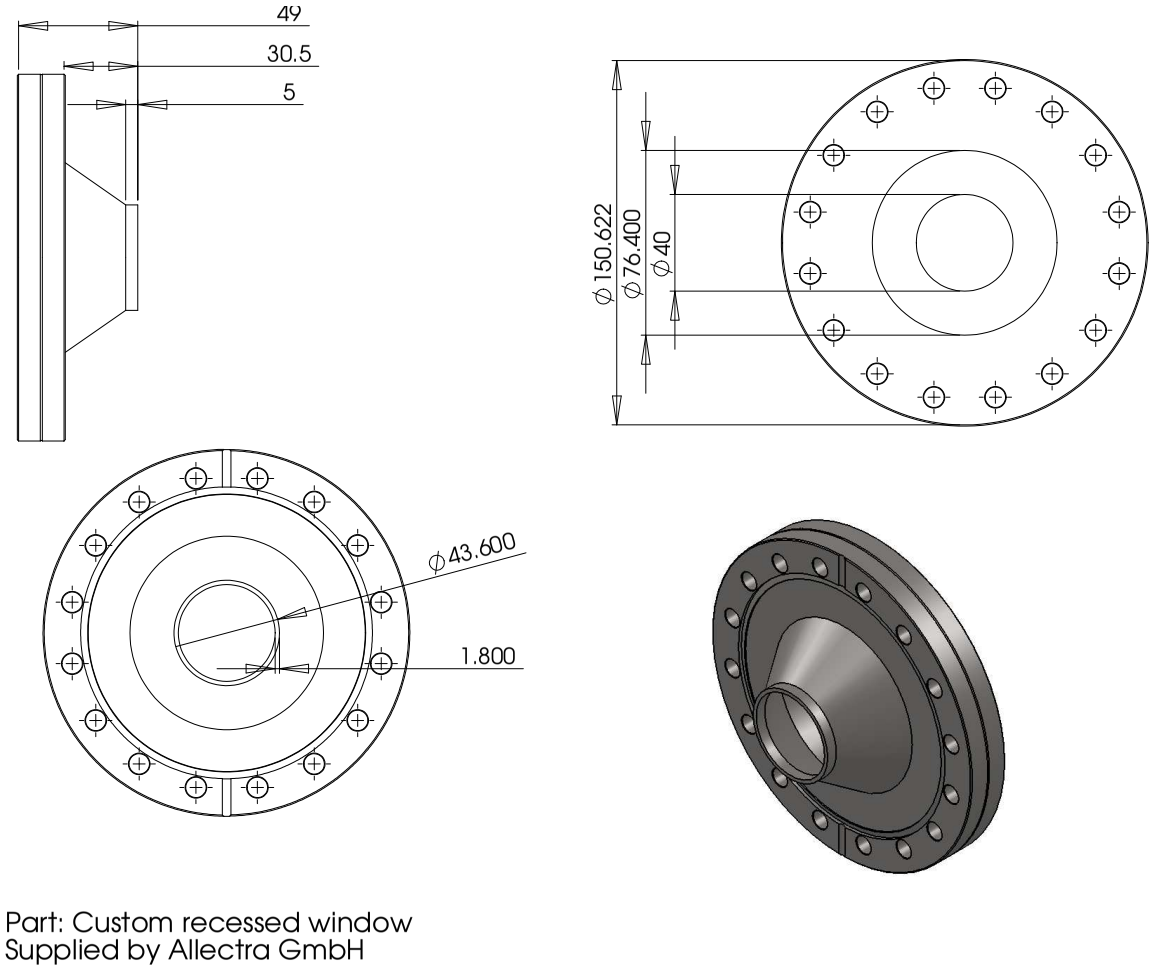


Figure C.12: A SolidWorks drawing of custom recessed window.

Appendix D

MaskLayout

D.1 Individual Mask Designs

Trap designs part of the mask layout presented in section 6.7. Electrode layer is marked blue, buried wire layer black and VIA layer red.

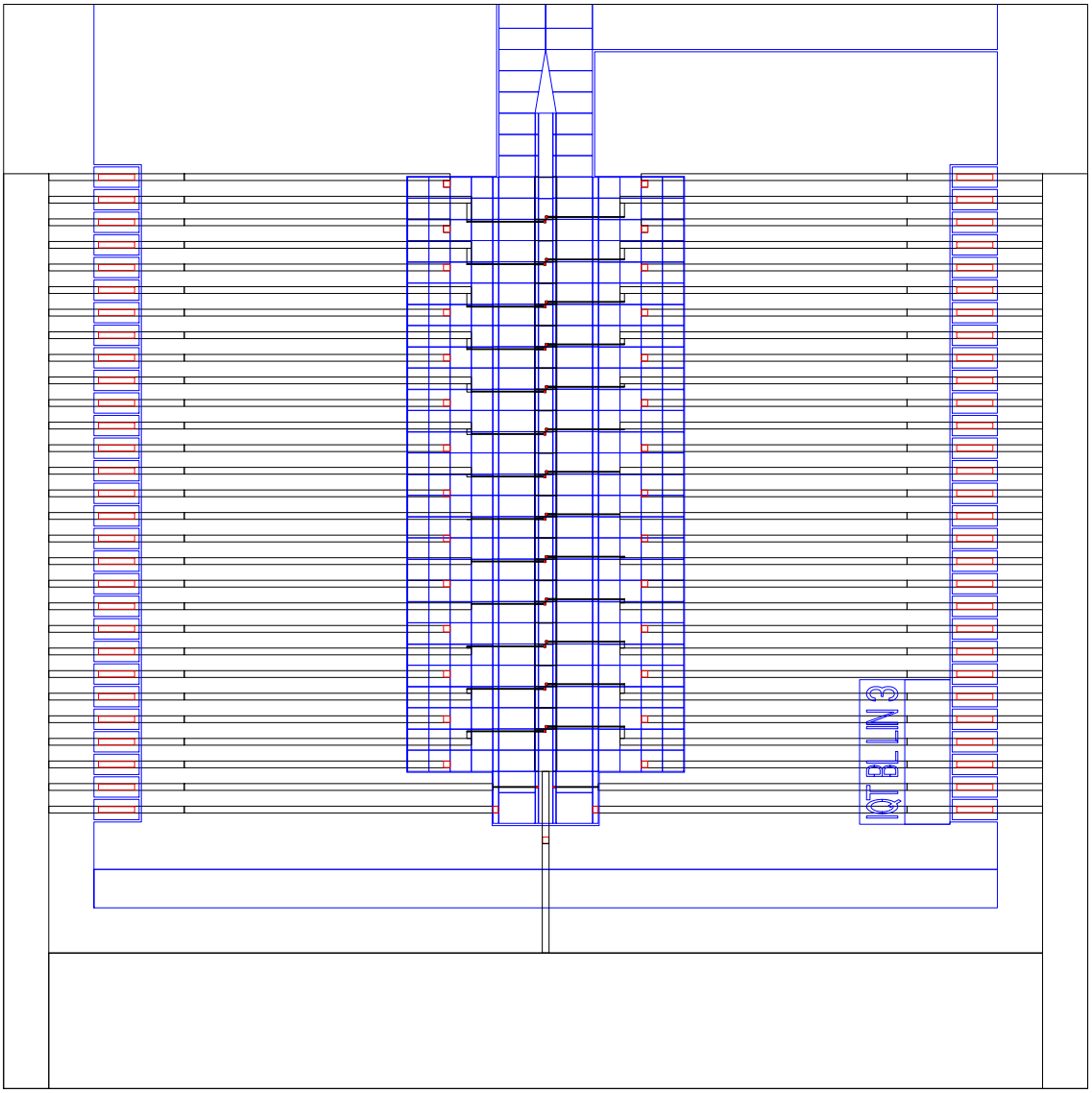


Figure D.1: Ion Trap Design 1: Linear ion trap, 250 μm ion height.

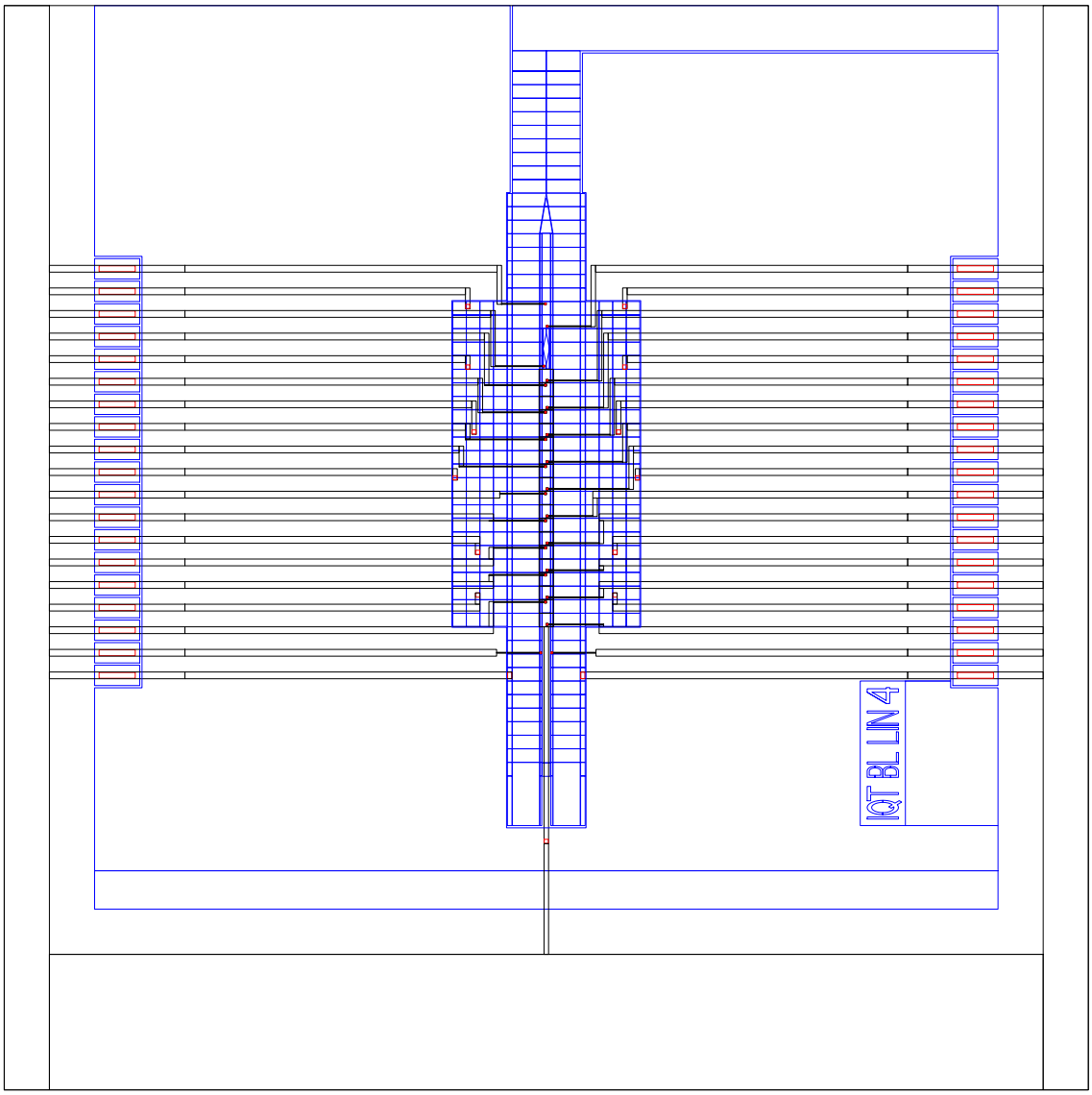


Figure D.2: Ion Trap Design 2: Linear ion trap with loading slot, 165 μm ion height.

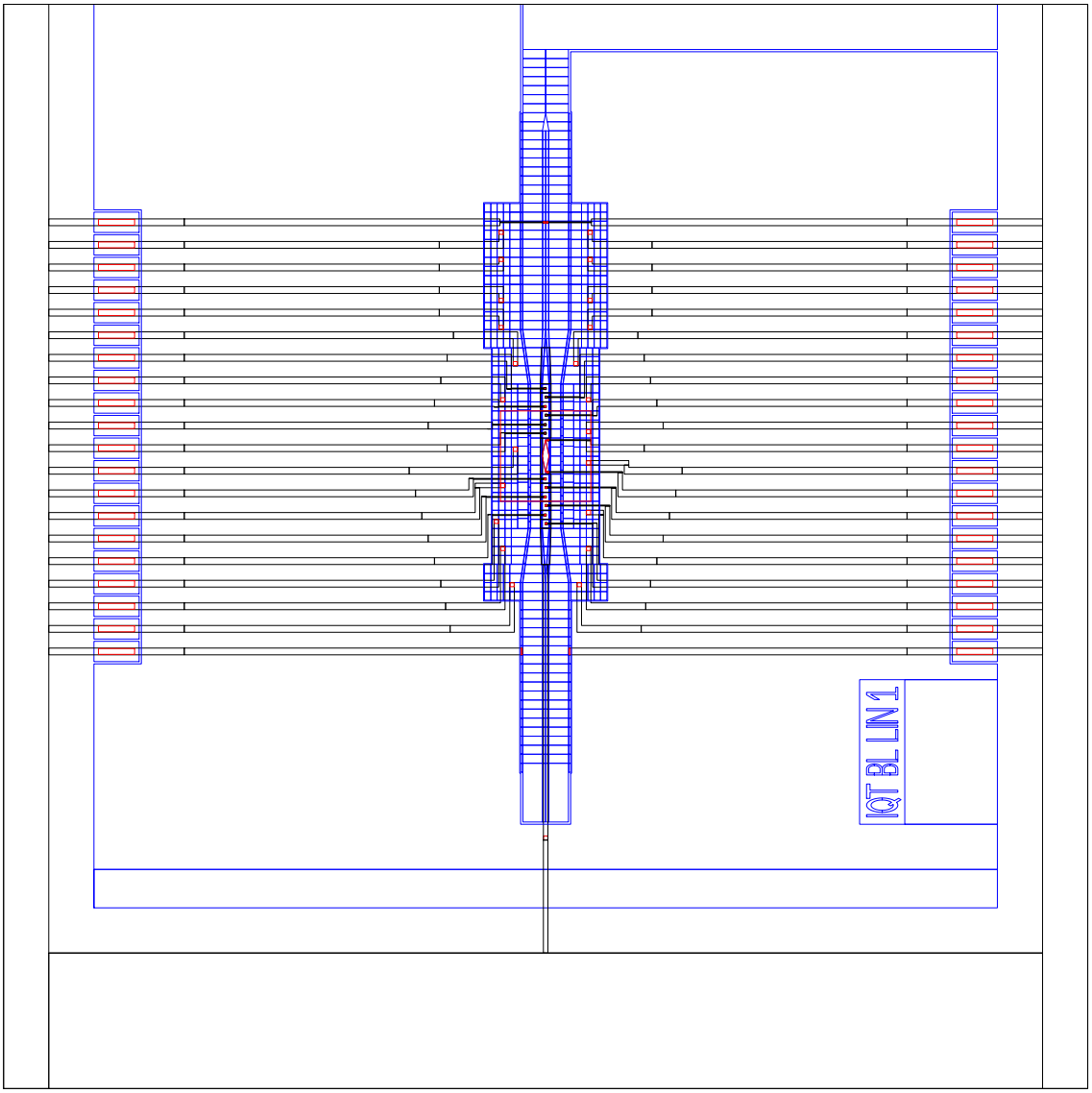


Figure D.3: Ion Trap Design 3: Linear ion trap with detection slot, 100 μm ion height.

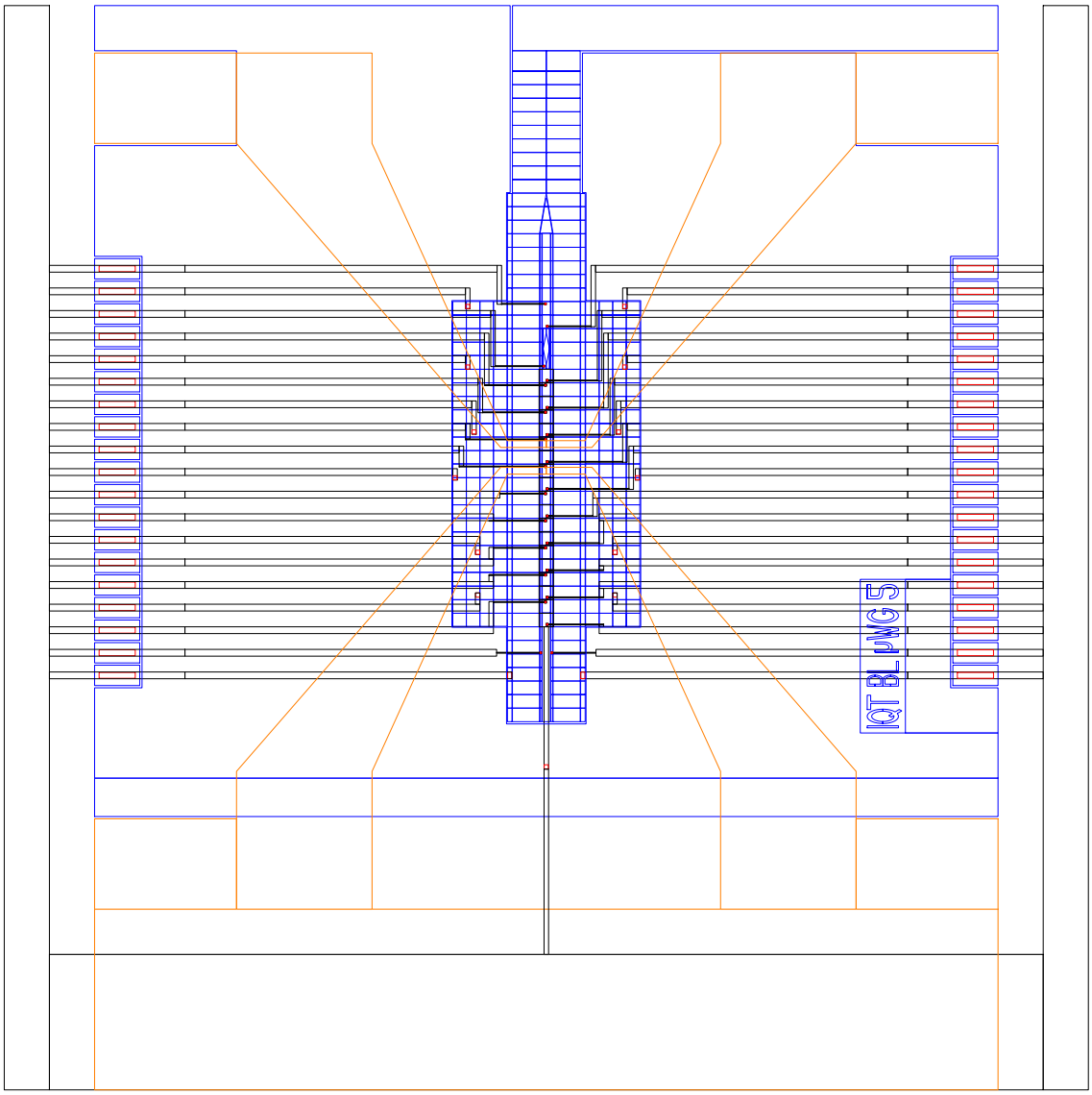


Figure D.4: Ion Trap Design 4: Linear ion trap with current-carrying wires and loading slot, 170 μm ion height.

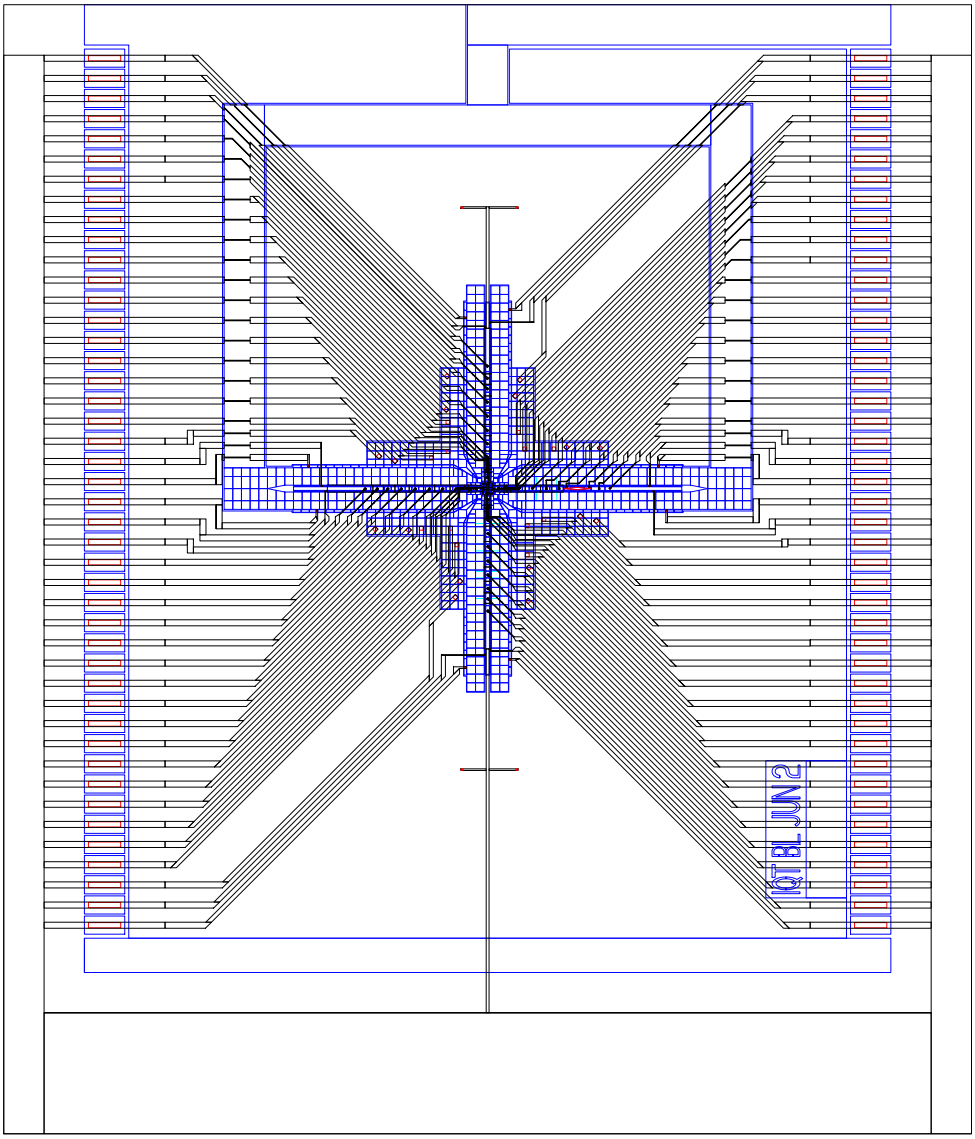


Figure D.5: Ion Trap Design 5: X-junction ion trap, 100 μm ion height.

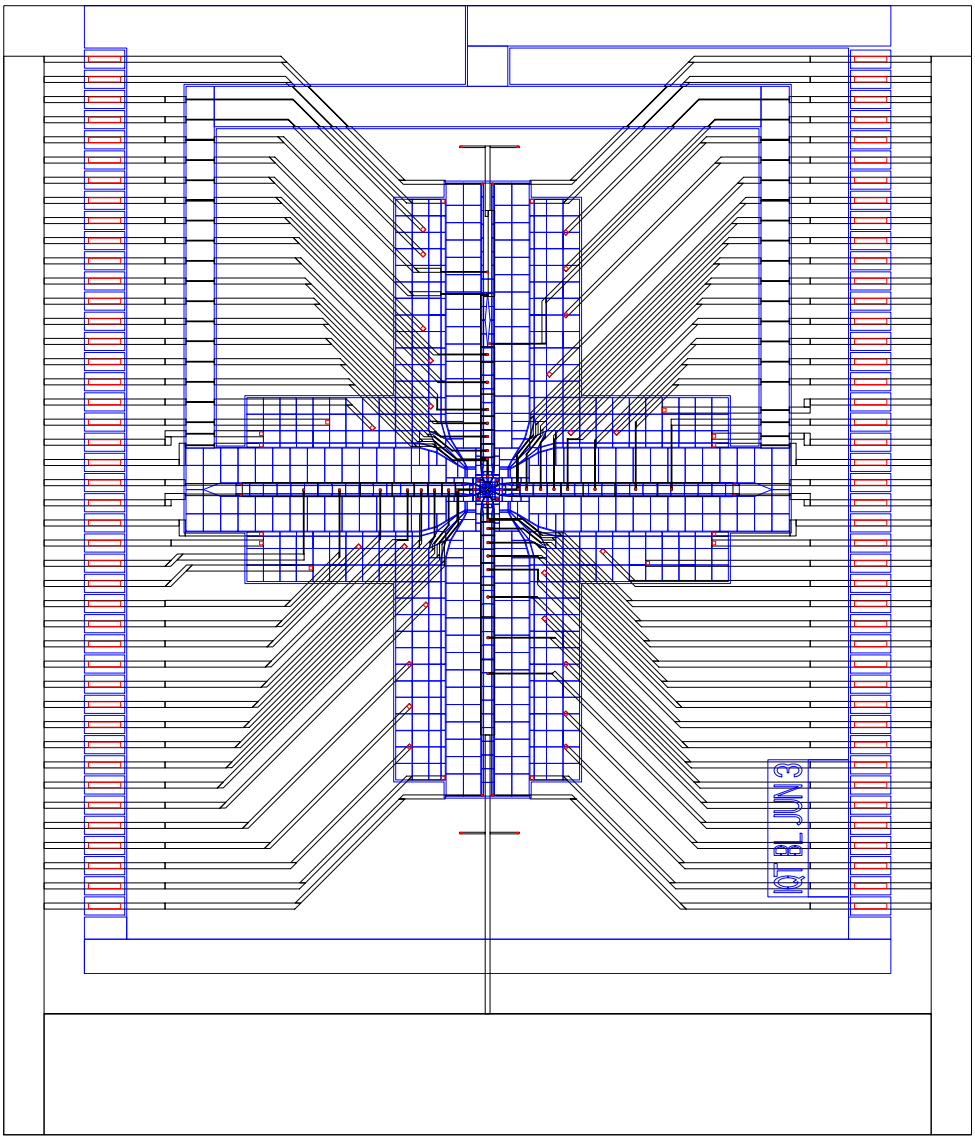


Figure D.6: Ion Trap Design 6: X-junction ion trap, 200 μm ion height.

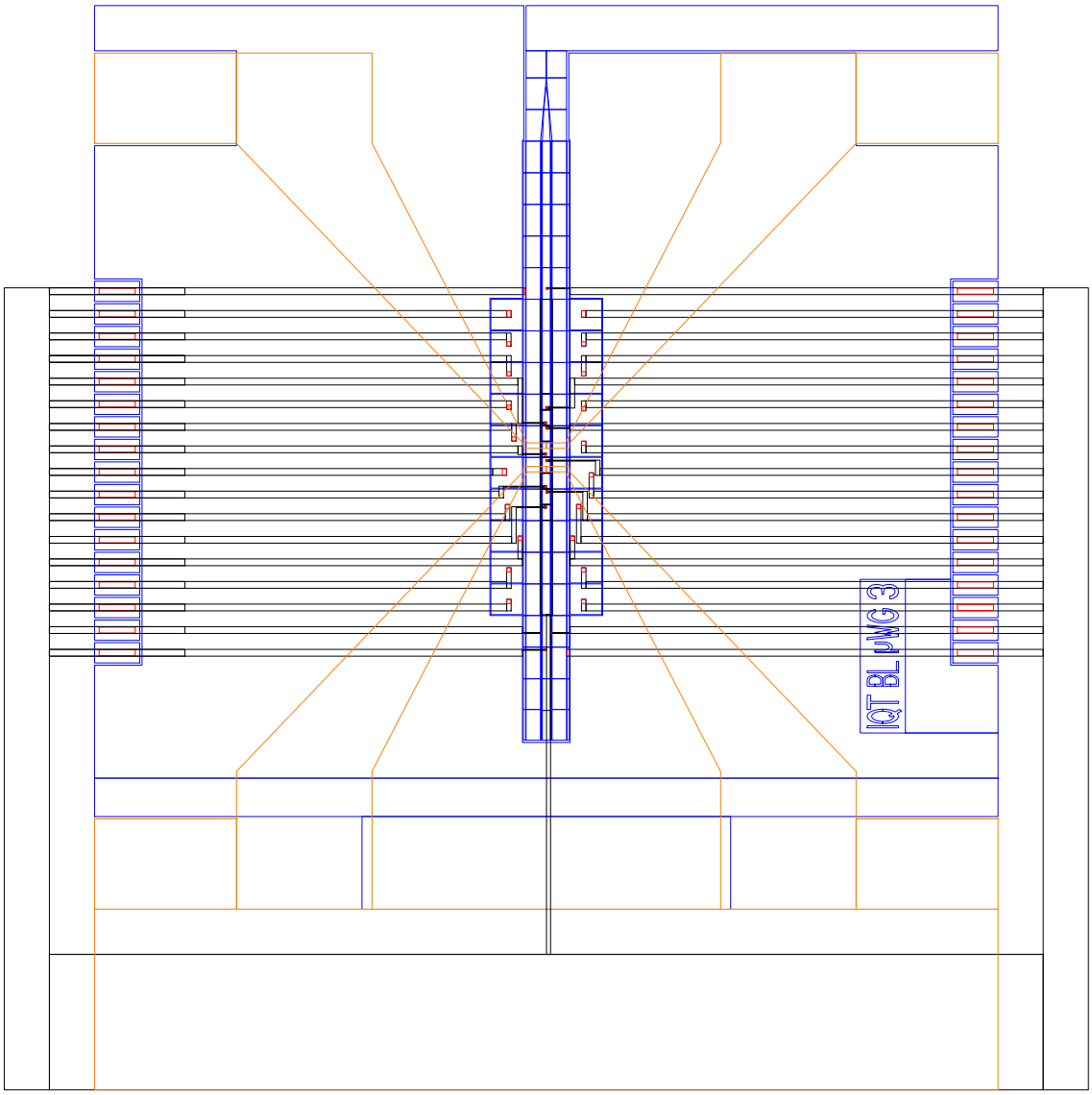


Figure D.7: Ion Trap Design 7: Linear ion trap with current-carrying wires, 120 μm ion height.

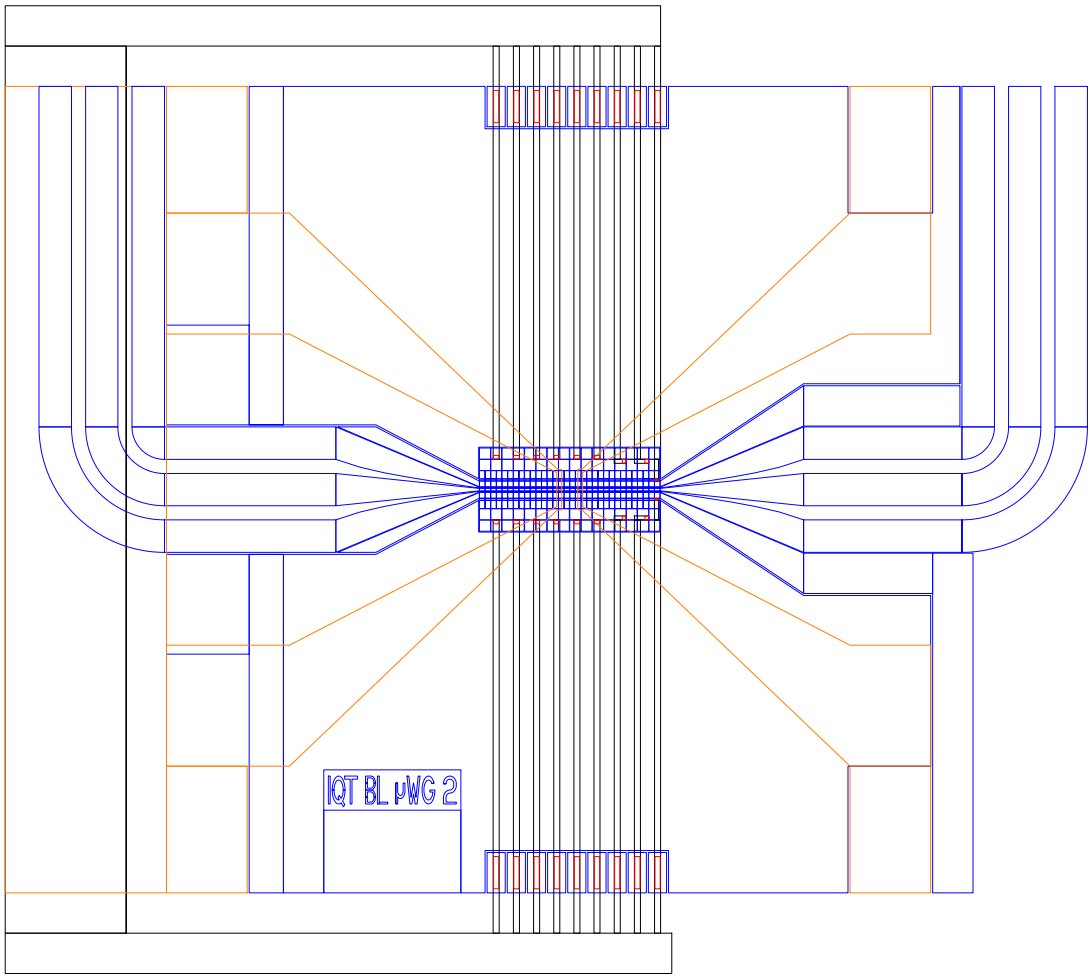


Figure D.8: Ion Trap Design 8: Linear ion trap with current-carrying wires and coplanar waveguide, 60 μm ion height.

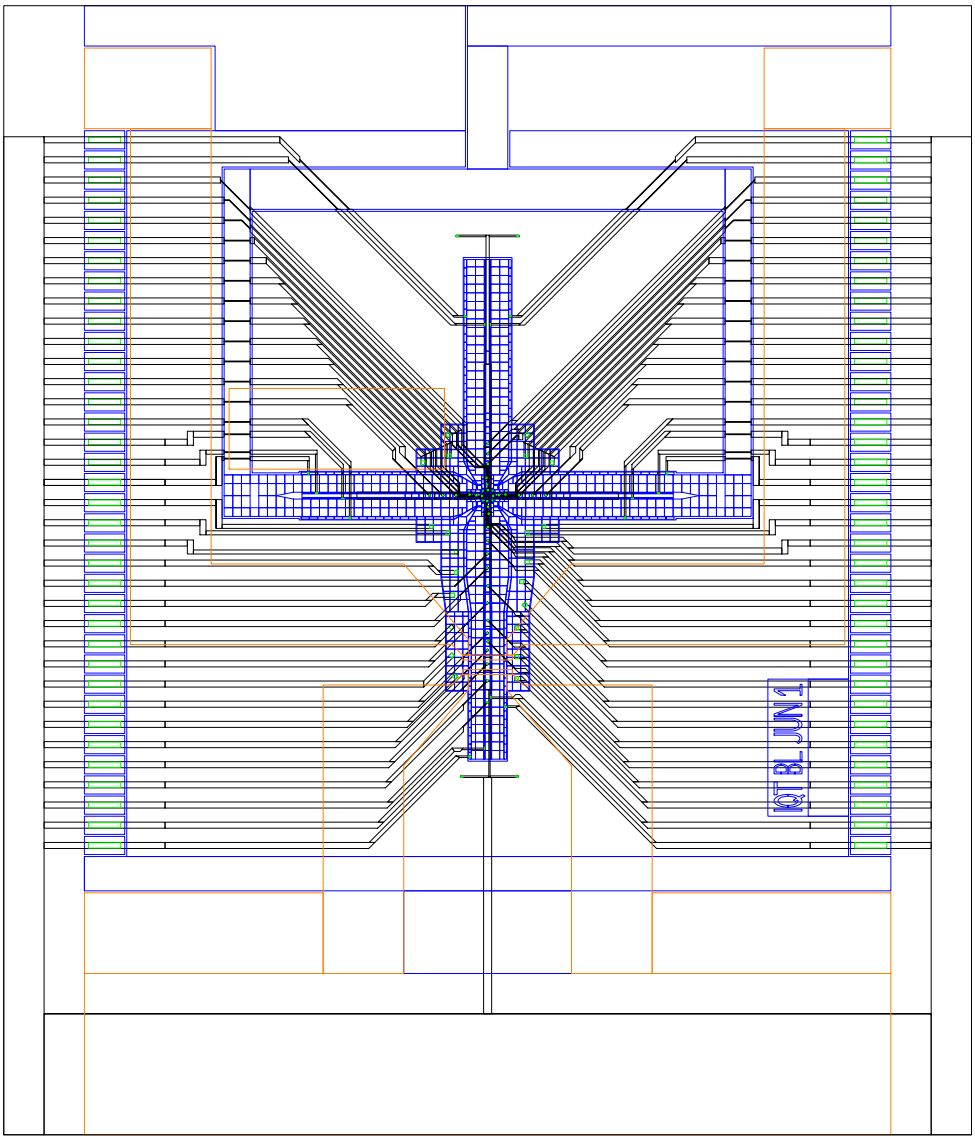


Figure D.9: Ion Trap Design 9: X-junction ion trap with current-carrying wires, 100 μm ion height.

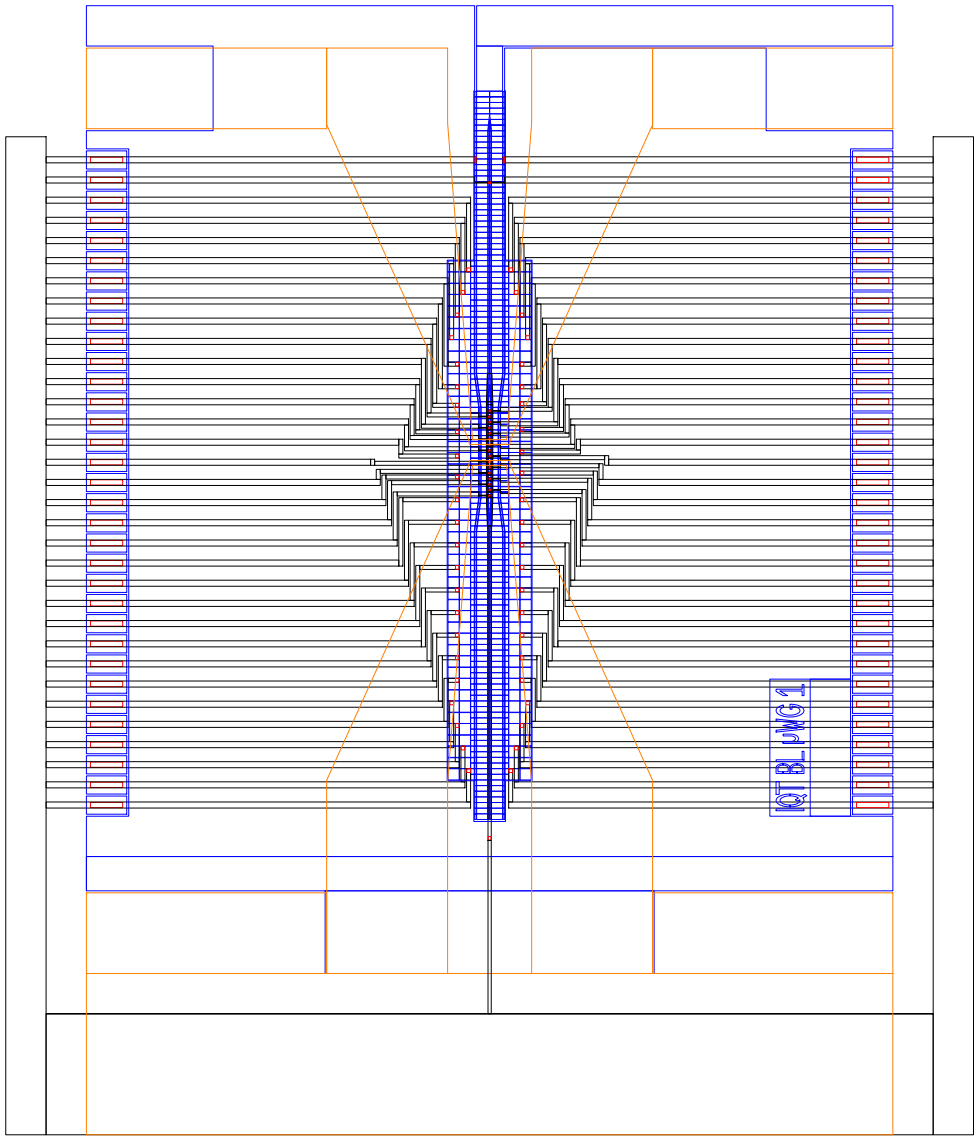


Figure D.10: Ion Trap Design 10: Linear ion trap with current-carrying wires, 60 μm ion height.

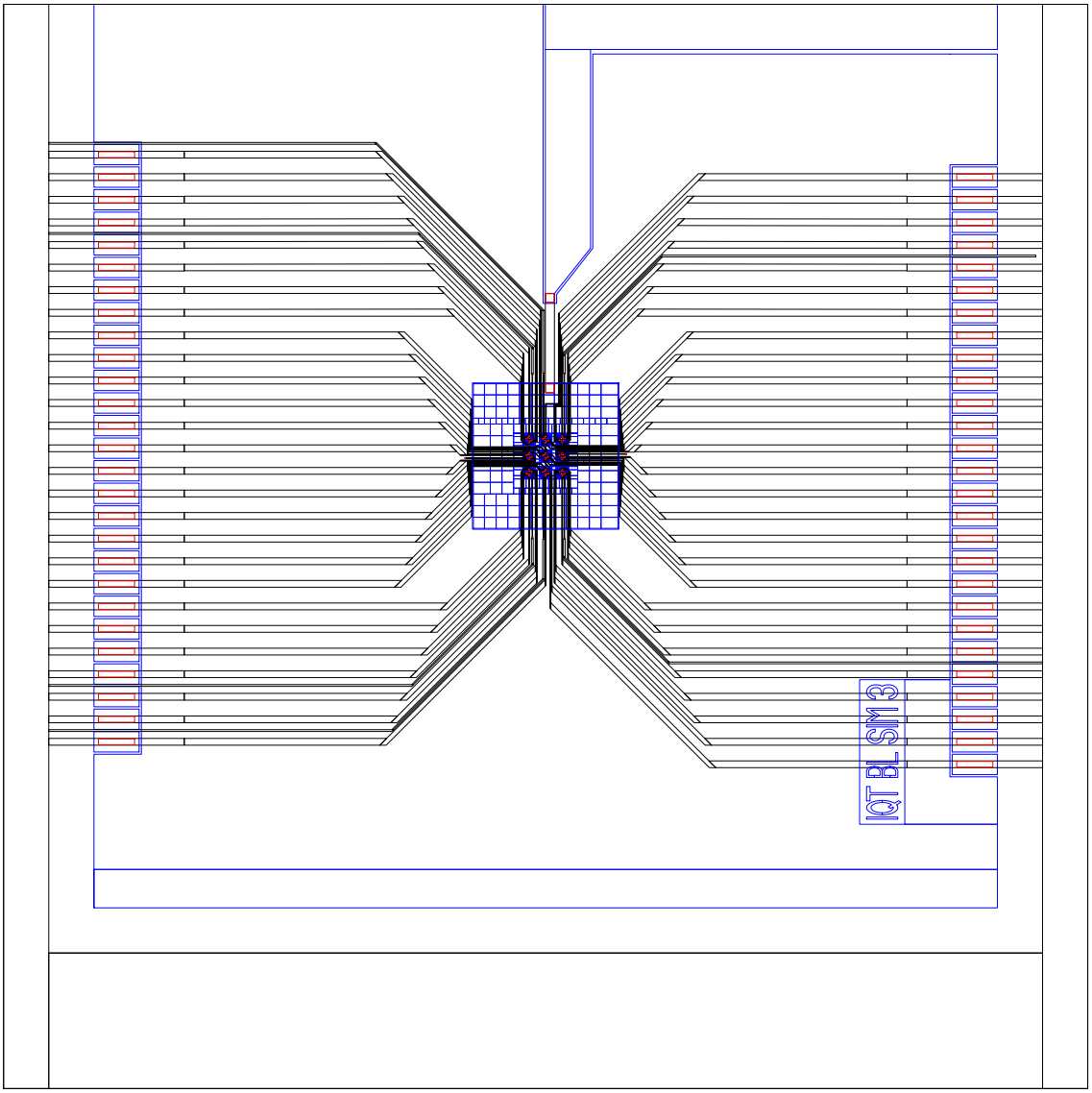


Figure D.11: Ion Trap Design 11: Two-dimensional ion trap array, 100 μm ion height.

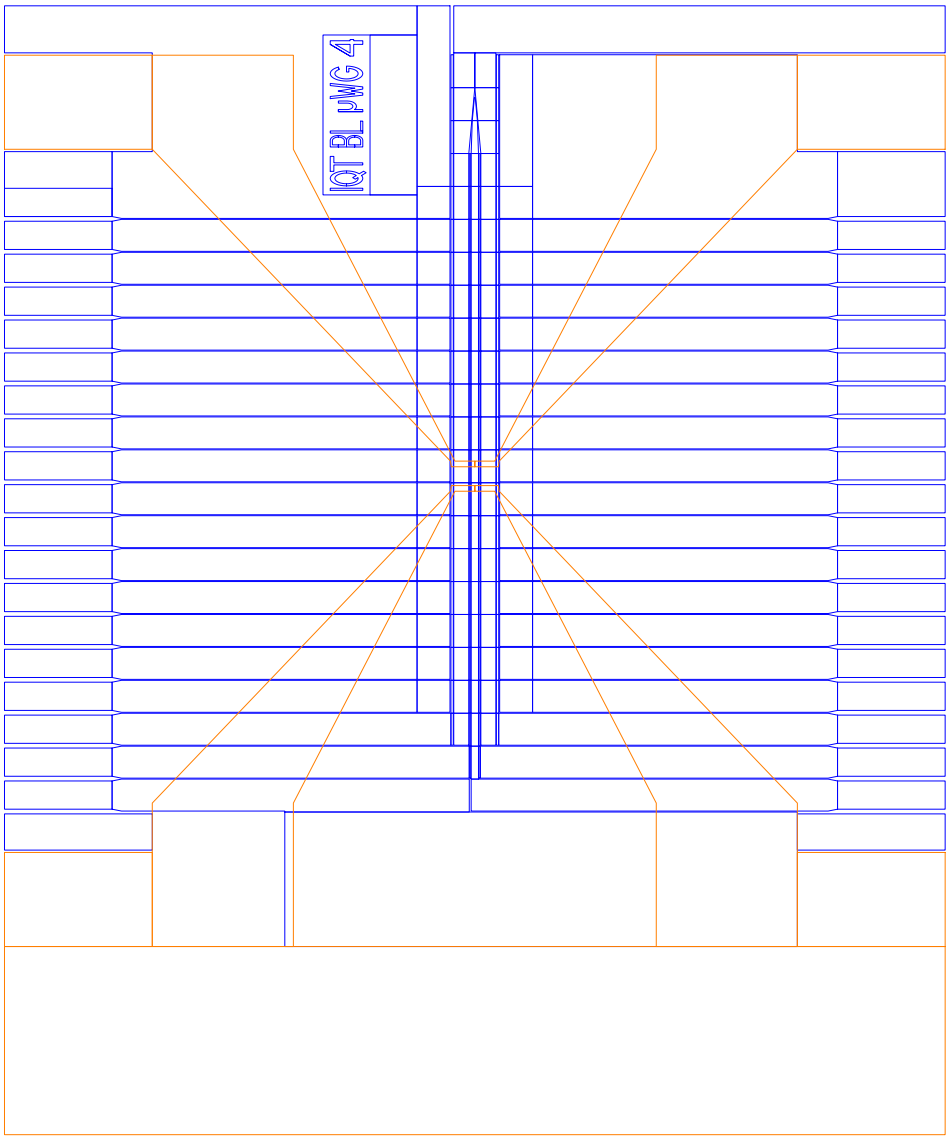


Figure D.12: Ion Trap Design 12: Linear ion trap with current-carrying wires, 120 μm ion height.

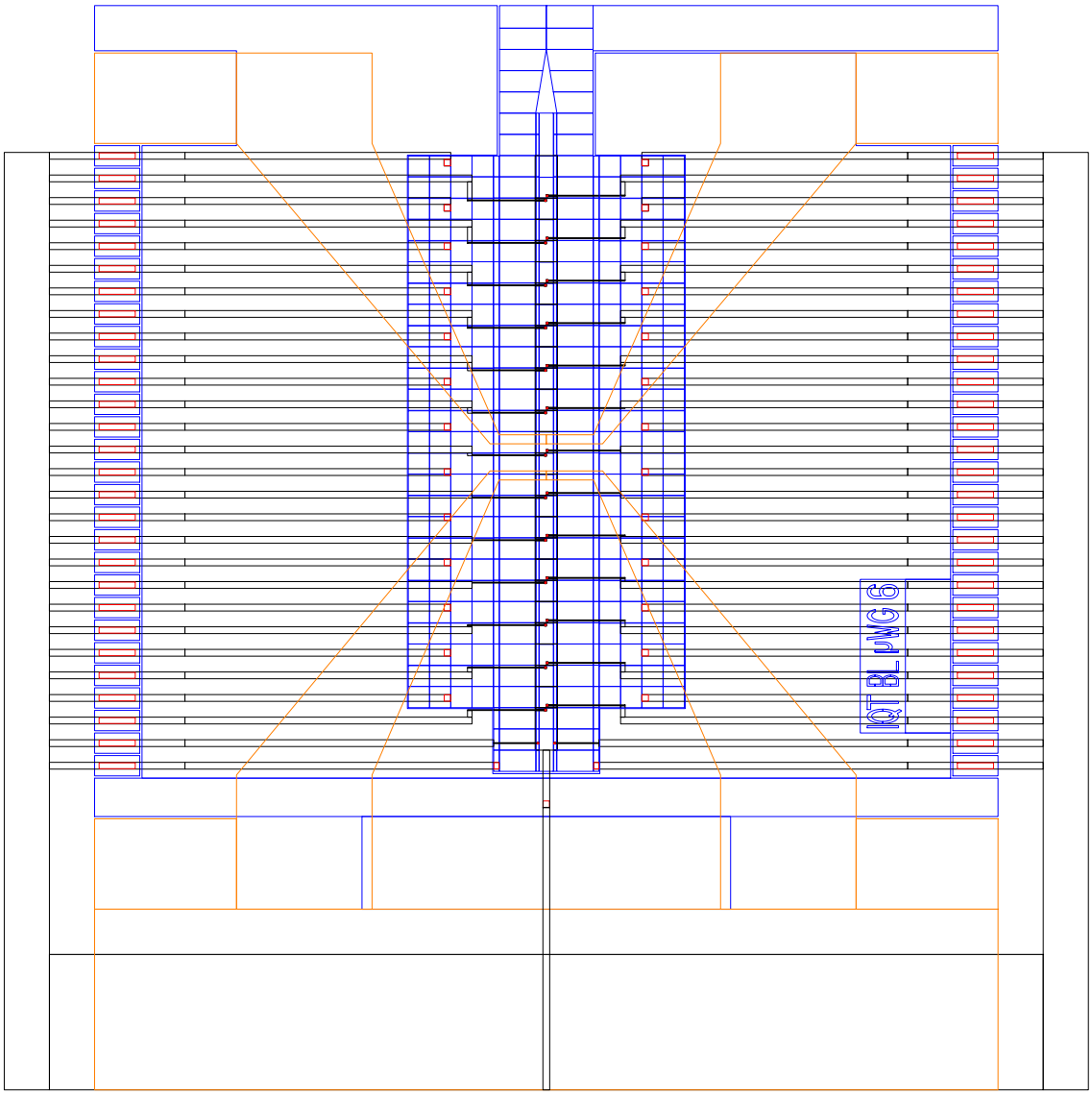


Figure D.13: Ion Trap Design 13: Linear ion trap with current-carrying wires, 170 μm ion height.

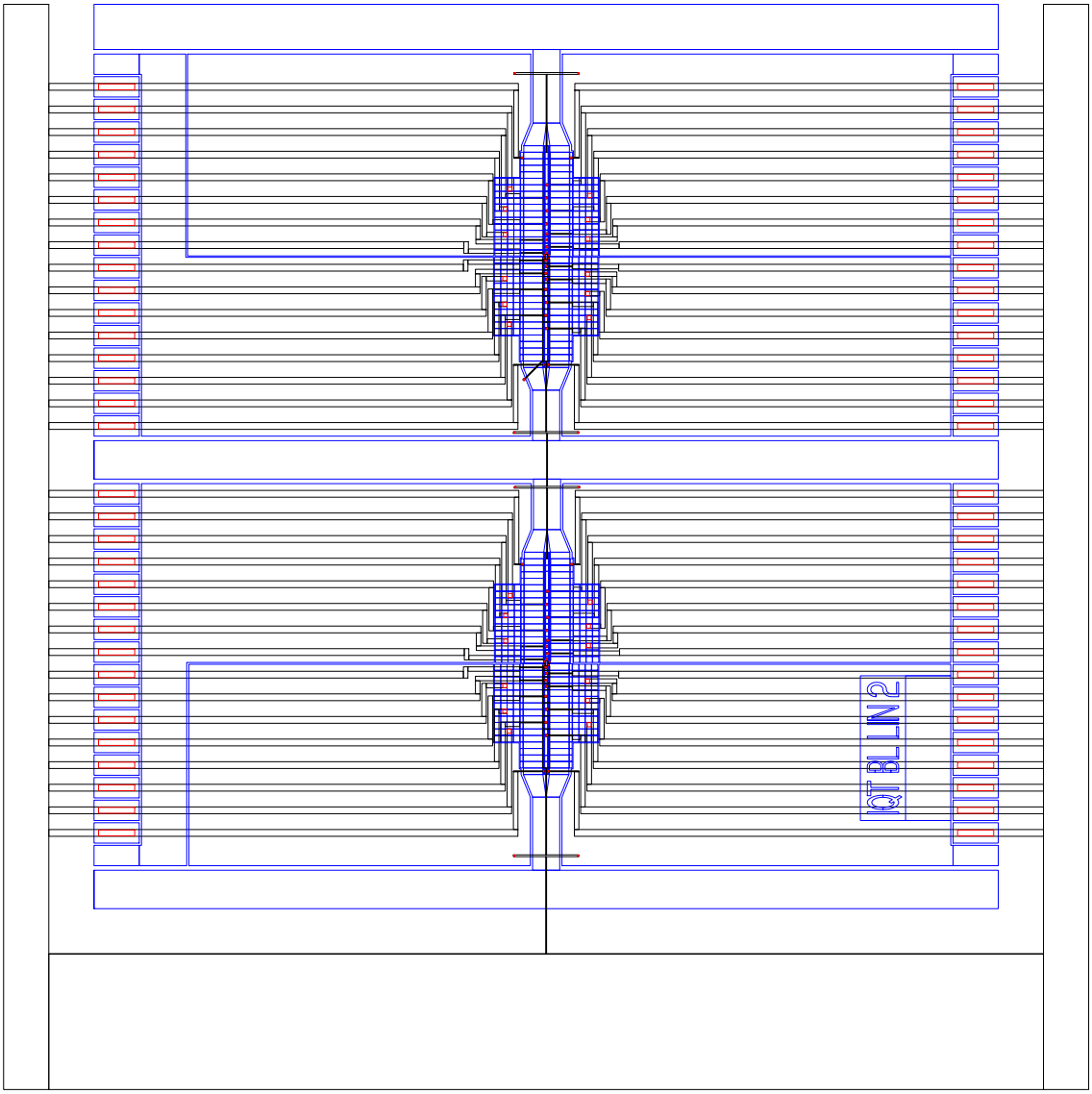


Figure D.14: Ion Trap Design 14: Two linear ion traps with separated rf rails, 100 μm ion height.

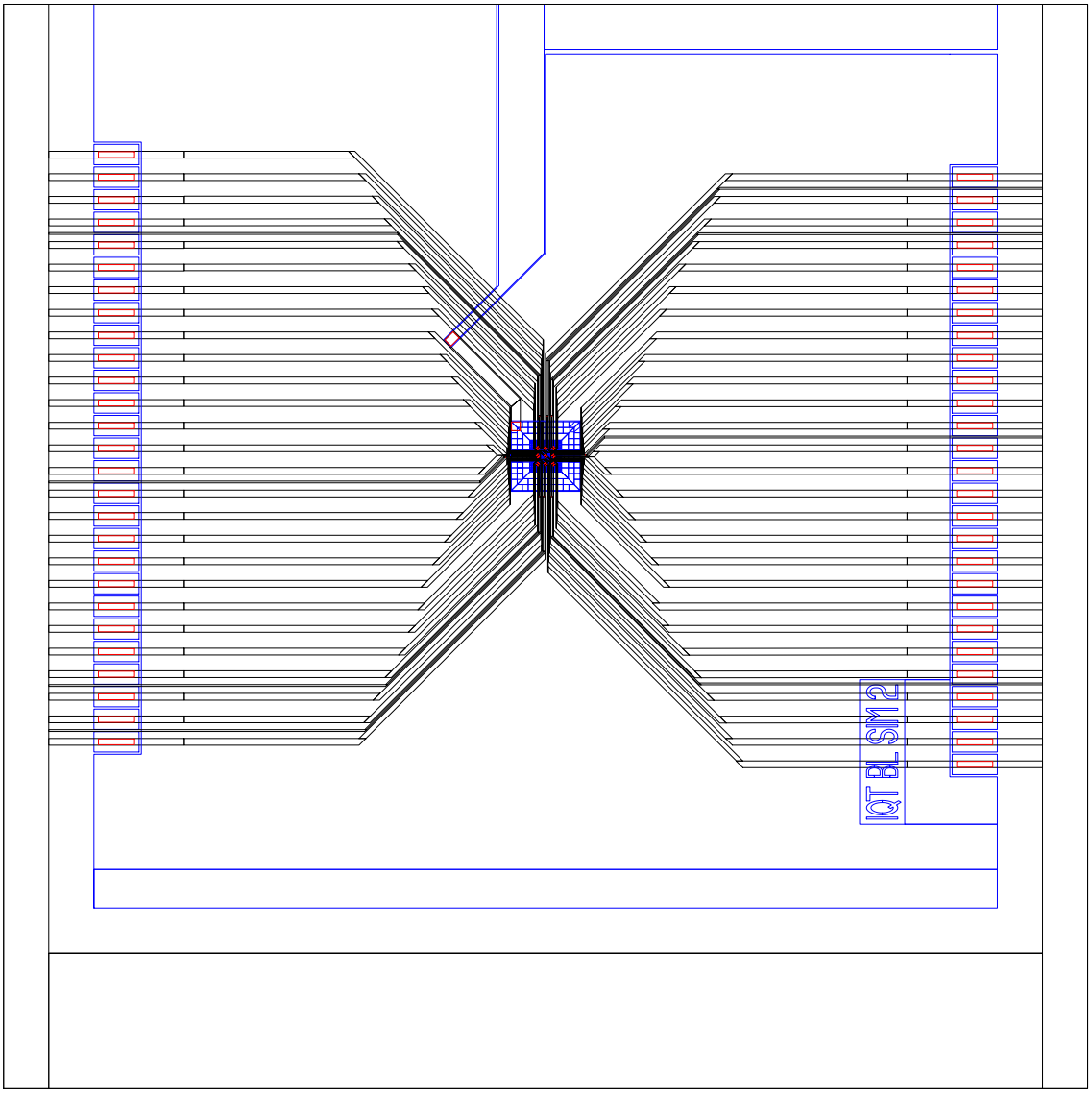


Figure D.15: Ion Trap Design 15: Two-dimensional ion trap array, 50 μm ion height.

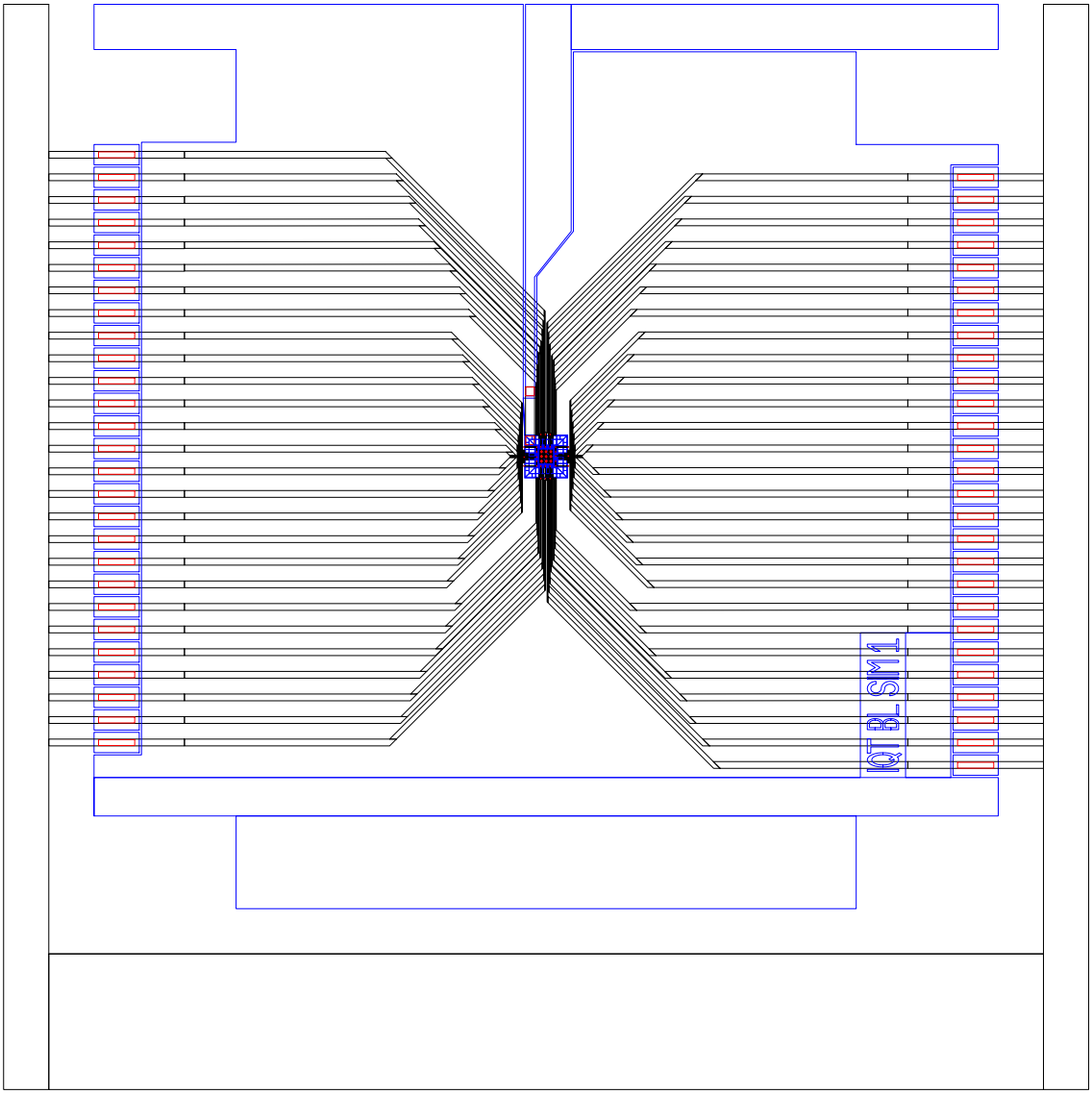


Figure D.16: Ion Trap Design 16: Two-dimensional ion trap array, 30 μm ion height.