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# *An Investigation into Multi-Spectral Excitation Power Sources for Electrical Impedance Tomography*

*By*

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*A thesis submitted for the degree of Doctor of Philosophy*

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*November 2017*

# Declaration

I hereby declare that this thesis has not been and will not be, submitted in whole or in part to another University for the award of any other degree.

Signature: ……...…….....

Tabassum-Ur-Razaq Qureshi

UNIVERSITY OF SUSSEX

TABASSUM-UR-RAZAQ QURESHI- PHD ENGINEERING

# AN INVESTIGATION INTO MULTI-SPECTRAL EXCITATION POWER SOURCES FOR ELECTRICAL IMPEDANCE TOMOGRAPHY

## ABSTRACT

Electrical Impedance Tomography is a non-invasive, non-ionizing, non-destructive and painless imaging technology that can distinguish between cancerous and non-cancerous cells by reproducing tomographic images of the electrical impedance distribution within the body. The primary scope of this thesis is the study of hardware modules required for an EIT system. The key component in any EIT system is the excitation system. Impedance measurement can be performed by applying either a current or voltage through emitting electrodes and then measuring the resulting voltages or current on receiving electrodes.

In this research, both types of excitation systems are investigated and developed for the Sussex EIM system. Firstly, a current source (CS) excitation system is investigated and developed. The performance of the excitation system degrades due to the unwanted capacitance within the system. Hence two CS circuits: Enhance Howland Source (EHS) and EHS combined with a General impedance convertor (GIC: to minimise the unwanted capacitance) are evaluated. Another technique (guard-amplifier) has also been investigated and developed to minimise the effect of stray capacitance. The accuracy of both types of CS circuits are evaluated in terms of its output impedance along with other performance parameters for different loading conditions and the results are compared to show their performance. Both CS circuits were affected by the loading voltage problem. A bootstrapping technique is investigated and integrated with both CS circuits to overcome the loading voltage problem. The research shows that both CS circuits were unable to achieve a high frequency bandwidth (i.e. ≥10MHz) and were limited to 2-3MHz. Alternatively, a discrete components current source was also investigated and developed to achieve a high frequency bandwidth and other desirable performance parameters. The research also introduces a microcontroller module to control the multiplexing involved for different CS circuit configurations via serial port interface software running on a PC.

For breast cancer diagnosis, the interesting characteristics of breast tissues mostly lie above 1MHz, therefore a wideband excitation source covering high frequencies (i.e. ≥1-10MHz) is required. Hence, a second type of the excitation system is investigated. A constant voltage source (VS) circuit was developed for a wide frequency bandwidth with low output impedance. The research investigated three VS architectures and based on their initial bandwidth comparison, a differential VS system was developed to provide a wide frequency bandwidth (≥10MHz). The research presents the performance of the developed VS excitation system for different loading configurations reporting acceptable performance parameters. A voltage measurement system is also developed in this research work. Two different differential amplifier circuits were investigated and developed to measure precise differential voltage at a high frequency.

The research reports a performance comparison of possible types of excitation systems. Results are compared to establish their relationship to performance parameters: frequency bandwidth, output impedance, SNR and phase difference over a wide bandwidth (i.e. up to 10MHz). The objective of this study is to investigate which design is the most appropriate for constructing a wideband excitation system for the Sussex EIM system or any other EIT based biomedical application with wide a bandwidth requirement.

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1. **Qureshi, T. R.,** Chatwin, C., & Wang, W. (2013), Bio-impedance Excitation system: A comparison of voltage source and current source designs. *APCBEE Procedia*, 7, pp42–47.

2. **Qureshi, T. R.,** Chatwin, C. R., Zhou, Z., Li, N. & Wang, W. (2012), Investigation of voltage source design's for electrical impedance mammography (EIM) systems. *34th Annual International Conference of the IEEE Engineering in Medicine and Biology Society*, pp1582–1585.

3. **Qureshi, T. R.,** Chatwin, C. R. & Wang, W. (2012), Design of Wideband Voltage Source Having Low Output Impedance, Flexible Gain and Controllable Feedback Current for EIT Systems. *International proceedings of chemical, biological and environmental engineering (IPCBEE)*, 34, pp45–50.

4. **Qureshi, T.,** Mehboob, B., Chatwin, C. R. & Wang, W. (2012), Optimal device for a low output impedance voltage source for electrical Impedance tomography (EIT) systems. *IEEE International Conference on Electro/Information Technology*, pp1–6.

5. **Qureshi, T. R.,** Mehboob, B., Chatwin, C. R. & Wang, W. (2012), Wideband voltage source design for EIT systems. *38th Annual Northeast Bioengineering Conference (NEBEC)*, pp353–354.

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7. **Qureshi, T. R.,** Li, N., Zarafshani, A., Béqo, N., Chatwin, C. R. & Wang, W. (2012), Performance comparison between voltage source design and current source for Electrical Impedance Mammography (EIM) systems, *13th International Conference on Biomedical Applications of EIT*, 23-25 May, Tianjin China (Accepted for Presentation).

8. Zarafshani, A., **Qureshi, T.,** Bach, T., Chatwin, C. R. & Soleimani, M. (2016), A 3D multi-frequency response electrical mesh phantom for validation of the planar

structure EIT system performance. *IEEE International Conference on Electro Information Technology (EIT),* pp0600–0604.

9. Zarafshani, A., **Qureshi, T. R.,** Bach, T., Chatwin, C. & Soleimani, M. (2016), An Electronic Mesh phantom for planar structure EIT systems *16th International Conference on Electrical Bio-impedance (ICEBI) and 17th Conference on Biomedical Applications of Electrical Impedance Tomography (EIT),* 19-23 June, Stockholm, Sweden, (Accepted for Presentation).

10. Zhang, X., **Qureshi, T.,** Chatwin, C. & Wang, W. (2014), Validity of Using the Sheffield Algorithm for the Sussex EIT MK4, *15th International Conference on Biomedical Applications of Electrical Impedance Tomography, Canada,* p68.

11. Beqo, N., Zarafshani, A., **Qureshi, T. R.,** Chatwin, C., Wang, W., (2013), Converting EIT voxel based imaging and pixel based ultrasound imaging to standardised DICOM, *XVth International Conference on Electrical Bio-Impedance (ICEBI) and XIVth Conference on Electrical Impedance Tomography (EIT),* 22–25 April, Heilbad Heiligenstadt, Germany (Poster Presentation).

12. Zarafshani, A., Hashemi, H., Beqo, N., Chatwin, C., Wang, W. & **Qureshi, T. R.** (2013), Multi-frequency response mesh phantom for validation of EIT system performance, *XVth International Conference on Electrical Bio-Impedance (ICEBI) and XIVth Conference on Electrical Impedance Tomography (EIT),* 22–25 April, Heilbad Heiligenstadt, Germany (Poster Presentation).

13. Li, N., **Qureshi, T. R.,** Zarafshani, A., Béqo, N., Zhou, Z., Xu, H., Chatwin, C. R. & Wang, W. (2012), Fast Lock-in System for Biological Cell Impedance Analysis *13th International Conference on Biomedical Applications of EIT,* 23-25 May, Tianjin China (Accepted for Presentation).

# List of Acronyms

| | |
|---|---|
| 2D: | Two-dimensional |
| 3D: | Three-dimensional |
| AC: | Alternating current |
| ACT: | Applied Current Tomography |
| ADC: | Analogue-to-digital converter |
| APT: | Applied Potential Tomography |
| BI: | Bio-Impedance |
| BIM: | Bio-impedance Measurement |
| BIS | Bio-Impedance Spectroscopy |
| CAT/CT: | Computerized axial tomography |
| CMMR: | Common-mode rejection Ratio |
| CMOS: | Complementary metal–oxide–semiconductor |
| CS: | Current Source |
| CSB: | Current Source Board |
| CSM: | Current Source Module |
| DA: | Differential Amplifier |
| DAC: | Digital-to-analogue convertor |
| DAS: | Data Acquisition System |
| DC: | Direct Current |
| DCCS: | Discrete Component Current Source |
| DCIS: | Ductal Carcinoma in-situ |
| DDS: | Direct Digital Synthesizer |
| DSP: | Digital signal processor |
| DV: | Differential Voltage |
| EHCS: | Enhanced Howland Current Source |
| EIDORS: | EIT and Diffuse Optical Tomography Reconstruction Software |
| EIM: | Electrical Impedance Mammography |
| EIS: | Electrical Impedance Spectroscopy |
| EIT: | Electrical Impedance Tomography |
| ERT: | Electrical Resistance tomography |
| ESM: | Electrode Support Module |
| FDM: | Finite Difference Method |
| FEM: | Finite Element Method |
| FFT: | Fast Fourier Transform |
| FG: | Function Generator |
| FISM: | Front-end Input Switching Module |
| FPGA: | Field programmable gate array |
| GA: | Guard Amplifier |
| GAM: | Guard Amplifier Module |
| GBP: | Gain Bandwidth Product |
| GIC: | Generalized Impedance Convertor |

| | |
|---|---|
| HCS: | Howland current source |
| HCSC: | Howland current source circuit |
| HF-CSM: | High Frequency-Current Source Module |
| IA: | Instrumentation amplifier |
| IC: | Integrated Circuit |
| IDC: | Invasive Ductal Carcinoma |
| ILC: | Invasive Lobular Carcinoma |
| IMM: | Impedance Measurement Module |
| IPM: | Internal Power Module |
| LCIS: | Lobular Carcinoma in-situ |
| LM: | Load Module |
| LPF: | Low-pass filter |
| MF-EIT: | Multi-frequency EIT |
| MPIM: | Microcontroller and PC Interface Module |
| MRI: | Magnetic resonance imaging |
| MUX: | Multiplexer |
| NCO: | Numerical controlled oscillator |
| NI: | National Instruments |
| NIC: | Negative Impedance Converter |
| OTA: | Operational trans-conductance amplifier |
| PCB: | Printed Circuit Board |
| PET: | Positron imaging test |
| PROM: | Programmable read-only memory |
| PSD: | Phase-sensitive demodulation |
| RC: | Resistor-Capacitor |
| RMS: | Root mean Square |
| SMC: | Surface mount component |
| SMD: | Surface-Mount Device |
| SMM: | Signal Multiplexing Module |
| SNR: | Signal-to-noise ratio |
| SUO: | Sample under observation |
| TAM: | Trans-admittance Mammography |
| THC: | Through-hole component |
| VCCS: | Voltage Controlled Current Source |
| VCVS: | Voltage Controlled Voltage Source |
| V-I: | Voltage-to-Current Converter |
| VMM: | Voltage Measurement Module |
| VS: | Voltage source |
| VSB: | Voltage Source Board |
| VSM: | Voltage Source Module |

# List of Symbols

%: Percentage
<: Less than
>: Greater than
±: Positive and Negative polarity
Δ: Delta
‖: Parallel combination
≈: Approximate
≤: Less than and equal to
≥: Greater than and equal to
ω: Angular frequency
µA: Microampere
µs: Microsecond
∞: Infinity
cm: Centimetre
dB: Decibel
F: Farad
*fc*: Relaxation frequency
fps: Frames per second
GΩ: Giga ohm
Hz: Hertz
I: Current
*j*: Complex number
*J*: Current density distribution
k: Kilo
kHz: Kilo-Hertz
M: Mega
mA: Milliamp
MHz: Mega-Hertz
mm: Millimetre
$mm^2$: Square millimetre
$mm^3$: Cubic millimetre
mS: Milli-siemens
mW: Milli-watt
MΩ: Mega-ohm
nA: Nano-ampere
nF: Nano-farad
° : Degree
pC: Pico-coulombs
pF: Pico-farad
p-p: Peak-to-peak
s: Seconds
$s^{-1}$: Per Second
tpc: Times per cycle
V: Voltage and Volts
Z: Impedance
*α*: Relaxation factor constant
*ε*: Permittivity
λ: Wavelength
σ: Electrical impedance distribution
Φ: Phase difference
Ω: Ohm
*ϕ*: Electrical potential distribution

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# Chapter 1

## A General Review of Cancer and its Diagnosis Methodologies

### 1.1 Introduction

Cancer is one of the major medical problems and cause of mortality in the world. Every year, 1-in-250 men and 1-in-300 women is diagnosed cancer. The incidence rises steeply with age so that over the age of 60, 3-in-100 men develop this disease every year. The diagnosis and investigation for this disease is costly and requires a time consuming and labour-intensive treatment. Mostly lung, breast, skin, gut and prostate gland cancers are common in the western world (Coleman et al., 2004; Parkin et al., 2005). Early and reliable cancer detection can deliver substantial health and benefits in the society. This has attracted many researchers around the world, who are contributing to cancer research.

The overall aim of this research work is to design and implement hardware, which will enhance the performance of an Electrical Impedance Tomography (EIT) /Bio-Impedance (BI) system and enable it to become a reliable cancer detection system. The survival rates can be increased by detecting cancer at an early stage. The detection system based on EIT technology provides an opportunity to detect an early stage cancer using a non-invasive method. The detection system's reliability depends on many factors and one of them is the quality of the measuring excitation signal source. The precise focus of this research work is to study the areas related to the improvement of the excitation source followed by the development of a precise and reliable signal excitation system having low noise interference, high frequency bandwidth and capable of driving higher loads. Different analogue circuit architectures for the excitation source have been designed in this research work. The designed excitation sources will have the ability to operate at frequencies between 1kHz to 5MHz. To assess the precision of the generated signal, a printed circuit board (PCB) was implemented with possible load patterns along with high amplitude

voltage measurement circuitry. This provides an opportunity to test the performance of the designed excitation sources for any impedance measurement system. In our case, the successful testing of the excitation source will lead the source circuitry to be integrated into our EIT breast cancer system for clinical application.

The aim of this chapter is to briefly describe the overview of cancer and its related terminologies. The chapter will firstly introduce the cancer and its types followed by the cancer staging, its importance and method to determine staging. This chapter will also describe the diagnosis methods for cancer detection in general. The primary focus of this research work is on breast cancer detection; therefore, the diagnosis methods used for breast cancer detection will also be presented in this thesis. Finally, the chapter will present the research objectives and achievements of this thesis along with thesis organisation.

## 1.2 What is Cancer?

A collection of related diseases can be termed as Cancer and it starts in our body cells. These cells together make up our body tissues and organs. Usually, the cells divide into new cells in a controlled way when the body requires them. Cancer is developed when the growth of cells is uncontrollable and it begins to produce abnormal cells. These abnormal cells keep on dividing and eventually form a lump, which is called a tumour. Not all tumours are cancerous. A lump can be tested to see whether it is cancerous or not, by extracting a small tissue or cell sample from the lump and examining it using a microscope. The tumour which is not cancerous is called benign which may grow but doesn’t spread into nearby tissues. Sometimes it can be large but usually causes problems when it puts pressure on nearby organs. However, when removed they usually don't grow again. The cancerous tumour is called malignant and can spread into nearby tissues. This tumour can sometimes spread from the point it is started (primary) to other parts of the body through the blood or lymphatic system and may begin to grow and form another tumour. This is known as secondary cancer or metastasis. The lymphatic system helps to protect our body from infection and diseases. It drains lymph fluid from body tissues. This system is made up of tubes (lymphatic vessels) which connect to groups of the lymph nodes inside the body. Lymph nodes/glands are a small bean shape, which filter bacteria and disease from lymph fluid.

Some of the UK statistics and information during last few years on cancer incidence, mortality and survival are presented. Statistics show that around 352k new cancer cases occurred in 2013 that gives ≈960 cases diagnosed per day. The ratio of diagnosed cancer in males (179k) was higher than females (173k). The overall contribution of certain cancer types (Breast, prostate, lung and bowl) are 53% of the total new cases in 2013. According to 2011-2013 survey, 50% of the cancer diagnosis were in people aged >70 years (Cancer Research UK, 2013b). Statistics further show that around 163k death cases occurred due to lung, bowel, breast and prostate cancer which is almost 46% of the death rate in 2014 (Cancer Research UK, 2014). Survival rate of cancer shows that 50% of cancer diagnosis cases in England and Wales survive their disease for ≥ 10 years (2010-11). The survival rate is higher in females as compared to males and has been improved in last 40 years in the UK (Cancer Research UK, 2011). The 20 most common cancer incidences in the UK during 2013 are shown in Figure 1.1. The analysis shows that the most common cancer in the UK is breast cancer, which accounts for 15% to the total cases. Other most common cancers account for 13% (prostate & lung) and 12% (bowel) to the total cases in the UK.

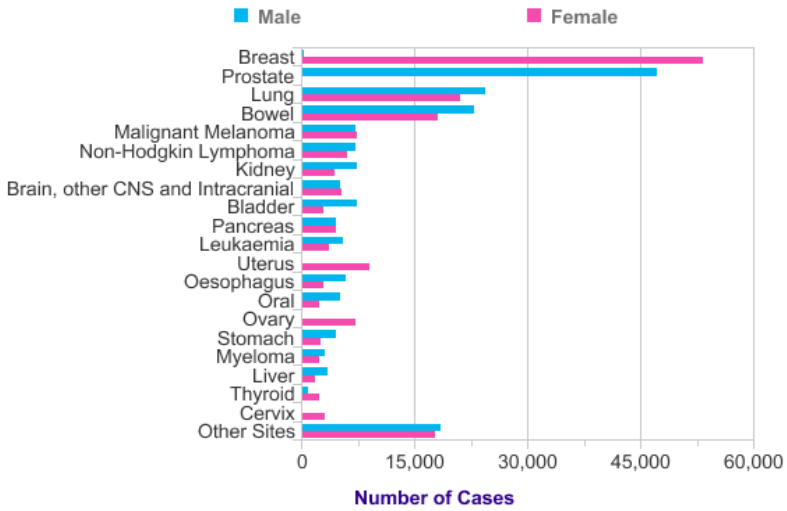



Figure 1.1: Most common cancers incidence in the UK (Cancer Research UK, 2013a)

## 1.2.1 Types of Cancer

There are many types of cancer and usually identified by the name of the organs or tissues from where it generates. The cell type (epithelial or squamous cell) can also describe

Cancer. This section describes the main types of cancer that begin in specific types of cells.

#### 1.2.1.1 Carcinoma

Carcinoma is the most common type of cancer that usually forms a solid tumour. It is formed by epithelial cells and begins in the skin or tissues, which covers the surface of internal organs and glands. There are many types of epithelial cells, which have a specific name for the corresponding carcinoma.

- **Adenocarcinoma** is the cancer created in the epithelial cell, which produces fluids or mucus. Tissues made up of these cells are mostly called glandular tissues. Breast, colon and prostate are classified as adenocarcinomas.
- **Basal cell carcinoma** is the cancer that begins in the lower layer of epidermis (outer layer of skin).
- **Squamous cell carcinoma** is the cancer formed in squamous cell, which lies under the outer surface of the skin. These cells also exist in many other organs: stomach, lungs, bladder, intestines and kidneys.
- **Transitional cell carcinoma** is the cancer formed in epithelial tissue (transitional epithelium). This tissue is made up of many epithelial cell layers and is found in the lining of the bladder, ureters, parts of kidneys and few other organs. Some cancers of these organs are transitional carcinomas.

#### 1.2.1.2 Sarcoma

Sarcoma is the type of cancer that is formed in the bones and tissues that support and connect the body. It can develop in muscles, fat, nerves, joints, blood or lymph vessels and fibrous tissue. The most common cancers of this type are: Osteosarcoma (bones), Kaposi sarcoma, malignant fibrous histiocytoma (soft tissue's) etc.

#### 1.2.1.3 Leukaemia

Leukaemia is the type of cancer that is formed in blood-forming tissue of bone marrow. It begins when healthy blood cells change, grow uncontrollably and usually don't form a solid tumour. Its types are grouped on the basis of: 1) How quickly disease get worse (acute or chronic) and 2) the type of the blood cell started in (lymphoblastic or myeloid).

#### 1.2.1.4 Lymphomas

Lymphomas is the type of cancer, which is formed in the cells of lymphatic system (lymphocytes: T cells or B cells). Lymphocytes are white blood cells that help in fighting against infection and disease. Abnormal lymphocytes build up in lymph nodes and vessels as well as in other body organs represents the existence of this cancer. Lymph tissue can be found throughout the body, as a result this cancer can begin anywhere. It is of two main types: Hodgkin and Non-Hodgkin. Mostly lymphomas are non-Hodgkin, only 1:5 are Hodgkin. Hodgkin has a specific appearance under a microscope and contains Reed Sternberg cells (B-lymphocyte) which become cancerous. Non-Hodgkin doesn't contain Reed Sternberg cells and has a different appearance under the microscope. It has >60 disease types that behave in different ways. It can be formed from B/T cells and can grow slowly or quickly. Both lymphomas can start at any lymph node of the body, but the most common place for its existence is in the neck.

Apart from these types, there are so many different types of cancer, which are difficult to describe in detail and is beyond the scope of this thesis. Detailed type of cancers can be found at: www.cancerresearch uk.org/about-cancer/type.

### 1.2.2 Cancer Staging and Grading

When a cancer is diagnosed, it is important to know its stage (size of a tumour) and grade (growth level). This information helps to decide regarding cancer treatment. During the initial cancer diagnoses, tests are carried out to check the cancer size and whether it has spread into surrounding tissues or another part of the body. To know the stage of the disease, the patient has to go through diagnosis tests or procedures, which are explained later in this chapter. The question may arise, why cancer staging is important? Staging helps in deciding the level of treatment required by the patient. If the cancer is at one place, then a local treatment (surgery or radiotherapy) is sufficient for that particular area of the body. If the cancer has spread then a treatment that circulates throughout the whole body (systemic treatments) is required. Sometimes the lymph nodes near the cancer are checked to assess the possibility of cancer spreading to another part of the body. If cancer cells are found in these nodes then it is an indication that cancer has begun to spread and requires adjuvant treatment (i.e. surgery followed by chemotherapy) with an intension to kill any cancerous cell, which have spread away from primary tumour location.

The cancer staging system can be mainly divided into two types to classify the malignant tumours: The TNM staging system and the Number staging system.

#### 1.2.2.1 The TNM Staging System

The TNM staging system is widely used in cancer diagnosis. This system provides information using three parameters: T (Primary Tumour), N (Regional Lymph Nodes) and M (Distant Metastasis). It uses numbers to specify: the size of the initial cancer, whether it has spread to the lymph nodes and the possibility of it spreading to a different part of the body. A brief explanation of each parameter is described:

- T refers to the size of the cancer and extent the cancer is spread into its surrounding tissues. It is presented by: X (Tumour can't be measured), 0 (Tumour can't be found) and from 1 (small) to 4 (large) tumour. The scale can be further divided to provide more detailed information e.g. T2a and T2b.
- N refers to the possibility of the cancer cell found in nearby lymph nodes and is represented by: X (can't measure cancer) and between 0 (no cancer cell) to 3 (Number and location of node containing cancer cell).
- M refers to the possibility that the cancer has shifted to another part of the body. It can be represented by: X (Metastasis can't be measured), either 0 (not shifted) or 1 (shifted).
- The letter "p" and "c" used before TNM represents the pathological and clinical stage respectively. Letter "p" and "c" refers to the stage based on tumour examination in the laboratory after cancer removal surgery and the cancer information before surgery (physical examination and test reports) respectively.

#### 1.2.2.2 The Number Staging System

This system uses the TNM system to divide the cancer into stages. Most of the cancers have four stages (1 to 4). The general stages for most of the cancers are briefly described here with a detailed breast cancer staging in section 1.3.2.

- **Stage 1:** This refers to a relatively small tumour, which is contained inside the primary location organ.
- **Stage 2:** This refers to the state in which cancer has not started spreading to the surrounding tissue but the size of tumour is larger than the stage 1 tumour. In this

stage, it can be assumed that sometimes the cancer cells have spread to the lymph node, which are closely located to the tumour.

- **Stage 3:** This refers to the state in which the size of cancer is large and it may has started to spread into nearby tissues with a presence of cancer cell in lymph nodes in the respective region.
- **Stage 4:** This refers to the state in which the cancer cells have spread from its initial location to another part of the body (metastatic cancer).

Another staging system, which is used for all types of cancer groups and is classified into five non-numeric categories as: In situ, localized, regional, distant and unknown.

#### 1.2.2.3 Cancer Cell Grading

Cancer cell grading is also an important parameter during diagnosis. It gives the information of how quickly the cancer might grow and is based on the appearance of the cancer cell compared to the normal cell under the microscope. It also helps in the post-surgery treatment. The grading can be categorized as:

- **Grade 1:** The cancer cell's appearance is identical to normal cells and usually has slow growth and less chances to spread into the surrounding tissue.
- **Grade 2:** The cancer cells appearance is abnormal and has a slightly faster growth rate.
- **Grade 3:** The cancer cells appearance is totally different from normal cells and has faster growth rate.

## 1.3 Breast Cancer and its Stages

### 1.3.1 Breast Cancer

An uncontrollable growth of the cells in the breast is an indication of breast cancer. It is mainly related to women's breast but has a possibility to begin in men too. The breasts are composed of: fat tissues, gland tissues divided into lobes and milk ducts. It can start from any part of the breast but mostly it begins in the ducts which carry milk to the nipple (duct cancer) and in the glands, which make milk (lobular cancer). It is not necessary that every type of breast cancer make a lump. It may have any of these signs of cancer: entire

or partly breast swelling, skin irritation, pain in breast/nipple, nipple retraction or discharge, redness/thickness of nipple/breast skin or in armpit lymph node/around collarbone. An important aspect is that most of the breast lumps are benign which don't spread outside the breast. However, some benign lumps can increase the risk to grow towards cancer and should be regularly monitored. Breast cancer can also spread through the lymph system. This is done if cancerous cells have entered the lymph vessels and started growing in the lymph nodes. Once spread to lymph nodes, the cancerous cells have higher chances to spread to other parts of the body and is termed as invasive breast cancer (ductal and lobular). The other type, which stays within the tissue at its primary location without any involvement with surrounding tissues, is termed as in-situ or non-invasive (ductal and lobular). Each type is briefly described:

**Ductal Carcinoma in-situ (DCIS):** It refers to the uncontrollable cells growth specifically in milk ducts without external spread and is considered as an early cancer stage often identified in a mammography scan. It usually doesn't form a lump but may cause breast pain or nipple discharge and can be dangerous if left untreated. It has a tendency of 25-50% to shift into an invasive type within 10 years. About 1:5 new cases (USA) and around 4800 cases (UK) are diagnosed of this type of breast cancer each year (American Cancer Society, 2016; Cancer Research UK, 2016).

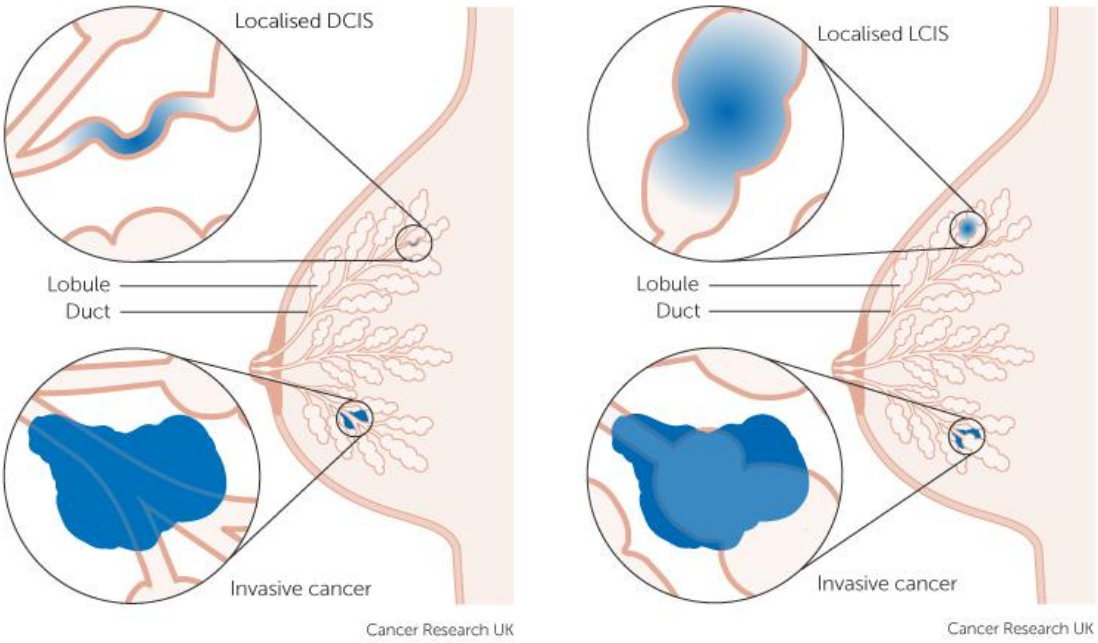
**Lobular Carcinoma in-situ (LCIS):** It refers to the growth of abnormal cells inside the breast lobules and is not identified in a mammography scan due to being symptom less. The cells are often present in the inner lining of the both breast lobules and diagnosed unintended during a biopsy for any other purpose. The existence of LCIS still give risk of being invasive and spreading of breast cancer in either breast over the next few years (1:5 in 15 years). It is diagnosed in about ≈525 women in the UK every year (Cancer Research UK, 2015a).

**Invasive Ductal Carcinoma (IDC):** It refers to the growth of cancerous cells in milk duct (primary location) and spreads into the fatty tissue of the breast by breaking the duct wall. It has an ability to further spread to other parts of the body through the lymph system and blood. IDC has the ratio of 8:10 in the diagnosed invasive breast cancer.

**Invasive Lobular Carcinoma (ILC):** It refers to the growth of cancerous cells in the lobules (primary location) and spreads into other body parts. It is most common in women aged between 45-55 years. Almost a 1:3 ratio of the ILC diagnosis will result in breast

cancer without proper treatment. Its existence is not always in the form of lump, and can appear as a hard/thick breast in the region between armpit and nipple. The ratio of ILC from the diagnosed breast cancer is 1:10.

There are also some less common types of breast cancer, which includes inflammatory breast cancer, nipple Paget disease, phyllodes tumour and angiosarcoma.




*(a)* *(b)*

Figure 1.2: a) Localised and invasive DCIS cancer b) Localised and invasive LCIS cancer (Cancer Research UK, 2016 & 2015a).

## 1.3.2 Breast Cancer Stages

As stated earlier, the main scope of the research work presented in this thesis is based on breast cancer detection using the EIT system. Therefore, it is important to describe the detailed cancer stages of the breast so that a precise measurement can be acquired by the EIT system. It is divided into four number stages. Often stage 1 & 2, 3 and 4 are referred to as early breast cancer, locally advanced breast cancer and metastatic breast cancer respectively. The breast cancer stages with detailed tumour size and extent of its spread is described as (Cancer Research UK, 2015b):

**Stage 1:** This stage is further divided into two sub-stages as:

- **Stage 1A:** In this stage, the tumour is <2cm and has not spread to the nearby lymph nodes and outside the breast.
- **Stage 1B:** In this stage, the tumour is not seen in the breast and few cancer cells exist in the lymph nodes in armpit or the tumour is <0.2cm with few lymph nodes in armpit.

**Stage 2:** This stage is divided into two sub-stages as:

- **Stage 2A:** In this stage, the possibilities are: 1) the tumour is <2cm and the lymph nodes in armpit are affected, 2) the tumour is >2cm but <5cm and lymph nodes in armpit are not affected, 3) No tumour is seen but 1-3 lymph nodes in armpit or near breastbone contain cancer cells.
- **Stage 2B:** In this stage, the tumour is >2cm but <5cm along with existence of cancer cells in the lymph nodes in armpit or near the breastbone, or the tumour is >5cm without any affected lymph nodes in the armpit.

**Stage 3:** This stage is divided into three sub-stages as:

- **Stage 3A:** In this stage either: 1) no tumour, 2) tumour >2cm but <5cm, 3) tumour >5cm is seen and 4-9 lymph nodes in armpit or near the breastbone are affected.
- **Stage 3B:** In this stage, the tumour is fixed to the skin or chest wall with: 1) no cancer cells in armpit's lymph nodes, 2) up to 9 lymph nodes in armpit or near the breastbone are affected.
- **Stage 3C:** In this stage, the tumour can be of any size and has spread to ≥10 lymph nodes in armpit and near the breastbone or to the nodes above and below the collarbone.

**Stage 4:** In this stage, the tumour can be of any size**.** The lymph nodes may or may not be affected with cancer but it has spread to other organs. If the cancer is only found in, lymph nodes under the arm than it can't be considered as stage 4 breast cancer.

## 1.4 Cancer Diagnosis Method

Different methods have been introduced to diagnose cancer. Advancement and more awareness in cancer research work around the world, has resulted in the development of new diagnostic tools and improvement of the existing methods that help to detect cancer.

If the cancer is suspected, the patient has to go through some tests for diagnosis (by pathologists and imaging radiologist). A second opinion regarding cancer diagnosis is highly recommended. Some types of cancer (lymphomas) may be difficult to classify even by an expert doctor. Hence establishing the exact cancer type and size allows the physician to choose the most effective treatment for the patient. The most common diagnostic methods are:

**Biopsy:** In this procedure, a small sample of tissue is removed and examined under a microscope. Depending upon the location, sometime this test can be performed on an outpatient by giving local anaesthesia. Imaging diagnosis tests, (i.e. X-rays) are helpful in detecting the areas or masses of the abnormality but if used alone it can't differentiate between cancerous and non-cancerous cells. Therefore, to make a definite diagnosis, a biopsy is performed for closer examination. A biopsy can be of various types:

- **Bone marrow Biopsy:** This type of biopsy is used if an abnormality is detected in blood or suspect that it has transferred to the bone marrow. This procedure is used to diagnose many blood problems (both cancerous and non-cancerous). During this procedure, a sample of bone marrow is taken out from the back of hipbone using a long needle.
- **Endoscopic Biopsy:** In this procedure a thin flexible plastic tube with a camera on the end, is used to observe the structure inside the organs and body. The tube can be inserted through mouth, rectum, urinary tract or a small skin cut. Specialized tools are passed through the tube to take a sample of tissue for analysis. Examples are: cystoscopy (bladder tissue sample), bronchoscopy (lung tissue sample), colonoscopy (colon sample) etc.
- **Needle Biopsy:** In this procedure, a special needle is used to extract suspicious cells from the affected region. It is often used on the outer region of the skin (e.g. suspicious breast lumps etc.). It can be combined with imaging procedures to collect a sample from the region, which can't be felt through the skin. This procedure includes fine needle aspiration, core needle biopsy, vacuum assisted biopsy, image guided biopsy and surgical biopsy.

**Laboratory Tests:** Low and high levels of certain substances (tumour markers) in the body can indicate the probability of cancer. Hence, laboratory tests of the blood, urine or

other body fluid used to measure those substances can be helpful in the diagnosis process e.g. a higher level of prostate specific antigen in the blood indicates the existence of prostate cancer. It is an important diagnosis tool but it should not be independently considered for conclusive cancer diagnosis decision because abnormal laboratory test results are not a guarantee of the cancer existence and other methods should be used to confirm its presence.

**Imaging Diagnostic:** In imaging diagnosis, pictures of internal areas of the body are produced to see the existence of the tumour. This procedure is significant because it is used as an initial guide to reach a decision before executing any surgery or biopsy procedure. The images are taken by a trained technician and analysed by a radiologist or physician to interpret the diagnostic images. There are many imaging techniques used for cancer diagnosis. These include: X-rays, Computerized axial tomography (CAT/CT) scan, Magnetic resonance imaging (MRI) scan, Ultrasound scan, Positron imaging test (PET) scan and Electrical Impedance Tomography/Mammography (EIT/EIM) for various parts of the body. A comprehensive description of imaging diagnosis techniques is presented in section 1.5.

## 1.5 Imaging Based Cancer Diagnosis

Early cancer detection plays an important role in the survival rate of the patient. Early diagnosis significantly relies on the imaging diagnosis procedures at the screening stage. Imaging and surgical procedures assist each other during the diagnosis process. Biopsy samples provides the stage of the cancer while the imaging procedure provides the location of the cancer region in the designated part of the body. According to the scope of this thesis, the imaging procedures described in this section will focus on breast cancer detection. At the early stage of the breast cancer, the uncontrolled growth of the cells is not started properly and remains with the primary tissue. Hence, the localized cancer can be removed without resorting to the breast removal. There are many different imaging techniques to detect breast cancer. Some of them are being used in medical treatments, whilst others are still in the research and development stages. Each technique has its advantages and disadvantages; therefore, a trade-off needs to be done on the best achievable performance by each technique.

For the case of breast cancer, a self-examination is recommended to identify any physical changes in or on the breast. The physical changes can be: a change in skin, a change in the nipple (either pulled-in or start discharging), lumpy feeling of the breast, breast swelling with reddish skin or a lump under the armpit due to cancer existing in the lymph nodes. In case of any physical changes, the patient should go through screening testing. There is a screening program in the UK for woman (aged 50-70 years), in which the patient is regularly checked using X-ray mammography. This section describes some of the popular imaging modalities used to detect the benign and malignant breast cancers.

### 1.5.1 X-ray Mammography Scan

Mammogram is one of the important, common and oldest tool used to detect breast cancer in early stage because it may show changes in breast months earlier before a patient can feel them. Mammography is of three types: digital mammography, computer-aided detection and breast tomo-synthesis. It is a specialized imaging method, which apply a low-dose of x-rays beam into the breast to identify abnormal tissues by capturing sharp digital images on screen or film. It also has an ability to identify breast changes and locate deep tumours of very small size. During the test, the breast is compressed between two firm surfaces (plates) which flatten the breast tissue for easier imaging. The top surface is adjustable and made of plastic while the bottom surface is fixed for holding x-ray film or digital detector to capture the image. Breast tissues have different attenuation coefficients. When an x-ray beam is passed through these tissues then it will show different levels of attenuation and result in a gray-scale mammogram. The cancer cells are seen as a change in shade (dense light section) in the image produced. This sometimes causes confusion in distinguishing between cancerous cells and normal dense tissue.

This is an invasive procedure due the application of ionising radiation to the body and may initiate cancer with multiple doses. An improved image contrast can be observed by either an increased radiation exposure, or flattened breast compression that results in reduced radiation dose. It restricts patient movement and result in a uniform density image, which make it easier to identity a tumour (Brien, 2011). This technique can identify the location of the tumour but is unable to distinguish between the benign and malignant tumours. Therefore, it is followed by invasive biopsy surgery to collect the sample of affected cells for further examination.

X-ray mammography is currently considered to be the best screening procedure for breast cancer but it doesn't mean that it is without any flaws. If a new imaging technique is developed, which can achieve at least a similar level result without a single mammography drawback then it can be a significant cancer detection equipment in the future. Mammography has a sensitivity and specificity of approximately 75-90% and 85-95% respectively (Liu, 2007).

### 1.5.2 Magnetic Resonance Imaging (MRI) Scan

MRI is the imaging procedure that creates detailed cross-sectional images of inner body structure using radiofrequency waves (40-130MHz), powerful magnets and a computer. It can distinguish between normal and cancerous tissues by precisely identifying the cancerous cells within the body and is useful to disclose metastases. MRI can provide greater contrast as compared to a CT scan within body soft tissues and often used for brain, spine, muscle, inside bones imaging.

During the procedure, the patient lies on a bed that slides into a tunnel shape scanner, which has a strong magnetic field, created by a permanent magnet or super conductor coil. This procedure uses the magnetic properties of certain atomic nuclei (hydrogen nucleus/proton) which are present in the water molecules throughout the body tissues. During this procedure, an electro-magnetic pulse is passed through the body, which excites protons of hydrogen atoms in human tissues, which are aligned by the strong magnetic field and rotated using radio waves. It oscillates in the magnetic field until it is returned into a balanced state. Simultaneously the proton also emits a radio signal that are detected using coils and used for detailed tissue imaging. The resulting images are created using the magnetic relaxation and phase changes within the cell. A few diagnosis procedures require an injection of a contrast dye agent (Gd-DTPA: Gadolinium-diethylenetriamine pentaacetic Acid) into patient's vein before the procedure to enhance the contrast of the image or certain area. These agents minimise the relaxation time of atoms within the body tissues (Carr et al., 1984).

This procedure is painless and usually take longer (30-60 minutes) with a still position otherwise, the image will be blurred. This procedure is not suitable for those patients who have metal (i.e. pacemakers, pins or rod in bones, cardiac defibrillators) inside their body. For breast cancer detection, it can be considered as a second test after initial x-ray

mammography. Breast MRI can't be used alone for cancer diagnosis because of relatively high ratio of false positives. MRI is used in some specific breast problems such as: silicone implant rupture evaluation, scar distinguishing from cancer recurrence and breast cancer local staging. MRI is more sensitive than mammography and doesn't emit any dangerous radiation (like x-rays). However, it is less specific, expensive and can be a difficult procedure for the patients that leads this procedure to not be appropriate for routine screening.

### 1.5.3 Ultrasound / Sonography Scan

This is an imaging procedure in which images of internal body parts/tissues are created using high frequency (1–10MHz) sound waves that are beyond human ear detection. This procedure creates images in real time and reveals the internal structure and movement of the body organs. It is mostly referred by specific body parts and are commonly used for scanning abdomen, breast, heart, prostate, kidneys, testicle etc. Another application of ultrasound in human diagnosis is to determine the blood velocity by the measurement of Doppler shift within a single frequency ultrasound beam (Brown et al., 1999).

A transducer is used to receive the bounced echoed sound waves from the organs. The transducer processes the reflected sound waves by converting them into an image of the detected organ/tissue and displays them on a computer. This procedure differentiates the tissue types by the speed and volume of the sound waves when received by the transducer. The reverberation of the sound waves for abnormal tissues are different from normal tissue that help to differentiate between normal and cancerous cells. Like other procedures, ultrasound also can identify the abnormalities and can be used as a guide for a follow-up biopsy.

During the procedure, the patient lies on the bed next to the ultrasound scanner, which is attached to a portable transducer. A gel is applied on the skin to help eliminate air pockets (which can degrade image quality). The portable transducer is pressed firmly on the targeted body part and the screen displays the internal image of the tissues or organs. The procedure usually takes ≈20mins. Breast ultrasound can't be used alone for cancer diagnosis because it may miss the tumours, which can be detected by mammography. Hence, it is used as an adjunct method with mammography to diagnose the cancer in dense breasts of young woman's (Beqo et al., 2013; Berg et al., 2012).

Ultrasound imaging produces high spatial resolution images without any exposure to dangerous rays and has high sensitivity especially in dense breast tissues. Ultrasound performance is limited due to its poor soft tissues contrast and inability to capture electrical properties to determine the difference between the tissues. Hence, detection is limited to only distinguish between solid and fluid filled tissues. As a result, breast ultrasound is not a common procedure for screening.

### 1.5.4 Nuclear Medicine Imaging Scan

Positron Emission Tomography (PET) is another non-invasive procedure that reconstructs the internal 3D images of organs and tissues using nuclear medicine imaging. PET imaging discloses the functionality level of body tissues, areas of abnormal metabolic activity and can identify the cellular level body changes with a possibility of early cancerous cells detection before it is apparent on other imaging procedures. Its advanced version is the integration of PET with CT in one machine. PET-CT scan has an ability to reveal both, the structure and functions of the body cells and tissues. The combination of two technologies provide a detailed imaging of the cancerous cells as compared to their separate imaging with a high accuracy level. PET-CT scanner is very expensive and is only available in few UK hospitals. PET is a gamma imaging technique, which uses radiotracers to emit positrons. Gamma rays are produced when positron combines with an electron inside the body. An encounter that annihilates both electron and positron and results in two gamma rays moving in opposite directions. Mapping of these gamma rays arriving at the same time, the PET scanner is able to produce a high spatial resolution image.

Before the scan, a glucose solution is injected into the patient, which contains a very small amount of radiotracers (Fluoro-deoxy-glucose: $^{18}$F-FDG). It reduces radiation exposure and has a short half-life (110mins) (Alauddin, 2012; Miele et al., 2008). Certain time must be given so that the material is absorbed by the body tissues. The patient lies on a bed that slides into a tunnel-shape scanner. The cancerous cells are identified by the level of glucose absorption in the cells (cancerous cells absorb high glucose) and the rate at which tumour is using glucose (determine tumour grade). In the PET-CT scan, additional x-rays around the body at different angles are taken and both information is integrated in to a single image.

PET and PET-CT scan are used to: detect cancer, check whether cancer has spread to other body parts, determine whether cancer has returned after treatment, determine blood flow to heart, evaluate brain abnormalities and map normal brain and heart functions. PET scans are not used for breast cancer screening because of its inability to detect small tumours. After breast cancer diagnosis, PET scans are useful to evaluate whether cancer has spread to lymph nodes/other parts of body or the cancer has returned after treatment.

### 1.5.5 Electrical Impedance Tomography (EIT) Scan

EIT is a non-invasive, non-destructive and under-developed medical imaging technique. It is used to investigate the internal impedance (permittivity/conductivity) distribution at an electrical frequency so that an early physiological or pathology change of body organs/tissues can be found. The benign and malignant tissue differ with each other in electrical impedance properties (Fricke & Morse, 1926). The difference of electrical properties is because of cell difference in: water and electrolyte content, membrane permeability changes, orientation and density (Surowiec et al., 1988). This electrical difference approach has been widely recognised and investigated for cancer detection. Hence all the impedance based imaging techniques being researched currently is the advancement of this concept and EIT is one of them.

EIT imaging can be applied to any part of the body. Its application for the breast cancer detection is widely referred as Electrical Impedance Mammography (EIM). Like other body tissues, breast tissues also have unique electrical properties, which can be shown using a breast impedance map to identify the presence of tumour. Malignant breast tissues will show higher conductivity/permittivity levels as compared to its surrounding tissues. Hence, a significantly high conductivity/permittivity area in the reconstructed image can be referred as breast cancer.

During the EIM scan, a small amplitude current/voltage is applied to the breast skin using several pairs of electrodes. The resultant voltage/current measurements are acquired from the surface of breast using the same or different electrodes. These measurements are reconstructed to show the internal conductivity/permittivity of the breast using EIT imaging software. Before the development of any physical tumour symptoms, cancerous cells must have developed some cytological and histological changes. Hence, the study of electrical properties of the tissues gives this opportunity and its implementation via EIM helps to detect the breast cancer at an early stage for effective treatment.

An early method of impedance mapping imaging (T-SCAN: detailed description in chapter 3) was also introduced to work along x-ray mammography and ultrasound with an intention to be its replacement. This system was a breakthrough for the impedance imaging community and attracted many researchers to further study this area of research that resulted in the development of the EIT technique.

EIT/EIM is a very useful imaging technique which is being studied by many research groups around the world but still suffering from significant challenges and it needs to be fully tested in clinical trials before it is launched as a replacement method for its competitor diagnosis technologies. Our research group at the University of Sussex has been researching on the EIM project for many years and have developed a series of significant breast cancer detection prototypes system. The detailed description of EIT method and Sussex EIM system is presented later in chapter 2 & 3 of this thesis respectively.

## 1.6 Research Objectives and Achievements

The aim of this research work is to focus on the performance constraints of the Sussex EIM system. The frequency bandwidth of the EIM system is the key parameter, which is going to be investigating in this research. The frequency bandwidth of the system is limited due to the presence of unwanted stray capacitance in the system. This research work will precisely focus on the analogue circuitry of the system and will identify all the possible sources of additional capacitance. The front-end analogue circuitry frequency bandwidth is limited due to the excitation system (current/voltage source) and the multiplexers. The research is going to investigate the ways to improve the quality of excitation system and method to minimise the effect of unwanted capacitance with the help of simulation tests and its validation by practical implementation. The intended frequency bandwidth to be achieved is at least 3–10MHz.

The major work in this research has been done on the excitation system of the EIT system. The achievements of this research are summarised as:

- The excitation system for the latest prototype Sussex EIM system is based on a current source. Its performance is limited due to current source output capacitance and stray capacitance of the system. The excitation source is further researched

by identification of all possible capacitance sources in the latest prototype system. A method called Generalized Impedance Convertor (GIC) for capacitance elimination/minimization has been introduced in the research. The parallel combination of the current source and GIC circuitry is evaluated. Multiple combinations of this circuitry are achieved for a limited frequency bandwidth. Although it has achieved a high frequency bandwidth (≈3MHz) but on certain selected frequencies.

- The excitation system has previously been implemented by low power supply voltages (i.e. ±5V). During its performance evaluation, signal saturation was observed when the excitation source drives a high load value. The GIC circuitry was also affected with this loading problem. To overcome this problem, a bootstrapping technique was introduced. Both circuits (current source and GIC) are bootstrapped and their high output voltage amplitude performance is achieved.
- A technique called Guard Amplifier is investigated and evaluated. This technique is also introduced to demonstrate the elimination of the unwanted capacitance. This technique is based on the principle that a high input impedance amplifier with a gain ≈1, drives a capacitor to make it smaller or a resistor to make it effectively large. This technique has been evaluated and has achieved good performance.
- A high frequency (10MHz) discrete component current source is designed and evaluated. The current source with capacitance cancellation circuitry (GIC) was not able to achieve a high frequency bandwidth response and its performance is limited to ≈2-3MHz. The discrete component current source has achieved a high value load drive with a good phase response.
- Before the integration of the new designed excitation system into the main EIM system, its performance should be evaluated independently. Hence, a PC interface was required to control the excitation source. A serial port interface controlled by an on-board microcontroller was implemented and evaluated. A software interface is written in visual basic and microcontroller controlling command routines are written using MPLAB C-compiler. The PC interface and microcontroller software has achieved the required performance for interfacing.

- An on-board power supply system was required to keep the external power inputs minimal. Hence, the required power supplies are generated internally using a linear voltage regulator to generate a fixed output voltage.
- An on-board variable testing load circuitry is implemented to evaluate the performance of the excitation sources. The multiplexing of the variable loads is controlled by the microcontroller.
- During investigation of current source circuitry, it was observed that the circuit becomes complex due to the addition of GIC, guard amplifier and bootstrapping circuits. Therefore, another excitation source based on a voltage source was designed and evaluated. The voltage source has achieved better frequency bandwidth performance as compared to the current source along with other performance parameters. The voltage source has an ability to generate a variable voltage again with controllable feedback current and can drive higher load values.
- A voltage measurement system is also designed and evaluated. It is used to measure the required voltages at selective ports. Two different circuit topologies are designed for voltage measurement: Differential measurement using op-amp and discrete components. Both differential amplifiers performance are evaluated and acceptable performance is achieved.

## 1.7 Thesis Organisation

This section briefly describes the contents of the thesis presented in each chapter. The thesis includes the author's research work related to the EIT technology specifically for the hardware part of the EIT system. This chapter presents the literature to understand the cancer, its types along with its staging and grading system. It also presents commonly used diagnosis method for cancer detection.

Chapter 2 provides the detailed literature regarding the EIT technology that includes: the concept of bio-impedance with its application, EIT applications and brief history in medical industry. The EIT principle along with its hardware and software components, its key progress and challenges along with proposed techniques to improve the EIT system performance related to the scope of this thesis.

Chapter 3 provides a detailed overview of the existing EIT excitation sub-system categorized on its measurement method. The chapter provides the EIT measurement methods along with excitation signal safety limit and benefits/limitations of both excitation protocols. The chapter mainly focuses on the existing popular EIT systems around the world, which are described according to the excitation type. Finally, the chapter presents a detailed description about the Sussex EIM prototype systems.

Chapter 4 introduces the performance evaluation of the excitation system based on a current source. A commonly used current source in the EIT community is chosen for further research. The chapter also introduces a method (GIC) used to cancel the additional capacitance involved in the system. The chapter provides the results using performance parameters (frequency-bandwidth and output impedance) for both circuits along with its limitations.

Chapter 5 introduces the solution for the problems identified in chapter 4 for current source based excitation system. The chapter introduces a bootstrapping technique and guard amplifier technique to resolve the loading voltage and capacitance problems respectively. The chapter provides the performance of the earlier described current source along with the additional developed circuitry. Finally, the chapter introduces a new discrete component current source design, which can achieve a high frequency bandwidth with constant amplitude.

Chapter 6 introduces a new excitation system based on a voltage source specially developed for Sussex next generation EIM system. The chapter also introduces a new voltage measurement system based on a discrete components and op-amp, which is capable to measure a precise high amplitude signal. The chapter also provides the performance of the voltage source and its benefits/limitations over current source design.

Chapter 7 provides the practical implementation for both types of developed excitation system. The chapter provides the block diagram for the PCB packaging to understand the architecture of the PCB. The chapter presents the performance of both excitation systems using experimental results. The chapter also provides the limitations of the designed circuit in comparison with the simulated results.

Chapter 8 provides a general discussion and conclusion of the thesis along with future aspects of this research work.

# Chapter 2

# Electrical Impedance Tomography: Background and Theory

## 2.1 Introduction

The imaging of an object internal structure using a non-invasive and non-destructive methodology has been a challenge for researchers over the years. The BI/EIT technique is one of the possible solutions and is used to obtain information from an inaccessible region within a closed and dense object under observation. This chapter reviews the principle of an EIT technique along with its applications in different fields. This chapter will briefly review the history of the EIT technique and will present its instrumentation and reconstruction algorithm. The advantages and limitations of this technique will also be presented along with the areas of improvement considered by most of the researchers. Finally, the chapter will present the proposed method to improve the performance of the excitation signal generator for the Sussex EIM system.

## 2.2 Bio-impedance of a Biological Tissue

The cell is a self-contained and fully operational living entity in a human being. Different types of multicellular organisms work together to sustain life. A group of cells working together to perform the same activity is known as tissue. It is important to know the properties of the object under observation before applying any measurement method. A living cell is composed of various organelles and the Nucleus is one of them. All the organelles are bonded in the presence of intra-cellular fluid within a cell membrane. The cell membrane is surrounded by an extra-cellular fluid, which bonds with other cells and forms biological tissue.

The electrical properties of biological tissue is a popular subject of research, especially for in-vivo studies. The parameter that describes the basic electrical properties of the

biological tissue in terms of current flow opposition is the impedance (Holder, 2005). It was suggested that electrical impedance properties of different tissues can be represented by combination of resistors and capacitors in the absence of magnetic effects (Fricke, 1925). An applied potential *(V)* across a biological tissue will tend to follow a current *(I)* through the tissue, which results in an electrical impedance *(Z)*. The impedance is a function of frequency and is described by a complex mathematical relation between voltage and current, which is: $Z = R + j\,X$. The resistance measures the opposition to the flow of current and capacitance measure the ability to store electrical charge.

Fricke and Morse represent the electrical properties of cell suspension by the equivalent 3-element model; this model was first used in the field of EIT by Cole and Cole described by a mathematical expression. The impedance of the cell was modelled as a parallel circuit containing two resistances and capacitance as shown in Figure 2.1(b). The resistances *($R_e$ & $R_i$)* and capacitance *($C_m$)* represents the extra-cellular fluid, intra-cellular fluid and bi-lip cell membrane respectively.

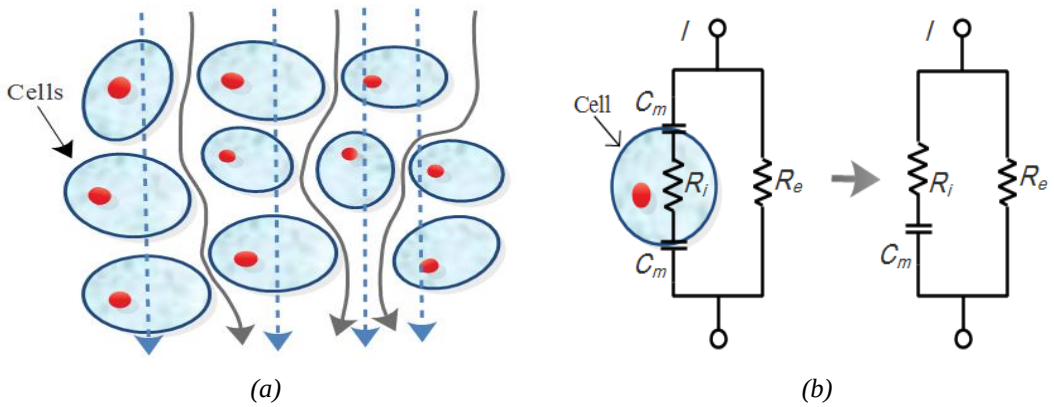



Figure 2.1: a) Current flow through cells at low (gray line) and high (blue dotted line) frequencies. b) The 3-element equivalent circuit model of biological impedance.

The resulting cell impedance is given by the Cole-Cole equation in Eq. 2.1.

$$Z = R_\infty + \frac{(R_0 - R_\infty)}{1 + \left(\frac{jf}{f_c}\right)^{1-\propto}} \qquad \text{Eq. (2.1)}$$

where $Z$ is the impedance at frequency ω; $R_0$ *and* $R_\infty$ are resistance values at low and high frequencies respectively; *fc* is the relaxation frequency; *f* is frequency; *α* is the relaxation factor constant and *j* indicates a complex number. The above equation is widely used to describe the dispersion in biological materials. All body tissues can be characterised with

different value of $R_e$, $R_i$ *and* $C_m$ in the equivalent 3-element circuit model. Any change in internal impedance will affect the path of the current through the tissue. If the impedance change is detectable and quantified then the individuality of the impedance value can be helpful in cell identification (Cole and Cole, 1941). Impedance characteristics of normal and cancerous tissue are different. It was suggested that cancerous tumour capacitance is increased as compared to a benign tumour. Later generally, it was suggested that cancerous tissue shows low impedance magnitude as compared to normal tissue particularly in breast tissues (Jossinet, 1998; Fricke & Morse, 1926).

At low frequencies, the current doesn't penetrate into the cell membrane due to its high impedance and follows the longer path through the extra-cellular fluid. The capacitance of the cell membrane acts as an open circuit and therefore the impedance is purely resistive *($R_e$)* and shows electrical properties of extra-cellular fluid. At high frequencies, the cell membrane become conductive and the current passes in straight lines through the cells. The capacitance of the cell membrane acts as a short circuit, which never get fully charged or discharged. Therefore, at high frequencies, the impedance is described by a combination of intra-cellular and extra-cellular fluid and can be modelled as a parallel combination of resistance $R_e$ *and* $R_i$. The current paths at different frequencies are presented in Figure 2.1(a). Hence, $R_0$, $R_\infty$ and $f_c$ in Eq. 2.1 can be expressed as:

$$R_0 = R_e \qquad \text{Eq. (2.2)}$$

$$R_\infty = \frac{R_i R_e}{R_i + R_e} \qquad \text{Eq. (2.3)}$$

$$f_c = \frac{1}{2\pi(R_i + R_e)C} \qquad \text{Eq. (2.4)}$$

Based on the above parameters, the calculated impedance value can be plotted against the acquisition frequency and represented as in the Figure 2.2. The biological tissue membrane behaves like a dielectric at low frequencies. This behaviour is shown in the plot as a drop off at ≈10kHz and full penetration of current is achieved at ≈1MHz. Therefore, using this method identification of cancerous tissue is possible with the help of impedance statistics.

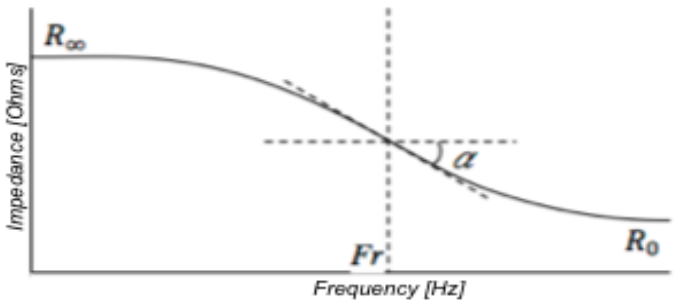



Figure 2.2: Impedance plot vs Frequency (Beqo, 2012).

**Bio-impedance Measurement (BIM):** Different methods have been employed to measure electrical impedance. The magnitude and phase information of the biological tissue extracted from the measurement is used for clinical diagnosis and research studies. The wheatstone bridge was the first circuit used in BIM. The measurement based on this circuit gives high accuracy but gives a slow measurement speed due to the bridge balancing problem especially at high frequencies and make it unsuitable for monitoring purposes.

The simplest method to measure biological impedance is through the I-V method. In this method, the unknown impedance can be calculated from voltage and current measurements. The current is calculated using the voltage measurement across a known low resistance. Two configurations are employed in BIM: 2-electrode/4-electrode method. In the 2-electrode method, the same electrodes are used to apply current to the tissue being observed and then sense the resulting voltage. The ratio between the output voltage and current compute the calculated impedance of the region under observation. In the case of an AC input voltage or current signal, the output voltage is modulated with a carrier and it needs demodulation of the signal to recover the biological impedance. The 2-electrode measurement method exhibits a polarization impedance between electrode and electrolyte, which is added in the total measured impedance. To resolve this problem, the injecting electrodes are separated from the sensing electrodes, which result in a 4-electrode measurement method. The 4-electrode configuration is illustrated in Figure 2.3.

The generated current from a voltage source $(V_{in})$ is injected into the tissue through electrode pair A & B via a series resistor $(R)$ and the voltage is measured on electrode pair C & D. The impedance measurement can be calculated using the V/I ratio from the collected data. The output signal is similar to input but has different phase magnitude properties. The collected BIM data is a combination of an in-phase and out-of-phase

signal, which reflects the resistive element and reactive elements of the tissue respectively. The injected current should be independent of the interference impedance, which can be achieved when the output impedance of the current source is larger as compared to the tissue and interference impedance. If the current injection electrode pair is moved apart from the voltage read pair, then the current transmission lines are uniformly distributed in the region. However, the distribution of current transmission lines is limited by the shape of the tissue and its physiological conditions. The voltage read electrode pair would still be affected by the polarization impedance and can be minimised by using a high input impedance measurement circuit. The architecture of the electrodes is still an important research area in BIM systems.

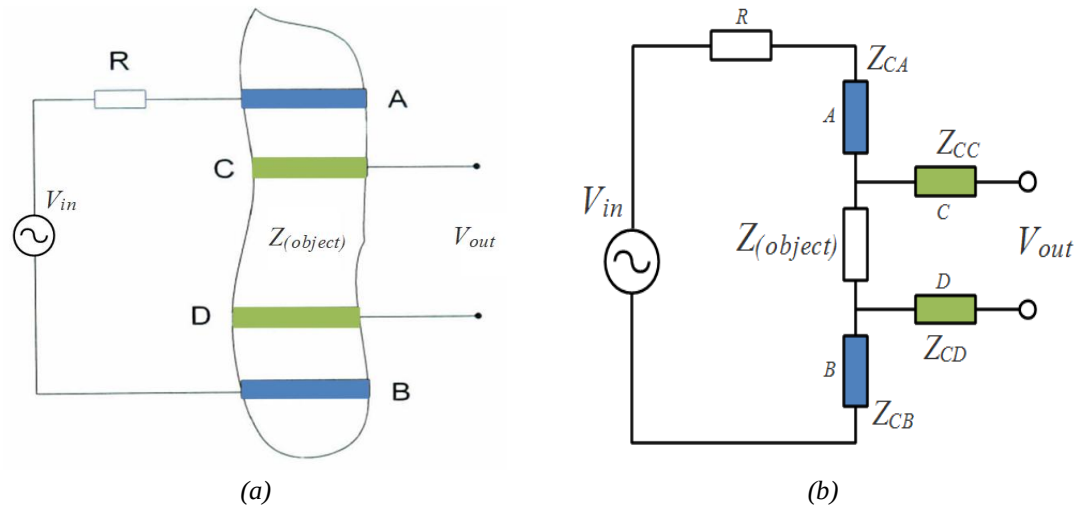



Figure 2.3: a) The 4-electrode measurement configuration. b) The equivalent 4-electrode measurement circuit with electrode contact impedance $Z_{CA}$, $Z_{CB}$, $Z_{CC}$ & $Z_{CD}$ (Yang, 2006).

***Bio-impedance Medical Application:*** BIM can be applied to many areas in the medical field such as diagnostic/monitoring applications, laboratory experiments and perception/hazard analysis. Some of its applications are: cellular fluid measurement, body volume change and composition measurement, tissue identification, and tissue/organ monitoring. Tissue identification is an important and significantly used bio-impedance application. Different tissues exhibit different electrical properties and are characterized by the Cole-Cole model. One of the most significant applications of bio-impedance characterization is detection of cancerous tissues. The cancerous tissue exhibits different bioelectrical properties to normal/benign tissues. During the early stage of a tumour, the tissue internal bio-impedance abnormalities can be detected by this method. The early method to detect cancer using this method was for breast cancer diagnosis (Fricke &

Morse, 1926). It is also applied to other cancer tissue detection like: premalignant cervical tissue, prostate cancer, bladder tissue etc. Another application of this method is tissue/organ monitoring during surgery using bio-impedance parameters: cardiac ischemia, cryosurgery, and to monitor organs to be transplanted and determine their suitability for transplantation by quantifying the ischemia damage during the transplantation process (Dai, 2008; Casas et al., 1999; Linhart et al., 1995). An extension of the bio-impedance method is electrical impedance tomography, which maps bioelectrical properties of an object onto a 2D image or 3D volume. An image of internal conductivity/permittivity distribution of the region is reconstructed from boundary electrical measurements. It is described in detail in the next section.

## 2.3 Electrical Impedance Tomography

Electrical impedance is a property that opposes the flow of current. Tomography is derived from Greek words *tomos* and graphy which means volume/section or slice and field of study/plot respectively. Combining these terminologies, EIT can be generally termed as to describe the impedance properties of the object under observation.

### 2.3.1 Background of EIT

Researchers from different disciplines have developed interest in the EIT imaging method. This includes mathematicians, physicists, instrumentation engineers and clinicians with an interest in mathematical problems related to image reconstruction, bio-impedance and clinical problems respectively. This technique captures the measurement around the boundary of the object by injecting alternating current (AC) to the object via attached electrodes or by induction. The resultant internal electrical properties distribution of the object is extracted by surface voltage measurement using an array of electrodes. A series of measurements are collected in the form of a data set by sampling the volume as much as possible. This technique provides a unique physical property of the object; therefore, it is believed that EIT has a great potential in functional imaging except for anatomical imaging. In the next section, a brief overview of the applications of the EIT method are described. The detailed description will be provided for the medical imaging specifically for the potential clinical applications of EIT.

### 2.3.2 Applications of EIT

The EIT technology has been applied in many applications and can be primarily classified in three major fields: Industrial, Geophysical and Medical. In industrial application (process tomography) it is used to monitor imaging of pipeline fluids, fluid distribution measurement in mixing vessels and crack detection (Ma et al., 2003; Alessandrini & Rondi 1999; Dickin & Wang 1996). It uses the impedance tomography method to image conducting fluids within vats or flowing within pipelines and uses the capacitive tomography method for dielectric material (Soleimani et al., 2009). Its intention is to measure the interested quantities distribution and to interfere the process taking place in different environments (i.e. pipes, tanks and vessels). It is specifically used as a monitoring method for chemical reactions, spatial/temporal concentration variations, phase fraction in mass flows and various mixing and separation processes (Razzak et al., 2009; Kourunen et al., 2008; Tapp et al., 2003).

The electrical properties of geophysical materials (soil, rocks and liquids) contains a variety of information about the geophysical/archaeological structures under the earth's surface. In geophysical tomography, the EIT technique is used for receptivity survey on geological structures, which includes geophysical prospecting, measurement of surface, and cross bore hole (Polydorides et al., 2002; Loke & Barker, 1996). Sensors are placed on the earth's surface or in holes to position resistivity singularities. For example, rock resistivity varies and will have several orders of magnitude depending upon the nature of the rock and water content in it. The EIT system for this particular field is equipped with an array of equally spaced sensors with a set pattern of geometrical factors to effectively represent the conductivities. The distance between sensors defines the spatial resolution (typically in order of meters) and penetration depth (typically ≤500m) of the object. These geophysical experiments typically require larger current amplitude (≤15mA) and sensors spacing (1000m). If high resolution is required then sensor spacing needs to be decreased. A difficulty in this field is earth's behaviour, which acts like a non-linear capacitor and results in a surface polarization with a satisfactory image reconstruction.

An important and widely used application of the EIT measurement is in medical research. This field of application is based on the fact that the biological tissues are recognised from their conductivity/permittivity which varies with health state and during physiological organ functioning (Kyriacou et al., 2000; Schwan, 1994; Stoy et al., 1982). For bio-

impedance EIT, the researchers have studied the difference in the electrical properties of the tumorous and normal tissues from clinical studies aspect. Malignant breast tissues electrical properties have been studied and showed a significantly higher permeability of tumorous tissue at low frequency (20kHz) as compared to normal tissues (Jossinet, 1996; Surowiec et al., 1988). Another aspect of bio-impedance EIT is based on a complete biological system for cardiac and respiratory functions, body fluid quantities and tissue composition (Kinouchi et al., 1997). Detailed study of tissue diagnoses can be obtained by taking BIM of the local affected tissues. By acquiring a couple of 2D sample slices from the patient, an image can be obtained which forms a comprehensive physiological model by combining the mechanical assembly and EIT imaging for a specific application. Hence, it shows that in the field of medical diagnosis, the interest mostly lies in imaging of the body organs, bones and breast tumour tissues that have different characteristics impendences.

### 2.3.3 Brief History of EIT in Medical Application

EIT imaging method has a long history and can be traced back from the time when it was mostly used in nonclinical applications (i.e. geological & industrial research studies). After 1978, Henderson and Webster published the first impedance reconstructed image related to human thorax tissue (Henderson and Webster, 1978). The image was a transthoracic impedance image instead of real tomographic image. The system was excited with a 100kHz voltage signal and sequential current measurements were made on each electrode. It was based on the theoretical assumption that the current signal flows in straight lines through the body and conductivity variation will be observed in the case with any obstacle in the path. The image was produced from the tissue's transmission map using a rectangular array of electrodes (≈144) on the chest with a large single electrode plate on the backside of the chest to make an earthed connection. Their result showed that the existence of lungs corresponded with a low conductivity area in the image.

After this step towards impedance imaging, the researcher focused on the development of different image reconstruction techniques. The first prototype clinical impedance tomography system was developed in 1987 at the University of Sheffield (Sheffield Mark 1) (Brown and Seagar, 1987; Barber and Brown, 1984). It consisted of 16-channels, single 50kHz current source and used a multiplexer to inject multiple current signal and making

voltage measurements at adjacent electrodes pair. This system was considered to be inexpensive and portable as compared to the imaging systems available at that time (i.e. MRI, CT and ultrasound scanner). This system has been used as a prototype system by many EIT research groups for clinical studies (Oh et al., 2011; Fabrizi et al., 2009; McEwan et al., 2006).

The Sheffield group also presented an algorithm to image a 2D cross-section based on the back-projection method with a reference measurement acquired at different frequencies with respect to each other (Hampshire et al., 1995; Brown et al., 1994). The first image using this approach was reported for a human arm in a saline tank having a very low resolution but regarded as the first ever in-vivo reconstructed image with a data acquisition system accuracy of ≈1% (Barber et al., 1983 & 1984). This group has developed a series of EIT systems (detailed description presented in chapter 3).

The successful Sheffield's EIT system encouraged researchers to further investigate different research areas in this vast field. Later a group in Gottingen developed a digital EIT system (named: GOE-MF-2) which was based on the Sheffield initial prototype system. It was used to monitor lung function by EIT experimental validation for physiological studies in clinical and volunteers research. Later in 2001 a project was started between the Gottingen research group and Drager Company, to jointly improve the EIT system for experimental research as well as commercial usage in daily clinical practice (latest reported device is Pulmo Vista 500) (Teschner et al., 2015).

3D imaging plays an important role in EIT research. 2D images usually take measurements in a single plane while the object under observation and corresponding internal electric fields are in a 3D volume. As a result, 2D measurement will likely be affected with errors. The first attempt to produce 3D conductivity images was done in 1990 using 64-electrodes on four planes for in-vitro measurements (Goble and Isaacson, 1990). Another 3D EIT in-vitro image was reported with a comparison of simulated and real images of conductivity changes in a saline phantom (Metherall et al., 1996). The RPI (Rensselaer Polytechnic Institute) further researched the developed 3D-EIT imaging algorithms to determine the conductivity distribution under a medium by acquiring the surface voltages data on a rectangular electrode array (Mueller et al., 1999). The algorithm was based on conductivity linearization on a constant value, implemented on a 4x4 electrode array with reconstruction obtained using numerical and experimental tank

data. (Mueller et al., 2001). Another research group from Moscow published in-vivo images for breast tissue (Cherepenin et al., 2001). Later McMaster University developed a 3D-EIT system in the frequency range of 0.1–125kHz, it was validated using a Cardiff-Cole phantom and saline filled tank. A 3D image reconstruction using time/frequency difference imaging was presented with a signal-to-noise ratio (SNR) of >60dB for most of the frequencies (Goharian et al., 2008). Due to thriving and emerging research in the field of EIT, few researchers have developed a freely available software toolbox kit (EIDORS) for 3D-EIT imaging (Loinheart, 2004; Polydorides and Loinheart, 2002).

Difference imaging (or Dynamic imaging) uses the difference of two measurement sets by eliminating the common errors in both data sets. Time-difference based EIT imaging methods have been applied in clinical studies to observe body functions in many applications: lung ventilation, cardiac cycle, brain neural depolarization and epileptic foci and gastric clearing (Holder and Tidswell, 2005; Mueller et al., 2001; Mangnall et al., 1987; Eyuboglu et al., 1989). The EIT imaging method can be considered as a diagnostic tool in clinical research with an ability to acquire a static image. Static imaging was difficult because of the fact that it required accurate modelling of the object under observation and significant sensitivity to error/noises. EIT hardware design improvements reduced the system error along with the accuracy of modelling, which resulted in the first successful static imaging implementation by choosing an optimum current pattern from the boundary of the object (Isaacson, 1986).

In early EIT systems, the excitation signals were applied at a single frequency to acquire static/difference imaging. The electrical properties of tissue contain resistive and reactive components due to the presence of cell membrane, which presents a frequency dependent response. Therefore, the researchers proposed a multi-frequency EIT (MF-EIT) system, which involved tissue differentiation, based on their impedance spectrum characteristics. The pioneering work for MF-EIT imaging was published with an intention to reduce the problems that occurred for in-vivo static imaging (Griffiths and Zhang, 1989). The in-vivo and in-vitro conductivity images were acquired at multiple frequencies (i.e. 40.96kHz and 81.92kHz) using a 16-electrode system. Another group published multi-frequency in-vitro images at dual frequencies of 31.25kHz and 250kHz (Jossinet and Trillaud, 1991).

Since then several MF-EIT systems have been reported in the literature. A MF-EIT system, capable of real and imaginary impedance measurement at 30 frequencies between 2kHz and 1.6MHz was reported for thorax imaging (Wilson et al., 2001). A MF-EIT system was reported which acquired images between 225Hz and 77kHz frequencies for brain imaging (Yerworth et al., 2002). A MF-EIT system was reported for breast imaging with a frequency range of 10kHz and 10MHz (Halter et al., 2004; Hartov et al., 2001). Another MF-EIT system for breast monitoring working in the frequency range of 1-100kHz was reported with successful reconstruction using experimental data for a tumour like phantom (Ye et al., 2006). An acute stroke imaging MF-EIT system operating in the frequency range of 20Hz to 1.3MHz (Packham et al., 2012; McEwan et al., 2006) and a frequency range of 1-190kHz (Shi et al., 2008) was also reported. A Korean group has focused significantly on MF-EIT system and has developed few systems, which operated in the frequency range of 10 Hz to 500kHz (Oh et al., 2011; Oh et al., 2007). This imaging technique is significantly sensitive in modelling errors along with poor SNR. This imaging method is in the early stages of development as compared to a time-difference EIT imaging system. This imaging method requires substantial improvement to noise and model's uncertainty for clinical usage. The detailed description of the prominent EIT systems are given in the chapter 3.

## 2.4 EIT Theory and System Components

### 2.4.1 EIT Principle and Mathematical Model

The EIT method is to image the electrical impedance distribution in an inhomogeneous medium by the application of external excitation signals across the medium and measure the resulting electric field on the surface of the medium. It is mostly based on a constant current source injection and measurement of subsequent differential voltage between neighbouring electrodes pairs. The process is repeated by applying different current distributions within the subject and a number of voltage measurements are acquired to form a data set, used to reconstruct a tomographic image. A repeated measurement process will result in a good spatial resolution reconstructed image. Figure 2.4 shows a simplified 16-electrodes model of an EIT system. The model injects a current $(I_{in})$ into opposite electrodes pairs and the resulting voltage distribution $(V_{out})$ is measured between each set of neighbouring electrodes. The current drive electrodes are switched to the next

adjacent electrode (opposite) and voltages at all electrodes are again measured. This is repeated until 256 data points of the differential voltage are acquired.

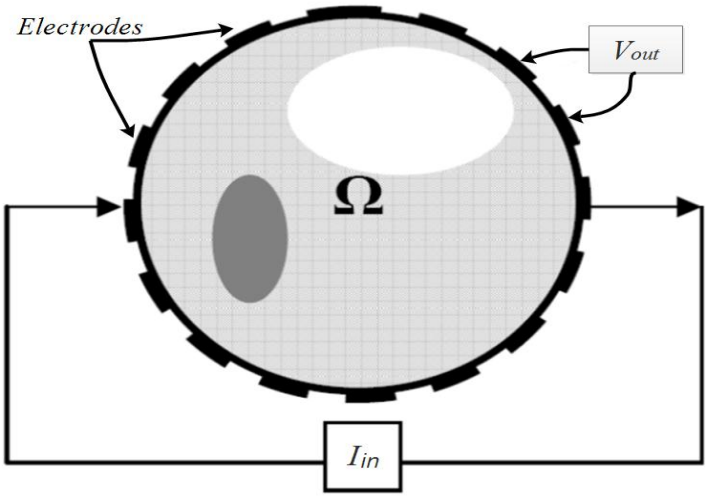



Figure 2.4: 16-Electrode EIT measurement diagram. Measurement of Voltage ($V_{out}$) after injecting the current ($I_{in}$) into the medium Ω (Molinari, 2003)

**<u>The Physical Model of EIT:</u>** The electromagnetic field within the body Ω is governed by the well-known Maxwell equations, which were studied in the context of EIT by Ackermann and Doerstling. In this process, two quantities (voltages and currents) are known for the region of interest. Evaluating the unknown quantity (resistivity/ impedance) within the interested region is the inverse problem for this measurement. The forward problem needs to be solved in order to solve the inverse problem. The simplified governing equation for EIT inside the body Ω derived from Maxwell equations is given as:

$$\nabla . \ (\sigma + i \, \omega \, \epsilon) \nabla \phi = 0 \qquad \text{Eq. (2.5)}$$

At low frequencies or direct current (DC) (i.e. ω ≈ 0), Eq. 2.5 reduces to the governing equation of Electrical Resistance tomography (ERT). This equation is mostly referred to as the governing equation for EIT along with its boundary conditions and are represented by Eq. 2.6 – 2.8:

$$\nabla . \ (\sigma \nabla \phi) = 0 \qquad \text{Eq. (2.6)}$$

$$\phi = \bar{\phi} \qquad \text{Eq. (2.7)}$$

$$\sigma \frac{\partial \phi}{\partial n} = J \qquad \text{Eq. (2.8)}$$

where $\sigma$, $\phi$, $\omega$ and $\epsilon$ represent the electrical impedance distribution, the electrical potential distribution, the frequency and the electric permittivity of the medium respectively. $J$ is the current density of the boundary region ($\partial X$) to be imaged.

The difficulty in solving this problem is due to the nonlinearity occurring in $\sigma$. This is due to the dependency of electrical potential on impedance (i.e. $\phi = \phi\ (\sigma)$). For an image reconstruction, the EIT technology solves two problems: forward and inverse problem. For a given conductivity distribution ($\sigma$) and boundary current density ($J$), the voltage and current density distribution are required, which is termed the forward problem. While alternatively, for a given voltage distribution ($\phi$) and current density distribution ($J$), the conductivity distribution ($\sigma$) is required and is referred to as the inverse problem. Therefore, it can be said that EIT image reconstruction is a process to solve the inverse problem also called a boundary value problem because of the fact that the voltage and current distributions along the boundary are known. The inverse problem is a non-linear ill-posed problem. Its solution involves transformation of the non-linear equation into linear equations followed by an iterative process solution based on numerical methods. To solve the inverse problem, first the forward problem needs to be solved. The forward problem is the process of establishing a linear mathematical model of the observed object using the finite-element method.

### 2.4.2 Hardware Components in EIT

The EIT hardware plays an important role in the image reconstruction of an object under observation. It is composed of four major modules: An electronics instrumentation unit, a computing system, electrodes array, and a phantom system/test object. The electronics instrumentation unit consists of excitation source system, data acquisition system and electrode switching system. A high quality precision design is required for the EIT electronic instrumentation. Poor spatial resolution affects the system performance, which depends upon on the independent available measured data from the boundary of the object to reconstruct the image. A possible solution for this problem is to increase the number of electrodes to acquire more boundary measurements for image reconstruction. However, this is not simple, due to the fact that object imaging surface area, larger number of electrodes, electrode complexity and large amount of acquired data will eventually turn the application into a complex problem which can't be handled easily. Different current

injection strategies and optimal voltage measurement schemes have been investigated in the literature (Molinari, 2003; Paulson et al., 1993; Hua et al., 1992).

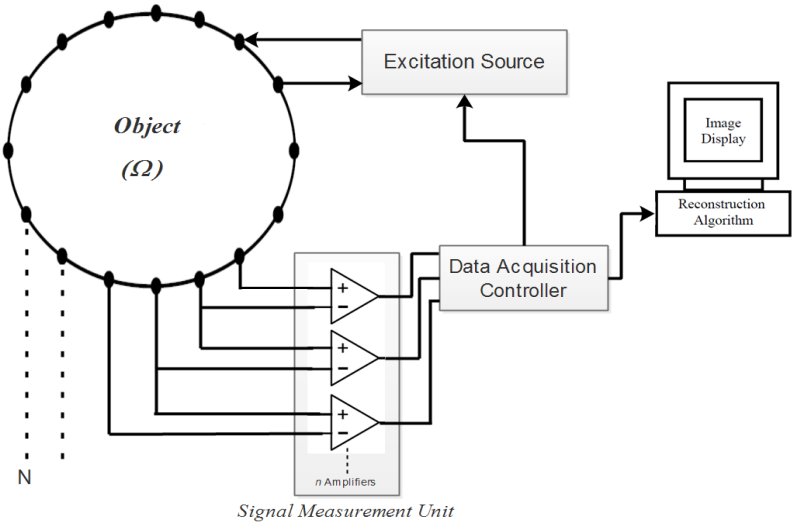



Figure 2.5: Block Diagram of a typical EIT system

### 2.4.2.1 EIT System Waveform Generator

To generate an input sinusoidal signal pulse for the excitation system, either an external function generator or on-board oscillator (analogue/digital) can be used. The modern EIT systems have shifted towards digitally generated waveforms with a benefit of high stability, low distortion, and better synchronization within the system. In a multi-frequency EIT system, the digital generators are very effective because its frequency can be changed easily during the measurement process.

The digital samples of the waveform, either from PROM (programmable read-only memory) or generated using DDS (direct digital synthesizer), are passed to a DAC (digital-to-analogue convertor) to produce an analogue waveform. The PROM stored the waveform sequentially in a look-up table while the DDS sinusoid generation is based on a NCO (Numerical controlled oscillator). The phase accumulator increments a phase step on each clock phase pulse. The sum of phase control word and phase register output will act as an address for the look-up table for a specific frequency sinewave. The amplitude information of a periodic sinewave is digitized and stored in a look-up table with each look-up table address corresponding to a phase point. The mapping of the address to the digitized amplitude assures the integrity of a periodic sinewave signal (Wu et al., 2009). The PROM method will have a restricted output frequency due to a certain length of the look-up table while in the DDS method a variable output frequency can be achieved by

changing the phase increment and clock frequency. However, due to the limited size of the ROM in field-programmable gate array (FPGA), phase truncation is needed to access the look-up table. This can be resolved by limiting the output frequency to those that corresponds to the address in ROM. A couple of digitally generated waveforms based on FPGA and digital signal processor (DSP) are reported in the literature (Halter et al., 2004; Liu et al., 2003; Lee et al., 2003; Wilson et al., 2001).

#### *2.4.2.2 EIT System Excitation Source*

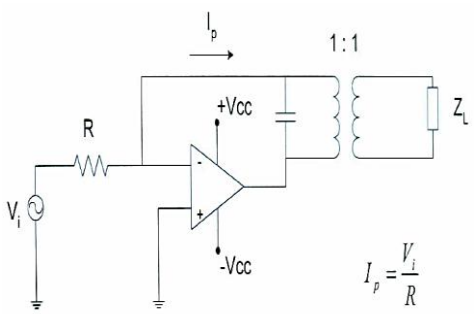
The Excitation source is considered to be a significant component in any EIT/bio-impedance system. The accuracy and reliability of the measured results significantly depends on the quality of the predefined frequency band excitation source. To achieve high resolution images, this excitation source should generate a stable and constant amplitude signal for a wide range of frequencies irrespective of the attached loads. The excitation source can be either current or voltage source (Qureshi et al., 2013). Most of the EIT system inject current into the object using two electrodes by maintaining a constant amplitude. The EIT system current injection strategy should be from any of the current driving strategies described in section 2.4.3.2. Irrespective of the excitation signal driving strategy, a voltage controlled current source (VCCS) is considered to be the backbone of an EIT hardware system. A few commonly used current sources in the EIT system are briefly described.

The first developed single source EIT system used an isolated negative feedback current source. The transformer provides DC isolation between the source and load, which limits the source performance and hence results in stray capacitance and limited trans-inductivity (Yang, 2006). Few EIT systems used the operational trans-conductance amplifier (OTA) circuit as a current source. It is a voltage-to-current converter circuitry, which produces output current as a function of the input voltage difference. It has the advantage of being simple and adjustment free but suffers from a low output impedance (Holder, 2005; Yerworth et al., 2002; Hartov et al., 2000). Current mirror with an ability to provide current sensing has also been used as current source. This source acts as an impedance multiplier, and the output impedance of the source is approximated as the impedance at the input is multiplied by the open loop gain of the op-amp. Limited open loop gain at high frequencies degrades the current source performance (Denyer et al., 1994). Bragos et al., 1994 also reported a current source based on current mirror.

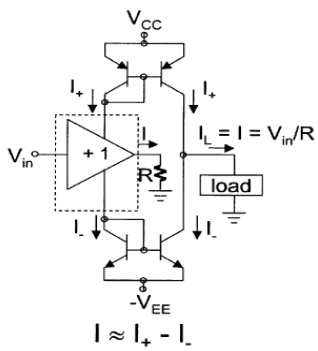
A three op-amps based current source is also used in EIT systems. An inverting-summing voltage amplifier is used in the forward path of the current source while a current sensing resistor, non-inverting buffer and inverting amplifier is used in the feedback path. It gives a high output impedance with proper trimming. It introduces phase shift in the feedback path at high frequencies along with significant trimming of resistors.

The Howland circuit remains a popular choice as a current source in most of the EIT systems. The source topology is based on an inverting amplifier in the forward path and positive feedback. A precise feedback resistor trimming can lead this circuit to achieve a high output impedance. But practically mismatching in the resistors, stray capacitance and frequency limitation of the op-amp used results in limited output impedance. The Howland based current source is described in detail in chapter 4 and 5 along with its performance obtained for this research work. The frequency bandwidth of the current source is limited by the bandwidth of the op-amp used along with the physical connection of the system with electrodes.

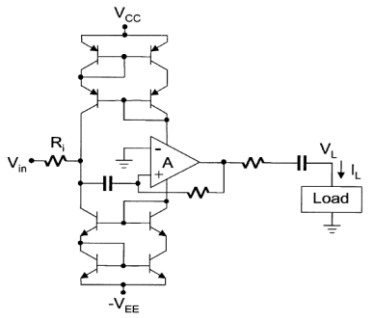
Alternatively, few EIT systems have used a voltage source as an excitation system. In the voltage source system, the requirement is to maintain a constant voltage across the load for a wide frequency bandwidth. However, by maintaining a constant amplitude of the voltage source, it is important to measure the resultant current applied to the object and should be under the electrical safety limits. The basic configuration used in a few EIT systems is a non-inverting op-amp configuration with a sense resistor in the feedback path to measure the current leaving the voltage source. The detailed requirements of the voltage source for an EIT system are described in the chapter 6 along with the performance parameters of a designed voltage source for this research work.



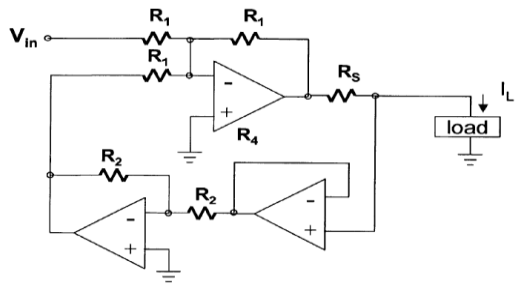

*(a)* Isolated negative feedback Current Source



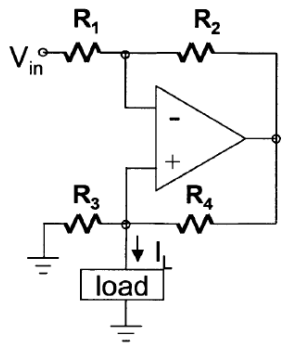

*(b)* OTA based Current Source



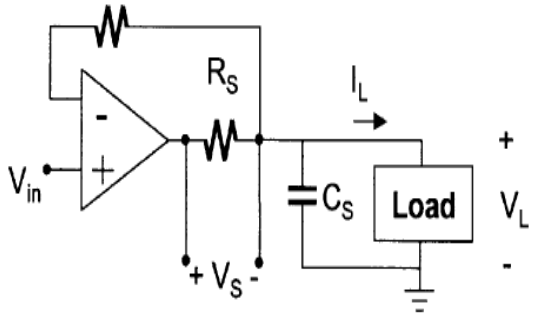

*(c)* Current-Mirror based Current Source




*(d)* Three-op amp based Current Source




*(e)* Howland Current Source




*(f)* Voltage Source with current measurement

Figure 2.6: Current and voltage sources reported in the literature for EIT (a–e), and (f) (Holder, 2005).

### *2.4.2.3 EIT Data Acquisition System (DAS)*

The DAS is another important component of the EIT system. The overall efficiency of the system depends on how fast the DAS can propagate the electrical signals between the system components. The DAS generally consists of three sub-components: electrode switching module, voltage measurement module, voltage signal demodulation, and synchronization device for communication between these components. The control device can be a microcontroller, a FPGA, a DSP or a combination of any of these devices. An overview of these components is provided in this section.

**Switching Module:** The excitation source of the EIT system generates a stable signal, which is propagated to a specific electrodes pair and the resulting boundary voltage is acquired using this switching module. This switching module can be either automatic in a predefined pattern or can be controlled manually using an interface software from the PC. It is composed of an analogue multiplexer controlled by the dedicated signals. The early EIT hardware systems used a single multiplexed excitation source and voltage measurement circuit, for each electrode using a digitally controlled multiplexer (MUX) and resulted in a sequential measurement system. Alternatively, a parallel measurement system can be considered which uses separate excitation/measurement circuit for each

electrode. It is not suitable for a high quantity electrode system due to increase in size and cost of the device. Therefore, realistically a semi parallel system can satisfy the high speed imaging demand. The signal transmission involved in both measurement systems will suffer from the associated stray capacitance that act as a low pass filter for these signals. Hence, this degrade the system performance and show difficulty at high frequencies i.e. (>2-3MHz).

**Signal Measurement Module:** After the excitation signal propagation, the next stage is of voltage signal measurement. A high input impedance and common-mode rejection ratio (CMMR) instrumentation amplifier (IA) is required for boundary voltage measurement that can potentially eliminate the contact impedance effect and common mode voltage introduced into the system. Practically the IA experience limited input impedance and decrease in CMRR with frequency increase (Saulnier, 2005). Limited input impedance of the IA can be compensated by using a voltage buffer in the preamplifier stage between measuring electrode and the IA (Naeini, 2008).

The early systems used an AC-coupled bootstrapped buffer before IA to avoid the measurement channel saturation by electrode-skin interface voltage and prevent op-amp bias current circulation in measurement electrodes. A typical IA used in this field consists of 2-stage three op-amp topology. This topology can be used with a wide bandwidth op-amp to achieve high CMMR and differential gain of an IA. Addition of a RC (resistor-capacitor) circuit will help to adjust the CMMR at low and high frequency by compensating the transfer functions imbalance in the differential branches (Yang, 2006; Pallas-Arney and Webster, 1993).

Few circuit topologies used as an IA in the literature are described. Transformer-coupled IA is classical three op-amp IA in which one op-amp is replaced by a transformer. This IA has a high CMMR (≈95dB) at low frequency (3.6kHz) which is limited by the usage of a transformer (Boone and Holder, 1996). Current-mode IA is another circuit topology, which performs like a non-inverting input differential amplifier, if the current mirrors and the first op-amp is considered to be ideal. The op-amps and current mirrors limits the circuit performance. A maximum of 80dB and 73dB SNR was reported at 10kHz and 50kHz respectively by replacing the current mirror transistor with op-amps (Zhu et al., 1992).

The CMMR performance of the IA is affected at higher frequency due to the common-mode voltage and was explored to resolve by common-mode voltage feedback. This was noticed with the commercially available integrated IA's, which are capable of achieving high CMMR at low frequencies. To compensate the problem, an inverting configured amplifier with its input attached to that electrode which is connected to the object and its output connected to another electrode attached to an object (Saulnier, 2005). This approach can only reduce the common-mode signals that affect all channels. A stable compensation circuit is difficult to achieve for a multi-frequency system; therefore, this method is not commonly referred in the literature. An imbalance in the driving impedances of IA degraded its performance even in the presence of common-mode compensation methods. This imbalance can be due to stray capacitance in the PCB board (Boone and Holder, 1996).

**Signal Demodulation:** The demodulation of the measured voltage signal is required to evaluate the conductivity and permittivity of the tissue. A high quality and precise extraction of the original signal from a modulated carrier signal will result in an accurate reconstructed image. It is a powerful technique and is used in the EIT system to extract the amplitude and phase of the electrode voltages in the presence of Gaussian noise or other interferences (Smith et al., 1992). This can be achieved by two methods: amplitude or phase-sensitive demodulation (PSD). The amplitude demodulation is mostly applied to the low frequency imaging system in which signal phase is not important due to tissues resistive characteristics. The drawback of this method is the rectification of the signal frequency noise present at other frequencies, which results in measurement errors (Nowicki, 1990).

Alternatively, PSD can be used which gives better performance in terms of SNR and minimal errors. Its principle is to shift the measured signal down to a low frequency by multiplying it with a synchronized reference signal with respect to the applied signal and filtering the generated high frequency harmonic. The PSD implementation follows two approaches: a coherent synchronous demodulator, which comprised of a four-quadrant linear multiplier OR a phase-sensitive synchronous detector comprised of an amplifier with gain between ±1 with respect to the reference signal. Both methods followed a low-pass filter (LPF). Being popular in analogue demodulation, it exhibits a drawback of transferring the odd harmonic components of the fundamental signal to the output, which leads to errors (Murphy and Rolfe, 1988).

This can be resolved by a band-pass filtering of the input before demodulation. The LPF extracts the DC component and eliminates the high-frequency harmonics. Narrow LPF bandwidth will result in a good SNR with a compromise of longer settling time (Nowicki, 1990). The settling time can be reduced by using an integrator instead of a filter. The output signal (used for acquiring real and imaginary part of impedance) is a DC voltage and will introduce error with any offset. The system design should ensure that the offset should remain within adequate limits.

Due to the technology enhancement and some limitation of analogue PSD, this technique has shifted towards digital implementation of PSD used in single and multi-frequency EIT systems. The digital PSD technique exhibits significantly less noise component and is not DC offset sensitive due to the presence of a lookup table stored in the internal memory of a DSP/FPGA device used as a reference signal. An anti-aliasing filter is used prior to the input of ADC (Analogue-to-digital converter). The digitized samples of the measured electrode voltages are multiplied by sine and cosine reference signal with the same frequency. The products are gathered over an integral number of input signal cycles to block double frequency components in ADC sample output and reference signals waveform. Some of the digital PSD used in the EIT system are reported in this section.

Cook et al., 1994 implemented a matched filter using DSP and multi-period under-sampling technique to increase the SNR of voltage measurement. Hartov et al., 2000 implemented a software based PSD technique in which the amplitude and phase of measured voltages were acquired by implementing a similar multi-period under-sampling technique. Dudykevych et al., 2001 reported the magnitude and phase of the load impedance using a correlation technique between excited and measured signal. Wilson et al., 2001 reported a system based on FFT algorithm to demodulate measured signals at 30 frequencies sequentially in different groups of ten. Oh et al., 2003 implemented a FPGA based PSD to measure in-phase and quadrature components using an under-sampling technique to achieve 16-bits precision. Liu et al., 2003 implemented a digital PSD using a complex matched filter on FPGA to obtain real and quadrature components of measured voltage. The 14-bit ADC of the system used the same multi-period under-sampling technique to achieve 19-bits precision for voltage measurement. Halter et al., 2004 implemented digital PSD for each channel using a DSP and FPGA. Two ADC's are used to obtain the amplitude and phase of the measured signals from its in-phase and quadrature samples. Yue and McLeod, 2008 implemented system demodulation using

convolution of the measured and excitation signal and its quadrature in FPGA using two concurrent multiplier-accumulators. The system acquired parallel measurements and used a single ADC for signal digitization.

A high-speed processing and data acquisition system is required by EIT system. The conventional data acquisition system implements separate hardware units for DAS. A recent development in the EIT system is the use of a data-acquisition card, which minimises the use of the separate hardware units and is capable of collecting data at a high sampling rate. The National Instruments (NI) cards are a popular choice for this application controlled with LabVIEW software during the measurement process.

#### *2.4.2.4 EIT Phantom System*

The phantom is a rectangular/cylindrical box filled with materials of homogenous resistivity or with a collection of dissimilar materials of different resistivity. It provides a controllable medium that can be used for the impedance system calibration and testing. The EIT system needs to be tested and precisely calibrated to ensure that it is safe, reliable and efficient before applying to patients. Experimental phantoms with electrodes attached at the surface, are used to test the performance of the system in terms of validation and calibration. It can be a tank or electronic phantom. The tank phantom consists of a liquid or a solid conductive medium that can be imaged by the EIT system using boundary electrodes. The conductive medium usually consists of a conductive gel or saline solution and the inserted object conductivity contrasts with the medium. Alternatively, electronic phantoms are made up of impedance components connected in a particular topology (Zarafshani et al., 2016b). These impedance components can be resistors, combination of resistors and capacitors, or active electronic components. Some popular component topologies reported in the literature are: the Cardiff phantom, the wheel phantom and two Gottingen phantoms. Tank phantoms provides more realistic signals while electronic phantoms can provide predictable, stable and reproducible signals. Due to the reproducibility characteristic, the electronic phantoms are preferred to assess the performance of the EIT systems (Zarafshani et al., 2016a).

### 2.4.3 Image Reconstruction in EIT

Image reconstruction is another key component in the EIT technique. This includes the knowledge of boundary measurements along with object boundary shape, position of

electrodes and the injected current to reconstruct the impedance distribution of the imaged object. The scope of this thesis is generally related to the hardware enhancement in the EIT system but it will be useful to briefly describe the involved imaging terminologies. Therefore, this section will give a general overview of the different aspects involved in image reconstruction like current driven pattern, reconstruction algorithm and finite element method.

#### *2.4.3.1 Current Drive Pattern in EIT*

The image resolution is determined by the distribution of electrodes and the measurement strategy. The current drive pattern defines the procedure of current injection into the object being imaged and determines the measurement boundary condition. Generally, it is categorized into two types: either current injection using one pair of electrodes, or using many/all electrodes at the same time. The main current drive patterns are briefly described:

- ***Neighbouring/Adjacent Pattern****:* In this pattern, the current is injected through adjacent electrodes and the voltage is measured sequentially on all other electrodes. This pattern is least sensitive in the centre as compared to other patterns but it is best at proportional selectivity and shows a high sensitivity distribution with four electrodes measurement. It was initially used with back-projection reconstructions and corresponds to the presence of pseudo-dipoles along the boundary (Barber & Brown, 1984).
- ***Opposite/Polar drive Pattern****:* In this pattern, the current is injected through electrodes on opposite sides of the object surface apart with 180º and the voltage is measured on all remaining electrodes. This method gives a uniform current density in the centre of the object and results in an increased sensitivity at the centre of the region.
- ***Cross/Diagonal drive Pattern:*** In this pattern, adjacent electrodes *(x & x+1)* are selected as current and voltage reference. The current is injected to the next alternative electrode *(x+2)* with respect to the reference current electrode. The voltage is measured on all electrodes *(x+3 to x+n)* with respect to the reference voltage electrode *(x+1)*. Now the current injection is shifted to the next alternative electrode *(x+4)* and voltages are measured on all electrodes and so on. This process continues until a complete set of measurements is taken with

respect to one voltage reference electrode *(x+1).* The same process is repeated for the next adjacent current and voltage reference electrodes. A uniform current distribution can be obtained when current is injected between a distant electrodes pair. This method doesn't have as good a sensitivity in the boundary region as the adjacent method but it has better sensitivity over the entire region.

- ***Optimal pattern:*** A current of adapted amplitude is injected through all electrodes simultaneously which leads to increased sensitivity for conductivity changes. Optimal current patterns were derived by adapting the reconstruction algorithm used to minimize the difference between measured potential values and those predicted by the model (Hua et al., 1991).
- ***Adaptive/Trigonometric Pattern:*** The current is injected through all electrodes and requires many independent current sources. Homogenous current distribution can be obtained in a homogenous volume conductor. If the volume is cylindrical with cross-section, the injected current must be proportional to $\cos\theta$ for a homogenous current distribution. Adaptive current patterns were used where an amplitude of injected current $(I_o)$ varies with an angular position $(\theta_l)$ of the electrode on a cylindrical surface boundary as: $I_l = I_o \cos(\theta_l)$. In this method, voltages are measured with respect to a single grounded electrode. The advantage of this method is its evenly distributed current density and increased sensitivity in the centre of the object being imaged.

### *2.4.3.2 Finite Element Method in EIT*

The forward problem needs to be solved for the conductivity images reconstruction. For an arbitrary resistivity distribution, it is difficult to solve the forward problem analytically. Therefore, a numerical technique is used such as the Finite Element Method (FEM) or Finite Difference Method (FDM). The FEM is suitable in most of EIT algorithms, due to the ability of modelling for the arbitrary shaped boundaries and piecewise approximation to the governing equation. In FEM, the observed region is discretised into a finite-element mesh, which is achieved by initial division of the whole region into one or more sub-regions called macro domains. Each macro domain is further divided into triangular elements to form a finite-element mesh. Two triangular elements connected via diagonally opposite corners nodes, form a quadrilateral element. The triangular elements are generally preferred over different shaped elements because of its ability to

approximate an equilateral shape. The solution is approximated within each triangular element by a fixed order polynomial. The FEM forward model contains the segmentation of the whole region/mesh and the conductivity value of each triangular element. The potential function $(u)$ value on each node is calculated by solving a system of N equations (where N is the number of nodes). The final solution $u(x)$ is searched in the N-dimensional discrete sub-space of the $H^1$ Sobolev space by interpolating the calculated values on each node according to the polynomial basis of elements (Malone, 2015). A typical 2D circular finite-element mesh is shown in Figure 2.7 with uniform conductivity distribution.

The accuracy of the FEM is dependent on the number of elements and order of the base function used in computation. An increase in the number of elements and order, will result in massive additional computing requirement. The FEM is also suitable for modelling 3D meshes and will be helpful in accurate simulation of real current field distribution of internal human bodies, which actually exhibits a 3D distribution. The FDM numerical solution employs a regular rectangular mesh and has been used for simple geometrical shapes.

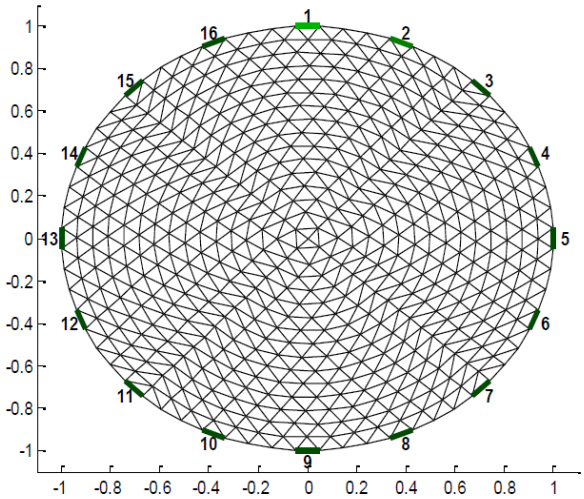



Figure 2.7: Typical 2D mesh for FEM with 16-electrodes.

### *2.4.3.3 Reconstruction Algorithms in EIT*

This is another key component in the EIT system. Its purpose is to reconstruct the conductivity/permittivity distribution within the observed region with the knowledge of boundary voltage and current density distributions. In an EIT system, different types of image reconstruction can be implemented based on the imaging configuration and type

of data collection. EIT image reconstruction algorithms can be broadly classified into two categories: Difference/Dynamic imaging algorithms and Static imaging algorithms.

The difference imaging algorithms reconstruct the impedance change between background and foreground based on linear approximations. In this algorithm, it is assumed that the foreground conductivity doesn't significantly differ from the background conductivity. The input of this algorithm is the measurement difference between the background and foreground. The output of the algorithm is the impedance difference between the foreground and background. The back-projection algorithm is an example of this imaging algorithm and was introduced by the Sheffield EIT group. It is based on an assumption of a linear relationship between a small change in impedance and small change in boundary measurements (Barber et al., 1983). The forward linear relationship is represented in a sensitivity matrix. Based on this linearization, Barber and Brown back-projects the boundary measurements along the equipotential lines as an inversion of sensitivity matrix to reconstruct the impedance image. It uses the pre-calculated equipotential lines in a homogenous medium and is popular in the EIT technique implementation due to its insensitivity to systematic errors and noise in the measurements. Its rapid processing time make it ideal for real time clinical diagnosis applications.

The static imaging algorithms reconstruct the absolute value of the impedance distribution. An initial impedance distribution is assumed followed by the corresponding boundary voltages calculations. Later the assumed impedance distribution is modified for a minimal difference between the calculated boundary voltages and the measured boundary voltages. The process is repeated until an acceptable solution is produced. The Newton-Raphson based (also known as nonlinear least square estimation) algorithm is its example (Bayford, 2006). It is a numerical method to solve the inverse problem by iterative linearization of the nonlinear relationship between resistivity and electrical measurement. It involves a longer running time and greater computing complexity. In this algorithm, the resistivity/conductivity distribution of the imaged object is modelled using a FEM. FEM is a basis for transformation of the partial difference equation electric field into a linear algebraic equation and the voltage distribution on the nodes of mesh can be solved. The forward problem solution in this algorithm is: For different resistivity/conductivity settings, the FEM model calculates the boundary voltage distribution on the imaged object and can be used as the reference measurement. The

difference between the reference measurements and the actual measured surface voltage reflects that the conductivity is not matched with the real internal conductivity. The Newton-Raphson algorithm iteratively modifies the FEM conductivity distribution for comparison between calculated voltage and measured voltage until their error is in an acceptable range. The final modified conductivity distribution matrix is displayed as a reconstructed EIT image. The algorithm was further modified to improve the matrix conditioning by using Marquardt regularization and claimed to have a more stable computation and better convergence (Yorkey et al., 1987). This algorithm gives an absolute value of internal conductivity distribution and requires a high quality boundary voltage measurement.

## 2.5 Key Progress and Challenges in EIT

### 2.5.1 Advantages

The EIT technology has many benefits over other medical imaging technologies and has been successfully applied to many parts of the body. Some of its significant advantages are described in this section.

- EIT is the functional imaging technique, which can image the electrical properties of the body tissues and can show physiological and pathological information. Each body tissue exhibits different electrical properties. Under different physiological conditions, sometimes the same tissue shows different electrical properties (Foster and Schwan, 1989). It has the potential to differentiate between normal and cancerous tissue.
- EIT is relatively inexpensive when compared to other medical imaging technologies. The electronics instrumentation involved in EIT is not too complicated and expensive (Either electrode or coils for current injection). The controlling software for EIT can be installed on a standard PC. The compatibility of this device to be built or fixed on an existing equipment results in a minimal cost as compared to MRI or CT x-rays machine.
- EIT is a non-invasive technique as compared to other cancer detection techniques. No physical instrument penetrates into the patient's body; rather the electrodes are only placed on the surface of body. It has no ionising radiation and can be used

for long-term monitoring at the bedside. It uses small amplitude excitation signal, which is safe for both patient and operator.

- EIT system has a big benefit due to its portability. It can be built on a small housing structure which will make it possible to move anywhere as per requirement. Due to its portability, this device doesn't necessarily need any special room for operation and is helpful for patients as well as operators.
- EIT image scanning is usually fast. The speed of reconstruction generally depends on the complexity of the required image. Due to fast acquisition system and significant improvement in the image reconstruction over recent years, it has been possible to acquire ≈10-25 frame/sec. 3D imaging is continuously being improved with an intention to further reduce the imaging time to <10mins.
- EIT can be helpful in early detection of cancer. Any change in tissue properties will show its respective affect at the output. Improvement in the EIT reconstruction and analysis system, will make it possible to detect cancer at an earlier stage as compared to other techniques, which require a certain tumour growth level for detection.
- EIT combined with other medical imaging techniques has potential to provide an increased diagnosis accuracy. For example, x-ray mammography can detect a breast tumour that has a density that significantly differs from the normal breast tissue. EIT can be used to detect a tumour, which is undetectable by x-ray mammography because it is based on contrast in electrical properties.
- EIT technology uses digital storage during the measurement process. This makes it easy for results comparison and future testing. Images are reconstructed from raw data and this data can be reconstructed with the development of imaging algorithms for better diagnosis.
- EIT can be applied for cellular identification and has no effect due to cell density. Younger people have denser tissue and can be tested using EIT reliably like adults (particularly for breast tissues). Other techniques show difficulty in identifying tumours in denser tissue. Excessive exposure to x-ray based technologies is considered a health risk at young age. However, EIT provides this opportunity without putting the patient at risk.

- EIT can be used in broad clinical applications. The electrical properties of human tissue changes with frequency that correspond to a specific impedance spectra. These spectra can be used as a characteristic standard to identify different tissues.

Therefore, based on these advantages, EIT imaging technique can play a significant role in medical diagnosis. This method is capable to give more advantages by exploring new ways to improve hardware and reconstruction software. Although it can be applied to many parts of the body, but its application to breast imaging is considered to be more promising due to its deformation to a regular shape which facilitates easy measurement.

### 2.5.2 Limitations

However, EIT technology has many advantages in medical imaging, but it suffers from some limitations as well. The diagnostic capability of EIT systems is mainly limited by the system performance, electrical artefacts and density of different tissues. These limitations need to be overcome before it can be significantly used for diagnosis and monitoring in hospitals. There are a number of areas, which need continuous research for the better performance of the EIT system. Some of its shortcomings are briefly described in this section.

- Low spatial resolution is one of the issues with EIT system. The low resolution issue of the reconstructed image is due to the limited number of electrode voltage measurements, electrode density, distance between object and electrodes, high impedance between electrodes to skin, noise interference and the mesh used in image reconstruction. Spatial resolution for a planar array is almost equal to the distance between adjacent electrodes and it reduces when the distance from the electrodes is increased. Mesh size also directly affects the spatial resolution. A fine mesh is helpful in improving the spatial resolution. However, a very fine mesh whose elements are much smaller than the size distinguished by the system will result in ill-conditioning. Some systems use small elements in the region near the electrodes and big elements in the region away from electrodes like ring electrodes in Mammography system. This will lead to a non-uniform spatial resolution and become worse in certain parts of the image. The low resolution problem also results in difficulty to identify any abnormal growth of tumour tissue.
- Detectability is system design dependent and determined by the number of electrodes, electrode arrangement, drive and measurement method and distance

between object and electrodes. Fewer electrodes corresponds to weak detectability and vice versa. The electrode geometry also affects the detectability. The ring electrode array is sensitive for tumour detection in the boundary of the observed region and is less sensitive towards the centre of the observed region. The detection of tumours is difficult when it is far away from the electrodes. Therefore, a relatively sensitive region close to the electrodes should be defined for the object. Simulation studies should be performed to analyse the electrode arrangement and the drive/measurement method.

- The EIT performance is also affected by the random system noise and ill-posed nature of the EIT inverse problem. Any small random change in measurements can lead to a large random change of the reconstructed impedance distribution. The electrode-skin contact impedance also introduces noise to the measurements. The physical contact of the electrode and skin result in a variable impedance and has effect on the measured results. The involvement of this contact impedance in the output can possibly decrease the image resolution. A preliminary study shows that wet electrodes can be a possible solution to reduce the contact impedance problem (Wang et al., 2006).
- The EIT system has to apply small amplitude signals due to safety requirements. Due to the small amplitude excitation signals, any internal or external noise can have a large effect on the system. Depending upon the application, some systems may need to be placed in an electrically isolated environment to avoid any electrical field interference produced by nearby equipment.
- The accuracy of the reconstructed image for an EIT system generally depends on the hardware and reconstruction algorithm. However, precisely it is limited due to the non-local characteristics of the impedance imaging technology. When the current is injected into an object, it spreads out when it enters into a conductive medium. A change in conductivity inside the target object will have an effect on its surface measurements. Hence, the reconstructed image of the object is not located at the same position and nor is its exact real shape. It has extensions and projections in its reconstructed image. This limits the accuracy of the reconstructed image but an efficient EIT system design and improved reconstruction algorithms can enhance the image accuracy facilitating distinguishability of tumorous tissue from the surrounding normal tissues.

### 2.5.3 Improvement opportunities

The EIT technique is still in the development phase. Several parts of the modern EIT system need to be improved before the system can be considered for full replacement of the existing imaging technology associated with a particular application. A brief description of some possible improvements are described here.

The electrode-skin contact impedance causes problems in the EIT measurement system. One way of improving this issue is to treat the skin directly before applying the electrode, but it will be uncomfortable for the patient. Another approach of applying the current can be through a contact-less method. Different EIT research groups are investigating this approach using magnetic induction of current, saline bath etc. This area gives an opportunity for new researchers to explore new mediums for making electrical contact.

The excitation signal of the EIT system has to be stable and steady over a large frequency bandwidth and should have high output impedance (in the case of current injection). Different research groups are trying to achieve high frequency response of ≥10MHz to acquire good quality EIT measurements specifically for breast tumour tissues. The impedance of the tissue being investigated, will possibly affect the output current of the source. Therefore, a high output impedance is required for the current source. Several different circuitries have been considered to achieve a good quality source and selection will depend upon the EIT system requirements. Hence, this area gives another opportunity for new researcher to explore new circuitry for EIT excitation system.

The signal measurement system of the EIT system should be able to collect measurements over a large frequency bandwidth with high precision and accuracy. This will help in extracting the Cole-Cole model parameters accurately from the measured signal. But due to the capacitance involved in the system and its response at higher frequencies, the measurement system performance drops when frequencies are ≥1MHz. Even a small input capacitance can have a significant effect on the system frequency bandwidth. Hence, an improvement opportunity is available for the measurement system.

The control system of the EIT should be able to synchronize effectively between the components of the EIT system. It has to control many functions from electrode switching to acquire raw measured data and it’s processing for image reconstruction. All these functions require a user-friendly interface for a non-technical user. This can be achieved

by the design and integration of high-speed acquisition systems. Therefore, this area also gives opportunity for researchers to explore new ways for fast data acquisition.

The image reconstruction algorithm can also be regularly improved. This can provide significant improvement in 3D imaging. The measured raw data can be improved to a certain level; therefore, the reconstruction method should have the ability to deal with the short-comings left in the raw data using advanced algorithm development for data analysis and image reconstruction so that it can be used as a diagnostic tool. This part of the EIT system can be rapidly improved due to availability of open source reconstruction software (EIDORS). This software is regularly updated with the latest advancement techniques from different EIT research groups around the world. This step gives an opportunity to researchers to see the latest improvements and can add their research work for further development.

## 2.6 Proposed Techniques

As stated earlier, the main scope of this thesis is to investigate the hardware performance of the EIT system; specifically, the excitation source which is an important component of the system. A stable and wide frequency bandwidth excitation source is required by the EIT system to achieve a high quality measurement from the electrodes; this will further help in the production of a high resolution reconstructed image.

The purpose of this research work is to replace the existing excitation source of the Sussex EIM system with a high frequency bandwidth excitation source. The latest prototype Sussex EIM system used an excitation source based on a current source. The current source (CS) was based on an Enhanced Howland (EH) circuit. Due to significant multiplexing of the excitation signal to the electrodes, the frequency bandwidth of the system was limited by the multiplexer capacitance. Hence the overall frequency bandwidth of the system was limited to <2MHz with a 100pF capacitance. Therefore, either a CS with significant high frequency bandwidth or a significant method to cancel the multiplexer capacitance was required for our Sussex EIM system.

For this research work, the EH circuit is further investigated using different wideband op-amps. The EH circuit is simulated with the selected high speed op-amp and its simulated performance is analysed for a wideband of frequencies. The EH circuit is further tested

with the involvement of multiplexer capacitance. A capacitance cancelation circuit is added in parallel with the EH circuit, to cancel the multiplexer capacitance. The detailed simulated performance of this parallel combination circuit is presented in chapter 4 & 5.

Most of the high speed op-amps have a low power supply voltage. The high power supply op-amp has relatively less frequency bandwidth when compared to the high speed op-amp. Hence, a low power supply voltage has resulted in a CS to drive an extremely small load due to the op-amp output saturation and loading voltage problem. Therefore, a bootstrapped circuit is introduced in the CS and capacitance cancelation circuit. The purpose of this bootstrapping is to achieve a high amplitude current source that is close enough to its external power supply voltage. The Guard amplifier technique based on discrete components is also introduced which is used to cancel the capacitance of the multiplexer. Due to inability of the EH circuit in achieving a significantly high frequency bandwidth, a separate discrete component current source is also designed specifically to achieve a high frequency (≥10MHz) current source excitation signal. The detailed simulated performance of these circuits is presented in chapter 5.

Another excitation source based on a voltage source (VS) is also designed in this research work. Due to the difficulty of achieving a high frequency bandwidth of the CS, few researchers proposed the voltage source as an excitation source for EIT. Hence, it is decided to investigate and design a VS for our Sussex EIM system. The VS design should be able to achieve a variable voltage gain and controllable feedback current. It will also sense the amount of injected current to the load. The VS circuit is bootstrapped to avoid the loading problem in the circuit and can deliver a high amplitude voltage signal. A high output voltage differential amplifier based on discrete components will also be designed to measure the voltage across the various parts of the voltage source and current source circuit. The detailed simulated performance of these circuits is presented in chapter 6.

An excitation source based on a combination of current and voltage can be achieved upon successful implementation of both the excitation sources. This combination will be implemented in the future development of this research project.

## 2.7 Summary

The chapter introduced the bio-impedance concept in the medical field. It introduced the basic principle behind the bio-impedance methodology along with its electrical equivalent model and mathematical model representation. The Cole-Cole mathematical model is briefly described. A brief application of the bio-impedance method in the medical industry is described.

The EIT technology is being introduced as an extension of the bio-impedance measurement method. This chapter described the general background of the EIT technology along with its applications in different fields of study. This chapter also presented the history of EIT along with some popular systems reported in the literature.

The chapter introduced the physical principle behind the EIT measurement system in terms of a mathematical model. The focus of this chapter was on the hardware architecture of the EIT system. The detailed hardware components description of the EIT system is presented along with popular hardware components reported in the literature.

The chapter briefly described the image reconstruction concept involved in EIT in terms of the inverse and forward problem. The FEM is briefly described to solve the forward problem along with different current drive strategies and reconstruction algorithms. The chapter also addresses the advantages, limitations and the areas of further improvement for the EIT technology.

Due the complex impedance property behaviour of tissue, the EIT hardware system needs to be designed for a wideband (≥1MHz) impedance measurement. Hence, this leads to a high demand of the high frequency constant current source and voltage measurement designs. Therefore, the chapter briefly introduced the method to achieve a stable and efficient excitation source.

Chapter 3 will present a broad literature review of the excitation source for the EIT system. The popular EIT systems will be presented based on two excitation systems categorization. The description of Sussex EIM will also be presented in the next chapter.

# Chapter 3

# Existing Methodologies in EIT System

## 3.1 Introduction

The EIT technique is one of the developing technologies for monitoring and analysis of tissue state and organ functions, which models the electrical properties of tissue in terms of its equivalent resistor and capacitor network (Silverio et al., 2012). It is a cheaper, smaller/portable, requires no ionising radiation and can produce many images per second as compared to other imaging techniques (Zanganeh, 2013; Zhao, 2011; Hong et al., 2007). It has been extensively developed in approximately the last 3 decades but there are some challenges, which still need to be further explored to make it a clinically applicable system (Bayford, 2006). It is still in the phase of improvement for better data acquisition hardware and image reconstruction algorithms. Many methods have been applied to improve the imaging quality. One of the most important factors is to further improve the acquisition hardware so that a high accuracy measured dataset can be obtained.

Different research groups related to EIT hardware design have focused on developing an efficient signal excitation and measurement subsystem for EIT / BI system. It is believed that the accuracy of the excitation subsystem can greatly influence the quality of the reconstructed images. The upgrading towards digital system, has resulted in advancement of the EIT system performance in term of frequency bandwidth and precision. Due to this digitization, the frequency of excitation signal has increased from 10-20kHz range to 1-10MHz range. The application of excitation signals over a frequency range will make it possible to perform impedance spectroscopy for various impedances over different frequencies. This has lead researchers to design systems, which can acquire measurements at multiple frequencies simultaneously. The literature available on medical EIT measurement systems is too extensive to be fully reviewed in this chapter. However,

the general method of an EIT measurement system is presented followed by a review of the popular existing EIT systems based on the excitation subsystem type. Finally, the description and performance parameter of the Sussex EIM system is presented.

## 3.2 EIT System Measurement Method

The response of any biological tissue to an excitation signal has been categorized into three dispersion ranges (Silverio et al., 2012; Schwan, 1994). The permittivity of materials is frequency dependant and referred to as dispersion. Permittivity is defined as the tendency of a material to be polarized by an electric field. Different frequency dispersions (based on relaxation mechanism) are called: alpha, beta and gamma with signal frequency ranges of 10Hz – 10kHz, >10kHz – 10MHz and >10MHz –1GHz respectively. The alternative concept of dispersion is known as relaxation (in time domain). Relaxation is a measure which represent how fast a material can be polarized (Grimnes et al., 2008). Mostly the alpha and beta dispersion frequency ranges have been applied in clinical testing.

In any typical EIT system, the sample under observation (SUO) is injected with a high frequency current with an amplitude in the range of µ-to-mA between two or more electrodes to generate a current pattern. The resulting boundary voltages of the SUO are measured at the other electrodes with a high CMMR and high input impedance instrumentation amplifier in a two/four electrode setup. In these BI-systems, mostly a voltage-to-current convertor is used to make a current source, which is driven by a voltage signal; hence forming a VCCS. The driving CS along with the detected bio-modulated voltages are used to obtain the impedance magnitude and phase of the SUO using demodulation/lock-in technique.

Alternatively, some of the EIT systems are based on voltage application and the resulting surface current is measured (Mohamadou et al., 2012; Qureshi et al., 2012d; Choi et al., 2003; Hartov et al., 2002 & 2000; Sansen et al., 1992; Zhu et al., 1993). The voltage source (VS) design requires a current sensing resistor. The VS-based EIT system forms a configuration of voltage division between the current sensing resistor and the external connected load. The current sensing resistor is varied to maintain the voltage division more or less equally, which is helpful to maintain a high SNR of the VS. The SNR is reduced at low impedance load due to the lower current requirement, which maintain a

constant voltage across the load. There are three common measurement methodologies in EIT, which are described in the following section (Naeini, 2008).

### 3.2.1 Applied Potential Tomography (APT)

When a sequential current using a pair of adjacent electrodes is applied to the SUO; this type of measurement configuration is termed the APT technique. Current is applied to the sample and the resulting voltages between adjacent non-current carrying electrodes are measured. A wide voltage measurement data set is obtained by repeating this procedure by injecting current between all other pairs of electrodes (Brown, 2003). In the APT method, one complete voltage measurement is considered as a reference dataset. Upon acquiring the next dataset of voltage measurements, both datasets of measurement are passed through the reconstruction algorithm, which back projects the weighted voltage difference between the two sets. It is considered a dynamic technique because it can measure the electrical characteristics with in the body. In this technique, the effect of skin-electrode impedance is minimised by avoiding the voltage measurement on the electrodes, which carries current (Cheng et al., 1990). The technique can be further improved by using opposite electrodes to inject current, which will result in improvement in the measurement sensitivity (McCann et al., 2006).

### 3.2.2 Applied Current Tomography (ACT)

The configuration in which a set of current patterns is simultaneously applied to all the electrodes and the subsequent voltages on each electrode are measured to generate a dataset for image reconstruction; this is termed an ACT technique. Each set of current patterns represents a specific value of the current for its corresponding electrode. Due to the large number of generated current patterns, the technique will result in complex hardware but it has an ability to generate static (i.e. absolute impedance) as well as dynamic images (Saulnier et al., 2001). In this technique, larger electrode voltages are produced for a change in impedance within the body, therefore it will result in better impedance distinguishability as compared to APT. As per the current safety regulation, the algebraic sum of all the applied current to the sample needs to be within the safety limit. This prevents the application of this technique to in-vivo measurement. Due to this fact, the difference between the ACT and APT performance is reduced (Brown, 2003).

### 3.2.3 Voltage Excitation

Practically, a very high output impedance is required by the CS, which is difficult to achieve due to non-linearities involved within the electrical circuit. Some of the EIT system prefer to use a voltage source (VS) as an excitation subsystem instead of a CS. A VS-based EIT system appears to be simple in electronics but it increases the sensitivity of electrode placement and size error within the system (Saulnier, 2005). Theoretically, a good VS tends to have a low output impedance as compared to a CS. Practically, an unknown contact impedance exists between the electrode and the SUO. This contact impedance is expected to be very low but still can affect the accuracy of the VS-based EIT system. A similar performance of input impedance of the data acquisition module is expected for voltage and current measurement methods. Theoretically, it is suggested that when an unknown variable contact impedance exists within the system then a voltage measurement technique can produce good results (Webster, 1990).

## 3.3 Consideration of EIT Excitation subsystem

The majority of the EIT systems use the topology of injecting current and measuring the resulting voltage. It can be classified as either a single or multiple excitation source subsystem. The intended applied signal can be generated digitally or through a function generator and is applied to a dual current source, which produces a pair of currents having equal magnitude but opposite phase. A 2xN multiplexer is used to multiplex the generated current signal for one electrode pair at a time. A shielded cable connection between the multiplexer and electrodes helps to protect the signal from noise and reduces the cable capacitance. Voltmeter (single-end/differential) is used to measure voltage across the electrodes. A multiplexed voltmeter will increase the time consumed to acquire a complete dataset for image reconstruction but it will reduce the hardware cost for the EIT system. This single source system can be associated to the APT-EIT system. In multiple excitation systems, each electrode will have a dedicated CS, which defines a current pattern for each electrode and the sum of all the current applied to the electrode must be equal to zero. The number of voltmeters are equal to the current sources involved in the system. Due to the larger number of system components, a compromise is needed to control costs. It can also be associated to the ACT-EIT system.

### 3.3.1 Excitation Signal Safety Limit

Many professionals are using medical equipment for monitoring, treatment and diagnosis. This raises the question of proper working equipment and safety when it is used by an untrained operator in an uncontrolled environment? Therefore, it is very important to consider the electrical safety policies.

For living tissue safety, a limited amount of current can be passed through the human body to avoid damage within the body. The International Electro-technical commission (IEC) has defined some safety limit for the maximum amount of current injected into the SUO in IEC 601-1 act. BS EN 60601-1 is the British alternative of the act (BSI British Standards, 2006) with the latest revision available in BS EN 60601-1-11:2015. This act describes the general requirements for basic safety and the essential performance requirements for medical devices.

The maximum amount of current amplitude that can be injected into the SUO is dependent on the signal frequency. A maximum of 10µA (equipment directly connected to heart) and 100µA (equipment not directly connected to heart) current can be injected for signal frequency range 0.1Hz to 1kHz (Borsic et al., 2009; Ghahary, 1990). For frequencies >1kHz, the maximum amount of injected current is calculated as: the product of current limit defined for <1kHz frequency and the required frequency (in kHz) up to maximum multiples of 100.

For example, the maximum amount of injected current at 10 kHz (equipment not directly connected to heart) can be calculated as 100µA x 10 (kHz frequency) = 1mA. Following this rule, for frequencies between 1-100kHz, injected current should be in the range of 100µA to 10mA. For frequencies >100 kHz, a maximum of 10mA can be injected.

The Medicines and Healthcare products regulatory agency is proposed to check the risk analysis of the medical equipment to be used in clinical trials. This analysis is also a requirement of 60601 act and CB scheme & CE mark (Beqo, 2012). General risk hazards applicable to any medical equipment are related to energy, functional failure, operational, environmental, biological, incorrect output of energy or substances and misuse of the user interface. Hence, all the medical equipment should fulfil the standards act set by the IEC.

### 3.3.2 Multi-Frequency Measurement EIT System

Multi-frequency data acquisition is considered to be important in the recent research of medical EIT systems. Multi-frequency data collection tends to increase the complexity of the system but alternatively it has improved the image quality, and better information related to the SUO can be obtained. However, there are several issues, which makes these system designs quite demanding. The electrode impedance is very high at low frequencies and result in difficulty to inject a constant current (Brown, 2003). The electrode used in medical equipment has non-linear I-V characteristics with a frequency dependent resistance and capacitance. The electrodes properties are variable even if they are connected to the same object. This effect is greatly observed for low frequency signals (Naeini, 2008; Boone & Holder, 1996). The temporal resolution degrades at low frequencies and IEC 601-1 act is compromised at frequency <1kHz (Boone et al., 1997; Webster, 1990). Alternatively, at high frequencies, the unwanted capacitance associated with input leads and internal circuitry can introduce errors in the acquired data. Therefore, a stable excitation source is required for a multi-frequency EIT system, which can cover a wide frequency range for a large range of load impedance.

### 3.3.3 Current Source Benefit and Limitations

The CS is an important module of an EIT/bio-impedance system. Its features are critical for overall performance of the system especially in the intended frequency and tested load range. A current driven system is the most popular approach in the bio-impedance system as it applies an essentially safe current-limiting mechanism and reduces possible nonlinearities and normally referred as a VCCS. Mostly the CS used in the EIT system is voltage-to-current converter (V-I) and its functional purpose is to generate an electric current signal with a constant magnitude that is proportional to an input voltage. To achieve safe current driven biomedical equipment, the accumulation of electrical charges should be avoided as much as possible by making the DC component of the stimulating current equal to zero. Ideally, the CS will provide a constant amplitude irrespective to the attached load and frequency. This means that the output impedance of the CS must be very large (i.e. $\infty$) at all frequencies. The performance parameter “output impedance” referred to in this thesis relates to the overall current source circuit performance. It should not be confused with the op-amp’s output impedance parameter; whose characteristic is opposite to the CS circuit (i.e. ideal op-amp has 0Ω output impedance).

In reality, the performance of the CS is limited because its output impedance shunts away the generated current from the attached load. As a result, the relationship between the applied load current and the generated source current varies with the load impedance. The output impedance of the CS has a real as well as an imaginary part. It is defined as a parallel combination of output resistance and capacitance, which leads to a reduction in the output impedance with the increase in frequencies for a multi-frequency EIT system. A constant output impedance of CS has been reported in the literature up to a frequency of 100kHz (Cheng et al., 2006; Bertemes-Filho et al., 2000).

To minimise the capacitive component of the output impedance at higher frequencies, various methods have been reported in the literature (Qureshi et al., 2010; Ross et al., 2003; Bragos et al., 1994). These methods have increased the design complexity along with retuning of the compensation circuit with frequency change, and therefore can't be applied to any multi-frequency system but can be limited to a single frequency system. The skin-electrode contact impedance will also effect the performance of the CS and results in a significant effect on image quality (Boone & Holder, 1996). The change in output current amplitude with frequency is made worse by the involvement of additional stray/parasitic capacitance (Saulnier, 2005). The difference in the generated current and load current not only cause an error in image reconstruction but also leads to error in calibration (Cook et al., 1994). Therefore, the output current (injected) amplitude is considered to be the most important characteristic of a CS design.

VCCS are mostly preferred in EIT system due to the ability to control current injection into a variable load impedance. Many current sources have been reported in the literature for EIT systems with different circuit topologies (Cheng et al., 2006; Saulnier, 2005; Ross et al., 2003; Li et al., 1994; Bragos et al., 1994; Cook et al., 1994; Murphy et al., 1987). The Howland based CS remains a popular choice because it is constructed using a single op-amp and few resistors. Past studies show that the Howland circuit has a better performance as compared to other current sources (Tucker et al., 2013). The Howland circuit topology is a unique circuit because of its positive and negative feedback paths. The balanced feedback path will result in a linear performance of the Howland circuit modelled as VCCS. The detailed analysis and performance of the Howland circuit is described in Chapter 4 & 5.

The effect of output and parasitic capacitance will make the CS performance worse and should be minimised. The widely used method for capacitance cancelation is a negative impedance converter (NIC) with several different topologies for its implementation. A well-known NIC topology used in the EIT system is GIC that synthesized an inductance between two points. In principle, the NIC circuit is connected in parallel with the output of the CS to obtain an output impedance that only contains a resistive part, by eliminating any capacitance associated with the circuit at a specific frequency. As a result, the output impedance will be only real and extremely large (GΩ) as claimed by Ross, 2003. The detailed description and performance of the GIC circuit is presented in Chapter 4 & 5. The use of NIC topology is limited for several reasons, it: increases the system instability, trimming requirement for each tested frequency, and time delay between measurements.

It can be stated that describing a general specification for a current source is difficult because different imaging systems have different accuracy requirements. Therefore, minimum performance criteria should be achieved as: a large current amplitude (within safety limit) without any compensation circuit, a high output impedance and should be >1MΩ, linear relationship between the input voltage and output, and a minimum common-mode voltage introduced to the measuring circuit. Mostly researchers have focused on the high output impedance, which appeared to be important for a static imaging system. Alternatively, in the dynamic imaging system, it is more important to minimise common-mode voltage and must be at least as small as the expected differential voltage for the system (Boone & Holder, 1996).

### 3.3.4 Voltage Source Benefit and Limitations

As described in the previous section, the implementation of a high precision CS requires complex circuitry and extensive calibration/tuning procedures. The complexity of the CS occurs due to the capacitance cancellation circuit. A few systems have been reported in the literature to resolve the CS issue by applying voltages instead of currents to the SUO (Yoo et al., 2010; Halter et al., 2008; Saulnier et al., 2007; Halter et al., 2004; Hartov et al., 2001 & 2000; Zhu et al., 1993). In the case of an applied voltage system, the resultant current must be measured precisely. The basic circuit topology used in VS based EIT system consists of a non-inverting op-amp buffer with a current sensing resistor within the feedback loop. The purpose of the sense resistor is to measure the current generated by the VS. Ideally, the voltage dropped across the load will be equal to the input voltage

and result in zero output impedance of the source. Due to simple circuitry, the VS design is generally less costly and easier to implement (Saulnier et al., 2006).

The simple implementation of the VS doesn't mean that it is without problems. Practically it was observed that the output voltage of the op-amp is a little less than the input voltage due to the limited open loop gain of the op-amp used. This is due to the non-zero output impedance of the VS and will result in errors in the applied voltage. If a constant voltage drop is desired across a wide range of load impedances, then the VS design should have low output impedance. The load voltage can be obtained by measuring the voltage at the lower potential of the sense resistor. This will enable us to precisely know the applied voltage to the load. The major issue in the VS design is the measurement of the precise load current. Like the CS problem, the parallel existence of stray capacitance with the load will shunt some current away from the load. This means that the current flowing through the sense resistor is not equal to the load current. The capacitance cancellation techniques can be used with VS design and will result in complex circuitry, hence removing the benefit of simple circuitry as compared to the current source.

A slightly modified VS design is proposed in chapter 6. The VS has a current sensing capability with variable voltage gain and controllable feedback current. The detailed circuit analysis and performance of the VS design is presented in chapter 6.

## 3.4 Existing EIT Systems

Many research groups around the globe have designed and developed EIT systems and are involved in the advancement of this field. Many commercial companies have also attempted to produce commercial/prototype instruments for EIT. The most important characteristic of any EIT system depends upon its architecture, either single or multiple excitation based system. The trade-off between the complexity and performance depends upon the functionality of the system. The EIT system was first used for pulmonary imaging and monitoring. With the passage of time and necessity, this technique was extended for other parts of the body, which include: lungs, brain, breast, pancreas, bones etc. The main purpose of this section is to categorise the EIT system based on current driven or voltage application irrespective of the application in which it is being used. The following are some of the prominent EIT systems that can be considered to have made progress in the field of EIT in medical instrumentation.

## 3.4.1 Existing Design Based on Current Source

Current driven EIT systems are widely used for bio-impedance measurement. This approach has its own benefits and limitations, which are described earlier in this chapter. A few systems based on this type are described below.

### *3.4.1.1 Sheffield EIT System*

This research group has developed a series of EIT systems named as Sheffield Mark-1, Mark-2, Mark-3A and Mark-3.5. Most of the EIT system used are based on Sheffield Mark-1 & 2, which consists of 16-electrodes and uses a single excitation source (Smith et al., 1995; Brown & Seagar, 1987). Later the group developed a multi-frequency system (Mark-3A), which can apply 8-frequencies between 9.6kHz to 1.2MHz with a single frequency at a time. The Mark-3.5 system is a successor of the Mark-3A introduced in 2001, which was a multi-frequency system but can apply 30 frequencies in the range of 20kHz – 1.6MHz simultaneously (Wilson et al., 2001).

Mark-3.5 system uses 8-electrodes in total while all the predecessor systems developed uses 16-electrodes. It was reported that all the systems developed at Sheffield provide imaging at a rate of ≈25 images $s^{-1}$. The latest Mark-3.5 system uses an adjacent drive and receive electrode combination and consists of 8 similar data acquisition board's (DAB's) to generate drive frequencies and to perform the fast Fourier transform algorithm (FFT) for signal demodulation. Each of the DAB's can be configured into two modes: a current drive mode and a voltage measurement mode. All DAB's are connected to a motherboard which contains a single microcontroller that controls the data transfer between DAB's, DSP's and the host PC. The current driven system is achieved through balanced modified Howland circuitry (Bertemes-Filho et al., 2000). The output of the VCCS is connected to the differential amplifier of the voltage measurement circuit, which result in charge retention and will limit the overall data acquisition speed of the system.

To overcome this problem, the gain of the amplifiers is reduced in current driven mode and the input to DAC and VCCS is set to zero in voltage measurement mode. However, any noise at the output of DAC/VCCS can produce a current drive and contribute towards noise. To solve this problem, the group had placed switches at the output of VCCS, which can disconnect the source from the electrode. The Sheffield EIT systems are the widely used system because of its hardware compatibility and reliability with an ability to

produce real time images. The systems have well designed instrumentation and have been optimized to capture the best available data using a single CS configuration. However, the system performance is limited by the use of a multiplexer to switch the CS between electrode pairs and its corresponding introduced shunt capacitance. This problem is partially solved by measuring the real part of the measured voltage but alternatively the drawback is the inability to handle the reactive part of the measurement.

#### *3.4.1.2 Kyung Hee Korean EIT System*

The impedance imaging research centre (IIRC) at Kyung Hee University have developed a series of EIT systems named as: KHU Mark-1, Mark-2 and Mark-2.5. KHU Mark-1 was the first EIT system developed at IIRC whose project started in 2002 with an intention to design a brain imaging system with the flexibility to address electrode and frequency range from 10Hz – 500kHz. KHU Mark-1 was manufactured in 16/32 channels and consists of two backplanes: analogue (top) and digital (bottom). The system contains one balanced CS, which is switched to a pair of electrodes for current injection. Multiple digital voltmeters placed around the CS to measure potential difference between adjacent electrode pairs, in a radially symmetric architecture to minimise cross talk and optimise the wires routing within the system. The CS and voltmeters are sandwiched between an analogue and digital backplane. The digital backplane consists of an FPGA and DSP for all control and data acquisition functions. KHU Mark-1 adopted several modules from existing EIT systems, which include digital waveform generation, a Howland source with a GIC circuit, digital phase-sensitive demodulation and tri-axial cables. KHU Mark-1 used multiple GIC circuits to maximise the output impedance of the CS at multiple frequencies. The voltmeter circuity measures contact impedance, data overflow detection, spike noise rejection automatic gain control and programmable data averaging. The KHU Mark-1 can measure both in-phase and quadrature components of the trans-impedance.

A new multi-frequency EIT system was presented in 2011, named as: KHU Mark-2 with improved circuit design and layouts. It has inherited most of the modules from Mark-1 with added new features of: flexible electrode configuration, multiple independent current sources and voltmeters for a fully parallel measurements and improved data acquisition. Due to a unique design of the analogue backplane, both current injections and voltage measurements can be done without any switches. It is based on a separate impedance measurement module (IMM) which consists of a CS, GIC circuits, differential voltmeter,

a FPGA to control all functions of this module, ADC and DAC (Oh et al., 2011). Using multiple IMM's, the KHU Mark-2 can be a multi-channel system comprised of 16/32/64-channels. It implemented a fully pipelined structure to improve the data acquisition speed and has achieved a data acquisition rate of 100 frames $s^{-1}$, that can be beneficial to detect fast physiological changes during cardiac and respiratory activity. The KHU Mark-2 system can measure both in-phase and quadrature components of impedance at multiple frequencies simultaneously. This system was able to achieve ≈84*dB* of SNR with a 0.5% reciprocity error. The requirements for a long-term stability of an EIT system differ between applications. A stable EIT system is essential in clinical monitoring with improved image reconstruction and compatibility with other existing clinical devices. The IIRC group felt that the system performance variation and calibration over a long time period is not sufficiently well presented in the literature. The long-term monitoring applications require auto-calibration and highly stable system over a long time period.

To address the clinical applicability of the EIT system, the group designed and tested a new MF-EIT system called the KHU Mark-2.5 over 24hours for 7 days continuously. The KHU Mark-2.5 introduced the additional features of auto self-calibration, additional control and timing signal to interface with external medical devices and improved system software. The CS calibrator was included in the IMM to: maximise output impedance, minimise the DC output current and balance the current between the source and sink path. A resistor phantom is placed inside the system for intra and inter channel calibration of all voltmeters in multiple IMM. Many improvements and modifications were done for calibration and long term stability. The system reports an SNR of 80*dB* for frequencies until 250kHz and <0.5% reciprocity error over continuous monitoring for 24 hours. The group also claims a SNR of 75*dB* and reciprocity error <0.7% for over 7 days at 1kHz frequency (with auto-calibration of at least every 3-days). The system performance degrades with the increase time between auto-calibrations. The detailed information of KHU Mark-2.5 is reported by Wi et al., 2014.

#### *3.4.1.3 Russian Academy EIT System*

A Moscow based research group developed a series of EIT systems based on a single source for thorax and breast imaging (Cherepenin et al., 2002 & 2001). The thorax imaging system works at 8kHz and uses 16-electrodes (on a rubber belt with coaxial cables connection) with a single multiplexed current source and voltmeter. The breast

imaging system also uses a single source and voltmeter with 256-electrodes configured in a round planar matrix and requires ≈20sec to collect data for a single image. The research group mostly published literature related to the breast imaging system.

The system consists of a hand-held probe (256-electrode array), two portable-electrodes and a computer for image reconstruction. During the data acquisition, the electrode plane is pressed from the top of the breast to make it flatten towards the chest and to ensure a good electrodes-body contact. Two portable-electrodes are attached to the wrist of the patient. One electrode is connected with the CS and the other portable electrode is connected with a potential difference detector and serve as a reference electrode. The CS module consists of a DAC, which provides the input to the V-I convertor comprised of a three op-amp topology. A bad contact with the patient's skin is detected by a voltage threshold detector connected at the output of the CS. The maximum operating frequency of this instrument is 110kHz but due to the capacitive behaviour of the skin impedance, it is easier to provide sufficient contact of the electrodes with the body at high frequencies without putting a highly conductive medium on the skin.

Alternatively, the parasitic capacitance limits the measurement accuracy at high frequency. After consideration, an excitation frequency of 50kHz with an amplitude of 0.5mA is used in this impedance system. During the measurement operation, the potential difference detector is connected to the first electrode in an array via a multiplexer along with the contact potential difference compensation. The CS is switched to each of the remaining electrodes of the array and measurements are acquired. The instrumentation amplifier gain is adjusted accordingly and depends on the distance between the injecting and measuring electrode. A complete dataset for 3D conductivity reconstruction of an image consists of 65280 measurements. Data processing and the measurement process is achieved via serial port connection between PC and the instrument. During device initial trials, it was concluded that the device can distinguish conductivity difference between normal and cancerous tissue but with limited performance when scanning dense breast and in the nipple area. The device received its EC certificate for clinical testing in 2006 and had been initially deployed in Russia. Later it was tested in Italy, Czech Republic and Malaysia (Campbell et al., 2007). The trials again faced the challenge of high conductivity in breast's nipple but it was concluded that the device can be used to monitor the whole breast instead of pure imaging. It produces grey scale cross sectional images at different

depths and reported that this single frequency device can detect early breast cancer with a size of ≈3-5mm with scanning limitation in certain area.

A multi-frequency system (named: MEM) was also presented by the group (Trokhanova et al., 2008) which is an updated version of single frequency system. This system operates at two frequencies: 10kHz and 50kHz. The frequency range is limited to 10kHz as the lower limit because frequencies <10kHz cause difficulties in providing reliable contact with the body and 50kHz is at the top limit, due to the significant influence of the multiplexer's stray capacitance at higher frequencies. The updated device uses the same electrodes structure and procedure to acquire measurement. The system reported that the device can differentiate a cystic mastopathy and is effective in diagnosis of malignant breast tumours.

After successful testing and usage of the mammography diagnostic system, the research group developed a 3D electric impedance imaging device for diagnosis of the cervix of the uterus and named it a gynaecologic impedance tomography (GIT) system. The GIT device allows to visually estimate the vaginal part of the cervix of the uterus and obtain its conductivity parameters at a depth of ≈1cm at a frequency of 50kHz and 10kHz. The prototype GIT device consists of an orthogonal 32-electrode scanning head arranged in a 2D flat array and provides the conductivity distribution in a few cross-sections with a depth up to 8mm and at more than one frame $s^{-1}$ measurement (Korjenevsky et al., 2010). An improved device consists of a non-regular, non-orthogonal 48-electrode array embedded on a small scanner probe of 30mm diameter and 20mm height (Cherepenin et al., 2012). The system provides one shot $s^{-1}$ of the spatial distribution of the static electrical properties of the cervix tissue. The authors report that the EIT for cervix diagnostics is especially effective to identify a higher degree of squamous intraepithelial lesion and suspicion of invasion. The GIT device had gone through clinical trials with first test results presented in Trokhanova et al., 2010.

#### *3.4.1.4 University College of London (UCL) EIT System*

This group has typically developed low frequency system used primarily in brain imaging. The UCLH Mark1a EIT (prototype) system was a current driven device with 16-electrodes designed for a pair driven measurement in a single impedance measurement and used a multiplexer to address electrodes (Holder et al., 1999). The system was designed to record measurement in the frequency range from 50Hz - 50kHz. A sinusoidal

voltage signal was generated by a digitally controlled function generator and passed to a current conveyor circuit, which act as a CS. Signal demodulation was performed using a synchronous rectifier and only the real component from the measured signal was extracted. At lower frequencies, extraction of imaginary components achieved but this is insignificantly reported.

The next system developed was UCLH Mark1b with 64-channels operating at a single frequency from 18 discrete frequencies in the range of 225Hz to 77kHz (Yerworth et al., 2002). The system uses cross point switches for electrodes selection with a system ability to collect data at 3fps having 31-active channels and 258-electrode combinations. This system was also based on a CS using a current conveyor circuit having an output impedance of 537kΩ. A synchronous demodulation voltage measurement circuit yields the magnitude of the impedance. Each electrode combination uses programmable phase to ensure that the analogue demodulation occurs in phase with the signal. The author calculated the SNR using the ratio of mean-to-standard deviation of reconstructed images from 200 data sets collected using a saline tank. The system was able to achieve a SNR of ≈30*dB* at 4.8kHz and 76.8kHz. An increased SNR of >50*dB* was reported for the frequencies between 10-30kHz with a max reciprocity error of <2% for most of the frequencies and least over the 10-40kHz frequencies. The CMMR for the voltage measurement circuit was reported to be 90*dB* for frequencies <20kHz and 70*dB* for frequencies >50kHz. They reported that the system has significant performance to image impedance changes in the brain during normal activity.

The UCLH Mark2 was the next system developed with integrated features of both Sheffield Mark-3.5 and UCLH Mark1b for simultaneous multi-frequency brain function imaging (Yerworth et al., 2003). The system used 32-electrodes (up to a maximum of 64-electrodes). It used a modified version of the Sheffield Mark-3.5 data acquisition module with an addition of a DSP via serial port link. It uses two cross-point switch boards designed according to its predecessor Mark1b system with an ability to serve 16-electrodes and a high pass filter for each board/channel. It reported a frequency bandwidth of 0.8MHz with an SNR of ≈50*dB* (<0.3%) at mid-band frequencies (8kHz – 0.8MHz). The system CMMR at 1kHz was decreased as a function of frequency and reported to be less than the Sheffield Mk3.5 system. They reported an accurate banana position in a reconstructed image using a saline tank with clear visibility up to 81kHz frequencies and spectral plots obtained from phantom data.

The UCLH Mark2.5 was the latest and compact system developed (as per our knowledge) by the UCL group (McEwan et al., 2006). It was an improvement in the Mark2 system and was based on a single acquisition module multiplexed between a maximum of 64-electrodes. This system frequency range was extended downwards to 20Hz as suggested by stroke modelling. The system used a four-electrode measurement method with a max of 133µA current injection with 30 frequencies from 20Hz to 1.3MHz (Packham et al., 2012). The output impedance (CS) and input impedance (voltage measurement circuit) was increased to 1MΩ with an increase in max linear load impedance to 70Ω. Fixed gain has caused noise at low amplitudes in the UCH systems. The gain was reduced from 100x to 30x to ensure high trans-impedance measurements on the head were not saturated. DC-blocking capacitors were used at each electrode contact for patient safety. Its effective bandwidth was in the range of 20Hz – 1MHz with a roll off by approximately <1*dB*. The CMRR was 79-89*dB* and didn't change significantly over the frequency range or without multiplexers. The variability over frequency for a single channel was less than ±0.2% between 20Hz to 1MHz for loads between 8.9-73Ω using four terminal loads with <0.1% SNR variability over time. They reported a significantly higher error in measurement at 80Hz, 32kHz and above 256 kHz frequencies using a saline tank, possibly due to the stray capacitance of the tank and longer leads. The authors reported that by avoiding these frequencies the error could be reduced to ±0.7% using tank and it was intended to apply the same strategy for human brain recording. The system also reported random noise over time but this was significantly smaller than the error due to frequency (>0.1%). Hence this limits the system's acceptable linear load range to 10-70Ω over the frequency range of 20Hz – 250kHz. The system frame rate is slow (26s per frame) due to the lowest measurement frequency of 20Hz and serial measurement of all 258-combinations.

### 3.4.2 Existing Design Based on Voltage Source

An alternative method used in EIT systems is to measure the current by using a voltage source to establish a potential difference between electrodes. High quality voltages sources are available in the form of op-amps, which can provide stable solutions over a wide frequency bandwidth. Its benefits and limitations are described earlier in this chapter. A few EIT systems based on this type are described in this section irrespective of the application in which it is used.

### *3.4.2.1 Dartmouth College EIT System*

This group has mostly focused on the development of an EIT system for breast cancer detection. The first generation at Dartmouth was a prototype EIT system developed in 2000 composed of a circular electrode array system and capable of data acquisition in either voltage/current mode over a frequency range of 10kHz to 1MHz. A signal was generated via a plug-in PC board and can generate arbitrary functions by DDS with 12-bit precision. The VS circuit consists of a non-inverting op-amp configuration while the CS was an operational trans-conductance amplifier circuit (Hartov et al., 2000). The DC bias current problem in CS has resulted in a safety issue for in-vivo application and has resulted in circuit limited frequency bandwidth (1.3MHz). Hence, it was mostly used in voltage application mode. The PSD was done in software with a mixing of reference and measured signals. High data acquisition bandwidth was achieved by sampling the data over multiple cycles and rearrangement of measured signal for mixing. The system contains a bed with a ring electrode array with 16-electrode adjusted radially and vertically. The patient lies on the bed with breast hanging in the circular electrode array. After a proper breast-electrode contact, an excitation signal (voltage/current) at selected frequencies is applied and the resulting measured signal (current/voltage) are recorded from same electrode. The 2D conductivity and permittivity images are produced from the recorded measurements. The group reports that high suspicion of lesions is identified by this system. The permittivity image provides more information as compared to the conductivity image; hence, it has become helpful to identify a malignant tumour in the breast. The system reported some significant results including an SNR of 75$dB$ with an accuracy of 99.98%. Channel phase mismatch was reported to be <0.05% with respect to 180º with a system frame rate of 0.22fps.

The second generation 3D EIT system was developed in 2008 at Dartmouth. The primary objective of improvement in the system was to incorporate a functional wideband EIT system for breast imaging at multiple high frequencies. The motive was to achieve a frequency bandwidth range from 10kHz to 10MHz with 16bits measurement precision, channel-to-channel phase and magnitude uniformity of better than 0.1%, SNR of >90$dB$ and a frame rate of 30fps. The updated version of the system uses fixed 64-electrodes at four levels with digital processing for all 64-electrodes. Each level has 16-electrodes configured in a round shape. The improved system has a better electrode-skin contact and hence results in a clear image for a scan with frequency >500kHz (Kerner et al., 2002).

Dry electrode contact method with conductive gel was used. The 2nd generation EIT system consists of three electronic subsystems: an interface computer, a control module and some measurement channel modules. A single control module communicates with all 64-channels implemented on 16 individual 4-channel board. Each 4-channel board provide signal generation and data acquisition. The control and measurement channel modules are designed with 32-bit DSP and FPGA to implement majority of the functionality in digital domain. According to the author's best faith, this is the first reported EIT system which is capable of impedance measurement up to 10MHz. It is based on a DSP architecture and allows high speed frequency signal generation and data collection with a flexible design option of arbitrary pattern generation, variable sampling and multi-toned testing. Authors reported a system channel SNR of ≈95$dB$ at low frequency spectrum (<1MHz) and this drops to 78$dB$ at 10MHz (Halter et al., 2008 & 2004). 96 patients were safely imaged by this system and their impedance spectra obtained from 3D images closely reports their literature. The group also reported a patent imaging system for detecting prostate cancer by combining ultrasound and EIT technology (Hartov & Paulsen, 2009). This group also reported an image reconstruction system designed specifically to work with individuals and relies on the knowledge of surface geometry of the patient with a successful image reconstruction (Forsyth et al., 2011; Tizzard et al., 2010).

#### *3.4.2.2 Rensselaer Polytechnic Institute (RPI) EIT System*

RPI is also a prominent research group in the field of EIT. This group has developed a series of EIT systems using ACT technology out of which the prominent systems are described here. The RPI research group built ACT3 (3rd Generation) in 1995. The ACT3 system consists of 32-channels with each channel having a separate CS and voltmeter. The same electrodes were used for current injection and voltage measurement. The system was able to take measurements and reconstruct the images at a rate of 20fps. This system was a fixed digitally generated sinusoidal signal of frequency 28.8kHz followed by a 16-bit DAC for analogue signal generation for the excitation circuit (Liu, 2007). The excitation circuit implements a CS using an instrumentation amplifier with the Howland topology. The output impedance of the CS is maximised by using a NIC in parallel with the current source. Digital potentiometers are used in CS and NIC to maximize the output impedance and capacitance cancellation of the source using automated calibration

system. Each electrode is equipped with a 12-bit ADC for voltage sampling and with a DSP chip to implement a matched-filter to measure real and quadrature parts of the complex voltage. The measured signals are sampled 5tpc (times per cycle) over multiples cycles (no of cycles are dependent upon the desired precision/ frame rate). For a 20fps, 160 samples per measurement are collected which gives a precision of ≈15bits. The system showed effective results but with a significant increase in the architecture complexity high costs and it is not easily portable. It reported a voltmeter SNR of >104*dB* at an acquisition rate of 7.5 fps for each 32-channels along with an absolute accuracy of 99.5% in known resistive loads. The acquisition rate can be increased at the cost of reduction in voltmeter SNR. A maximum of 480fps can be achieved with the voltmeter SNR reduced to 86*dB* (Cook et al., 1994). With the usage of ACT3 for a long time, the RPI research group developed interest in the implementation of the next generation of ACT system.

The ACT4 is the 4$^{th}$ generation EIT system developed by the RPI research group with the intention for its usage in breast cancer detection (Saulnier et al., 2007; Kao et al., 2007; Liu et al., 2003). It was considered to be a major improvement on its predecessor ACT3 system. The ACT4 system has a similar interface to other mammography devices and consists of two parallel planar electrode arrays. ACT4 has a modular design and can support a maximum of 72-electrodes. Practically it uses 30-electrodes in a single planar electrode array arranged in a rectangular manner. The ACT4 system is formed of an electrode support module (ESM) and consists of an analogue front-end and digital interface for a single electrode. The ESM is interfaced with an FPGA that is used to implement signal generation, voltmeter and control signals for ACT4 analogue circuits. A precision of 16-bits for sources control and 16-19bits for voltmeters were required. A 14-bit digitally generated sinusoidal excitation with controllable amplitude, frequency and phase at 20MHz sampling rate is fed into a DAC to generate an analogue excitation signal. A complex matched filter was implemented in an FPGA to produce the real and quadrature part of the measured voltages. A graphical user interface and data management system was implemented for storage of hardware, patient/phantom and reconstructed image data.

The ACT4 system can apply discrete excitation frequencies in the range of 300Hz to 1MHz. The system has an ability to apply either voltages/currents to all electrode channels simultaneously and measure the resulting currents/voltages. The CS was

implemented using Howland topology parallel with a GIC circuit and a calibration procedure used to obtain high performance of the source at each excitation frequency (Ross et al., 2003). VS with integrated current measurement circuit was implemented and used extensively in calibration to achieve high precision. The ESM module contains a switching network to calibrate all the sources on a central calibration board and maintain a common standard. This system applies voltage sources of orthogonal patterns and measures both the applied voltages and its resulting currents on the electrodes (Kim et al., 2007a; Saulnier et al., 2006) which are used to reconstruct the permittivity and conductivity images of breast tissues. Further analysis was performed on the reconstructed images by applying electrical impedance spectroscopy (EIS) plots and the linear correlation measurement method. The group reported that straight lines are highly correlated to the malignant tissue in EIS plots. The higher grey value indicated the higher correlation with the line in a grey scaled linear correlation measure image and is expected to be tumour tissue. It is reported that the ACT4 system can distinguish malignant from normal and benign tissue. The group reported that the planar electrode configuration has a penetration sensitivity problem and needs more research to overcome this problem (Kao et al., 2008). It was also reported that the voltage SNR of $\approx 106dB$ across all frequencies gives ≈17.5-bits precision in voltage mode for a specific channel. The current SNR was variable over different frequencies and in the range of 16.5 (≤333kHz) to 14.5 (@1MHz) bits precision. The SNR was estimated by applying the same amplitude signal a couple of times to a dummy load and calculate the mean and variance of the result but it varies from channel to channel (Saulnier et al., 2007).

#### *3.4.2.3 Kyung Hee University EIT System*

The IIRC research group at Kyung Hee University has developed a number of instrument series based on VS for bio-impedance spectroscopy (measure admittivity spectra of biological tissues) and Trans-admittance scanner (breast cancer detection). This BIS (bio-impedance spectroscopy) series includes the KHU Mark1-3 BIS system. The KHU Mark1 mfEIT (multi-frequency EIT) is the first BIS system developed by the IIRC group. This system performs time-difference imaging at multiple frequencies range from 10Hz to 500kHz. This single channel system uses ten frequencies in the above range and consists of a CS and a voltmeter. The system uses stainless steel electrodes configured in a four-electrode method in the form of a chamber with separate electrode pairs for current

drive and voltage measurement. The GIC circuits are used to minimise CS output capacitance for frequencies >5kHz. The system performance was degraded at frequencies >500kHz due to stray capacitance even the CS was calibrated for maximum output impedance.

Consequently, the IIRC group designed a new prototype system called KHU Mark2 BIS system based on VS with an intension to be a portable device with preliminary measurement results (Yoo et al., 2010). The next system developed was KHU Mark3 BIS system, which is an improved version of its predecessor. The improved system was based on two IMM's with low noise components and an improved PCB layout. The Mark3 BIS system consists of a controller, constant VS, two voltmeters implemented as an instrumentation amplifier, programmable gain amplifier, analogue filters and signal convertors. An FPGA implements the IMM controller and controls: a DAC to generate variable amplitude and frequency sinusoidal waveform, two ADC's to convert measured voltages and then performs digital PSD. A DSP controls all the communication from the PC and forwards the intended commands to the IMM controller. A digitally generated variable frequency sinusoidal voltage signal is applied to the series connection of the sense resistor and SUO connected via electrodes pair. The differential voltage is recorded via tetra-polar measurement configuration.

The VS-based BIS system acts as a voltage divider circuit between the internal sense resistor and SUO. To achieve a high SNR of the source, the internal sense resistor is changed until the source voltage is divided more or less equally. System calibration was performed by measuring the transfer function of the BIS system with several known resistive and capacitive loads. The resistance and capacitance of the tissue was estimated using the least square method to minimise error between the measured trans-impedance, which excludes the system transfer function and from an impedance model.

The VS-based BIS system was tested with discrete resistors, capacitors and saline/agar phantoms, and gave a wider frequency bandwidth of 10Hz to 2.2MHz with <1% deviation from the expected spectra. The system reported a SNR of at least 60$dB$ up to 2.2MHz, which was higher than the CS-based BIS system. The electrode used for the measurement system of living tissues, has different characteristics and contact impedance. As a result, the system measurement accuracy will be affected due to change in the total transfer function of the measurement system. The group introduced two types of electrodes for

samples made with saline or agar: 1) a cubic container of size 50x50x50 $mm^3$ with large injection and ground electrode with small voltage measurement electrodes filled with saline/agar, 2) a needle-shaped electrode made of four gold needles, which can be inserted 10mm into the sample of saline/agar. The conductivity is computed by multiplying the ratio of the cross-sectional area of the container and its length by the inverse of the resistance. They computed the SNR and conductivities with both type of electrodes on several samples using the VS BIS system (Mohamadou et al., 2012).

The group also developed a trans-admittance mammography (TAM) system as an alternative method to x-ray mammography for breast cancer screening. The approach is to extract the features of lesions inside the breast instead of the cross-sectional imaging. A patient holds a reference electrode through which a constant voltage is applied to the scan probe (planar array of electrodes) placed on the breast. A current flow due to the potential difference produced by the hand-held electrode to each ground electrode of the probe through the breast. A trans-admittance map is obtained by measuring the exit currents from all electrodes in the probe. The complex conductivity distribution within the breast is extracted from the trans-admittance map for the region under the probe.

The first TAM system developed by the group was an 8x8 planar electrode array with a single 50kHz excitation signal. This system consists of a total of 64-channels with 8-channels per ammeter and relay switches. The measurement accuracy of the system was demonstrated using a resistor and saline phantom. The results need improvement in the SNR and increase in number of electrodes (Lee et al., 2004). An improved version of the TAM system was implemented and utilized to validate the lesion estimation algorithm (Oh et al., 2005). It consists of a hand-held electrode, scan probe with 256 gold coated planar current sensing electrode (each of 1.5mm diameter) array integrated with relay switches, constant VS (with variable amplitude of 0-2.5V at 50kHz), 16-channel per ammeter, main controller and a PC with interface control software. The main controller synchronizes all ammeters with VS for precise PSD and communicates with the PC via a wireless serial data link.

This system performance was evaluated using resistor and saline phantoms. This system was reported to have a better SNR of 82$dB$ as compared to its predecessor. The system reported the depth and size estimation in the range of 4-15% and 7-27% respectively with a suggestion to improve the algorithm for size estimation. The system also reported

successful detection of anomalies located deeper than 20mm due to the use of a wider planar electrode array. The authors realized that the performance of these systems depends on the size and number of electrodes in the scan probe along with SNR in measured exit currents. Hence, the authors investigate other ways to improve the performance of system. The intention was to achieve a SNR of 100*dB* by redesigning the PCB's of the system along with improvement in scanner probe and the operating frequencies of the system. The lesion estimation algorithm defines a direct relation between lesion and trans-admittance data and uses a non-iterative algorithm to extract the lesion's main features. A drawback of this method is the requirement for reference trans-admittance data acquired without a lesion. It was suggested that to make the method more practical the reference data should be eliminated. Therefore, the authors focused on a multi-frequency technique which relies on the difference in trans-admittance maps obtained simultaneously at two or more frequencies.

Hence, the group developed a multi-frequency TAS system that can capture trans-admittance maps with an improved scan probe with a gold-coated planar 320-electrode array in the frequency range of 10Hz to 500kHz (Oh et al., 2007a). This new system follows the same architecture as its predecessor system, apart from improvement in the electronics components and CMOS switches instead of relays inside the scan probe. Each electrode is a circular sensor with 2mm diameter having a contact area of 3318.3 $mm^2$ for the total 320-electrodes. This system integrates a total of 16-ammeters, each connected sequentially to a block of 20 current sensing electrodes and calibrated for different gains and frequencies using a resistor phantom. The group presented an anomaly detection algorithm, which provides its location and size using a frequency-difference trans-admittance map, which reflect the complex conductivity distribution underneath the scan probe. It was evaluated using a saline phantom experiment. The anomaly location and depth under the probe region was estimated, however anomaly size estimation requires calibration to remove the unknown scale factor. A minimum 4mm diameter and at a maximum depth of 15mm can be detected from the frequency-difference trans-admittance map having one frequency <500Hz and the other >50kHz (Kim et al., 2007b). Further analysis was suggested to understand the complex conductivity of anomalies and normal tissue using frequency difference trans-admittance map. Improvements are required to reduce estimation errors in detection of small anomalies located away from the probe plane. It was suggested that with an improvement in SNR in measured trans-admittance

data will help in detecting an anomaly with smaller size and larger depth. The spatial resolution of measured data is limited by the number, size and distance of current sensing electrodes.

The group presented a new design of the TAM system with better spatial resolution and performance (Zhao et al., 2013; 2012; 2010). The improved system used two parallel plates instead of hand-held electrode and scan probe. The plates can be rotated for consecutive projection imaging at any angle. This system includes an array of 60x60 current sensing electrodes. Scanning procedure is similar to x-ray mammography in which the breast is placed between two parallel plates. A sinusoidal voltage signal is applied through top large solid electrode plate (180x180 mm) in the frequency range from 50Hz to 500kHz. The bottom plate consists of 3600 current sensing electrodes kept at ground potential. Each electrode is gold plated to minimise contact impedance with a diameter of 2mm and at a 3mm distance from other electrodes.

Current is generated from the top plate and flows through the breast towards the TAM system using a current sensor at the bottom plate. The system consists of 6 switching modules connected to 600-electrodes each and is used to measure exit currents. Each switching module consist of 12-ammeter channels that are switched sequentially to 50 of the 600-electrodes for each measurement. Each ammeter channel contains a current-to-voltage convertor, gain amplifier, ADC and digital PSD. The authors reported that the TAM system produced time-difference and frequency-difference trans-admittance images (both real and imaginary part) using a saline phantom at 10 different frequencies with a fact that the contrast between background and the anomaly changed according to the conductivity of the tested material. They reported that the large number of sensing electrodes improved the spatial resolution of the TAM system and is capable to detect a small anomaly with an average noise level of 38nA and 70*dB* SNR (5-500kHz) and 50*dB* (50Hz – 1kHz) (using 100 repeated measurements) from the trans-admittance images (Zhao et al., 2012). Another study by the authors showed that the TAM system can estimate the depth within 20mm with an increase in the error over this depth. The estimation results from the saline experiment show the ability to detect a breast tumour using TAM frequency difference images. This detection algorithm significantly depends on conductivity contrast and requires an improved algorithm before implementing the system for clinical experiments (Zhao et al., 2013).

#### *3.4.2.4 Trans-Scan TS2000 System*

This is the first commercial EIM system implemented for breast cancer detection (Assenheimer et al., 2001; Piperno et al., 1990). The system consists of cylindrical planar electrode array, a scan probe, and a computer. The system comes with three different probes: 8x8 electrode array (small probe), 16x16 electrode array (big probe) and 16x16 electrode array (small probe) (Zhang, 2015). The system works over the frequency bandwidth range of 100Hz to 100kHz (Ammari et al., 2004). All the electrodes are held at a virtual ground while a voltage signal of 1-2.5V amplitude is applied through the cylindrical electrode. A current is induced due to the potential difference between the cylindrical electrode and the breast, and flows out of the scan probe electrodes. Current at all the electrodes are measured using a fast filtering algorithm and transmitted to a computer for conductance and capacitance extraction in the form of two gray scale images for the SUO. During analysis, any white spots in the images are considered likely to be tumour tissue. The clinical trial of the system reported the system's ability to detect a breast tumorous tissue of minimum 3mm diameter in size with an inability to detect the tumorous tissue near nipple/deeper in the breast (Melloul et al., 1999; Scholz & Anderson, 2000; Malich et al., 2001). They report a system accuracy of 5% for capacitive loads in the range of 20pF – 1nF and conductance loads in the range of 1-20mS. The system also achieved a SNR of 70*dB* at low frequencies (100Hz) and is reduced to 40*dB* at higher frequencies (100kHz).

## 3.5 Sussex EIT System

The biomedical research group at the University of Sussex is one of the leading research groups and have produced a series of impedance measurement systems over the last 2 decades. The research group's idea was to build a breast cancer detection device using EIT technology and was named as Electrical Impedance Mammography (EIM) system because it was an EIT system used to measure mammary glands. The research group was initially established at De Montfort University (DMU) in 1995 followed by a collaboration with Leicester control systems group for the ongoing EIM project in 2005. In 2008, the research group re-located to the University of Sussex where the group has continued the journey in EIM research. For the last 16 years, the group has developed different EIM systems, which show the group's prominent progress in the field of EIT

development. The system developed by the group are identified as MK1, MK2, MK3 (a& b) and MK4/MK4b. This section will briefly describe the architecture of the system along with improvements in the design and its performance.

The first generation EIM system: MK1 was developed by the DMU biomedical research group. It was designed to detect in-vitro breast cancer in a specialized impedance chamber where excised tissues were placed in a body temperature filled with saline. The MK1 system was a single channel measurement device with a four-electrode measurement configuration: two for current injection and other two for voltage sensing. The MK1 system consists of a CS based on an RC oscillator circuit and can generate current excitations with 31 different frequencies ranging from 1kHz to 4MHz. Practically, the precision of the signal frequency from the oscillator circuit was hard to satisfy the need of spectrum scanning and has to be formed by stacking all the single frequency measurements manually due to a lack of auto-timing and ADC in each sample measurement. The MK1 system was based on analogue technology and its measurement accuracy was affected by the harmonics frequency of the injected current and loss of signal transmission by long cabling. It was felt that without digital control timing and ADC within the system, MK1 system can't be applied for long measurements. The complex impedance of the measured signal was obtained by using software. Several tests were completed using the MK1 system in 1997 (Tunstall et al., 1997). It was reported that mean conductivity values in fat and other tissue are 8mV/mm and 1.5mV/mm respectively. With some promising results achieved by the MK1 system, the group was ambitious to build an in-vivo version of the system and further develop an EIM system for 2D and 3D imaging.

The second generation EIM system: MK2 was built in 1998 with a very unusual design and was the first attempt by the research group to detect in-vivo breast cancer. The MK2 system consists of 32 dry-electrodes in a ring configuration embedded inside a specialized bra. The hardware and software in the MK2 system were updated. The MK2 system still uses four-electrode measurement configuration. A DDS oscillator was used to digitally generate a good quality sinusoidal wave with minimal harmonic components, flexible frequency and phase selection. The DDS was digitally controlled and programmed using the C-programming language. The test analysis was done in Matlab software and stored in a Microsoft Access database. The MK2 system intended frequency of operation was in the range from 1kHz to 5MHz but the system only showed a linear behaviour over the

frequency range of 1kHz to 1MHz due to a roll-off at higher frequencies because of the increasing effect of phase distortion and stray capacitance at higher frequencies (Wang et al., 1998). The scanning method of the MK2 is simple: the patient was required to wear the bra and the operator controlled the scan from a PC. The scan is fast, comfortable and potentially doesn't require any qualified operator. Due to ring electrode configuration, the MK2 system can only generate a 2D cross sectional image. The image reconstruction algorithm used in the MK2 system was a modified version of the back-projection algorithm (Avis & Barber, 1995). It was only a prototype design and was not able to achieve any significant results. It was limited due to the size variation of different breasts, which required different bra sizes and also the electrode skin contact was not sufficiently good. Hence, this introduced a significant error in the measured data and reduced the repeatability of the scans.

The third generation EIM system: MK3 was started in 2006 in which for the first time the concept of a bed scanner was introduced in this group. The MK3 system uses a similar examination process used by Ye et al., 2008 in which the patient lies on the bed and the breast is inserted in a saline filled tank. The problem of different breast size and the electrode skin contact problem was improved as compared to the MK2 predecessor. Two versions of the system were introduced and categorised as: MK3a and MK3b. A constant CS was used for both versions of the MK3 system, based on a modified Howland circuit topology. The MK3 system was intended to achieve measurement at 16 different frequencies up to 5MHz. The scanner head consists of 32/64-electrodes and 128-electrodes in MK3a and MK3b systems respectively. The MK3b system only uses 85-electrodes out of 128 for measurement. The scanner head of MK3 also introduces the option of breast height adaptation. The scanner head of MK3a system presents a bowl design interface with electrodes arranged in 3 levels. The MK3b system uses an updated version of the scanner head by replacing the bowl shape scanner with an adjustable planar electrode array with electrodes slightly recessed from the surface. The system uses a warm tank and the plate is adjustable vertically according to the predefined breast cup size. Electrodes are fixed within the plate and are recessed 2mm from the surface. The system ensures that there will not be a direct skin-electrode contact with the patient but an interface of conductive medium will always be present to assure a predefined conductivity path and value to reduce the contact artefact. With the knowledge of the electrode position and height, the reconstruction algorithm of the MK3 system uses the

predefined accurate mesh, which results in an increased accuracy of impedance mapping. The MK3b system was considered as a prototype of the next generation EIM system. The MK3b system was built in China but unfortunately, due to high standards of safety engineering required for medical instruments, the system was not placed into clinical trials.

The latest 4$^{th}$ generation EIM system is MK4 which involved a new fully integrated system in Matlab software used to control all the data input and output flows of the system. The system architecture is similar to MK3b. A digitally generated sinusoidal voltage signal through a DSP, creates a current signal via an analogue CS and is being driven to electrodes via MUX. The received voltage signal is captured at MUX, which transferred the captured signal to a computer via DSP for impedance measurement. The bed system was completed in this version with a new heating system introduced to heat the saline in the tank for patient comfort. This version of the system was completed in 2006 but the MK4 system didn't receive ethical approval due to the safety issue related to the saline tank being close with the main power voltages. Therefore, the system was further researched to improve its limitations.

After continued hard work, another version of the system was developed at the University of Sussex in 2010 and was named the Sussex MK4b. This version has gone through full clinical trials with proper ethical approval and passed health and safety requirement to measure in-vivo impedance of breasts and cancer identification. It is easier to achieve overall system compliance if the individual parts of the system are already complaint with some recognised standards (Béqo et al., 2010). This is one of the main reasons for implementing the new architecture of the MK4 system, which is based on the PXI chassis and modules. The Sussex MK4b system data acquisition and controlling software has been changed to LabVIEW (National Instrument's) due to the easier programming interface. The clinical trials were performed in the John Radcliffe Cancer Centre, Oxford University Hospitals NHS Trust.

The MK4b system has gone through many improvements and the final appearance of the system is still in the form of bed with a circular scanner having variable depth of electrode plate to accommodate different breast sizes. The bed is equipped with a saline pumping system, saline warming system, saline cleaning system, an electrode adjustment system, a PXI based data acquisition and control system on a laptop, a safety and emergency

system, dual power system and smooth bed with height adjustment. During examination, the patient lies on the bed with their head facing down with their breast in the saline tank. The saline pumping system will pump fresh saline into the tank until it is fully filled with saline then stop due to an overflow sensor. The conductivity of saline changes with change in temperature. Therefore, the saline is maintained at a constant temperature by a heating control system that is continuously monitored via a temperature sensor.

A planar electrode array is placed at the bottom of the cylindrical saline tank, which can inject excitation current and collect measured voltages. The cylindrical tank is 18cm in diameter with a depth of 5cm, which can easily accommodate the maximum sizes of breasts. The electrode array moves vertically inside the cylinder to accommodate different breast sizes by gently pressing the planar electrode array against the breast to reduce the thickness of the breast and to adjust the breast position to be within the sensitive area of the electrode array. The safety and emergency system is activated in case of any sudden system fault. During the fault, the safety system will cut off the electrical power of the system using a circuit breaker and limit the system to manual operation for patient safety. Once the measurement is completed, the cleaning system is activated and will empty, disinfect and rinse the saline tank. Dual power systems are introduced in the system: data acquisition is achieved using a battery power supply to provide a stable source, the main external power supply is used by the saline system and electrode adjustment system.

The DAS of the MK4 systems is an important unit of the system. It is based on a PXI chassis with a number of dedicated PXI modules controlled by custom software written in LabVIEW. The research group has used the PXI product family of PXI-62XX so that the maximum flexibility of an EIT system can be achieved. The intended specifications of the MK4 system are summarized in Table 3.1.

The Sussex EIM system uses a quadrature impedance detection method. The scanner head of the DAS is a fully programmable planar electrode array and consists of 85 stainless steel electrodes employed in a hexagonal configuration. The electrodes are 2.5mm in diameter and placed at 17mm from each other. The electrodes are slightly recessed (≈2mm) to form a conductive interface between the electrodes and skin by providing a stable contact surface and reduction in contact impedance.

A 4-electrode measurement configuration is employed in the system. The injected currents are provided by a signal source with available output frequencies over a wide

frequency bandwidth. Two single ended balanced current sources with 180º phase shift are used for current injection. By this configuration, one electrode becomes a source and the other electrode acts as a sink for a balanced current source.

The system uses a setup of 9 frequencies: 10kHz, 20kHz, 50kHz, 100kHz, 200kHz, 500kHz, 1MHz, 2MHz and 5MHz. A PXI-54XX series function generator provides signals to a *V-I* convertor for application to the body. The electrode configuration is selected by the PXI-62XX module and can be either configured in current injection or voltage measurement. Each electrode can only act as a differential current injection (*I-0deg* or *I-180deg*) or voltage measurement (*V-0deg* or *V-180deg*) at one time. The acquired signals are fed into a MUX, which are further digitized using a high speed ADC (PXI-5122, 100M Samples/s with 14bit resolution). The acquired signals are stored onto a hard drive and as per requirement recalled for analysis, image reconstruction and image algorithm calibration. Due to the flexible open PXI architecture, other research groups have also opted to use it in their EIT systems (Kourunen et al., 2009; Halter et al., 2008).

Table 3.1: Sussex MK4 system specifications (Béqo et al., 2010)

| ***Parameter*** | ***Requirements*** |
|---|---|
| Frequency Bandwidth | 100Hz – 10MHz |
| Peak to Peak Current | 0.01 – 1mA |
| System Accuracy | >1% |
| SNR | >60*dB* : 1kHz – 1MHz<br>>46*dB* : 1MHz – 5MHz |
| CMRR | >46*dB SNR* : @ 1 – 5MHz |
| Channels | Max 265 (85 active) |
| Detection Method | Quadrature |
| Imaging Frame Rate | <1 frame/sec/Frequency |
| Calibration | Automatic, Software based |
| Channel Selection mode | Single End / Differential |
| Frequency Selection | Software programmable |
| Electrode Selection | Software programmable |
| ADC | 12-bit (Minimum) |
| Digital addressing protocol | 32-bit |
| Data Storage | PC hard drive |

An important characteristic of the Sussex MK4 system is the hexagonal planar electrode design plate. Electrodes are selected in a hexagonal pattern at an angle of 0º, 120º and 240º with five-electrodes in each direction in the pattern, which together define the

hexagonal measurement area. In each hexagonal measurement area, three current excitations are applied from the boundary of the hexagon on two opposite electrodes. The resulting voltage measurements are collected sequentially between adjacent electrodes within the hexagon area (Zhang et al., 2014).

In any selected hexagonal measurement area, current excitation at three angles (0º, 120º and 240º) will correspond to 12 voltage measurements between 12 adjacent pairs and therefore will have a total of 36 (3x12) independent measurements in a single hexagonal area as shown in Figure 3.1. According to the hexagonal electrode array, there are 123 drive pairs corresponding to 1416 significant independent measurements due to the electrode arrangement and distance from each other. This method ensures that the small hexagonal measurement area will scan the whole field and only the strongest measurements in the corresponding hexagon are selected which will guarantee a high SNR for the Sussex MK4 system.

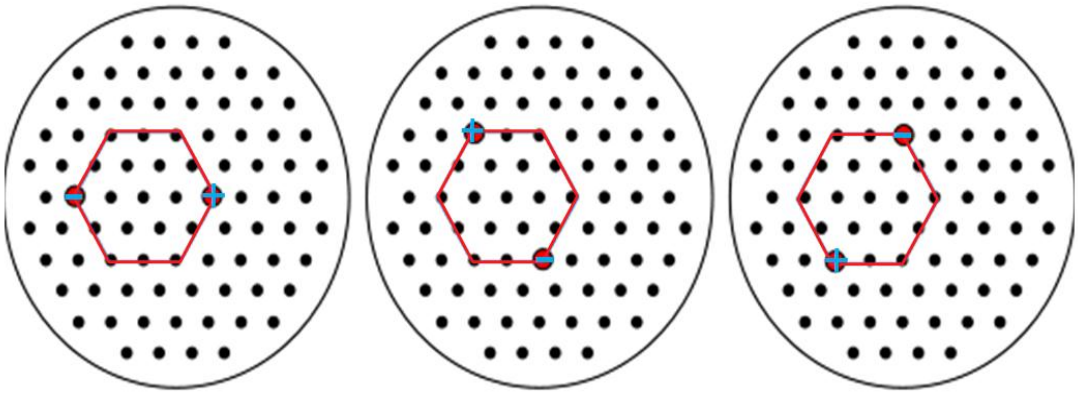


Figure 3.1: Current injection configuration in a Hexagonal electrode configuration: 0º (left), 120º (middle) and 240º (right). Dots with + & - represents the current drive pairs. Dots in the red hexagonal area represent the voltage measurement electrodes (Sze et al., 2011).

The bandwidth of the current EIM system is limited by the output capacitance of the CS and input capacitance of the multiplexer used for switching. Currently, an additional 100pF capacitance is introduced by the multiplexer. An increase in the diagnostic value can be achieved, if an excitation signal above 1MHz is applied. The current injection of the EIM system uses two single ended current sources with 180º phase shift. The transmission of analogue signals through multiplexers creates a low pass filtering effect of 100pF and limits the system bandwidth to 1.55MHz. The SNR of the latest EIM system was recorded to be 40*dB* from the front-end data acquisition hardware. Using signal processing methods, the SNR was improved to ≈56-60*dB*.

The scope of this thesis is to improve the performance of the excitation subsystem in term of system bandwidth, output impedance and SNR of the excitation subsystem. An alternative approach based on a VS excitation subsystem needs to be considered to improve the performance parameters primarily the system bandwidth. The plan was to design a prototype excitation subsystem (PCB boards) and integrate them with the EIM system to check its performance. The scope of the research was slightly changed and resulted in the performance validation of individual excitation subsystem before integration, along with some additional designed modules. The detailed change of project scope is described in a later part of the thesis.

## 3.6 Summary

This chapter described the general measurement method for any EIT system. It explains the signal application protocol on which any BIM system can be designed. The chapter described the safety limits for the excitation signal used in the impedance measurement system based on the specific frequency range. The chapter also described the benefits and limitations associated with the current and voltage source.

The chapter reported the existing prominent EIT systems developed for different bio-impedance applications and categorised based on their excitation signal generator along with the system performance as reported by the authors.

Finally, the chapter presented the development history of the Sussex EIT system. The chapter presented the architecture of Sussex MK4 system based on the NI-PXI platform, which added flexibility and fast system prototyping as compared to DSP based architecture. The chapter described the hexagonal data acquisition measurement protocol used for the planar electrode array.

Chapter 4 will address the circuit analysis of a single-ended CS based on the Howland topology along with the capacitance cancellation circuit (GIC). It will also present the simulation performance of the single-ended current source (EHCS circuit and EHCS-GIC circuit) along with circuit performance parameters.

# Chapter 4

# Development of an Optimised Current Source for an EIT System

## 4.1 Introduction

EIT is an imaging technique that reconstruct images based on the electrical conductivity/permittivity of the SUO in response to an injected electrical signal applied on the surface. EIT is a challenging problem but the technique has some advantages of: low cost, no hazard to the patient, simple application, high speed data acquisition. (Zhao 2011; Yan et al., 2006). To get a high quality, accurate and precise imaging instrument, EIT still needs to overcome some challenges. Presently, most of the work is done in developing hardware for data acquisition and image reconstruction algorithms. There are many methods to improve image quality but most important is the hardware improvement to acquire high accuracy measured data. Therefore, research needs to be focused on developing a high quality, efficient and accurate signal generator for EIT or any Bio-impedance hardware.

EIT instrumentation sensitivity varies according to the required clinical application (Boone & Holder, 1996). To find the unknown impedance two approaches can be used: either apply a voltage and measure the resulting current passing through SUO or inject current and measure the resulting voltage across SUO. In most of the BI-systems, an unknown contact impedance exists between the electrodes and the SUO. This unknown impedance effect on output will be minimum if the current source has a high output impedance (Qureshi et al., 2010). While this unknown impedance will degrade the voltage source performance which has low output impedance. Therefore, to get better accuracy of the overall EIT system it is preferable to use a current source as the excitation source of the EIT system. It is reported that spatial variation creates noise in the injected current

or applied voltage. It is shown that noise is reduced if current is injected and voltages are measured instead of applying voltage and measuring currents (Isaacson, 1986).

The accuracy of the acquired data depends on the quality of current source (CS). The most important parameter of a CS is its output impedance. This output impedance appears in parallel with the load. It is very important in any BI-system that the CS has a constant amplitude over a wide frequency range, which can be achieved by maintaining high output impedance of the source. Ideally, the injected current should be load independent, having an infinite output impedance. However, practically current sources are limited by stray capacitance and non-ideal behaviour of the used operational amplifiers, which reduces current amplitude and results in finite output impedance and introduces phase errors at higher frequencies. This problem shunts the output current away from the load as shown in Figure 4.1.

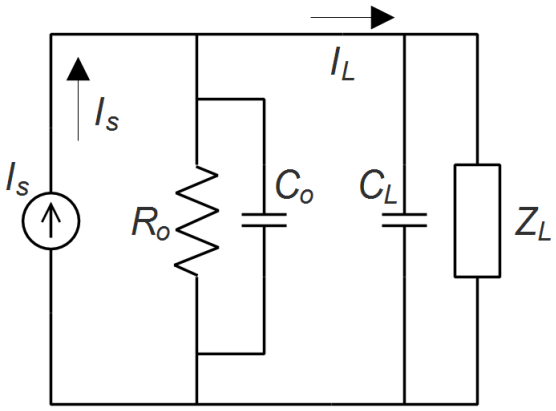



Figure 4.1: Norton equivalent of a practical current source

Therefore, the injected current *($I_L$)* and the source current *($I_S$)* varies with the value of load impedance *($Z_L$)*. The output impedance of the CS is normally defined as a parallel combination of resistance *($R_o$)* and capacitance *($C_o$)*. Due to the presence of the capacitance in the combination, the output impedance *($Z_o$)* of the CS reduces in the multi-frequency EIT (MF-EIT) as the frequency increases. To compensate the change of CS output impedance at higher frequencies, various schemes are proposed which results in complexity of the excitation subsystem of EIT hardware such that the hardware should be retuned whenever the frequency is changed. The current amplitude further decreases by the presence of stray or parasitic capacitance introduced by leads, PCB tracks etc. Electrical safety for the patient is also very important and needs to be considered. Any medical device has to follow the IEC60601-1 act. The detail of the electrical safety signal limits are described earlier in section 3.3.1 of this thesis.

This chapter presents two circuits, which can be used as a current source in an EIT system. 1st is the optimised Enhanced Howland circuit while 2nd is the optimised Enhanced Howland circuit with parallel GIC circuit to improve the capacitive loading problem of the current source circuit. Both CS circuit designs are explained and their output is compared in terms of better circuit frequency bandwidth, and output impedance based on Pspice® simulations. Both types of the CS circuits show saturated output signals at higher load due to operational amplifier limitations. To improve and overcome the problems identified in this chapter, a bootstrapping and a guard amplifier technique are introduced and are presented in the next chapter. Both CS circuits are tested with different RC loading to simulate the effect of impedances within the body. All the work presented in this chapter and next chapter was carried out by the author and two conference papers have been published (Qureshi et al., 2010).

## 4.2 Voltage Controlled Current Source

VCCS has been used in many applications such as in electrode capacitive sensors, neuron-stimulation system, EIT system, BI analysis system etc. (Bertemes-Filho et al., 2013). VCCS plays an important role in the process of imaging and final image quality (Zhangyong et al., 2010). Therefore, the design of VCCS is extremely important. An ideal VCCS requires high precision and stability. Two main approaches have been used in current source design (Seoane et al., 2008). This can be categorised in: voltage-based and current-based structures. In voltage-based structures, voltages at active nodes of the circuit are responsible for the generation of the output current. In the case of op amps, virtual ground can be an active node. While in current-based structures, an active device with intrinsic current mode operation is generally responsible for generating output current e.g. Current conveyors, Trans-conductance amplifiers etc.

A VCCS circuit that can provide a controllable current injection into a variable load impedance are mostly preferable in EIT systems. A couple of configurations of VCCS have been used in this research area. These are: a feedback inverting amplifier, transformer coupled VCCS (Li et al., 1994), positive feedback amplifier or supply sensing circuit, single and multiple op-amp circuits, Howland circuit, Double operational amplifier current source. Some (Murphy et al., 1987; Van der Walt, 1981) have also used

an oscillator in the EIT system but it has caused them frequency and amplitude stability problems (Bertemes-Filho et al., 2000).

VCCS can also be termed as a voltage-to-current (V-I) converter. Our biomedical research group at Sussex university has also used V-I converter as an excitation source for electrodes in the EIT application. The VCCS selected for current source design is the Howland current source circuit (HCSC). This HCSC is selected due to its simplicity and one of its advantages is that it doesn't necessarily require any special input buffering. There are two factors, which are considered most important while designing a current based excitation source.

1. The current source should have a large bandwidth to allow us to investigate a wide range of frequencies. This range is set to be at least 4-5MHz *(-3dB)* bandwidth and we have also tried to achieve 10MHz *(-3dB)* bandwidth.
2. High output impedance is also required for a stable current source. Ideally, it should be infinite but due to stray capacitance it degrades. Therefore, for a stable current source it should be as high as possible.

Many groups have studied CS performance at different frequency bandwidths. Alexander Ross research group at RPI USA, had also worked on it and had introduced a technique with current source to maximize its output impedance. They claim that it could provide an extremely high output impedance (Ross et al., 2003). The technique was investigated and further improvements are made to obtain a wideband and stable current source with high output voltage swings (Qureshi et al., 2010). These techniques are explained in the later part of the chapter.

The simplest V-I converter is a voltage source attached with a load resistance. In this configuration, the amount of current passed through the load is dependent on the attached load. This type of CS is not suitable for EIT/BI system because the amount of current passing through subject will change even when the electrode is attached to different part of the body. This leads a requirement for a CS to be independent of the attached load.

Many other current sources have been used in biomedical instrumentation but the Howland current source (HCS) remains the popular choice of researchers, due to its simple construction using a single op-amp and a handful of resistors (Tucker et al., 2013).

The detailed circuit analysis of HCS along with its mathematical equations for output current, output impedance and resistor ratio matching condition are presented in appendix A. The output impedance will degrade due to unmatched resistors and will be infinite with perfectly matched resistors. The common mode voltage *($V_b$)* follows the change of load impedance. When the required current is large or the attached load is large then the common mode voltage drives the op-amp into saturation mode. Therefore, the loading voltage directly limits the performance of the basic HCS circuit.

Another weakness of the HCS is its output capability. Its output node doesn't normally swing very close to the power rail. If the output node rises a lot, the op-amp's output would have to rise about twice as high, and when it is not possible some alternatives should be considered. The HCS can only swing its output node to ±5V or 6V, with a ± 15V power supply with a circuit gain of one. For a circuit gain of 10, the output node would rise to 10V with a good amplifier. However, it will be less accurate and will introduce offset and noise. The precise matching of the resistors and CMMR of the op-amp also play an important role in circuit performance and should be considered. These weaknesses can be avoided by slightly changing the HCS circuit, which results in a new topology known as the Enhanced Howland Current Source circuit.

### 4.2.1 Enhanced Howland Current Source (EHCS) Circuit

The EHCS circuit does generally solve many of the weakness of the basic HCS circuit. As the feedback resistance values decreases, the op-amp is forced to provide a higher voltage output to compensate the effect of the load resistance. This is often impossible due to the fact that the op-amp can only source voltages up to the value of its rail-to-rail power supply voltages.

The EHCS circuit improves the problem of HCS circuit by adding a resistor between the non-inverting input of the op-amp and the output of the current source. The added resistor reduces the amount of voltage the op-amp needs to provide to give correct output current (Brien, 2011; Instruments, 2008). Our research group was already working on current source based on EHCS circuit. My role was to further investigate the CS, to improve its bandwidth, output impedance and stability of the current source (Qureshi et al., 2010). The EHCS circuit configuration is given in Figure 4.2.

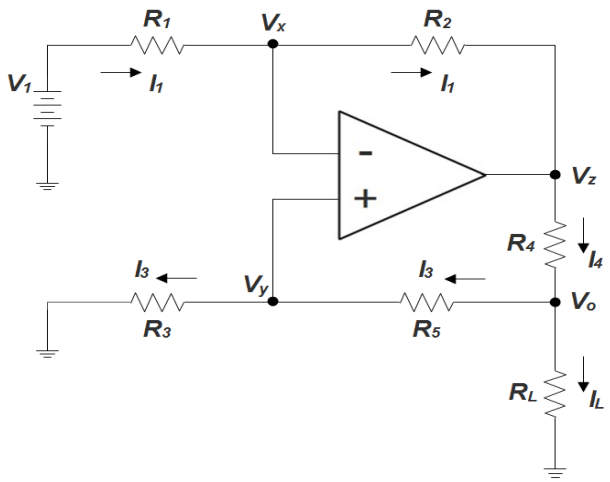



Figure 4.2: A differential VCCS using Howland circuit

Assuming that the operational amplifier is ideal then following circuit analysis can be used to find the output current expression, which is passed through the attached load. Applying the Kirchhoff current law at node $V_o$ to describe load current:

$$I_L = I_4 - I_3 \qquad \text{Eq. (4.1)}$$

The above equation shows that the load current can be found once the current passing through resistor $R_4$, $R_3$ and $R_5$ are found. The detailed mathematical expressions are given in the appendix B. After finding the respective unknown current expression, the output current passed through the load can be expressed as:

$$I_L = -\frac{V_1 R_2}{R_1 R_4} + \frac{V_o R_3}{R_4(R_3 + R_5)}\left[\frac{R_2}{R_1} - \frac{(R_4 + R_5)}{R_3}\right] \qquad \text{Eq. (4.2)}$$

If the resistors are perfectly matched and it also satisfies the ratio:

$$\frac{R_2}{R_1} = \frac{R_4 + R_5}{R_3} \qquad \text{Eq. (4.3)}$$

Then the output current equation can be expressed in a simpler form as:

$$I_L = -\frac{V_1 R_2}{R_1 R_4} \qquad \text{Eq. (4.4)}$$

It can be clearly seen in the above equation that the output current is independent of the load value and depends on the input voltage ($V_1$) and three resistors. If the conditions are satisfied, then it can form an ideal current source. Under the same circuit condition, the

input voltage ($V_1$) can be connected to the non-inverting terminal of the op-amp. The output current in this case will be:

$$I_L = \frac{V_1 R_2}{R_1 R_4} \qquad \text{Eq. (4.5)}$$

The output impedance ($Z_o$) of the EHCS circuit can be calculated by the following procedure. Assume that the input voltage ($V_1$) is short circuited i.e. $V_1 = 0$, then Eq. (4.2) can be written as:

$$I_L = \frac{V_o R_3}{R_4(R_3 + R_5)}\left[\frac{R_2}{R_1} - \frac{(R_4 + R_5)}{R_3}\right] \qquad \text{Eq. (4.6)}$$

Output impedance of any circuit can be calculated by finding the ratio between the output voltage at the load and the current passing through that load. Solving Eq. (4.6) for ratio $V_o$ / $I_L$ will give the output impedance expression for the EHCS circuit. Therefore, the output impedance of the circuit is:

$$Z_o = \frac{V_o}{I_L} = \frac{R_1 R_4 (R_3 + R_5)}{R_2 R_3 - R_1(R_4 + R_5)} \qquad \text{Eq. (4.7)}$$

It can be noticed that, $R_3$ plays an important role in increasing the output impedance of the circuit. The output current of the circuit was dependent on $R_1$, $R_2$ and $R_4$ along with input voltage. This gives us flexibility to control the output impedance of the circuit using one resistor ($R_3$). As mentioned earlier, the resistors ratio should be met in order to make EHCS circuit close to an ideal source as possible. But on the other hand, if the resistor $R_3$ is slightly altered (up to ≈1%) then there will not be a noticeable change in the output current but it will play an important part in increasing the output impedance of the circuit.

It is worth saying from the analysis that the performance of the EHCS circuit is dependent on the resistor matching network and characteristics of the op-amp used. Let's assume that the op-amp has a very large open loop gain for the intended frequency range, then the accuracy of the CS is controlled by the tolerance of the resistors used. A larger gain will definitely improve the output impedance of the CS but negative feedback of the op-amp should also be considered to avoid the amplifier's oscillation. The tolerance of the resistor network also influences the amplitude of the CS. It is more problematic for the case of multiple CS based system in which it is difficult to maintain a uniformed

amplitude in all current sources. Therefore, the CS design can be considered as trade-off between the performance of source and cost of electric components used.

## 4.3 Generalized Impedance Converter

Those active RC circuits which are designed to stimulate frequency dependent elements such as inductances for use in active filter synthesis, are known as Impedance converters. One of the popular configurations among the various configurations is the GIC. It is not only used to simulate inductances but it can also be used to synthesize frequency dependent resistances.

The GIC circuit based on two op-amps and five two-terminal elements (R's or C's) can be used to synthesize impedances to ground of the form, $Z(s) = sX$ or $Z(s) = 1/s^2D$. These impedances can be combined with other R's, C's and op-amp to generate various quadratic transfer functions. The analysis of the GIC driving point impedance is made easier if we assume that the op-amps used are ideal (Northrop, 1997).

As we know, HCS circuits apply both positive and negative feedback. Therefore, it can be said that it is based on a NIC. Normally basic op-amp's only uses negative feedback, but NIC uses both types of feedback at the same time to create a negative impedance value. The GIC is based on combining two NIC to create a circuit, which can be used as a simulated inductor. To find the equivalent impedance Z at node X, a test voltage ($V_i$) is applied and the resulting current ($I$) is measured. After finding the current, the impedance generated by the circuit can be described as $Z = V / I$. The circuit configuration of GIC is given in Figure 4.3.

The circuit analysis for the GIC circuit is also based on the assumption that the op-amp is ideal. To find the resultant current generated by the applied input voltage ($V_i$), ohm's law is applied to the node X and the resultant current $I_1$ can be expressed as:

$$I_1 = \frac{V_i - V_1}{Z_1} \qquad \text{Eq. (4.8)}$$

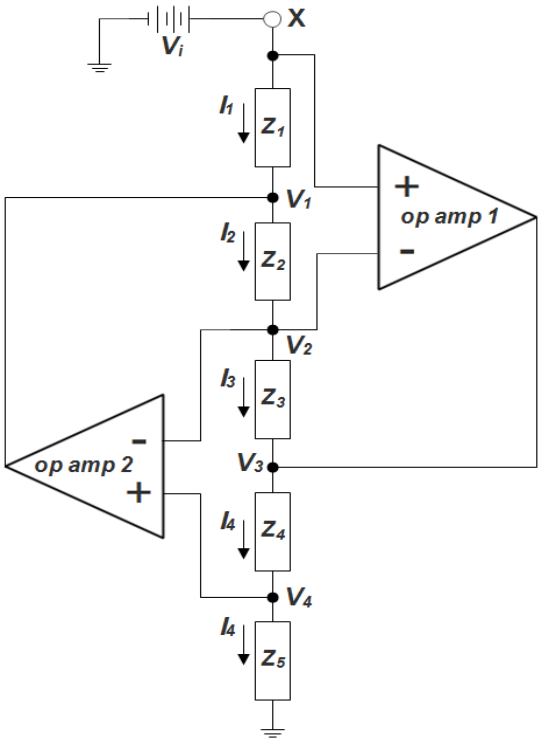



Figure 4.3: Generalized Impedance Converter circuit

It can be seen in Eq. (4.8) that the resultant current is dependent on the voltage $V_1$. Therefore, a detailed circuit analysis needs to be done to find out the unknown current and voltages involved in the GIC circuit. The detailed circuit analysis of the GIC circuit is given in appendix C. Substituting the value of $V_1$ from the analysis into Eq. (4.8) gives:

$$I_1 = \frac{V_i - \left[V_i - \frac{V_i Z_4 Z_2}{Z_3 Z_5}\right]}{Z_1} \qquad \text{Eq. (4.9)}$$

Rearranging the above equation, the input impedance of the GIC circuit can be described as,

$$Z_i = \frac{V_i}{I_1} = \frac{Z_1 Z_3 Z_5}{Z_2 Z_4} \qquad \text{Eq. (4.10)}$$

Depending upon the types of components used for $Z_1$ to $Z_5$, the circuit can be configured for various impedance types. In our case, we want the GIC circuit to act as an inductor. Therefore, our configuration will include all Z's as resistance except $Z_2$ or $Z_4$ as capacitance. Let's assume $Z_4$ is a capacitor.

$$Z_4 = \frac{1}{j\omega C_4} \qquad \text{Eq. (4.11)}$$

The impedance equation of the GIC circuit will become:

$$Z_i = \frac{j\omega C_4 \, Z_1 Z_3 Z_5}{Z_2} \qquad \text{Eq. (4.12)}$$

If all other impedances are resistances then the inductance value can be calculated from the following equation:

$$L = \frac{C_4 R_1 R_3 R_5}{R_2} \qquad \text{Eq. (4.13)}$$

## 4.4 Circuit Simulation Results

The analysis in section 4.2 is based on an ideal amplifier assumption. However, practically the operational amplifier is far away from ideal behaviour especially at higher frequencies. The gain bandwidth product (GBP) or unit gain bandwidth is considered as a design reference, which is provided in the device datasheet. It indicates that the op-amp doesn't provide a high open loop gain with increase in the phase shift, if the current working frequency reaches closer to the higher end of the GBP. Sometimes the bandwidth of the device is given by compensated gain. This allows the user to design the circuit using a specific device without any compensation circuit, which is used for circuit stability and accuracy. After using this compensation circuit, the bandwidth is much lesser than the normal bandwidth of the device. Care must be taken when an uncompensated op-amp is used in the circuit design because this can lead to a totally different GBP as compared to the one in the device data sheet. It has seen that most of the times it won't work properly without compensation circuitry. This compensation circuit cancels oscillation and many unwanted behaviour of the op-amp. On the other hand, it decreases the circuit working bandwidth. Further, different power output will also affect the bandwidth parameter. For high speed applications, generally bipolar transistor op-amps have higher bias currents. Some op-amps have asymmetrical output capability through which it can sink more current than they can source or vice versa. Therefore, symmetrical structure amplifiers are a better choice.

Having considered many market available op-amps, two devices were chosen to design the CS. These devices were THS4304 and AD812. Initially, the CS was designed using THS4304 but due to some performance problems this had to be changed to AD812. The problems are described in detail in the later section with the help of simulation results.

The THS4304 was the device selected from Texas instruments. It is a wideband, voltage feedback op-amp used in high speed Analog processing applications with a single supply. The THS4304 uses a traditional voltage feedback topology that provides the benefits of balanced inputs, low offset voltage/current/drift, high common mode and power supply rejection ratio. Alternatively, this device can be run on a dual supply with a maximum supply of ±2.5V. It can give a GBP of ≈870MHz for gain >10. Low voltage noise, high bandwidth and slew rate make this amplifier suitable for radio frequency applications and can be of benefit in making a CS for any BI system (Datasheet THS4304, 2004).

The commercial available THS4304 PSPICE® model was used to analyse the performance of analogue circuits and systems. As per manufacturer's information, this model has considered parasitic capacitance and inductance, which can affect the performance of the circuit. Simulation was performed to demonstrate the performance of the op-amp in the CS circuit over the working frequency bandwidth with constant current amplitude. Two different circuits were simulated and their results were compared: EHCS and EHCS circuit in series with a GIC (EHCS-GIC). The circuits were designed using Orcad-Pspice® simulator software. Both circuits were optimised till the best current stability has achieved. The load current was measured and the output impedance produced by both circuits were calculated and compared.

Previously, our group has used the OPA620 op-amp to design the CS for the EIT system. This op-amp was preferred due to its low noise but unfortunately, this op-amp was discontinued from manufacturer. Furthermore, different op-amps (like OPA656, MAX4223 etc.) were used to design the CS but due to different performance limitations they were not able to give required performance. Therefore, further investigation was done to build an optimised and stable CS for an EIT system. A few multiplexers are required to propagate the voltage signal from an external source into the VCCS and transmit its output to the attached load. These multiplexers have a built-in capacitance that varies with different types of multiplexers. Therefore, the circuits were tested at different capacitance loading in parallel with resistive loading. These capacitance loadings were 10pF, 30pF, 50pF and 100pF. Both circuits were tested with parallel RC loading combinations and the results were reported.

The output impedance of the circuit was calculated using following procedure. It is known that any circuit can be represented by its Norton's equivalent. We assume that the VCCS

circuit can also be converted to its Norton equivalent and represented by its equivalent Norton current in parallel with its Norton resistance. In this case, the equivalent Norton current source will be the total theoretical current or ideal current generated and Norton resistance will be referred to as the output impedance of the CS shown in Figure 4.4. To realize ideal load current, either it was assumed that ≈1mA will pass through load when a 1V input signal is applied as per Eq. (4.5) or a small load (i.e. $R_L$ = 0.1Ω) was attached to the circuit and the amount of current passing through $R_L$ was measured.

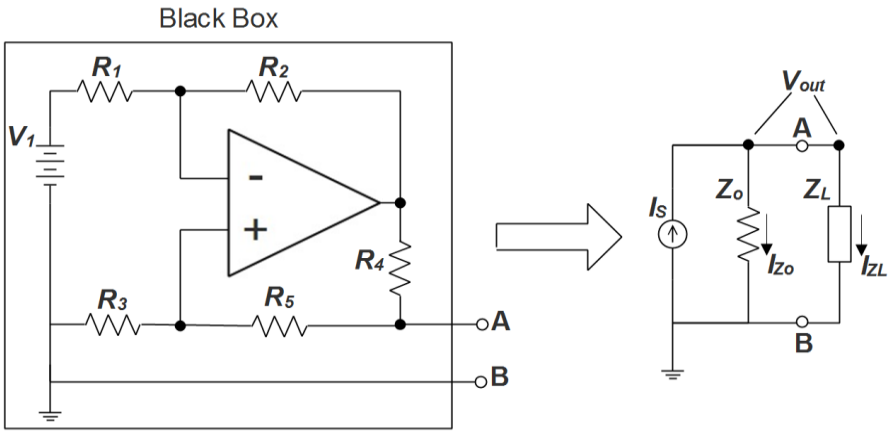



Figure 4.4: A VCCS and its Norton equivalent circuit

It is assumed that this will be the total amount of current our source can generate and is represented as $I_S$. The output impedance of the source can be calculated as:

$$Z_o = \frac{V_{out}}{I_{Zo}} \qquad \text{Eq. (4.14)}$$

It can be seen from the Figure 4.4 that the voltage drops across both the load *($Z_L$)* and output resistance *(Zo)* is the same and the current passing through each component can be found be using Kirchhoff's current law. Therefore, it can be written as:

$$V_{out} = Z_L I_{ZL} \qquad \text{Eq. (4.15)}$$

$$I_{Zo} = I_S - I_{ZL} \qquad \text{Eq. (4.16)}$$

Substituting Eq. (4.15) & Eq. (4.16) into Eq. (4.14),

$$Z_o = \frac{Z_L I_{ZL}}{I_S - I_{ZL}} \qquad \text{Eq. (4.17)}$$

The -3dB frequency bandwidth of both circuits were calculated and mentioned in the later part of the chapter. The output impedance was also calculated by the above procedure using Eq. (4.17).

## 4.4.1 EHCS Circuit Performance

Figure 4.5 shows the circuit simulation setup along with passive components value. The power rails for the op-amp were set to ±2.5V DC source without any external noise included. The resistor values satisfy the ratio condition described earlier. An extra 0.3pF capacitance is added to the circuit simulation to model PCB pads capacitance.

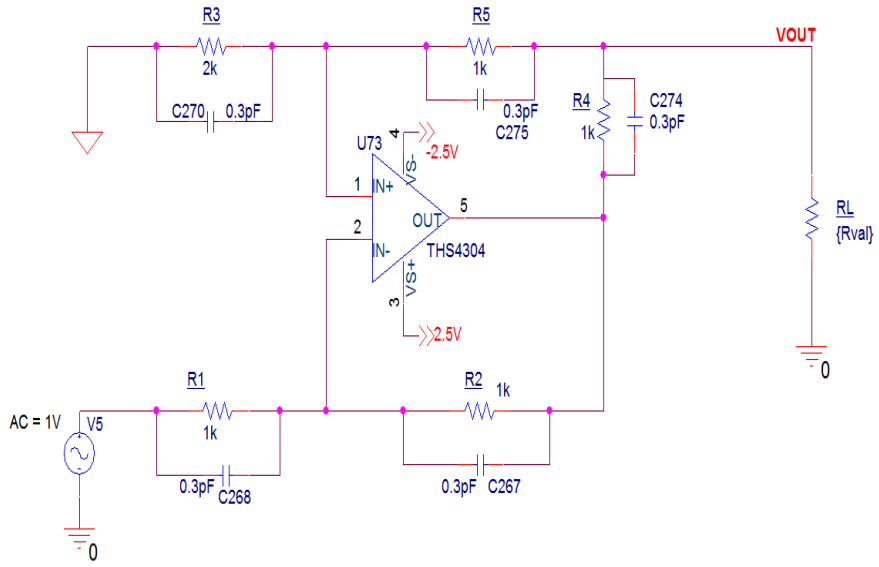



Figure 4.5: EHCS circuit simulation setup

### *4.4.1.1 AC Response of the EHCS Circuit*

The circuit shown in Figure 4.5 was operated using an AC sweep analysis with the variable load resistance from 5kΩ to 30kΩ with a step size of 5kΩ. The AC response showed that the EHCS circuit produced some output capacitance and resulted in amplitude reduction of the output current after >1MHz and dropped to very low amplitude until 10MHz. A slight difference in the amplitude of the output current was also observed with variable loads, which in turn will reduce the output impedance of the EHCS circuit. The finite open-loop gain of the op-amp used can be another reason for the amplitude reduction.

The output capacitance produced by the EHCS circuit was measured. To do this, the non-ideal op-amp in Figure 4.5 was replaced with an ideal op-amp and the load value was fixed. An additional capacitor is added in parallel with load in the circuit that has an ideal op-amp. The AC response was observed for both circuits under the same conditions and the output capacitance of the EHCS circuit was determined by comparing the load current curves. To minimise the difference in the amplitude of the load current or in other words

to improve the output impedance of the circuit, the value of $R_3$ in Figure 4.5 was slightly adjusted. The adjustment of the resistor value is dependent on the open-loop gain of the op-amp and is multiplied by its closed loop gain. The same circuit setup (Figure 4.5) was used apart from the resistor *($R_3$)*, which allows some adjustment in improving the circuit performance. The simulation results are shown in Figure 4.6, which plots the output load current versus corresponding frequency sweep.

It was observed in Figure 4.6, that the difference between the amplitude of load current was reduced, which in turn had improved the output impedance of the circuit. The output capacitance of the EHCS circuit was found to be approximately 1.9-1.7pF for load ranges between 5kΩ to 30kΩ. The value of $R_3$ was triggered to 2004Ω so that the difference in amplitude of the load current was reduced as much as possible.

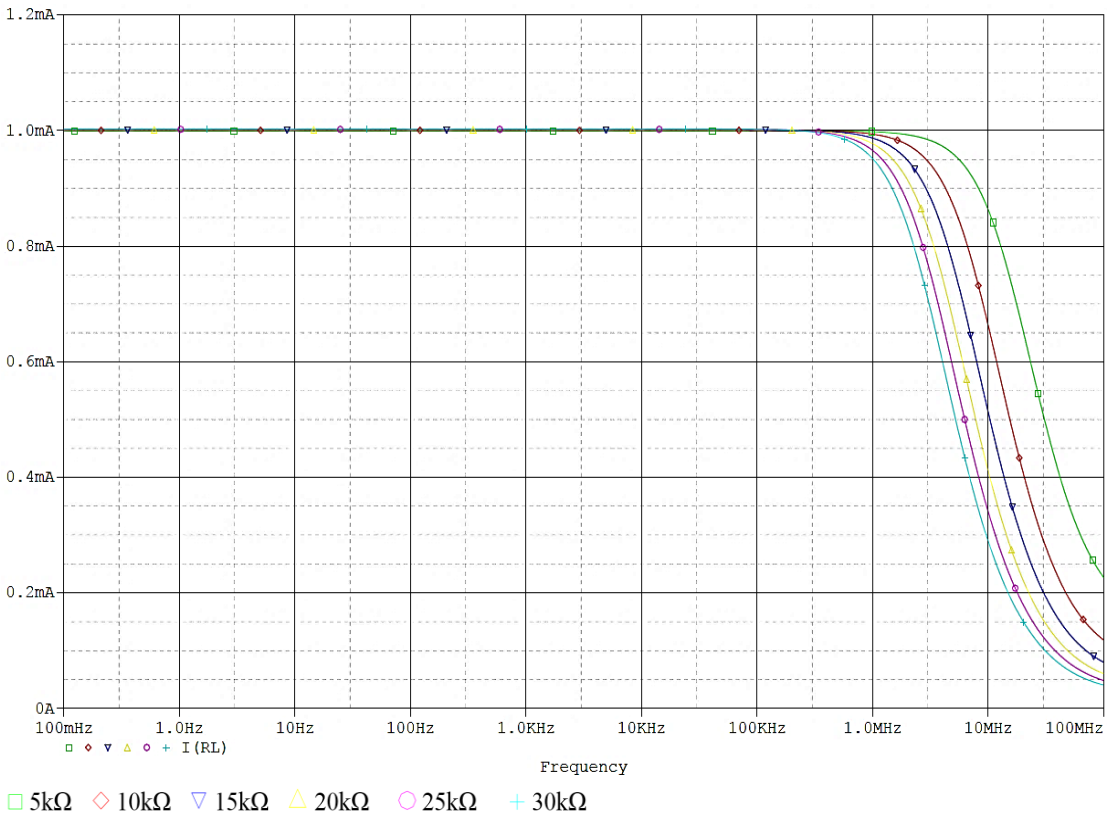



Figure 4.6: EHCS-circuit AC response with amplitude adjustment and without loading capacitance

As mentioned earlier, the external voltage signal was propagated through the VCCS to the attached load via two cascaded multiplexers. If their capacitances are considered then the frequency bandwidth of the EHCS circuit will be further reduced. Reduction in the frequency bandwidth of the circuit was observed with a loading capacitance of 10pF, 30pF, 50pF and 100pF.

### *4.4.1.2 Transient Response of the EHCS Circuit*

The AC response of the circuit shown in Figure 4.5 shows good behaviour with a reasonable amplitude of the load current, which gives an acceptable value of output impedance. However, this AC response doesn't consider any nonlinearities in the Pspice® model of the components without considering the actual response of the op-amp power supplies and will just give an overall performance of the circuit. In order to test the circuit, a realistic working transient response of the circuit should also be evaluated. If both responses give an acceptable level of output then it can be assumed that the practical results will be similar to the simulated results.

Therefore, the EHCS circuit transient response was setup. The simulation was applied with a signal having: 100kHz frequency, 1V amplitude and 0V offset voltage. The tested load values were: 5kΩ and 10kΩ. The simulation was setup to run for 30µs with a maximum step size of 0.001µs. The amplitude of the load current was measured and compared with the AC response of the circuit. The transient response of the circuit is shown in Figure 4.7, which shows the amplitude of the load current at respective frequency.

The result showed that the amplitude of load current of the EHCS circuit was saturated and a small amplitude current was passed through the load (i.e. few µA's). The reason is that the op-amp used in the EHCS circuit has a supply voltage of ±2.5V. When the output of the op-amp reaches near to the power supply rails then its output starts clipping and as a result the signal amplitude decreases and doesn't deliver the expected amount of current. The circuit gave the same behaviour at the other tested frequencies (i.e. 10kHz, 1MHz and 10MHz). As long as the load remains small and the output voltage of the op-amp remains less than the power rails supply, then the circuit will deliver the expected amount of current. It was noticed that if the load remains <300Ω, then EHCS circuit performed as expected (i.e. 1mA).

A similar behaviour of the EHCS circuit was observed in the presence of loading capacitance. It can be concluded from the above results that some modifications are needed to operate the EHCS circuit as per our requirement. These changes are described in detail in the chapter 5. Due to the finite open loop gain of the non-ideal op-amp, its frequency bandwidth is affected and reduces the overall frequency bandwidth of the circuit.

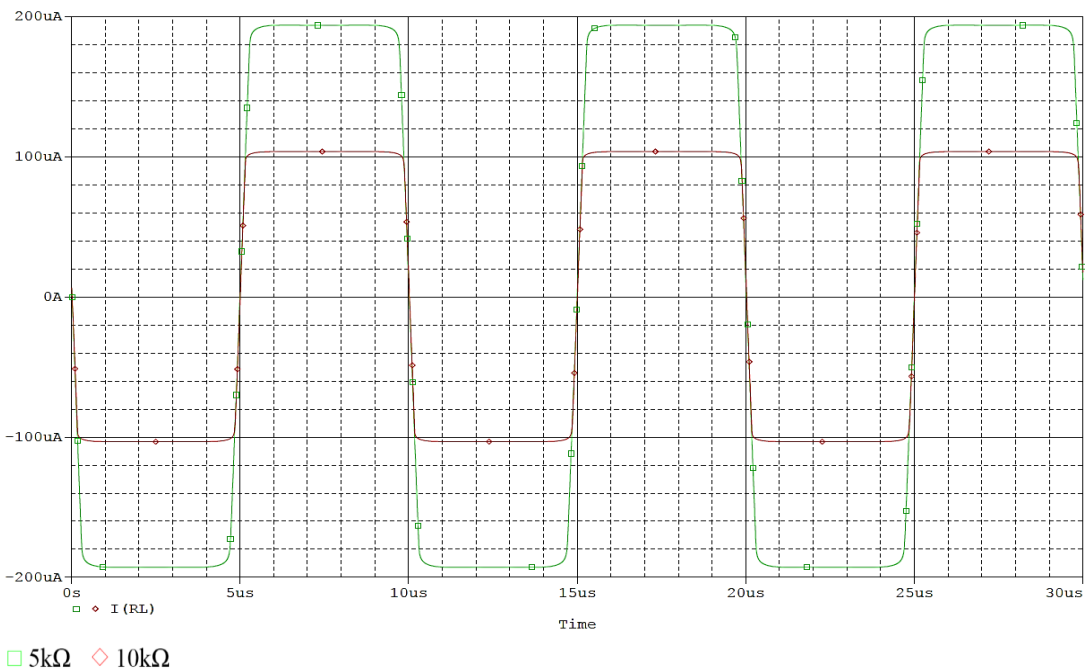



Figure 4.7: EHCS-circuit transient response at 100kHz without loading capacitance

### *4.4.1.3 Bandwidth and Output Impedance of the EHCS Circuit*

The frequency bandwidth and output impedance of the EHCS circuit was recorded. Due to the saturated transient response of the circuit, the detailed performance parameters were not presented. However, the presented result will give an overview of the circuit performance based on its AC response.

The frequency bandwidth of the circuit was observed at the -3dB point (referred to the frequency at which the amplitude of the signal drops below 70.71% of the initial amplitude). The bandwidth of the EHCS circuit was effected by the loading capacitance involved in the circuit in addition to the non-linearities of the op-amp. The frequency bandwidth of the EHCS was found to be between 2.7MHz to 52kHz for different RC loading combination (R= 5kΩ to 30kΩ, ΔR=5kΩ and C=10pF, 30pF, 50pF and 100pF). The results show that the bandwidth of the circuit dropped with an increase in the loading capacitance. The overall bandwidth of the circuit can be improved with the minimisation of the loading capacitance.

The output impedance of the EHCS circuit was calculated using Eq. (4.17). It was observed that without additional capacitance loading, the maximum output impedance achieved was approximately between 33MΩ to 12kΩ across a frequency range between 100Hz – 10MHz for 5kΩ to 30kΩ resistive loading. A stable output impedance response

was observed for the frequency range between 100Hz – 100kHz. For >100kHz, it started decreasing and reached a low amplitude up to 10MHz. A similar response was observed with an increase in the resistive loading value. In the presence of loading capacitance, the output impedance was stable for wide frequency range until the loading capacitance remained small. A reduction was observed in the stable frequency range band from 0.1–100kHz to 0.1-1kHz with an increase in the loading capacitance. The output impedance was slightly increased at 10kHz and starts decreasing above this frequency and reaches a low value at 10MHz when the load value was >10kΩ to 30kΩ. It was observed that with the additional capacitance loading, the maximum output impedance was approximately between 33MΩ to 157Ω across a frequency range between 100Hz – 10MHz for different RC loading combination (R= 5kΩ to 30kΩ, ΔR=5kΩ and C=10pF, 30pF, 50pF and 100pF).

### 4.4.2 EHCS with GIC Circuit Performance

This circuit was designed by an American group with the intention to create a high output impedance current source (Ross et al., 2003). Further investigation was performed to check the performance of the circuit and feasibility of its usage in our research group EIT device at the University of Sussex (Qureshi et al., 2010). Section 4.4.1 shows the performance of the EHCS circuit without the addition of the compensation circuit (GIC) for loading capacitance. Results from the section 4.4.1 show that the additional loading capacitance significantly affects the output impedance and frequency bandwidth of the CS. Therefore, compensation circuit needs to be considered to minimise the effect of this extra loading capacitance. Simulation setup was performed for EHCS-GIC circuit as shown in Figure 4.8 using the same circuit configuration described in section 4.4.1. The resistor network of the EHCS part of the circuitry satisfies the resistor matching condition (Gain = one) described earlier. One passive component in the EHCS part and three passive components in the GIC part were kept variable in the current source. These components were tuned for the target frequency range and optimised until the maximum possible simulated performance was achieved from the circuitry.

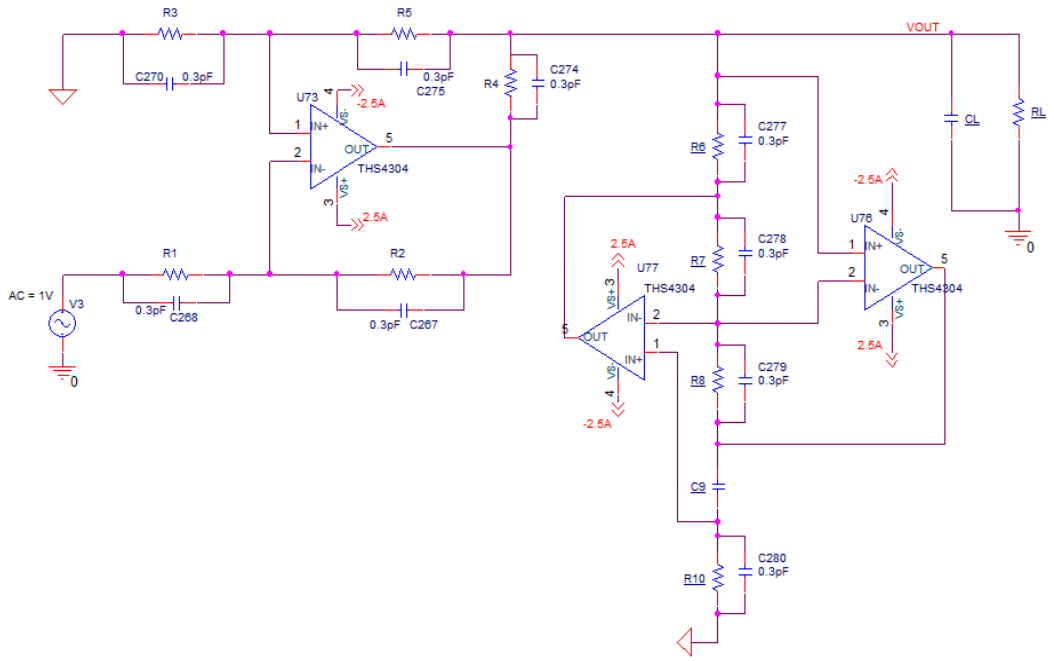



Figure 4.8: EHCS-GIC circuit simulation setup

### *4.4.2.1 AC Response of the EHCS-GIC Circuit*

The circuit shown in Figure 4.8 was operated with an AC sweep analysis with variable load resistance *($R_L$)* as described in section 4.4.1. The resistor ratio (gain) was exactly matched as per Eq. 4.3. As mentioned earlier, the EHCS circuit was affected by output capacitance that resulted in a frequency bandwidth drop-off at >1MHz frequency along with a steady response at lower frequencies (i.e. ≈400kHz). A particular resistor *($R_3$)* needs to be adjusted to improve the amplitude of load current, which in turn will improve the output impedance of the source. The behaviour of the EHCS-GIC was further investigated for the case of capacitive loading along with circuit optimisation to overcome the effect of capacitance and output impedance enhancement. Efforts were made to reduce the effect of extra capacitance as much as possible.

Possible loading capacitances considered were: 10pF, 30pF, 50pF and 100pF. The circuit shown in Figure 4.8 was operated with an AC sweep analysis in the presence of loading capacitance. The simulation setup was still the same apart from: adjustment of resistor ($R_3$) to improve the circuit's performance and the fact that EHCS-GIC circuit setting was changed for different set of frequencies to get the optimum source performance at a specific frequency or small frequency bands. The frequencies were divided into groups and efforts were made to cover as many frequencies as possible in a group. If a large number of frequencies can be covered in a group then it can be helpful to minimise the

tuning of the EHCS-GIC circuitry. The EHCS-GIC circuit will still give a peak value for the load current amplitude in such groups but care was taken to ensure that all other frequencies have an acceptable amplitude of load current in addition to the design frequency. This response clearly shows some improvement in the load current amplitude. In the first group, two frequencies i.e. 100Hz & 1kHz were covered. Other groups covered 10kHz, 100kHz, 1MHz and 10MHz frequencies. The simulation results for few tuned circuit configuration, are shown in the Figure 4.9 to Figure 4.11 that describes the load current against its tuned frequency sweep.

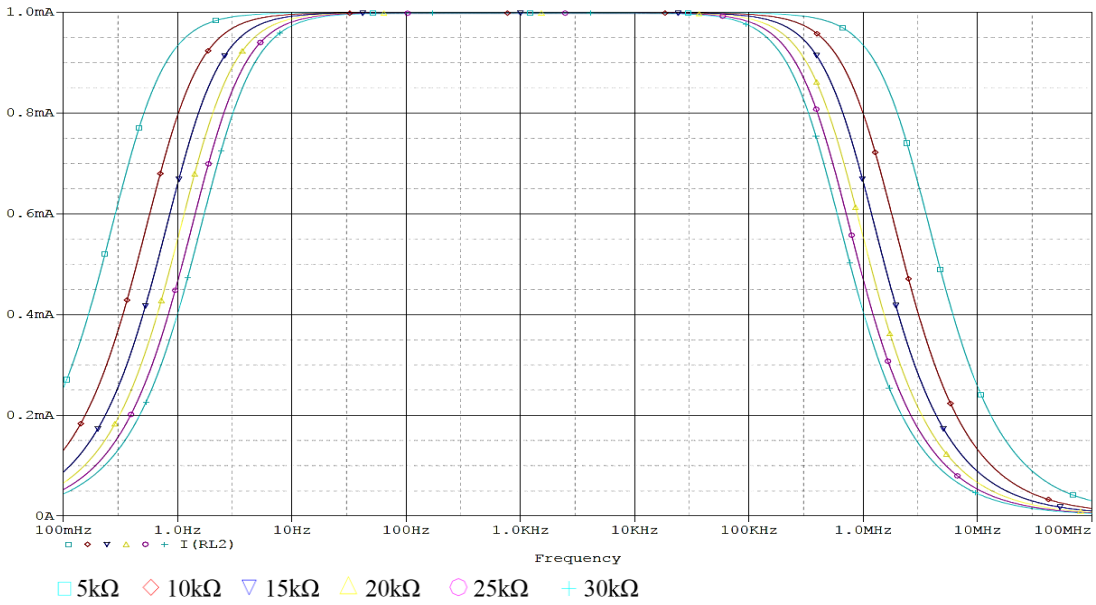



Figure 4.9: EHCS-GIC circuit Improved AC response for 100Hz –1kHz with 10pF loading capacitance

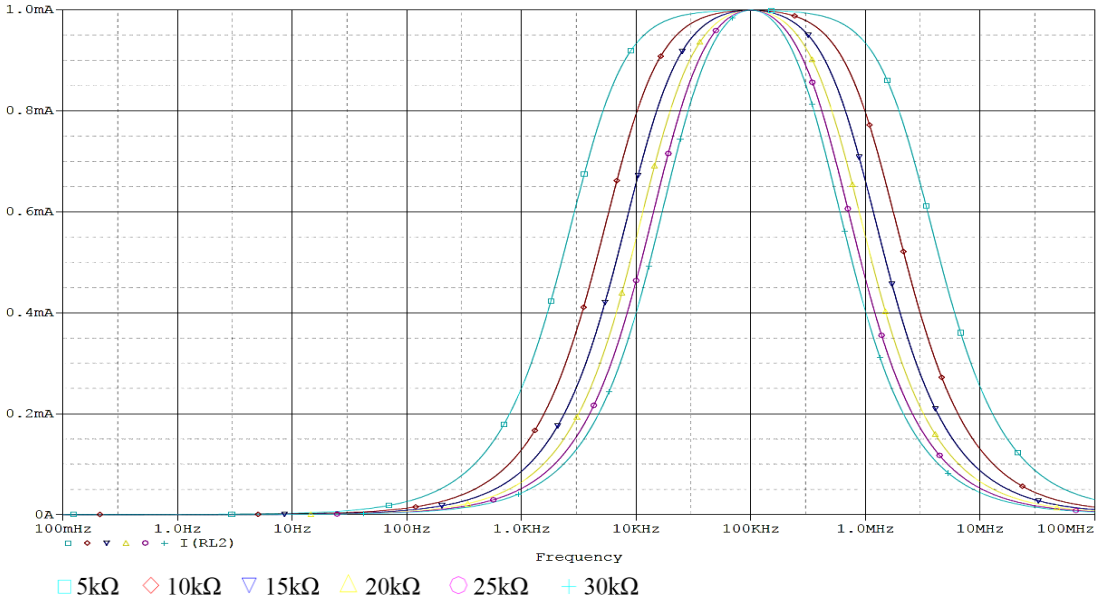



Figure 4.10: EHCS-GIC circuit Improved AC response for 100kHz with 10pF loading capacitance

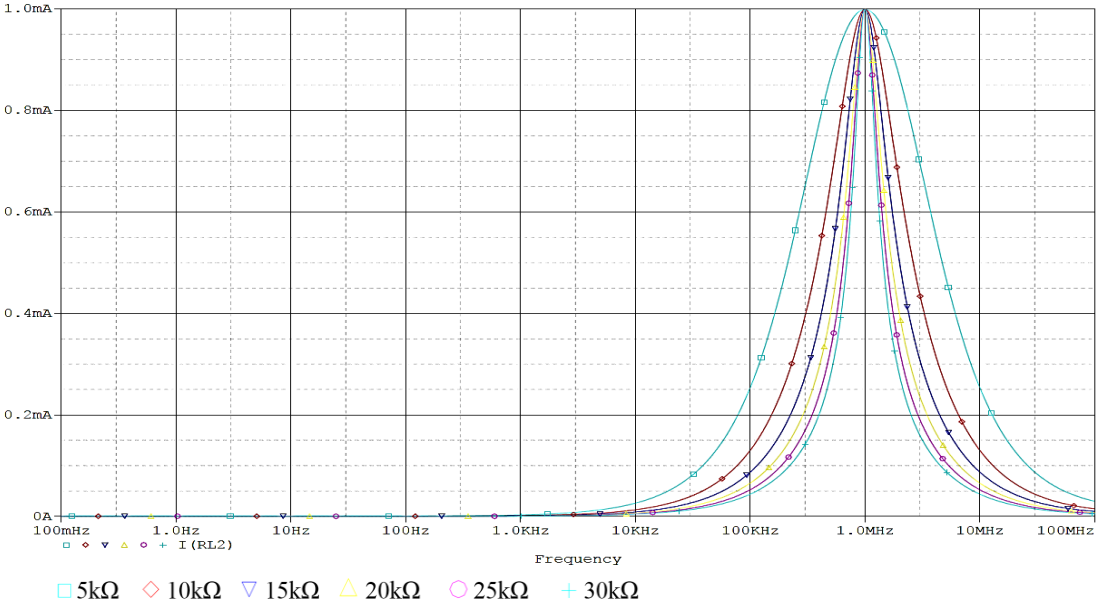



Figure 4.11: EHCS-GIC circuit Improved AC response for 1MHz with 10pF loading capacitance

The AC response of the EHCS-GIC circuit shown in Figure 4.8 with specific loading capacitance shows a reasonable performance with an acceptable load current amplitude having an overall narrow bandwidth for the circuit at that particular resistor network setting. This circuit configuration gives a better performance in term of the source output impedance but over a limited bandwidth and can be considered as specific to a single frequency or limited frequency band. Therefore, the circuit was tuned with different resistor settings to cover the maximum number of frequencies. This alteration increased the amount of work but the main focus was to cover as many frequencies as possible with an acceptable amplitude of the load current.

The peak amplitude response of the EHCS-GIC circuit was observed for variable resistive and 10pF capacitive loading over different frequency bands as: 1) A peak response at ≈977Hz for the frequency band between 100Hz to 1kHz and was stable for frequencies between 155Hz to 6kHz, 2) peak response at ≈9.8kHz for 10kHz frequency band and was stable for frequencies till ≈12kHz and, 3) peak response is limited to a specific single frequency for >10kHz (i.e. 100kHz, 1MHz and 10MHz). Similar behaviour was expected and observed for other RC loading combinations with a reduced frequency bandwidth with the increase in loading capacitance. Hence, it was concluded that capacitance does affect the performance of the circuit and we can overcome its effect to some extent if its value is known.

### 4.4.2.2 Transient Response of the EHCS-GIC Circuit

The transient response of the EHCS-GIC circuit was setup at different frequencies and tested with a variable resistive (5kΩ and 10kΩ) and fixed capacitive (10pF) loading. The simulation was demonstrated with a 10kHz frequency signal having 1V amplitude and 0V offset voltage. The transient response of the circuit is shown in Figure 4.12 , which plots the load current amplitude at respective frequency.

The transient response of the circuit showed a saturated output because the amplitude of the output signal exceeded its supplied power rails. A similar kind of behaviour was noted for other frequencies (i.e. 100kHz, 1MHz and 10MHz) with the above mentioned RC loading. Some improvements need to be made to reduce the signal clipping in the circuit to operate the EHCS-GIC circuit as per our requirement otherwise the circuit performance will be limited to drive a smaller load value so that the op-amp outputs don't saturate. These improvements are described in detail in the forthcoming chapter 5 of the thesis.

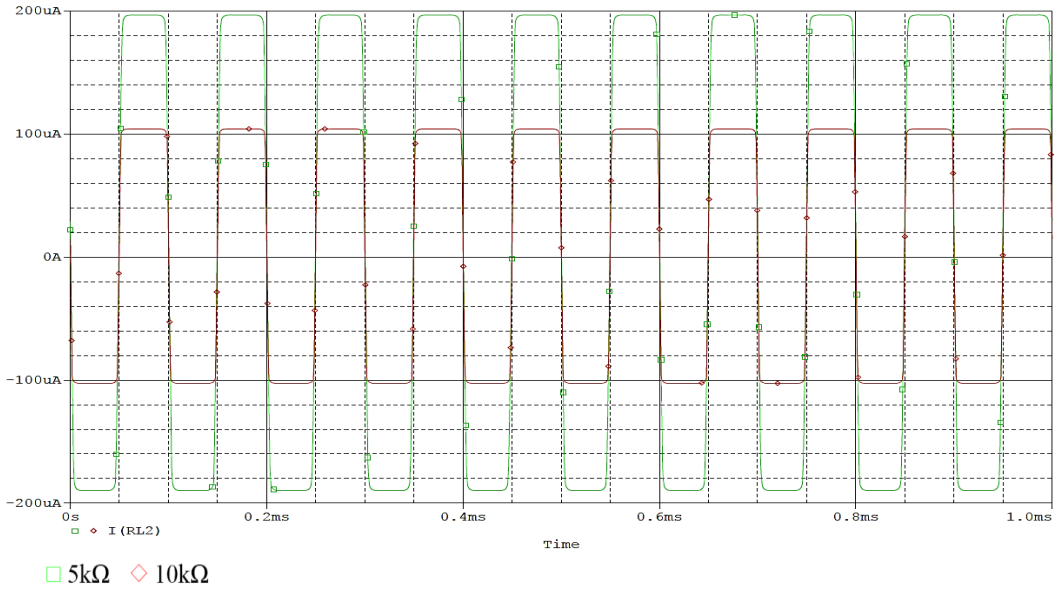



Figure 4.12: EHCS-GIC circuit transient response at 10kHz with loading capacitance

### 4.4.2.3 Bandwidth and Output Impedance of EHCS-GIC Circuit

The frequency bandwidth and output impedance of the EHCS-GIC circuit was also recorded. Due to saturated circuit output, the detailed performance for this circuit is not presented in this section.

The frequency bandwidth of the EHCS-GIC circuit was also affected due to the loading capacitance within the circuit. According to the AC response of the EHCS-GIC circuit, the circuit load current gives a peak amplitude response over a limited frequency bandwidth and was divided into a different set of tuneable settings to cover our frequency requirements. As long as the loading capacitance was smaller, the output peak amplitude achieved with the EHCS-GIC circuit can cover a wide band of frequencies but only at low frequencies. As the loading capacitance increases, the current peak amplitude reduced to a limited frequency bandwidth. The circuit was tuned to cover 100Hz to 1kHz, 10kHz, 100kHz, 1MHz and 10MHz frequency band. Due to the cumulative amplitude peak response for each tuned frequency, the overall frequency bandwidth of the circuit is not affected for a specific RC loading combination. The overall frequency bandwidth *(-3dB)* of the EHCS-GIC (for 100Hz to 1MHz tuned circuit) was found to be between 2.65MHz to 53kHz for different RC loading combinations (R= 5kΩ to 30kΩ, ΔR=5kΩ and C=10pF, 30pF, 50pF and 100pF). The frequency bandwidth of EHCS-GIC (for 10MHz tuned circuit) was found to be between 3.67MHz to 567kHz. At 10MHz tuned configuration, the bandwidth is high due to low amplitude drop over wide frequency range.

The output impedance of the EHCS-GIC circuit was calculated using Eq. 4.17 for the same tuned frequencies described earlier with a peak amplitude in respective frequency band. It was observed that without the loading capacitance, the maximum output impedance achieved by the circuit was between 63MΩ to 1.3MΩ across a frequency range between 100Hz – 10MHz for 5kΩ to 30kΩ resistive loading. A stable response was observed for frequency until ≤1MHz. For >1MHz frequencies, the output impedance response started decreasing and reached a low value until 10MHz. A similar response was observed with an increase in the resistive loading. A stable response of the output impedance was observed for a wide frequency range until the loading capacitance remain small. A reduction was observed in the stable frequency range band from 100Hz – 1MHz to 0.1-10kHz with an increase in the loading capacitance. The output impedance started decreasing above this frequency and reaches a low value up to 10MHz for all tested RC loading combination. It was observed that with the additional capacitance loading, the maximum output impedance was approximately between 56MΩ to 3kΩ across a frequency range between 100Hz – 10MHz for different RC loading combination (R= 5kΩ to 30kΩ, ΔR=5kΩ and C=10pF, 30pF, 50pF and 100pF). Graphical representation of the

output impedance at a particular load value is given in Figure 4.13 with different loading capacitance.

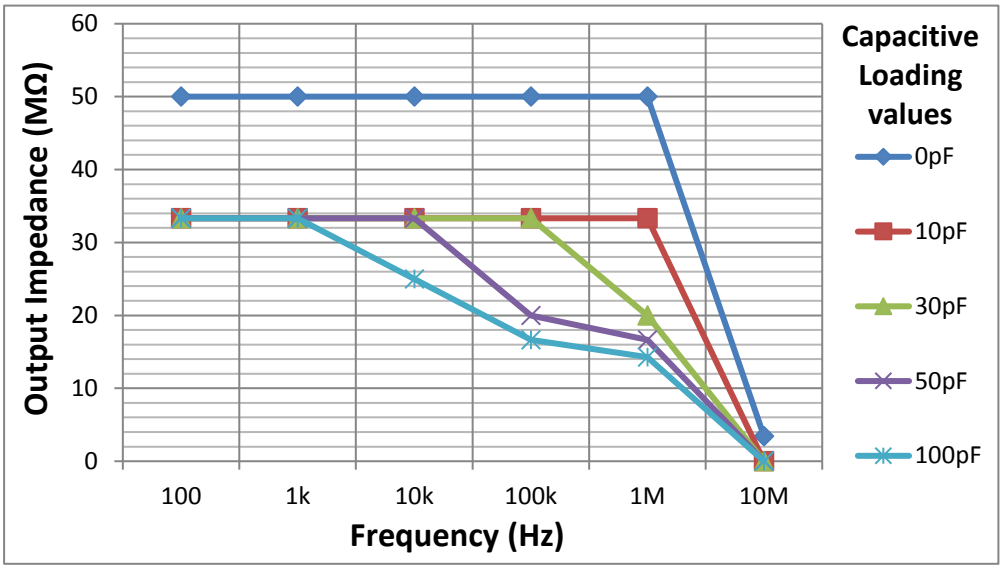



Figure 4.13: EHCS-GIC circuit output impedance with 10kΩ resistive loading

## 4.5 Summary

In this chapter, two VCCS circuits are presented, which can be used as an excitation source in any EIT or bio-impedance system. The VCCS sources were simulated using high speed op-amp and the results give strong support to the mathematical analysis and came to the following conclusions.

The resistors tolerance play an important role in the performance of any circuit. Both source circuits are sensitive in resistor network matching. If high tolerance resistors are used in the circuit then we came across difficulty in resistors matching. Therefore, using low tolerance resistors can be an easy solution in circuit implementation. It was decided to use 1% tolerance resistors in the circuit implementation.

The simulation results showed that the performance of the circuits were limited to low frequencies due to the op-amp characteristics and unwanted capacitance caused by any medium (i.e. op-amp, passive devices, multiplexers, cables). At high frequency, finite open loop gain of the op-amp limits its performance. To improve the output impedance of the source, some compensation needs to be done for this limited gain effect and unwanted capacitance. These circuits can give a better performance with a high GBP op-amp.

The result showed that the CS based on the EHCS circuit can be used as a stable multi frequency source over a wide frequency range with high speed op-amps. This circuit can be used in the system, which requires low frequency input (i.e. few kHz). At higher frequency, its performance degrades due to its output capacitance and additional loading capacitance involved in the circuit. Saturated op-amp output was also observed for the case of a higher driven load. A parallel combination of the EHCS and the GIC circuit was used to simulate a constant CS, to overcome the loading capacitance problem. A stable output was observed with the parallel combination but was limited to a narrow frequency bandwidth. The EIT system mostly depends on source stability over various frequencies but the EHCS-GIC circuit does not provide a satisfactory wide bandwidth. However, this combination did produce good quality results at single frequency or over a small frequency band. The combination was also effected due to its op-amp saturation problem for a higher loading voltage condition. After resolving the op-amp saturation problem, it can be concluded that this combination can be useful for the system, which requires single frequency input or a system, which does not require instant input frequency change. The identified issues must be considered to develop a stable and reliable CS. The solution to these problems are discussed in the following chapter.

Chapter 5 will address the solution for the limitations found in EHCS and EHCS-GIC based current source in this chapter. A technique called bootstrapping is explored, which involves driving the power rails of the op-amp at high voltage and is applied to both the circuits. A differential current source based on the EHCS-GIC is also described in the next chapter.

# Chapter 5

## Improvement in Optimised Current Source for an EIT System

## 5.1 Introduction

It was described in chapter 4 that for exciting tissues over a wide frequency bandwidth, the CS based on Howland circuits have been very widely used as a powerful VCCS circuit. When a CS based on a Howland architecture is designed, the selected components should be able to deliver the desired characteristics. It was concluded in chapter 4 that the op-amp limitations and resistor tolerances can cause undesired behaviours in the circuit performance. The simulation results obtained in chapter 4 also show that both output current and impedance are very sensitive to the resistors variations. In order to get higher output impedances, high op-amp gains and a precise resistor network are required. The op-amp open-loop gain increases with increasing sensitivity of the output impedance.

It was also observed that the CS based on the Howland architecture was effected by a loading voltage problem. A larger loading voltage will cause signal saturation in the op-amp output when it reaches near the op-amp rail voltage. Hence, the circuit was limited to drive a very small load. This also brings to our attention that the high speed op-amp with a low supply voltage will not be helpful to design a CS and can't give a high output voltage swing. This was noticed in the chapter 4 simulation results, which uses a THS4304 (±2.5V) op-amp. One solution to resolve this problem can be to use a high supply voltage op-amp. Although this solution will help to some extent, it will limit the circuit performance as soon as the output signal reaches close to the op-amp supply voltage. Therefore, it was decided to still use a high voltage supply op-amp but with some additional circuitry which can boost the op-amp output swing.

This chapter discusses the same circuits described in chapter 4, which can be used as a current source in any EIT system. A bootstrapping technique is described. Both the CS circuits (EHCS and EHCS-GIC) are bootstrapped to overcome the clipping signals problem and to achieve a wide output voltage swing with a larger driven load. The bootstrapped CS circuits design are explained and there output is compared in terms of better circuit bandwidth, and output impedance based on a Pspice® simulation. The guard amplifier technique is also introduced and explained. This technique is used to cancel the known capacitance by switching the rail voltages up and down for a particular component. This technique is specifically introduced to cancel the known capacitance of the multiplexer's used in our excitation subsystem.

This chapter also discusses the bipolar-CS design based on the EHCS-GIC circuit and simulation results are shown to compare its performance. A discrete component CS having low output capacitance and stable amplitude output current at high frequency (i.e. 10MHz) is also presented. This work takes into account the influence of different design parameters in the CS circuit over the frequency range of 0.0001-10MHz. This will improve the implementation of practical current sources used in electrical BI systems.

## 5.2 Bootstrapping Technique

It is desirable in many applications to have an output of an amplifier to swing close to its power supply rails. Many amplifiers can have an output voltage swing of ±10-12V, when operating on its standard ±15V power supplies. To get the maximum output voltage swing of an amplifier, bootstrapping can be used. Bootstrapping is simply a method of controlling a device's power supply voltages based on its output signal (Grayson and Tim, 1999). One question may arise, why use the bootstrap method instead of any other method? The reason is because op-amps offer simple and effective alternatives and have been proven in various applications due to their usefulness. Some applications may require output voltage swings greater than normal standard op-amps, EIT can be considered to be one such application.

The direct approach to achieve high output voltage swings can be the manufacturing of amplifiers using discrete components like transistors etc. This direct approach will give us the flexibility to design a fully customisable amplifier as per application requirement with the ability to achieve a high output power signal. The drawbacks of this direct

approach can be: 1) time involved in the discrete circuit design process and complicated manufacturing using more parts, 2) the difficulty in achieving precision due to device matching and temperature gradients.

A high voltage op-amp can be an alternative method. These devices are just like the monolithic op-amps but are in the form of hybrid modules. These modules allow us to give high voltage and high power performance with factory specified and tested performance. It has a disadvantage of high cost and a limited range of available hybrid op-amps. Hence giving an option to use a large number of low cost monolithic op-amp for this technique. Discrete component designs can also be of lower cost but the design complications and characteristic effort often negate this benefit.

To illustrate the technique, a non-inverting amplifier configuration is chosen to show the improvement in the output voltage swing of the circuit configuration shown in Figure 5.1. Supplies voltages ($V_{CC}$ and $V_{EE}$) are fixed but the device supply voltages ($V_+$ and $V_-$) changes dynamically as a function of the device's output voltage ($V_{OUT}$). As a result, the op-amp can cover a peak-to-peak voltage swings far greater than the total voltage applied on its supply rails. The maximum voltage (as per IC manufacturing process) that can be applied across a monolithic op-amp power rails is generally around 30-40V. If the difference of $V_+$ and $V_-$ remains constant at ≈30V, then the absolute voltages $V_+$ and $V_-$ will swing >70V to follow the output voltage ($V_{OUT}$). Two emitter follower and two resistor pairs will generate this $V_+$ and $V_-$ voltages along with additional two diodes to improve the output voltage swing (Grayson and Tim, 1999).

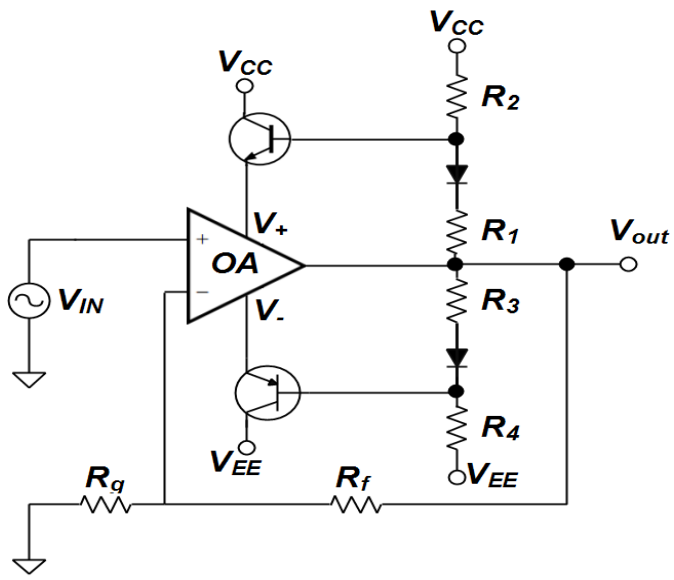



Figure 5.1: A bootstrapping circuit used in which $V_+$ and $V_-$ changes as a function of the output voltage

Initially by ignoring the diode voltage drop and $V_{BE}$ drops, the voltages $V_+$ and $V_-$ shown in Figure 5.1 can be expressed as:

$$V_+ = \frac{V_{CC}R_1 + V_{OUT}R_2}{R_1 + R_2} \quad \text{Eq. (5.1)}$$

$$V_- = \frac{V_{EE}R_3 + V_{OUT}R_4}{R_3 + R_4} \quad \text{Eq. (5.2)}$$

Considering the effect of transistors $V_{BE}$, the device supply voltage expressions can be represented as:

$$V_+ = \frac{V_{CC}R_1 + V_{OUT}R_2}{R_1 + R_2} - 0.6 \quad \text{Eq. (5.3)}$$

$$V_- = \frac{V_{EE}R_3 + V_{OUT}R_4}{R_3 + R_4} + 0.6 \quad \text{Eq. (5.4)}$$

To find the maximum achievable output voltage ($V_{OUT}$), we assume that $V_+ = V_{OUT}$. Solving the expression for $V_{OUT}$, will result in an expression as:

$$MAX\ V_{OUT} = V_{CC} - 0.6\left(1 + \frac{R_2}{R_1}\right) \quad \text{Eq. (5.5)}$$

If the diodes presence are considered to compensate transistor $V_{BE}$, the device supply voltages shown in Eq. (5.1), (5.2) and the maximum output voltage shown in Eq. (5.5) becomes:

$$V_+ = \frac{(V_{CC} - 0.6)R_1 + V_{OUT}R_2}{R_1 + R_2} \quad \text{Eq. (5.6)}$$

$$V_- = \frac{(V_{EE} + 0.6)R_3 + V_{OUT}R_4}{R_3 + R_4} \quad \text{Eq. (5.7)}$$

$$MAX\ V_{OUT} = V_{CC} - 0.6 \quad \text{Eq. (5.8)}$$

This shows that the peak output voltage increases by 0.6 times$\left(\frac{R_2}{R_1}\right)V$. If the ground potential is at equidistant between $V_{CC}$ and $V_{EE}$ then it can be assumed that $R_3 = R_1$ and $R_4 = R_2$. Substituting this assumption in Eq. (5.6) & (5.7) will conclude that the difference between $V_+$ and $V_-$ is constant if it is assumed that $V_{CC}$ and $V_{EE}$ are constant. This difference equation can be written as:

$$V_+ - V_- = \frac{R_1}{R_1 + R_2}(V_{CC} - V_{EE} - 1.2) \quad \text{Eq. (5.9)}$$

**Bootstrapped Circuit Testing:** An experiment was setup to demonstrate the performance of the bootstrapped circuit. The schematic shown in Figure 5.1 was simulated using a high voltage AD812 op-amp with a power supply up to ±18V. The transient response of the circuit was tested with a 10kHz signal having a 25V amplitude and 0V offset.

Suppose $V_{CC}$ = 60V, $V_{EE}$ = -60V, $R_1$ = $R_3$ = 10kΩ and $R_2$ = $R_4$ = 28kΩ, then using Eq. (5.9) it can be calculated that voltage drop across the op-amp remains constant and is ≈30-31V throughout the $100V_{p\text{-}p}$ output swing. This mathematically calculated value can be verified by using simulation result of the circuit shown in Figure 5.2. The simulation result obtained shows that the voltage drop across the positive rail ($V_+$) and negative rail ($V_-$) of the op-amp is $\approx 75V_{p\text{-}p}$. It was observed that the $V_+$ and $V_-$ voltages have an offset of ≈15V. Approximately 30V voltage difference between the power rails of the op-amp was observed through-out the $100V_{p\text{-}p}$ output swing of the op-amp and is accordance with Eq. 5.9. These results clearly show the benefit of using bootstrapping for high output voltage swings in any circuit. Therefore, it was decided to use this technique to resolve the clipping problem in our excitation source circuit with high amplitude output voltage and make it suitable to be used in any BI-system.

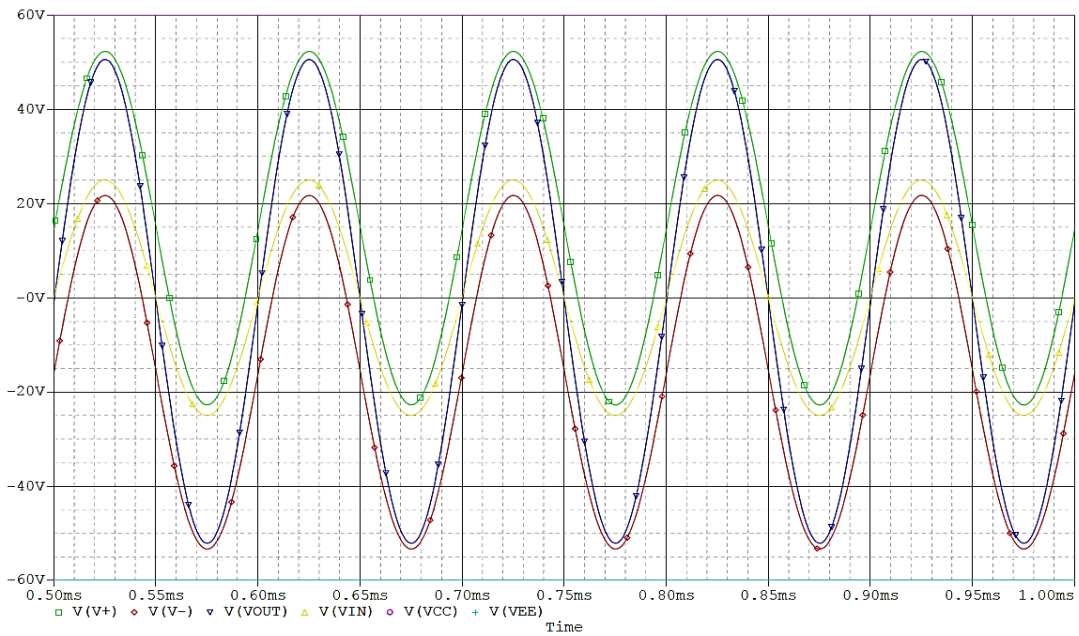



Figure 5.2: A bootstrapped circuit simulation providing $\approx 100V_{p\text{-}p}$

The voltage at the non-inverting input terminal of the device should remain within its common mode input range, especially in bootstrapping architecture circuits in which the op-amp power supply rails change with its output. Therefore, if $V_+$ and $V_-$ changes, the

input voltage must always remain between it, otherwise a circuit latch up condition will occur. To ensure this common mode input range under all conditions: dc, transient, phase reversal and power conditions for bootstrapping circuit should be addressed.

The gain of the bootstrapped op-amp circuit is described by: $A_V = 1 + R_F / R_G$. When $V_{CC} - V_{EE} < 2(V_+ - V_-)$ then this circuit configuration can run at any gain including inverting gain. A higher power supply rail and high output swings, requires a carefully selected gain in non-inverting mode. If too high gain is set then, it will cause $V_+$ & $V_-$ to exceed $V_{CM}$ on both positive and negative side which violate the op-amp input common mode range and result in the power supplies being shifted away from ground potential and result in latch-up condition. A low enough gain will saturate the output before the input and the power supplies rails stop increasing before they exceed the input. Therefore, the circuit gain play a significant role in the circuit performance (Grayson and Tim, 1999).

In the bootstrapped circuit, the op-amp output has a finite slew rate and its power supplies are output dependent. Therefore, a step function at the op-amp input can easily exceed the op-amp power supply range when the op-amp is just beginning to slew and causes a latch-up condition. It can be avoided by placing a slew limit on the input signal to remain ≤ to the op-amp slew rate. It is implemented by a simple RC circuit before the op-amp input.

Another problem can occur if $V_{CM}$ exceeds the power supply rails which can be avoided by limiting the current into the saturated input mode by adding a series resistor at the input. Input driving of some op-amp to one of the power supply rails may lead to a phase reversal and the op-amp output slews to its opposite power rail and stays there until the input stage recovers from its saturation. In a bootstrapped circuit, the op-amp power supply rails slew as a function of its output. This situation leads the input far outside its power supply rail which is most likely unrecoverable and may lead to op-amp destruction. If a phase reversal op-amp is chosen then, the input amplitude must be limited so that the input voltage and $V_{CM}$ never exceed the op-amp common mode input voltage range. In short it can be said that dc gain problem occurs when $V_{CM}$ is closer to the ground instead of either supply rail. Phase reversal is a problem when $V_{CM}$ is distant from ground instead of either supply rail.

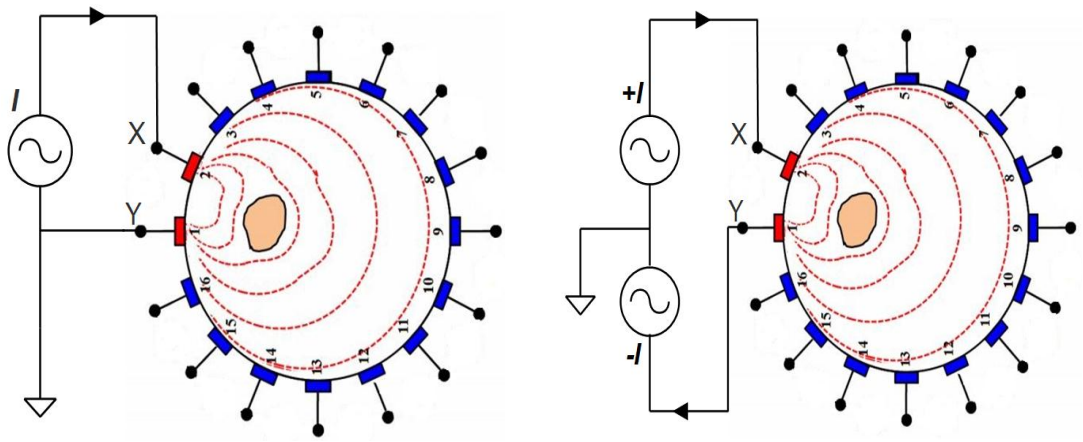
Being sensitive to latch-up, power supply sequencing should be carefully applied. If the positive rail is supplied a few milliseconds before the negative rail than it possibly can

shift the device supply voltages towards the positive rail and stays there until the input remains at ground which violates the op-amp input common-mode range. To avoid latch-up caused by this condition, the input should be at ground potential with simultaneously applied power supplies. To use this circuit, a high voltage power supply (30-40V) is recommended and avoid using the device with a maximum supply of only 5/10V. Individual system requirements should be considered before op-amp selection.

## 5.3 Bipolar Current Source

Traditional current sources and V-I converters, which are based on instrumentation/operational amplifier, gives high output impedance at low frequencies due to the amplifier's good low frequency CMRR. At higher frequencies, this CMRR decreases and some other factors (output capacitances, slew rate etc.) will prevent this realization from becoming a high quality CS. In case of a single-end CS (Figure 5.3-a), there is some voltage drop across the grounded electrode and the SUO which induces a common-mode voltage at the input terminal of amplifier. The common-mode voltage will have several orders of magnitude higher than the differential measured signal. So, in order to limit this effect, a differential CS is suitable to inject current into the SUO.

In a differential CS for a given injection pattern, the common-mode voltage will be minimum for the pair of measurement electrodes, which is opposite to the injection pair. In the absence of a common-mode feedback, the closer one gets to the injection pair will result in increase of common-mode voltage. This method can be used for injection, which involves a pair of electrodes that inject current with equal amplitude but opposite signal phase. A typical differential CS is shown in Figure 5.3-(b).




*(a)* *(b)*

Figure 5.3: A Current Source injection for EIT system: (a) Single-end (b) Differential

The output impedance of the CS is assumed to be infinite due to its nominal component value. In practice, the resistor used always differs from there nominal values that result in a difference of the measured and calculated current value. In case of two signal generators used to make a differential source, a little deviation from the components nominal value will influence the circuit overall performance by affecting the current and output impedance for each generator. Therefore, the component's tolerance is an important factor in a symmetrical drive CS design for an EIT system. Practically implemented CS circuit will always have different and finite output impedance values. A simplified circuit model of the differential CS is shown in Figure 5.4.

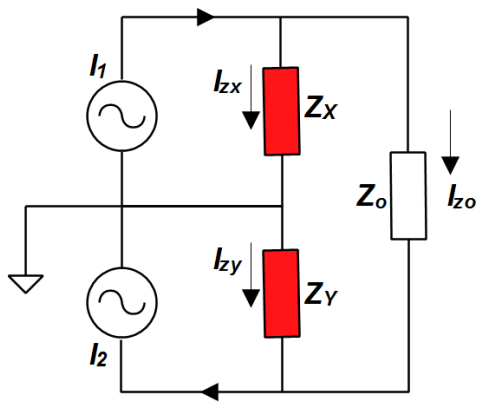



Figure 5.4: A Differential CS equivalent circuit model (Yang, 2006).

For the above circuit model, the load current delivered to the SUO and the common-mode voltage can be described as:

$$I_{ZO} = \frac{Z_X I_1 + Z_Y I_2}{Z_X + Z_Y + Z} \qquad \text{Eq. (5.10)}$$

$$V_{com} = \frac{V_1 + V_2}{2} = \frac{Z_X Z_Y (I_1 - I_2)}{Z_X + Z_Y + Z_O} + \frac{Z_o (Z_X I_1 - Z_Y I_2)}{2(Z_X + Z_Y + Z_o)} \qquad \text{Eq. (5.11)}$$

Eq. (5.10) represents a slight difference between the injected and calculated current value. This current difference can be ignored when an individual current generator is designed with a very high output impedance as compared to the load impedance and it will not induce any large error even if both sources are not perfectly matched. This imbalance will induce some common-mode voltage to the amplifier. It can be seen in the Eq. (5.11) that the common-mode voltage consists of: 1) the difference in the two current amplitudes ($I_1 - I_2$), and 2) the imbalanced output impedance of both sources. If both sources current are equal then:

$$V_{com} = \frac{Z_o (Z_X - Z_Y)\, I_1}{2(Z_X + Z_Y + Z_o)} \qquad \text{Eq. (5.12)}$$

The output current for the differential CS built using EHCS circuit, are dominated by the resistive-network and can be expressed as:

$$-\frac{V_i R_2}{R_1 R_4} - \frac{V_o}{Z_o} = -\left(-\frac{V_i' R_2'}{R_1' R_4'} - \frac{V_o'}{Z_o'}\right) \qquad \text{Eq. (5.13)}$$

Eq. (5.13) represents the components representation for 0° and 180° source circuits. Keeping the fact in mind that $Z_o$ and $Z_o'$ are very large, the performance of the CS will depend on the resistive components matching in both circuits. Another factor of input voltage needs to be considered, and should be of same amplitude with a 180° phase shift.

## 5.4 Guard Amplifier (GA) Technique

A modern inductor free technique to eliminate/minimise the unwanted capacitance can be achieved by using a guard amplifier within the circuit. This is a simple principle in which any high input impedance amplifier having gain near but <1 is used to drive resistors to make them effectively bigger or to drive the capacitance to make it smaller, can be termed as a guard amplifier. The best performance of the GA can be achieved when it has a low input capacitance and its gain is near but <1 across the whole frequency range of interest. Gain above one may result in the circuit oscillation. This technique allows to measure impedances without adding significant impedance in parallel with the measured impedance and measured potentials without affecting the potentials.

A block diagram of a GA is shown in Figure 5.5, which shows a network of potential divider having a gain G2 and a guard amplifier with a gain G1. As per the block diagram of GA, the effective increase of the driven resistor is by a factor of approximately 1/ (1-G1 * G2). Similarly, in case of effective loading capacitance, the capacitance will be decreased by a factor of approximately (1 – G1*G2). Mostly this approach is used to decrease the effect of stray capacitance associated with any component, which connects to the input (Bach, 2003). The capacitance of a typical surface mount 0805 resistor is ≈0.3pF (including mounting pads on the PCB). Therefore, the input bias resistor *($R_1$)* will have 0.3pF capacitance in parallel with the resistance. This will add 0.3pF parasitic capacitance to the input. Guard action is applied to make this capacitance smaller by a factor of (1-G1*G2). Let's assume that G1=0.999 and G2=0.99, then 0.3pF capacitance becomes 0.3pF x (1 - (0.999*0.99)) = 0.0032pF, which will load the input with much smaller capacitance. As per GA principle, both G1 and G2 needs to be close to one in

order to get an optimized performance of the guard. An increase in $R_2$ and $C_1$ will result in G1 being near one. It is difficult to achieve a G2 near one across a wide band of frequencies and it will require optimization of the guard amplifier using electronic design, PCB construction and SMD component selection. To understand its functionality, a simple guard circuit was checked initially and later it was extended to more complex circuitry, which is considered to be useful for any BI system to cancel known capacitance introduced by the multiplexers. Simulation circuit of this technique and its ability to decrease the capacitance is described in appendix D.

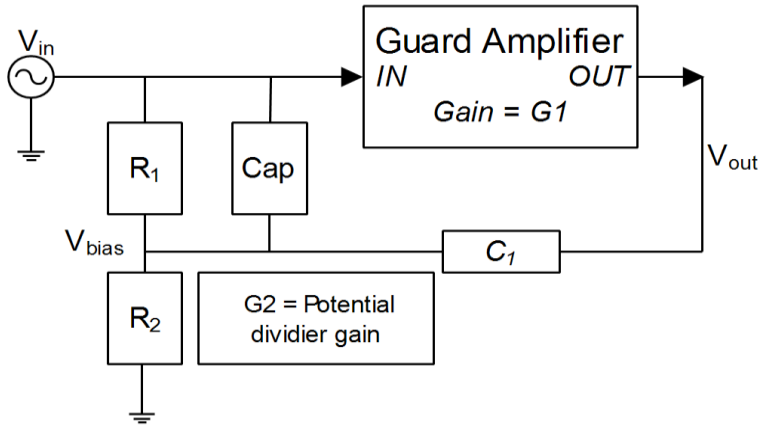



Figure 5.5: Guard Amplifier block diagram

Our CS circuit design, will consist of two multiplexers (ADG1204 and ADG1219) to switch the 0-degree input signal to the load. These MUX's were modelled in terms of their On Resistance ($R_{ON}$), input and output capacitance because of their PSPICE model non-availability. An experiment was setup to check the performance of the GA in which the signal was propagated through MUXs model and applied to the attached load (5kΩ and 30kΩ) as shown in Figure 5.6. The GA takes its input from the loading voltage. The GA was designed and optimised in such a way that it generates three voltages based on the loading voltage considered as input. These voltages are referred as GA power rail buffered voltages and are denoted as: $V_{ddBuf}$, $V_{ssBuf}$ and $GND_{Buf}$.

Based on the resistor network settings and the applied DC voltages to the GA, the circuit will shift the buffered voltages up and down and will always remain within the applied DC voltages. The amplitude of the $V_{ddBuf}$ and $V_{ssBuf}$ voltages should be approximately equal to the amplitude of loading voltage. These buffer voltages should follow the same amplitude pattern attached to any load value. The $GND_{Buf}$ voltage should always remain within the voltages generated by the GA. In an optimised GA circuit, the voltage $GND_{Buf}$ should be approximately equal to the loading voltage.

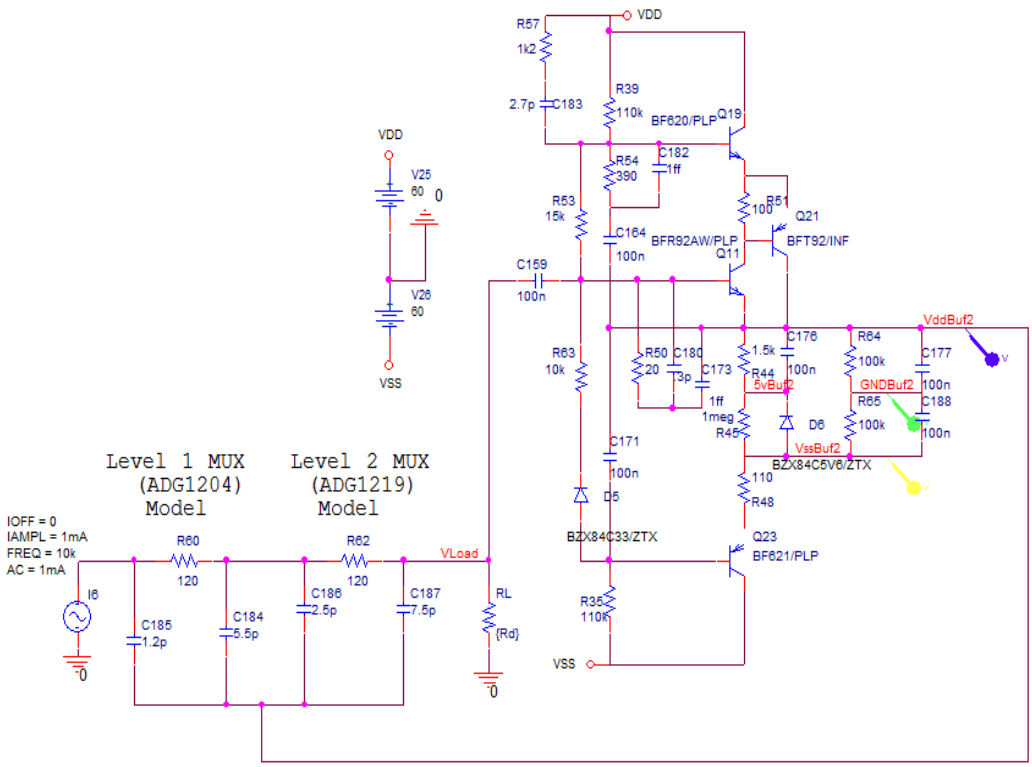



Figure 5.6: Designed Guard Amplifier for current source circuit

**<u>GA AC Response:</u>** The MUX equivalent model circuit was simulated without applying the GA effect (referenced to ground: 0V). The AC response showed amplitude reduction at high frequencies and limits the overall frequency bandwidth of the circuit (≤1MHz) due to the MUX's capacitance effect. It also showed an amplitude drop at 100Hz followed by a steady increase (≥1kHz) until it reached the -3dB cut-off point (≤1MHz).

Later, the circuit was simulated using the GA effect with an approach to drive the capacitors of the circuit model with the GA output voltage. The capacitors need to be charged all the time so that they will not lose any charge and will result in a maximum amplitude signal delivered to the load. At low frequency, the capacitor behaves as an open circuit and its continuous charging is insignificant. The capacitor acts like a short circuit with an increase in the frequency and results in signal amplitude reduction. Its continuous charging from the GA output voltages will help to solve this problem at higher frequencies with a maximum amplitude signal delivered to the load. Practically the output voltages of the GA are applied to the power supply and ground pins so that it can shift the power rails according to the loading voltage, which in turn minimises the capacitance involved due to the MUX's. The AC response showed that the capacitance will not affect the performance of the circuit over a wide frequency band (>10MHz). The capacitance effect of the MUX's at higher frequencies is minimised due to the continuous charging

by the GA output voltage and is shown in Figure 5.7, which represents the loading voltage versus frequency sweep.

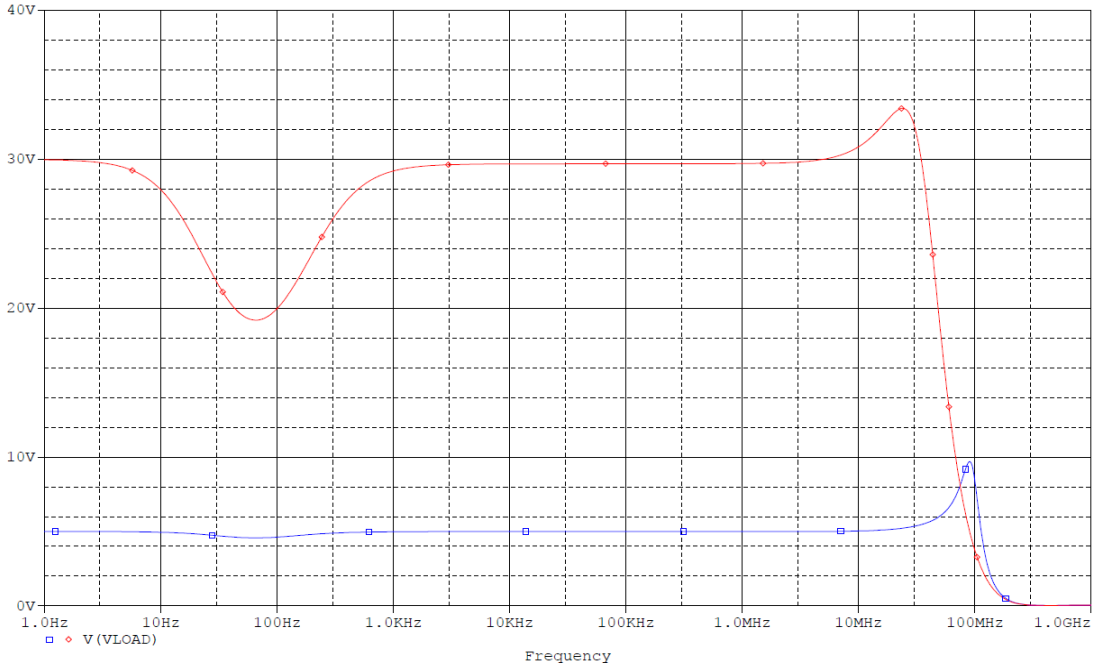



Figure 5.7: AC response of GA circuit with capacitance cancelation

**GA Transient Response:** A transient response of the GA circuit was tested for 5kΩ and 30kΩ loads. The simulation was applied with a frequency of 10kHz and 10MHz having 1mA amplitude and 0mA offset current. Initially the circuit model was tested without any GA effect. At 10kHz frequency, it was observed that the load voltage amplitude was approximately 5V and 30V which showed that ≈1mA current was delivered to the load. At 10MHz frequency, the result showed that the amplitude of the load voltage dropped dramatically due to the major affect caused by the capacitance and shunt away the maximum current from the load. The overall frequency bandwidth of the circuit dropped and was limited to <1MHz.

The circuit was also simulated using a similar transient setup, to show the effect of GA. The GA generated rail voltages were used to drive the capacitance of the MUX circuit model, which avoid capacitance's short circuit behaviour at high frequencies and resulted in capacitance minimisation. It can be seen from Figure 5.8 that the load voltage amplitude is approximately 5V and 30V (at 10MHz frequency), which shows that ≈1mA current is passing through the load. The load voltage is considered as input to the GA that will shift its generated rail voltages accordingly with an amplitude equal to the loading voltage amplitude. The GA will also generate a reference signal for both rail voltages that should always be in between the guard rail voltages with an amplitude equal to the loading

voltage amplitude. It can be seen from Figure 5.9 & Figure 5.10 that the amplitude of the referenced signal ($GND_{Buf}$) is ≈9.98$V_{p-p}$ & ≈60.6$V_{p-p.}$ The amplitude of the GA power rails ($V_{DDBuf}$ & $V_{SSBuf}$) shifts its output signal by approximately 5.02V and 30.3V up and down.

The GA also showed a similar performance at 10kHz frequency by minimising the effect of the unwanted capacitance. The response showed that the amplitude of the load voltage was approximately 5V and 30V. It shifts the rail voltages by approximately 4.98V and 29.5V up and down with a 5kΩ and 30kΩ load respectively. The amplitudes of the referenced signal ($GND_{Buf}$) were found to be approximately 9.98$V_{p-p}$ & 60.6$V_{p-p}$ for the same tested loads. This shows that the effect of unwanted capacitance is minimised and maximum voltage is dropped across the load.

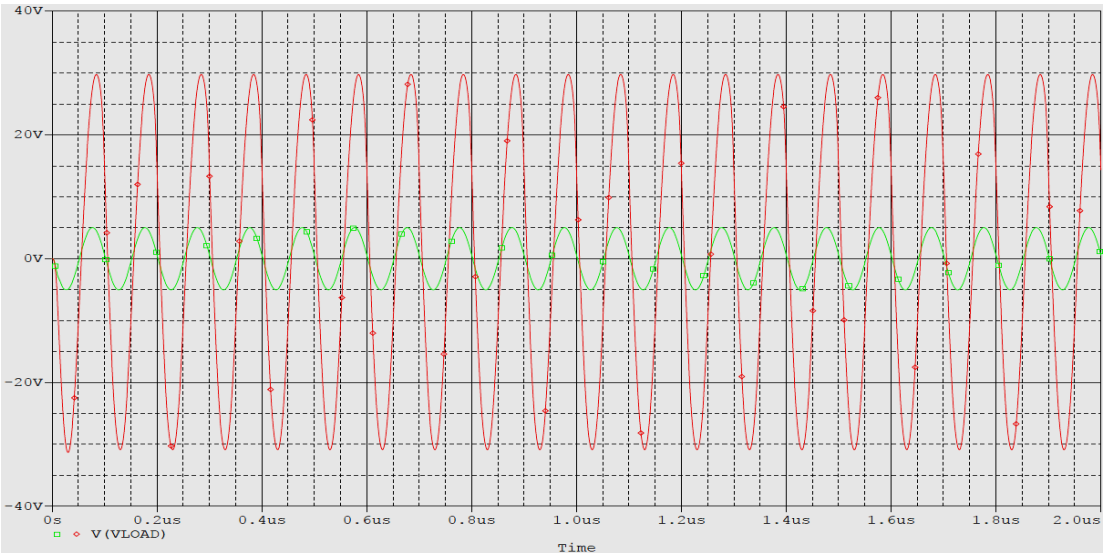



Figure 5.8:Transient response of GA circuit at 10MHz using 5kΩ and 30kΩ Load

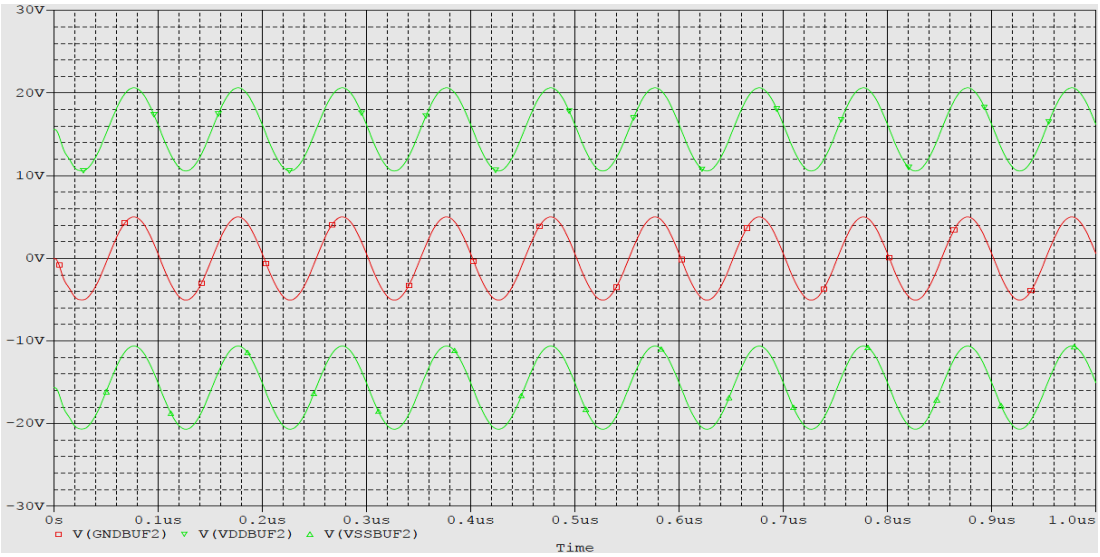



Figure 5.9: GA circuit buffered output voltages at 10MHz using 5kΩ Load

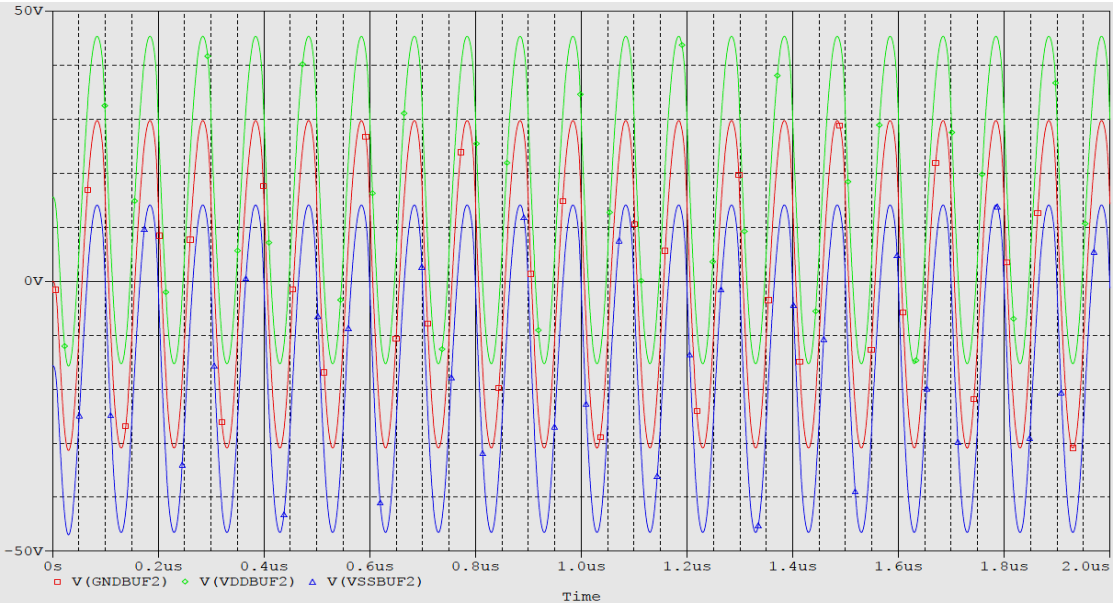



Figure 5.10: GA circuit buffered output voltages at 10MHz using 30kΩ Load

## 5.5 Current Source Circuit Simulation Result

The simulation results presented in chapter 4 shows that the performance of the CS was degraded at higher frequencies by the unwanted capacitance caused by op-amp, MUX's, cables etc. The op-amp saturation problem was also observed in the simulation results achieved for the CS. A low power rail voltage op-amp was used in the circuit design of the EHCS and EHCS-GIC.

Therefore, it was decided to use a high voltage op-amp with some additional circuitry to avoid the op-amp clipping problem in the circuit and achieve a high output voltage swing. It was decided to use two different op-amps in the circuitry i.e. AD812 and THS4304. AD812 is a low power, single/dual supply amplifier capable to deliver a high output current and is ideal for professional usage. It has outstanding bandwidth of 145MHz with a good slew rate making it useful in many general purpose high speed applications with dual power supplies (Datasheet AD812, 2016). This op-amp was used in the EHCS circuit because of its high bandwidth along with high power supplies required at a certain circuit gain. It was noticed that normally the EHCS circuit does not require a larger circuit gain in our design application. In most of our tested configurations, the gain of the EHCS circuit was 1 or 2. Therefore, the AD812 op-amp was selected due to its high bandwidth performance at smaller gain.

The THS4304 op-amp was used in the GIC part of the CS circuitry. To cancel the effect of capacitance, the GIC circuitry needs to be tuned for different frequencies and may require different gain for different frequencies. The gain can be higher to get an optimized performance. Therefore, it was decided to use this op-amp, which can give a higher bandwidth with large gain. A high speed op-amp is required in the GIC part of the circuitry because of the circuit tuning over a narrow frequency band. In this section, the bootstrapped EHCS and EHCS-GIC circuit are presented. The simulation results show a clear improvement in the output signal without clipping.

### 5.5.1 Bootstrapped EHCS Performance

Figure 5.11 shows the EHCS circuit simulation setup. The power rails for the op-amp were set and controlled as a function of op-amp output signal without any external noise included. The resistors network ratio should satisfy the condition,

$$Gain = \frac{R_2}{R_1} = \frac{R_4 + R_5}{R_3} \qquad \text{Eq. (5.14)}$$

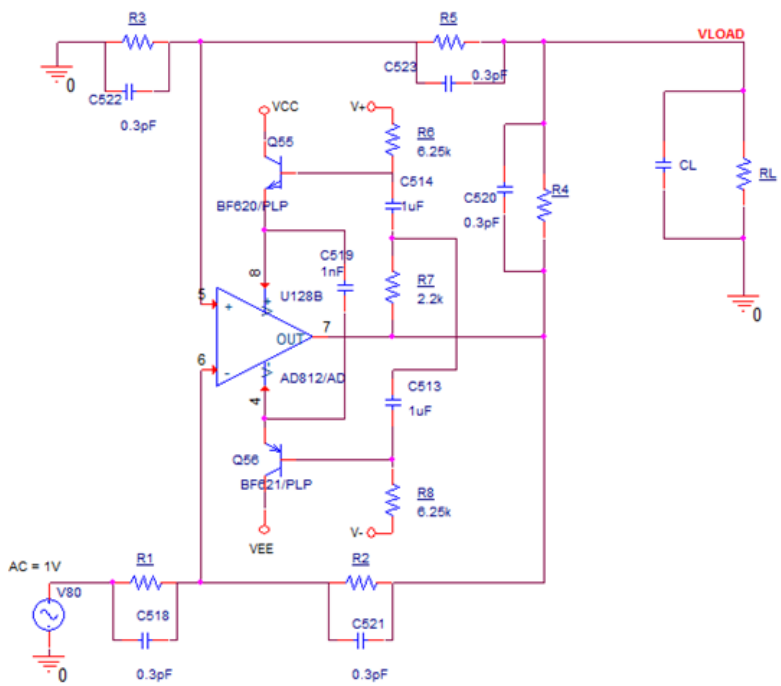



Figure 5.11: Bootstrapped EHCS-circuit simulation setup

During testing the bootstrapped based CS, we understood that the resistor matching ratio can be satisfied on two configurations: 1) a gain of 1 can be obtained by setting resistors $R_1$, $R_2$, $R_4$ and $R_5$ to 1kΩ and $R_3$ to 2kΩ. The resistor $R_3$ was tuned precisely to achieve

high amplitude load current and impedance, 2) a gain of 1 can also be obtained by setting $R_1$, $R_2$ to 1kΩ, $R_3$ to 2kΩ, $R_4$, $R_5$ to 1.020kΩ and 980Ω respectively. This configuration will give a high amplitude load current without tuning any specific resistor. This configuration fully satisfies the theoretical ratio condition in Eq. 5.14. In the second configuration, the precise adjustment of resistor $R_4$ (<1kΩ) will result in less voltage drop across it, and maximum current delivered to the load. Therefore, it was decided to simulate the EHCS circuit using the second resistor-network configuration and compare its performance with EHCS simulation using setting 1, achieved in chapter 4. The bootstrapped circuit used in the EHCS part was slightly different from the circuit explained before but it will not affect the performance and principle behind this technique.

The AC response of the EHCS circuit was observed using variable load resistance (R: 5kΩ to 30kΩ, ΔR=5kΩ). The AC response showed that the overall frequency bandwidth of the EHCS circuit was effected due to its output capacitance (≈1.9-1.7pF). It was observed that the amplitude of the load current was ≈1mA without necessarily adjusting any triggering resistor. The multiplexing of the excitation signal involves additional capacitance in the circuit and will further reduce the frequency bandwidth of the EHCS circuit. This behaviour was observed in the simulation test with additional 10pF and 50pF loading capacitance.

To validate the AC response, transient response of the circuit was observed. The transient response was setup with a frequency of 1kHz, 10kHz, 100kHz and 1MHz having 1V amplitude and 0V offset voltage. The tested load resistance values were 5kΩ, 10kΩ and 15kΩ with a 10pF, 30pF, 50pF and 100pF loading capacitance. The only difference noticed was the amplitude reduction in the output voltage of the circuit with an increase in loading capacitance and frequency, which illustrate an overall frequency bandwidth reduction of the bootstrapped EHCS circuit. The result showed that the frequency bandwidth was limited to <1MHz in the presence of loading capacitance. It was observed from the transient response that the voltage dropped across the tested loading was 5V, 10V and 15V (i.e. at low frequencies). This shows that the load current is 1mA at the different tested frequencies until the drop off in the signal amplitude starts due to the finite open loop gain of the used op-amp, output capacitance of the circuit and other nonlinearities involved within the circuit. This amplitude drop-off in the output signal represents the frequency bandwidth limitation of the circuit.

The frequency bandwidth comparison of EHCS and the bootstrapped EHCS circuit doesn't show much difference. The output impedance was also at an acceptable level because of the 1mA load current. It was also observed that with an increase in the load value and for frequencies >100kHz, there is a slight phase shift in the output signal in the presence of loading capacitance. In the light of above results, it can be said that bootstrapping the EHCS circuit has improved the circuit performance and the circuit can operate with a higher load (i.e. 30kΩ) without any loading voltage problem. This has resolved the op-amp clipping problem and the circuit can be operated at a higher voltage by simply driving the bootstrapped part with a high supply voltage.

### 5.5.2 Bootstrapped EHCS with GIC Performance

The EHCS-GIC circuit was also effected by the op-amp clipping problem (section 4.4.2). Although the EHCS-GIC circuit increases the complexity of the current source but it can give good performance at selected frequencies. Therefore, it was decided to further investigate this circuit and improve its performance so that it can be used in our BI system.

Bootstrapped EHCS-GIC circuit simulation was performed. AD812 and THS4304 were used in the EHCS and GIC part of the circuitry respectively. The first resistor-network (described in section 5.5.1) configuration was used in which the resistor *($R_3$)* was slightly altered to improve the load current amplitude that in turn improve the output impedance of the CS. One passive component in the EHCS part and three passive components in the GIC part were kept variable in the CS design. These components were tuned according to the selected frequency range and optimised until the optimum possible simulated performance was achieved from the circuitry. The EHCS and GIC part op-amps were bootstrapped and simulation was performed with the circuit schematics shown in Figure 5.12.

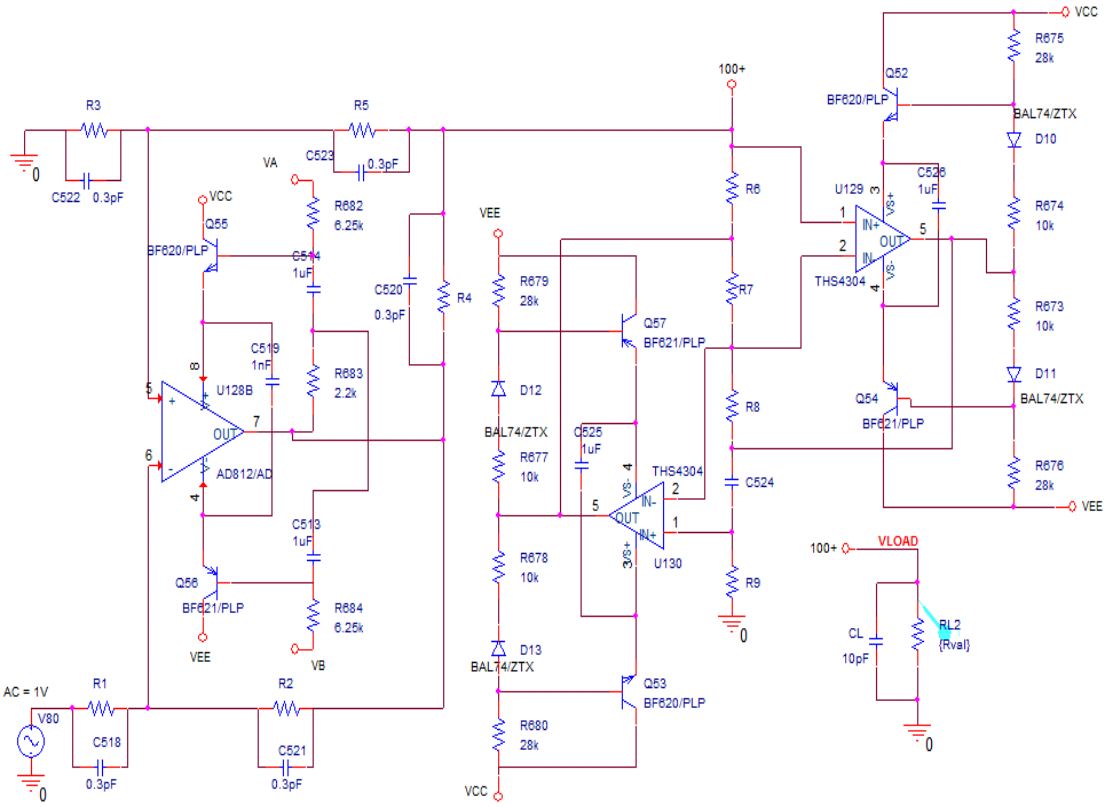
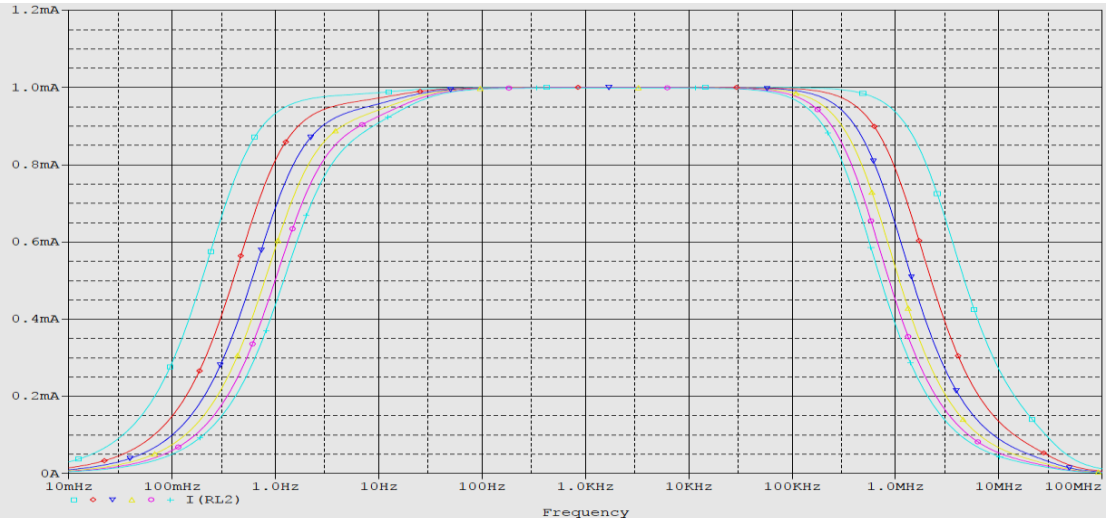



Figure 5.12: Bootstrapped EHCS-GIC circuit simulation setup

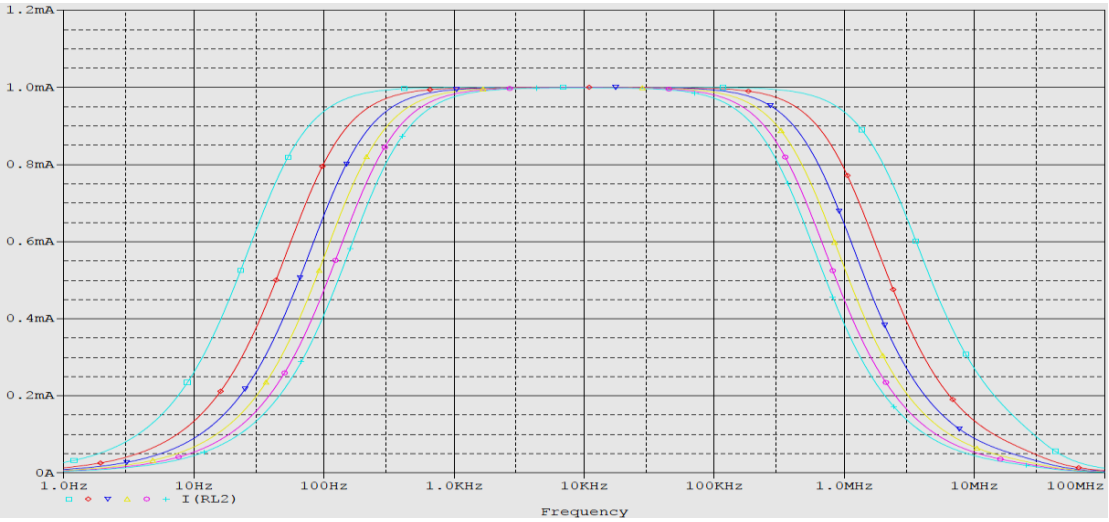
### *5.5.2.1 AC Response of Bootstrapped EHCS-GIC Circuit*

The circuit shown in Figure 5.12 was operated with an AC sweep analysis. The power rails for all the active elements in the circuitry were bootstrapped without any noise included using variable load resistance ($R_L$: 5kΩ to 30kΩ, ΔR=5kΩ). The power rails ($V_{CC}$ and $V_{EE}$) and the bias voltages ($V_A$ and $V_B$) of the bootstrapped circuit were set to ±60VDC and ±36VDC respectively. The circuit was simulated with no loading capacitance and with possible loading capacitance of: 10pF, 30pF, 50pF and 100pF. The bootstrapped EHCS-GIC circuit setting was altered for a different set of frequencies to get the optimum performance of the source at a specific frequency/frequencies band. The frequencies were divided into groups to cover maximum possible frequencies testing. A group of large number of frequencies will minimise the circuit tuning. The EHCS-GIC circuit give a peak amplitude response for the load current in such groups, care was taken to ensure that all other frequencies will have an acceptable amplitude of load current apart from the peak frequency. The frequency groups were 0.1-1kHz, 10kHz, 100kHz, 1MHz and 10MHz. The simulation results are shown from Figure 5.13 - Figure 5.17, describing the output load current *($I_L$)* against its respective frequency sweep.



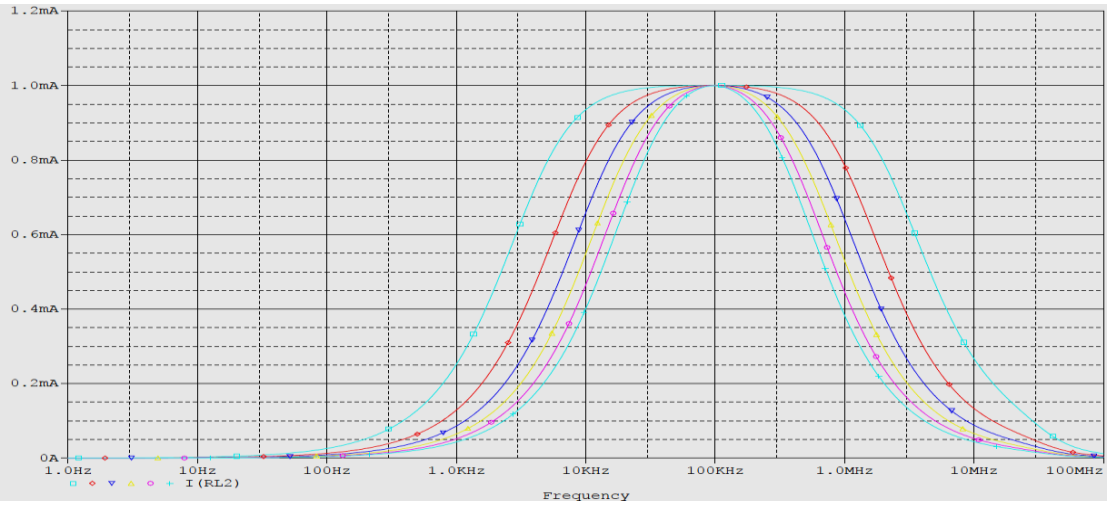

5kΩ 10kΩ 15kΩ 20kΩ 25kΩ 30kΩ

Figure 5.13: Bootstrapped EHCS-GIC circuit AC response for 0.1–1kHz with 10pF loading capacitance



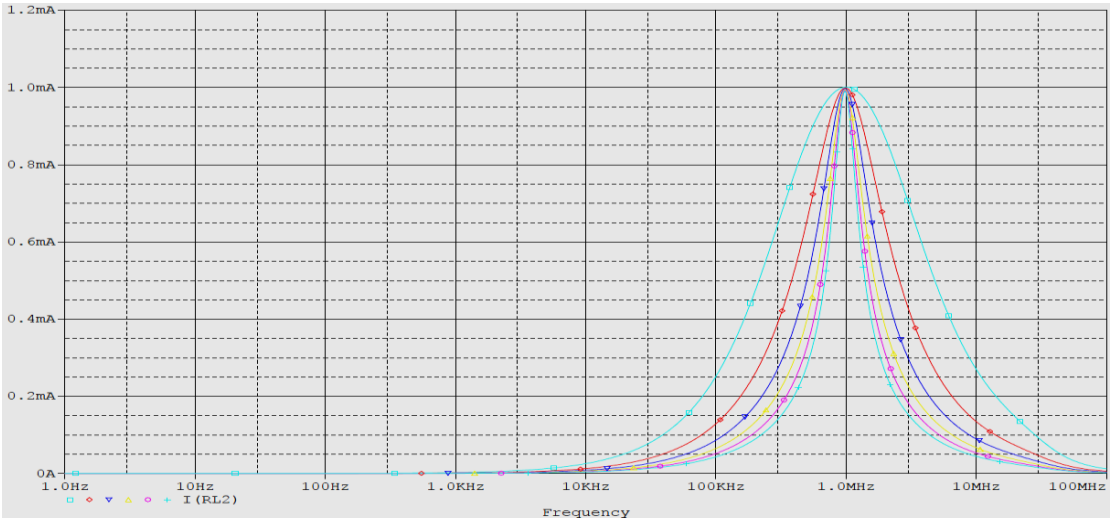

5kΩ 10kΩ 15kΩ 20kΩ 25kΩ 30kΩ

Figure 5.14: Bootstrapped EHCS-GIC circuit AC response at 10kHz with 10pF loading capacitance



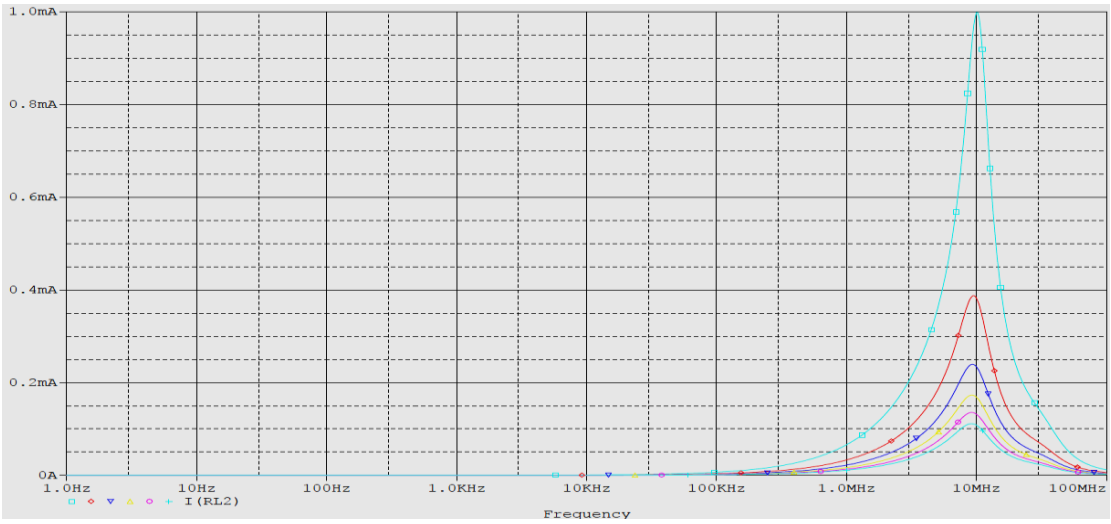

5kΩ 10kΩ 15kΩ 20kΩ 25kΩ 30kΩ

Figure 5.15: Bootstrapped EHCS-GIC circuit AC response at 100kHz with 10pF loading capacitance




5kΩ 10kΩ 15kΩ 20kΩ 25kΩ 30kΩ

Figure 5.16: Bootstrapped EHCS-GIC circuit AC response at 1MHz with 10pF loading capacitance




5kΩ 10kΩ 15kΩ 20kΩ 25kΩ 30kΩ

Figure 5.17: Bootstrapped EHCS-GIC circuit AC response at 10MHz with 10pF loading capacitance

The AC response of the bootstrapped EHCS-GIC circuit with specific loading capacitance shows a reasonable performance and an acceptable amplitude of load current having an overall narrow frequency bandwidth at a particular resistor-network setting. This circuit configuration gives a better performance in terms of the source output impedance but over a limited frequency bandwidth. It was observed that the circuit configuration used for the frequency band between 0.1-1kHz gives an amplitude peak response at ≈2.9kHz and was stable for frequencies between 720Hz-5kHz, in the presence of additional 10pF capacitive loading. The circuit output amplitude didn't drop immediately beyond these frequencies rather it was still high and close to the peak value for the corresponding frequency group. Similarly, the circuit configuration used for 10kHz frequency gives an amplitude peak response at 10kHz and was stable for

frequencies from 8.5-11kHz. Above 10kHz, the circuit configuration also gives a peak response but was limited to a single frequency (i.e. 100kHz, 1MHz and 10MHz).

Later the response was observed with 50pF loading capacitance. It was noticed that the circuit configuration used for frequency band between 0.1-1kHz gives a peak amplitude response at ≈1.4kHz and was stable for frequencies between 410Hz-1.9kHz. Similarly, the circuit configuration used for 10kHz frequency gives a peak amplitude response at 10kHz and was stable for frequencies between 9.5-10.5 kHz. Above 10kHz, a peak amplitude response was limited to a specific single frequency. A similar behaviour was expected and observed for other tested loading capacitance. Hence, it concludes that capacitance effects the performance of the circuit in term of frequency bandwidth reduction and its effect can be reduced to some extent if it is known.

### *5.5.2.2 Transient Response of Bootstrapped EHCS-GIC Circuit*

The AC response was validated using a transient analysis setup. The simulation was applied with a 1kHz, 10kHz, 100kHz, 1MHz and 10MHz signal having a 1V amplitude and 0V offset voltage simultaneously. The tested loads were 5kΩ, 10kΩ and 15kΩ in the presence of loading capacitance at different frequencies. A few selective simulation results of the circuit, in the presence of 10pF capacitance in parallel with fixed resistive loading are shown in this section. The transient responses of the circuit with the loading capacitance are shown in Figure 5.18 to Figure 5.21, which describe the load voltage at respective frequency.

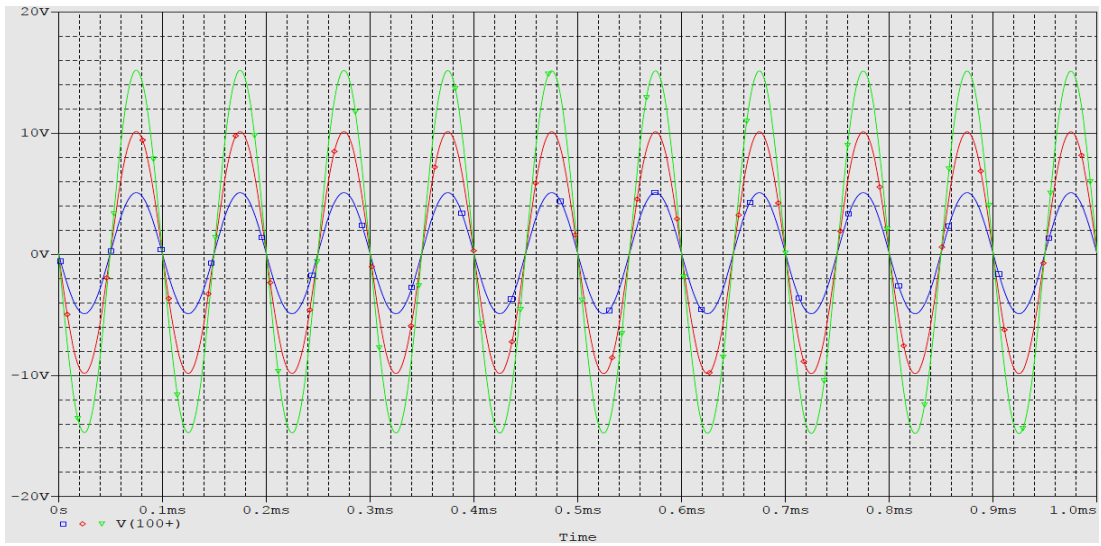
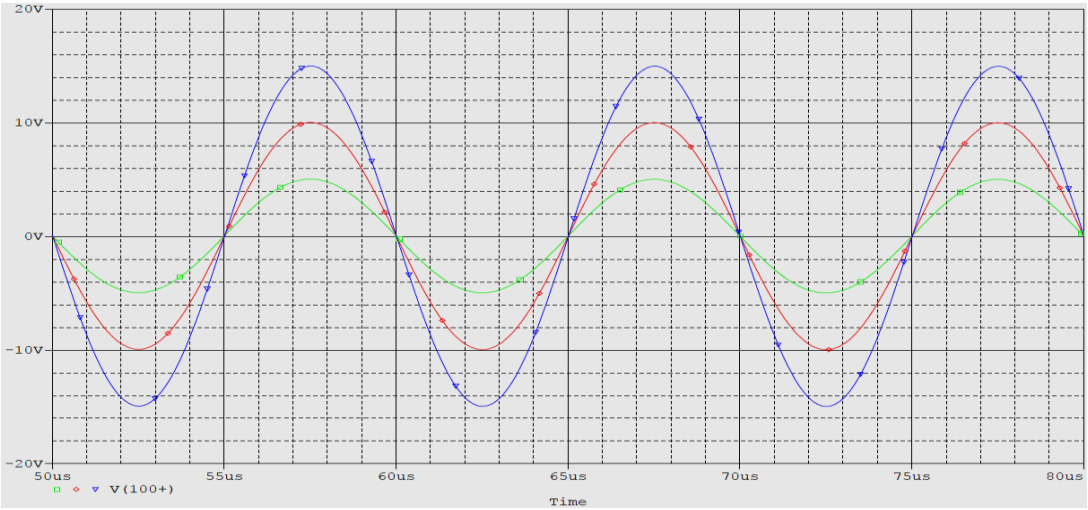
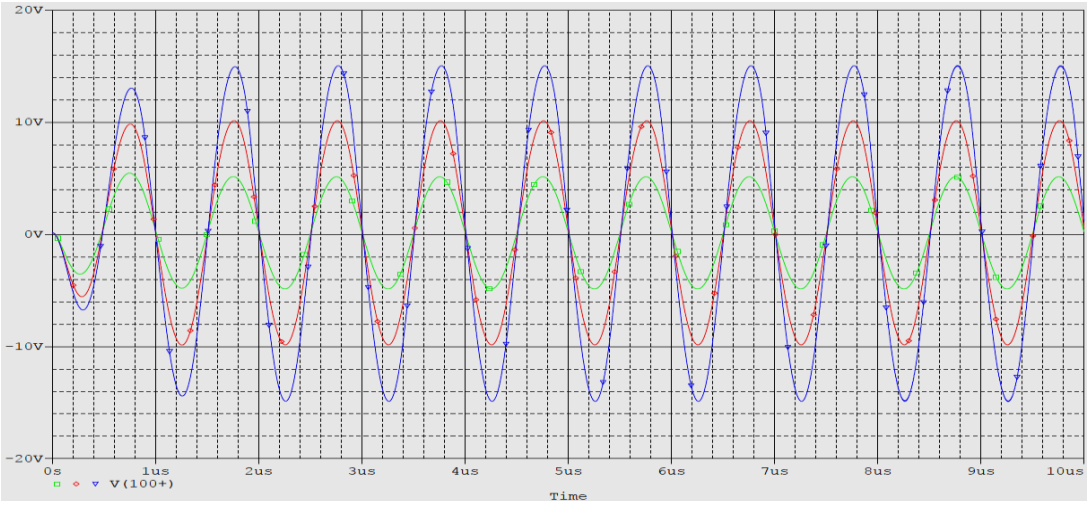



Figure 5.18: Bootstrapped EHCS-GIC circuit transient response at 10kHz with 10pF loading capacitance



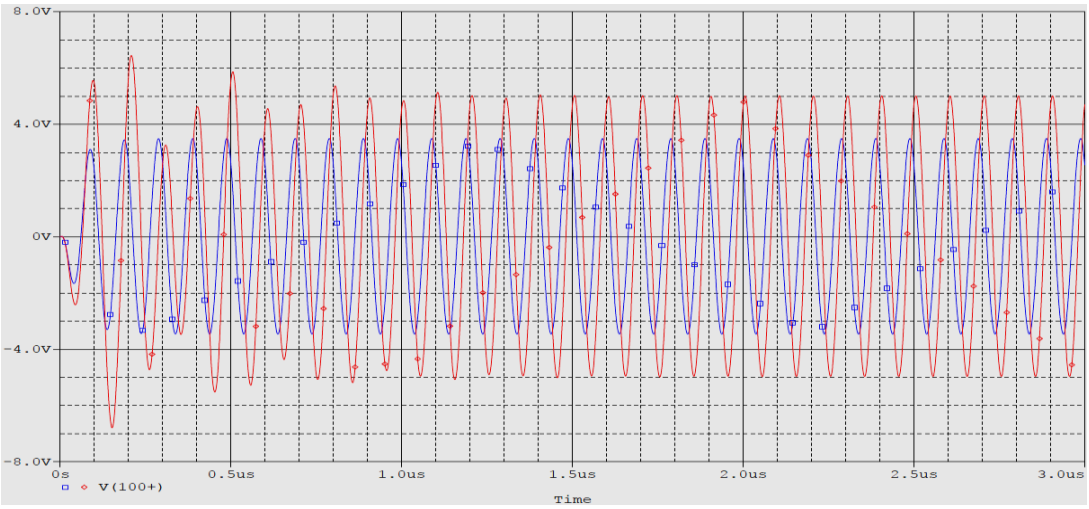

5kΩ 10kΩ 15kΩ

Figure 5.19: Bootstrapped EHCS-GIC circuit transient response at 100kHz with 10pF loading capacitance




5kΩ 10kΩ 15kΩ

Figure 5.20: Bootstrapped EHCS-GIC circuit transient response at 1MHz with 10pF loading capacitance




2kΩ 5kΩ

Figure 5.21: Bootstrapped EHCS-GIC circuit transient response at 10MHz with 10pF loading capacitance

The transient response of the circuit shows good behaviour overall. The voltage drop across the respective tested load indicates that the load current is ≈1mA. This response was observed till 1MHz and can be considered to give good CS performance until this frequency or slightly above (i.e. 2-3MHz). At 10MHz frequency, the circuit response observed was not as expected. According to the tuned circuit, it doesn't behave like a constant CS. The circuit was able to deliver 1mA to a 5kΩ load at 10MHz but circuit oscillation was observed with a higher load value (>5kΩ). A higher load voltage was observed when the load value was decreased (<5kΩ) and resulted in a load current of >1mA. This behaviour is shown in Figure 5.21, which represent the loading voltage across 2kΩ and 5kΩ load.

A similar transient response was noted for all tested frequencies with 5kΩ, 10kΩ and 15kΩ resistive load in parallel with 30pF, 50pF and 100pF loading capacitance. The only difference noted was the reduction of circuit frequency bandwidth with an increase in loading capacitance. It can be clearly seen from the above results that the output of the circuit doesn't clip even when a higher load (30kΩ) is attached. The bootstrapped improvement has resolved the lower driven load problem in the EHCS-GIC circuit without effecting other circuit performance parameter like frequency bandwidth and output impedance.

#### *5.5.2.3 Bandwidth and Output Impedance of Bootstrapped EHCS-GIC Circuit*

The unwanted loading capacitance involved in the circuit mainly effect the frequency bandwidth of the circuit. The result showed that the load current gives a peak amplitude response over a limited frequency bandwidth and was divided into different sets of tuneable settings to cover our selected frequencies. As long as the loading capacitance was smaller the peak amplitude of the output can cover a wideband of frequencies (at low frequencies only). As the loading capacitance increases the peak amplitude of the output reduced to a limited bandwidth. The EHCS-GIC circuit frequency bandwidth was observed with the loading capacitance and resistive load. Table 5.1 presents the overall frequency bandwidth of the bootstrapped EHCS-GIC circuit.

Table 5.1: Bootstrapped EHCS-GIC Circuit Frequency Bandwidth Response with 10pF loading capacitance

| $R_L$ | *-3dB Bandwidth (MHz)* | | *-1dB Bandwidth (MHz)* | |
|---|---|---|---|---|
| | *100Hz-1MHz* | *10MHz* | *100Hz-1MHz* | *10MHz* |
| 5kΩ | 2.61 – 2.66 | 4.55 | 1.33 – 1.35 | 2.34 |
| 10kΩ | 1.26 – 1.28 | 5.72 | 0.640 – 0.651 | 2.77 |
| 15kΩ | 0.828 – 0.843 | 6.09 | 0.422 – 0.430 | 3.17 |
| 20kΩ | 0.618 – 0.629 | 6.28 | 0.315 – 0.321 | 3.28 |
| 25kΩ | 0.493 – 0.502 | 6.38 | 0.252 – 0.256 | 3.35 |
| 30kΩ | 0.411 – 0.418 | 6.45 | 0.209 – 0.213 | 3.37 |

The output impedance of the bootstrapped EHCS-GIC circuit was calculated using Eq. (4.17), described in chapter 4.

Table 5.2: Output impedance of Bootstrapped EHCS-GIC Circuit with 10pF loading capacitance

| $R_L$ | ***Frequency* (Hz)** | | | | | |
|---|---|---|---|---|---|---|
| | ***100*** | ***1k*** | ***10k*** | ***100k*** | ***1M*** | ***10M*** |
| 5kΩ | 50M | 50M | 50M | 50M | 50M | 5.55M |
| 10kΩ | 11.11M | 20M | 20M | 20M | 11.1M | 6.19k |
| 15kΩ | 8.32M | 16.67M | 16.67M | 18.76M | 4.27M | 4.59k |
| 20kΩ | 7.68M | 15.38M | 15.38M | 16.67M | 3.12M | 4.06k |
| 25kΩ | 7.12M | 15.62M | 15.62M | 15.62M | 2.59M | 3.80k |
| 30kΩ | 6.64M | 14.99M | 14.99M | 14.99M | 2.26M | 3.64k |
| | ***Output Impedance* $Z_o$(Ω)** | | | | | |

Table 5.3: Output impedance of Bootstrapped EHCS-GIC Circuit with 30pF loading capacitance

| $R_L$ | *Frequency* (Hz) | | | | | |
|---|---|---|---|---|---|---|
| | ***100*** | ***1k*** | ***10k*** | ***100k*** | ***1M*** | ***10M*** |
| 5kΩ | 50M | 50M | 50M | 50M | 50M | 5M |
| 10kΩ | 11.11M | 20M | 20M | 20M | 5.00M | 5.55k |
| 15kΩ | 8.32M | 16.67M | 16.67M | 16.67M | 3.74M | 4.15k |
| 20kΩ | 7.68M | 15.38M | 15.38M | 15.38M | 3.32M | 3.69k |
| 25kΩ | 7.12M | 15.62M | 15.62M | 14.70M | 3.10M | 3.46k |
| 30kΩ | 6.64M | 14.99M | 14.99M | 14.27M | 3.04M | 3.32k |
| | ***Output Impedance* $Z_o$(Ω)** | | | | | |

Table 5.4: Output impedance of Bootstrapped EHCS-GIC Circuit with 50pF loading capacitance

| $R_L$ | *Frequency* (Hz) | | | | | |
|---|---|---|---|---|---|---|
| | ***100*** | ***1k*** | ***10k*** | ***100k*** | ***1M*** | ***10M*** |
| 5kΩ | 50M | 50M | 50M | 50M | 50M | 3.57M |
| 10kΩ | 11.11M | 20M | 20M | 16.67M | 3.99M | 5.54k |
| 15kΩ | 8.32M | 16.67M | 16.67M | 15.00M | 3.05M | 4.15k |
| 20kΩ | 7.68M | 15.38M | 15.38M | 14.28M | 2.73M | 3.69k |
| 25kΩ | 7.12M | 15.62M | 15.62M | 13.15M | 2.56M | 3.45k |
| 30kΩ | 6.64M | 14.99M | 14.99M | 13.03M | 2.45M | 3.32k |
| | ***Output Impedance $Z_o$(Ω)*** | | | | | |

Table 5.5: Output impedance of Bootstrapped EHCS-GIC Circuit with 100pF loading capacitance

| $R_L$ | *Frequency* (Hz) | | | | | |
|---|---|---|---|---|---|---|
| | ***100*** | ***1k*** | ***10k*** | ***100k*** | ***1M*** | ***10M*** |
| 5kΩ | 50M | 50M | 50M | 50M | 50M | 2.52M |
| 10kΩ | 11.11M | 20M | 20M | 12.5M | 3.99M | 4.34k |
| 15kΩ | 8.32M | 16.67M | 16.67M | 9.99M | 2.87M | 3.85k |
| 20kΩ | 7.68M | 15.38M | 15.38M | 9.08M | 2.49M | 3.30k |
| 25kΩ | 7.12M | 14.70M | 14.70M | 8.60M | 2.26M | 2.85k |
| 30kΩ | 6.79M | 13.62M | 13.62M | 8.55M | 2.10M | 2.50k |
| | ***Output Impedance $Z_o$(Ω)*** | | | | | |

Table 5.2 to Table 5.5 lists the calculated value of output impedance of the bootstrapped EHCS-GIC circuit at a selected frequency based on Pspice® simulation. The result shows that the calculated output impedance give an acceptable value of output impedance over a wide frequency bandwidth even at a higher load value. The presented result show that the output impedance remains stable for a wider bandwidth as long as the loading capacitance remains smaller.

Each bootstrapped EHCS-GIC circuit configuration, was tuned to give a peak output signal. For 5kΩ // 10pF loading, the 0.1-1kHz, 10kHz, 100kHz and 1MHz tuned configuration, showed a stable output impedance response and is ≈50MΩ. At 10MHz frequency, the output impedance reduces to 6MΩ. It showed a stable output impedance response through the tested frequency bandwidth. Above 5kΩ loading, the amplitude peak of the load current is clearer. The peak amplitude of the load current consequently

resulted in the peak amplitude response of the output impedance, for the corresponding tuned frequency. Using 10kΩ // 10pF loading, the output impedance of the circuit gives a peak amplitude response between the frequency range of 1k-100kHz and is ≈20MΩ, which is high enough and acceptable at this frequency/loading. For >100kHz frequencies, the output impedance of the circuit started decreasing in general but it gives the amplitude peak for its respective tuned frequency at a specific loading and is limited to a single frequency rather than a band of frequencies. At 1MHz, the output impedance of the circuit still gives an acceptable value of ≈11.1MΩ, but it drops down rapidly after 1MHz and reaches a low value up to 10MHz frequency. This behaviour is noted in all loads tested up to 30kΩ. The maximum achievable output impedance by this circuit setup, is ≈50MΩ with a 5kΩ loading.

A similar kind of response was observed for other tested loading capacitance in parallel with a fixed resistive loading. The results show that the output impedance was also effected due to the increase in loading capacitance. The output impedance was still high in MΩ's but its value was reduced due to amplitude decrease in the load current at a higher load. Graphical representations of the output impedance curve at fixed resistive load value with different loading capacitance, is shown in Figure 5.22.

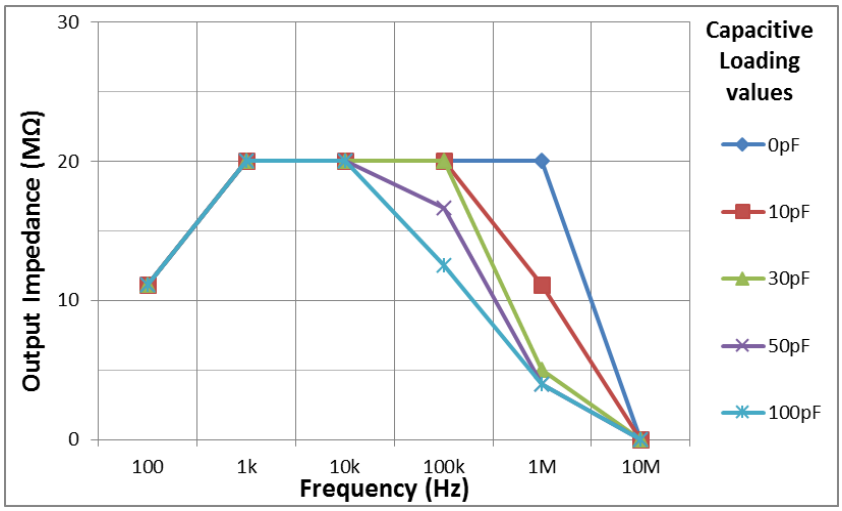



Figure 5.22: Bootstrapped EHCS-GIC circuit output Impedance with 10kΩ resistive loading

### 5.5.3 Bipolar Bootstrapped EHCS-GIC Current Source

The polarity of the CS depends upon the system requirements and are application specific. In case of BI/EIT system, common mode voltage at the input of amplifiers can be problematic. This common mode voltage can be higher than the measured differential

signal having different amplitudes. Therefore, to limit this problem, a differential/bipolar CS is recommended in most of the BI/EIT systems.

In any BI system, serial current injection is applied to two electrodes (McEwan et al., 2007) and the developed electric potential is measured on a different pair of electrodes. Differential current injection can be done in two ways:

1. Two external signals having a 180° signal phase shift with each other can be applied to two identical single-ended (referenced to ground) current sources to inject current.
2. One external signal is passed through an inverting amplifier configuration to obtain a 180° phase shift signal. Then the 0° and 180° signals can be applied to two identical single-ended current sources to inject current.

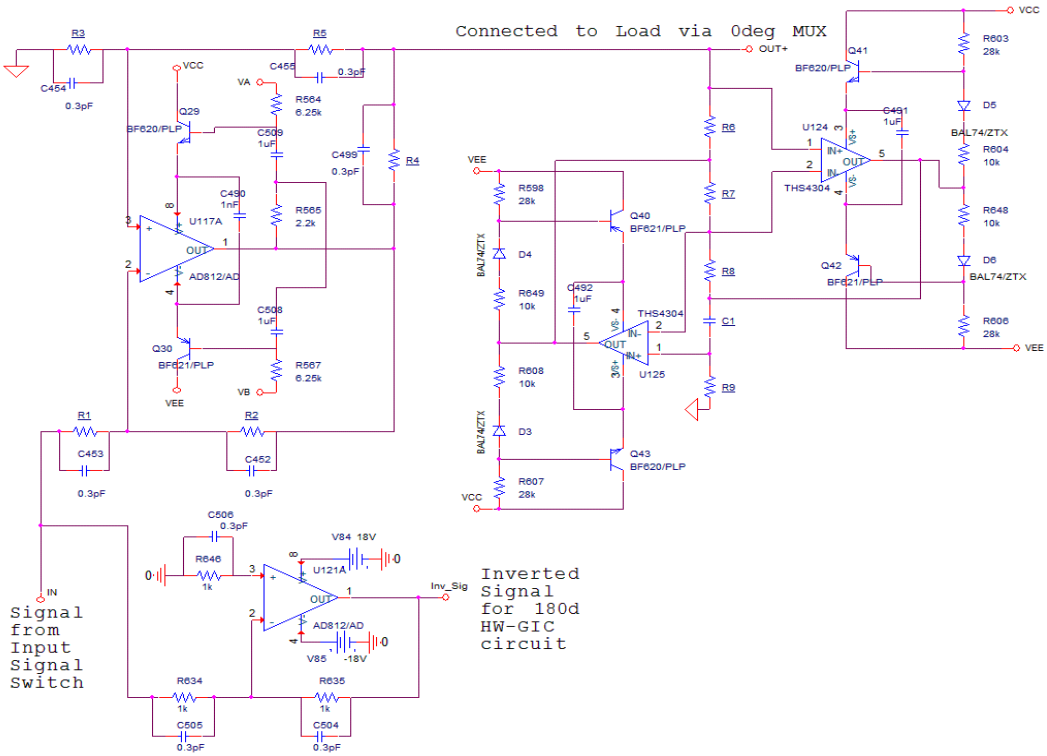
After achieving an acceptable level of performance in section 5.5.2 from single-ended bootstrapped EHCS-GIC circuit, the next step was to check the performance of a bipolar EH-GIC based CS. A bipolar-CS was found to be more complex because it is formed of two single-ended Howland-GIC current sources working in parallel. Hence, ignoring the complexity of the circuit the bipolar CS circuit was further investigated. The main motive was to achieve its good performance at multiple frequencies.

Bipolar bootstrapped EHCS-GIC circuit schematics and simulation was performed using a similar setup described in section 5.5.2. The second resistor-network configuration was used which satisfies the Howland circuit gain equation Eq. (5.14). To achieve a maximum circuit performance, the resistor $R_4$ and $R_5$ values were slightly varied to cover different frequency bands but alternatively it always satisfied the overall gain equation of the Howland circuit. For example, let's consider the frequency band, which covers the 100Hz and 1kHz frequencies. The resistors $R_1$, $R_2$ were set to 1kΩ. The resistors $R_4$, $R_5$ were set to 970Ω and 1.030kΩ respectively and resistor $R_3$ was set to 2kΩ. Substituting these resistor values in Eq. 5.14,

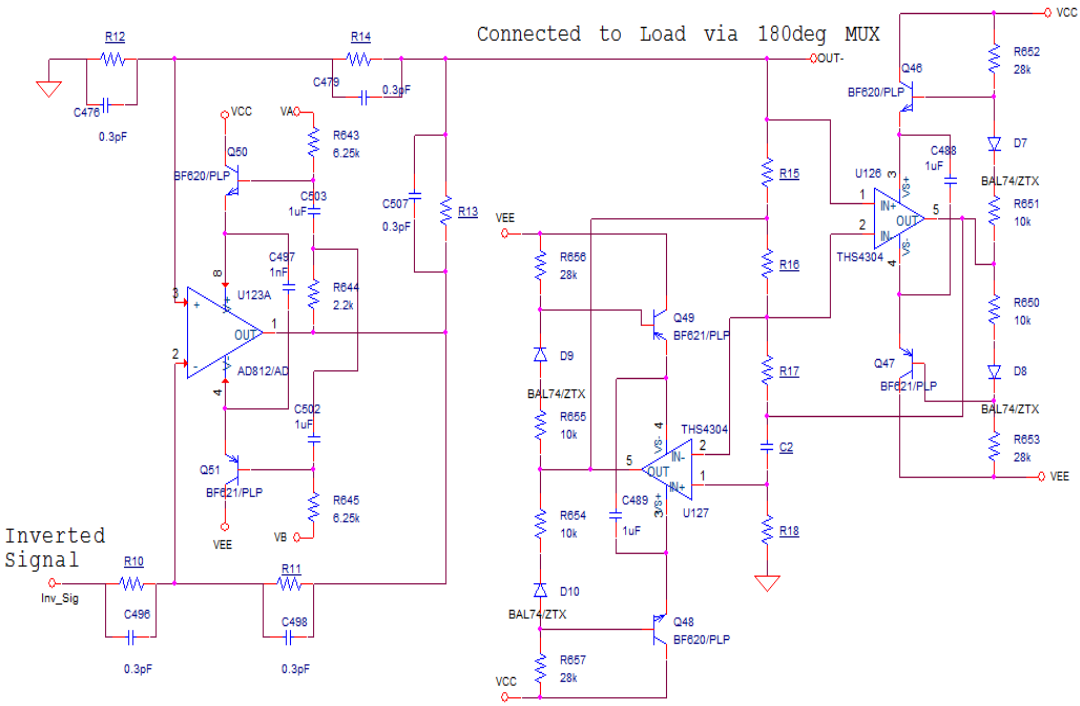
$$Gain = \frac{1k\Omega}{1k\Omega} = \frac{970\Omega + 1.030k\Omega}{2k\Omega} = 1 \qquad \text{Eq. (5.15)}$$

Similarly, the resistors in the 180deg part of the Howland circuit was set according to the configuration explained above. Two passive components in the EHCS part and three passive components in the GIC part were kept variable in the current source. These

components were tuned according to the required frequency range and optimised until the maximum possible simulated performance was achieved from the circuitry. The bipolar bootstrapped EHCS-GIC circuit simulation was performed with the circuit schematics as shown in Figure 5.23.




*a)* 0-deg EHCS-GIC circuit




*b)* 180-deg EHCS-GIC circuit

Figure 5.23: Bipolar Bootstrapped EHCS-GIC circuit simulation setup

### 5.5.3.1 AC Response of Bipolar Bootstrapped EHCS-GIC Circuit

The circuit shown in Figure 5.23 was operated with an AC sweep analysis. The simulation setup for the circuit was exactly same as described earlier in section 5.5.2.1. The bipolar circuit setting was also changed for different sets of frequencies to get the optimum performance of the source at a specific frequency. The same circuit tuning procedure was followed as described for a single-ended bootstrapped EHCS-GIC circuit and covers the same frequency groups described earlier. It was observed that due to the bandwidth limitation of the op-amp used, it was difficult to achieve any useful results at 10MHz. The bipolar EHCS-GIC circuit can achieve some good results at higher frequencies (i.e. b/w 2-4MHz) but in general will not be able to achieve very high frequency results. Although the frequencies between 2-4MHz were not simulated but it was expected that it can easily achieve good results from the current passive devices used in the EHCS-GIC circuit. The simulation results are shown from Figure 5.24 - Figure 5.28, describing the load current *($I_L$)* against its respective frequency sweep.

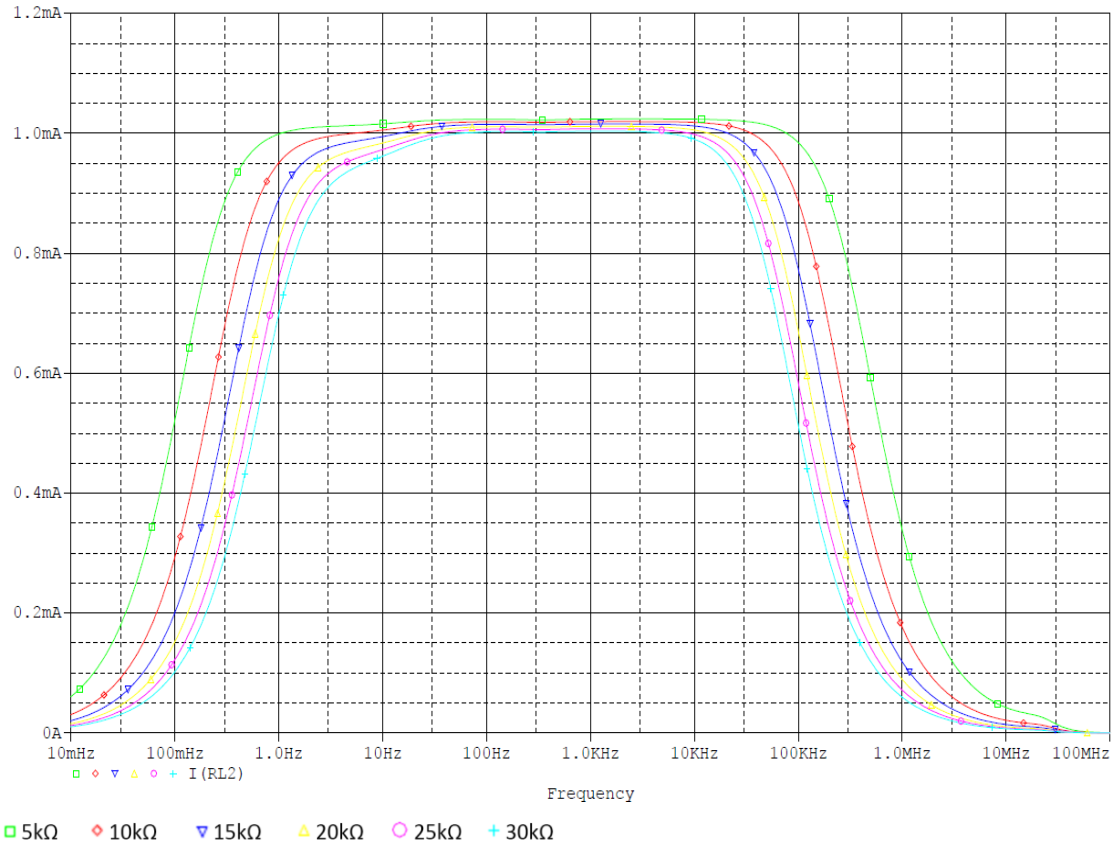



Figure 5.24: Bipolar Bootstrapped EHCS-GIC circuit AC response for 100Hz – 1kHz with 10pF loading capacitance

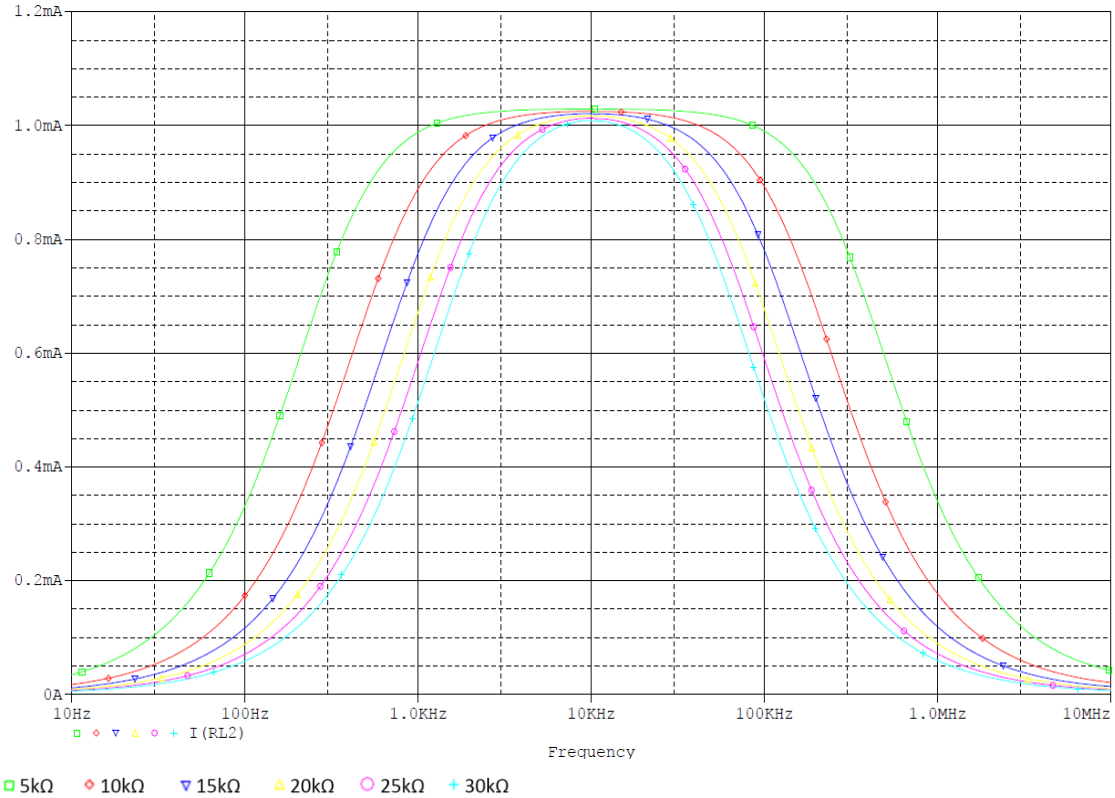



Figure 5.25: Bipolar Bootstrapped EHCS-GIC circuit AC response for 10kHz with 10pF loading capacitance

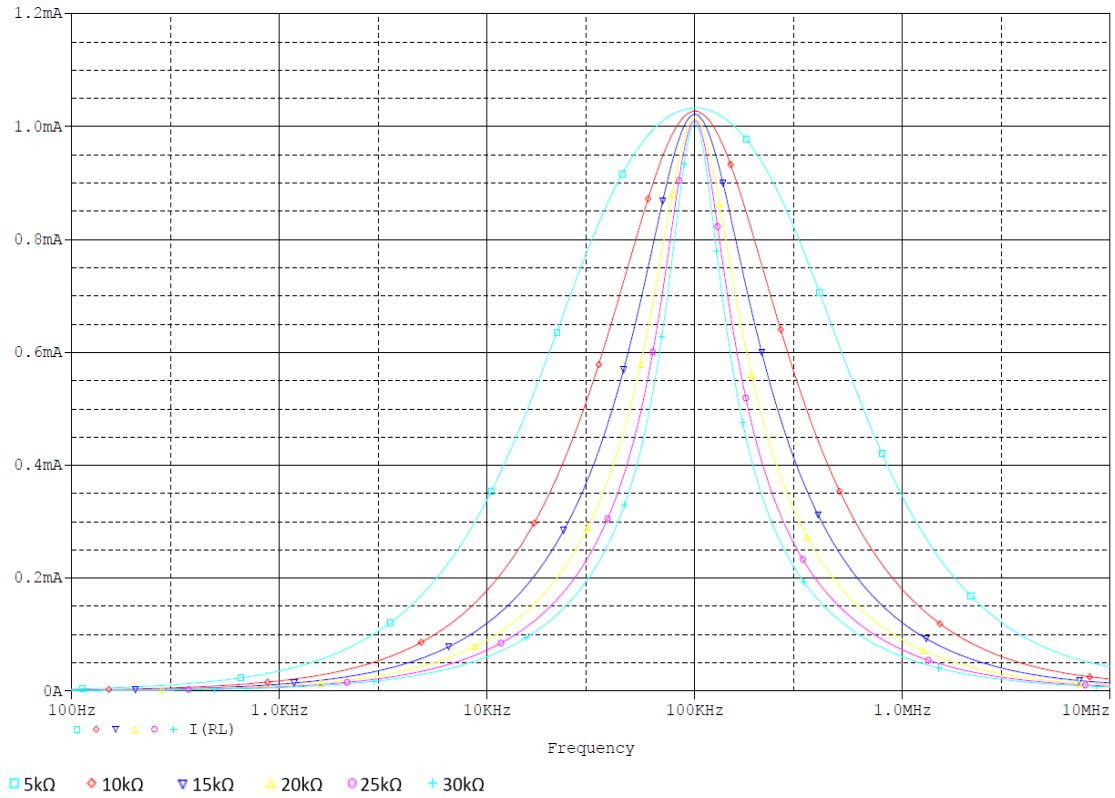



Figure 5.26: Bootstrapped EHCS-GIC circuit AC response for 100kHz with 10pF loading capacitance

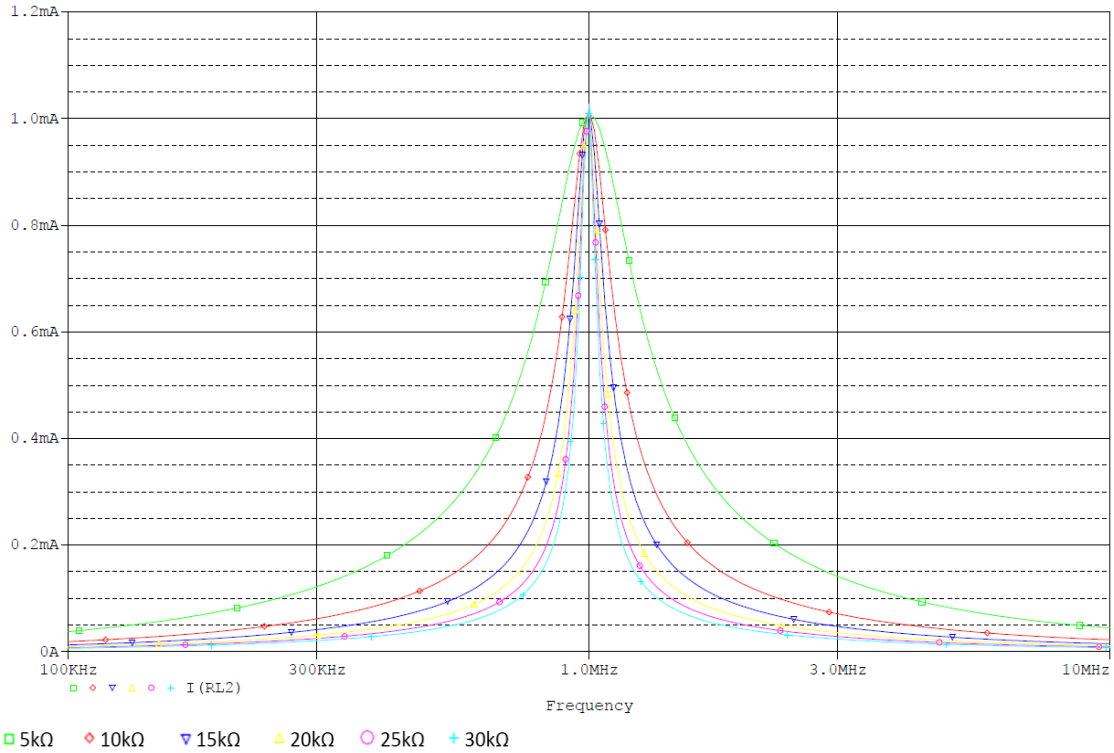



Figure 5.27: Bootstrapped EHCS-GIC circuit AC response for 1MHz with 10pF loading capacitance

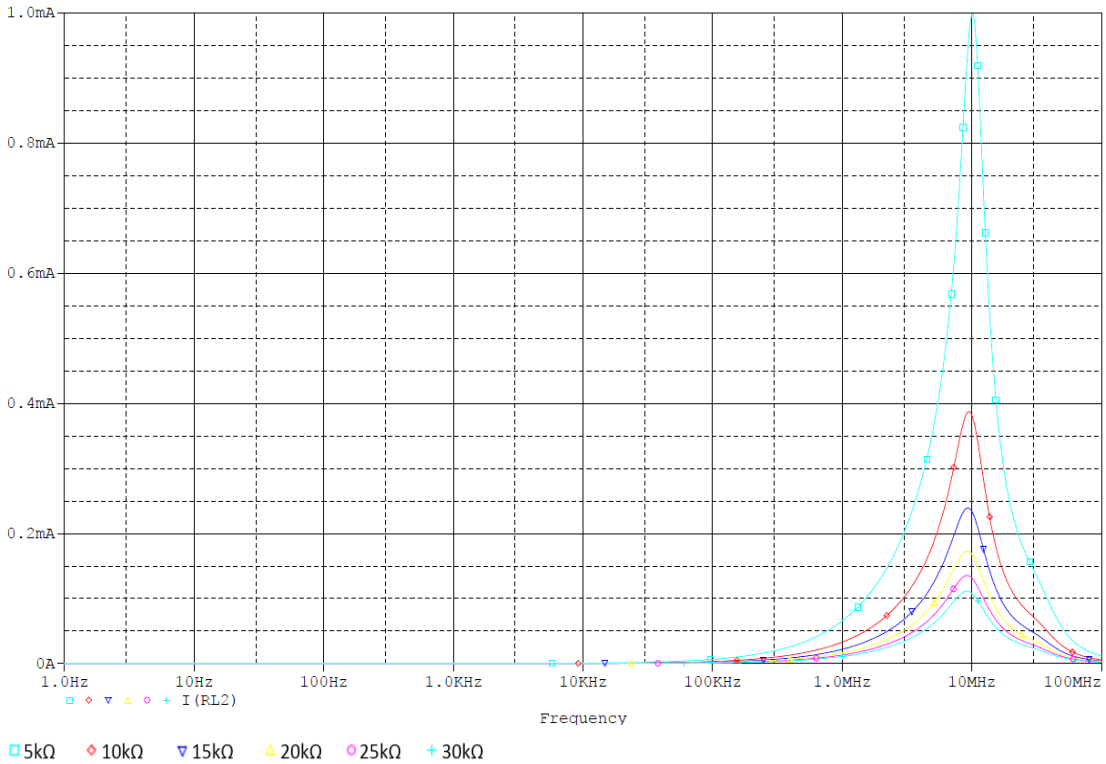



Figure 5.28: Bootstrapped EHCS-GIC circuit AC response for 10MHz with 10pF loading capacitance

The AC response of the bipolar bootstrapped EHCS-GIC circuit shows a similar behaviour to the AC response of a single-ended bootstrapped EHCS-GIC circuit. The

response shows a narrow frequency bandwidth and reasonable output impedance of the CS circuit. It was observed that the circuit configuration used for the frequency band between 0.1-1kHz gives a peak amplitude response between 107Hz to 2.8kHz, in the presence of additional 10pF capacitive and 5kΩ to 30kΩ resistive loading. Similarly, the circuit configuration used for the 10kHz frequency gives a stable peak amplitude response for frequencies between 9.5-10kHz. Above 10kHz, the peak amplitude response was limited to a specific single frequency (i.e. 100kHz, 1MHz and 10MHz). The circuit was tuned in the same pattern and similar behaviour was expected and observed for 30pF, 50pF and 100pF capacitive loading. It was concluded that the bipolar CS performance was also effected by the unwanted capacitance.

### *5.5.3.2 Transient Response of Bipolar Bootstrapped EHCS-GIC Circuit*

The AC response of the bipolar bootstrapped EHCS-GIC circuit was also validated using the transient analysis setup. The simulation was applied with a 1kHz, 10kHz, 100kHz, 1MHz and 10MHz signal having a 1V amplitude and 0V offset voltage simultaneously. The transient response of the circuit was checked with and without loading capacitance at different frequencies. This section presents the simulation results for different RC loading combinations (R=5kΩ, 10kΩ, 15kΩ and C=10pF). The transient responses of the circuit with the loading capacitance are shown in Figure 5.29-Figure 5.32, which describes the load voltage at respective frequency.

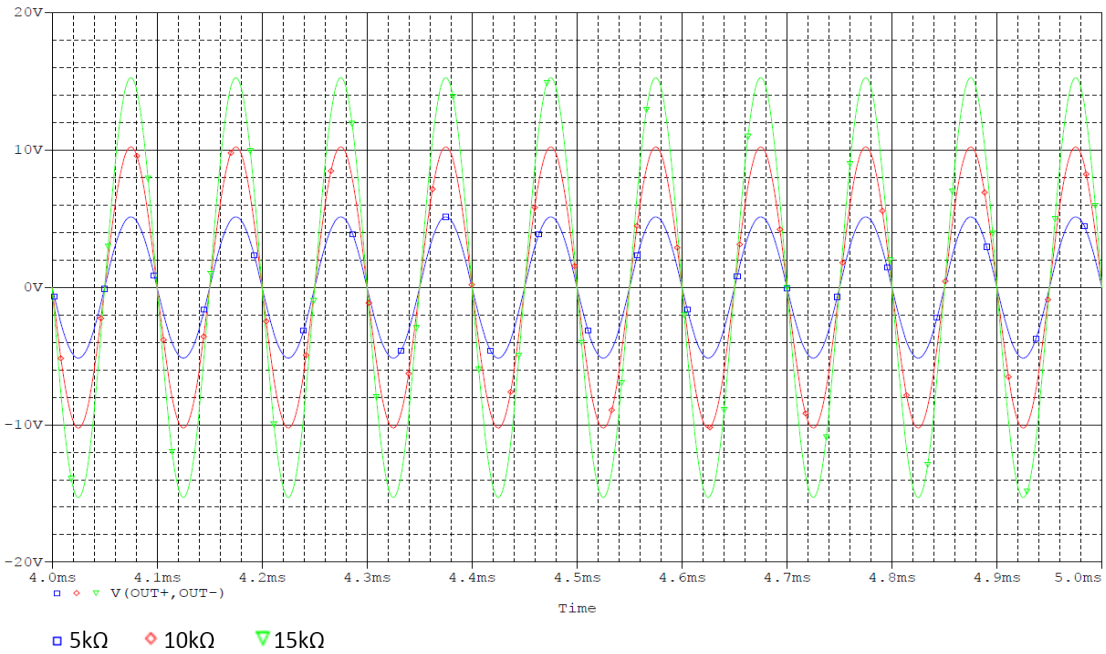



Figure 5.29: Bipolar bootstrapped EHCS-GIC circuit transient response at 10kHz with 10pF loading capacitance

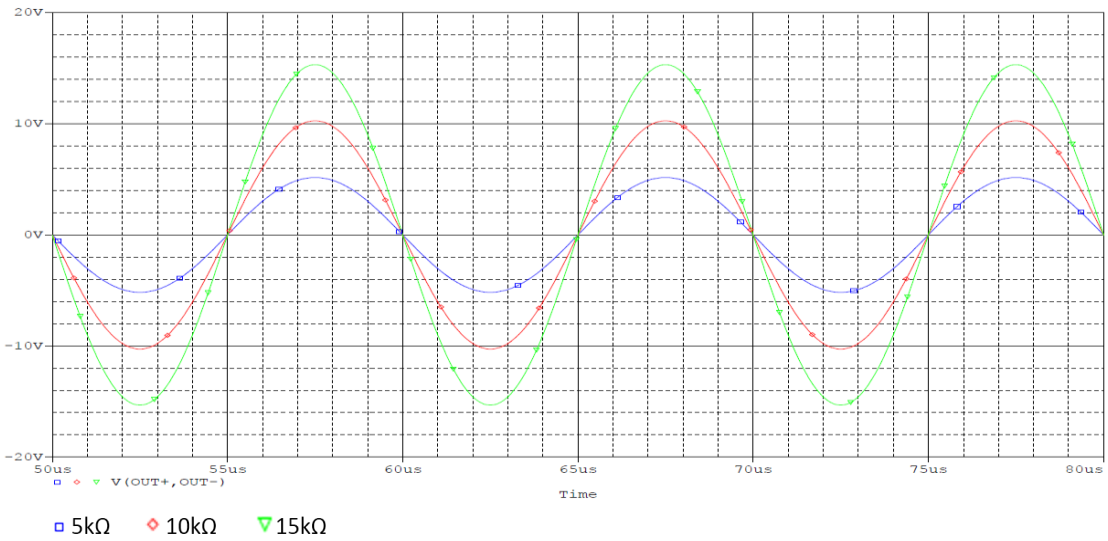



Figure 5.30: Bipolar bootstrapped EHCS-GIC circuit transient response at 100kHz with 10pF loading capacitance

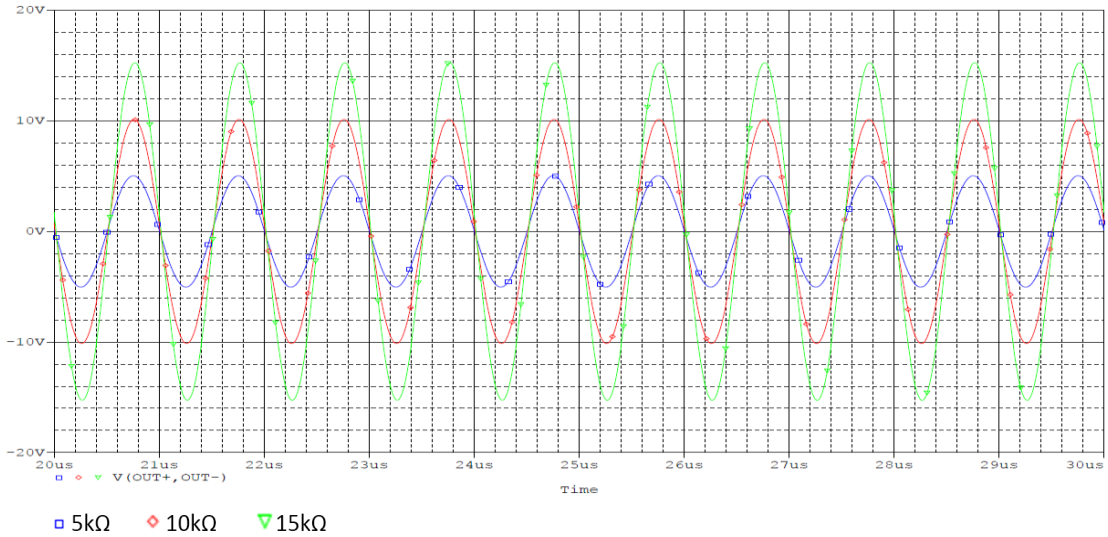



Figure 5.31: Bipolar bootstrapped EHCS-GIC circuit transient response at 1MHz with 10pF loading capacitance

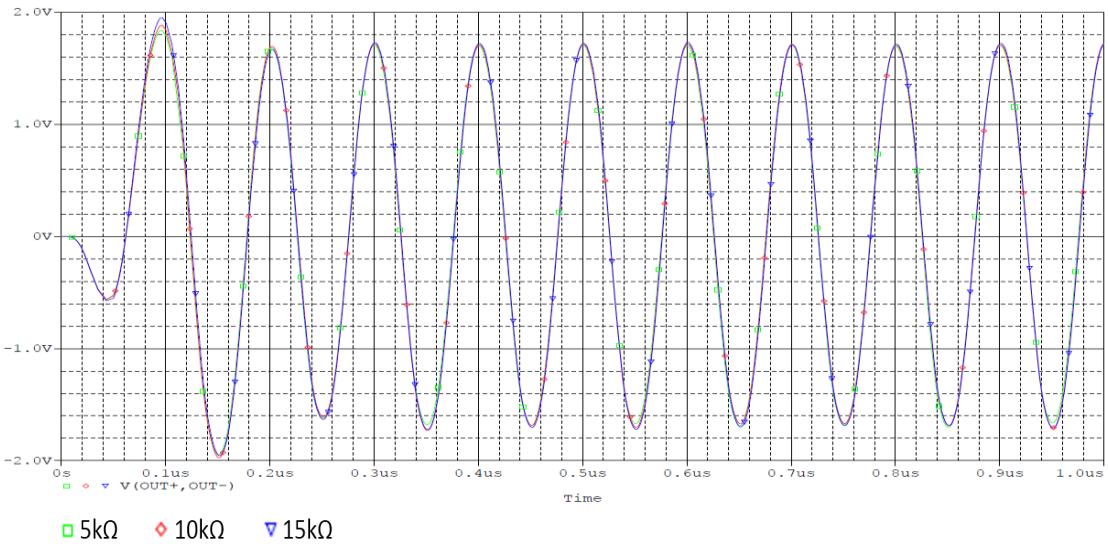



Figure 5.32: Bipolar bootstrapped EHCS-GIC circuit transient response at 10MHz with 10pF loading capacitance

The transient response of the circuit shows an overall good behaviour and is similar to the amplitude response of the single-ended CS. The voltage drop across the respective load indicates that the load current is ≈1mA, which was observed up to 1MHz and considered to be a good CS performance. A similar behaviour was observed for the frequencies slightly above 1MHz (i.e. 2-3MHz). The circuit performance was also observed at 10MHz and showed an unexpected performance. According to the AC response of the circuit, ≈1mA current was delivered to 5kΩ load. The current amplitude was decreased with an increased loading, and showed that the circuit was able to deliver 1mA current to ≤5kΩ load. The transient response of the same configuration showed that the voltage drop (≈1.7V) across the load was fixed irrespective of the attached load, and behaves like a constant VS circuit. Hence, it can be concluded that this circuit configuration for a constant CS is not suitable at higher frequencies, which is due to op-amp bandwidth and open loop gain limitations along with the capacitance involved in the circuit. This behaviour is shown in Figure 5.32, which represents the loading voltage across 5kΩ, 10kΩ and 15kΩ load.

A similar transient response was noted for all tested frequencies using the same resistive loads in parallel with 30pF, 50pF and 100pF capacitive loading. The reduction of the circuit frequency bandwidth was observed with an increase in loading capacitance. The above results clearly show that the output of the circuit doesn't clip even with a higher load (30kΩ) and can achieve good results until ≈3MHz frequency. The bootstrapped improvement has resolved the lower driven load problem in the bipolar EHCS-GIC circuit without effecting other circuit performance parameters like frequency bandwidth and output impedance.

#### *5.5.3.3 Bandwidth and Output Impedance of Bipolar Bootstrapped EHCS-GIC Circuit*

The effect of the loading capacitance was also observed in the frequency bandwidth and the output impedance of the bipolar EHCS-GIC circuit. According to the AC response, a peak amplitude response of the load current was observed using the circuit. Different frequencies bands were achieved by separate tuneable circuit settings. The result showed a reduction in the frequency bandwidth of the circuit with an increase in the loading capacitance. Table 5.6 gives the overall frequency bandwidth of the bipolar bootstrapped EHCS-GIC circuit.

Table 5.6: Bipolar bootstrapped EHCS-GIC circuit frequency bandwidth response with 10pF loading capacitance

| $R_L$ | *-3dB Bandwidth (MHz)* | | *-1dB Bandwidth (MHz)* | |
|---|---|---|---|---|
| | *100Hz-1MHz* | *10MHz* | *100Hz-1MHz* | *10MHz* |
| 5kΩ | 0.349 – 0.371 | 1.82 | 0.178 – 0.189 | 0.919 |
| 10kΩ | 0.175 – 0.184 | 1.69 | 0.090 – 0.094 | 0.848 |
| 15kΩ | 0.828 – 0.122 | 1.65 | 0.060 – 0.061 | 0.825 |
| 20kΩ | 0.117 – 0.092 | 1.63 | 0.045 – 0.045 | 0.814 |
| 25kΩ | 0.071 – 0.074 | 1.61 | 0.036 – 0.036 | 0.808 |
| 30kΩ | 0.059 – 0.062 | 1.61 | 0.030 – 0.029 | 0.804 |

The output impedance of the bipolar bootstrapped EHCS-GIC circuit was calculated using Eq. (4.17), as described in chapter 4 and is mentioned below.

Table 5.7: Output impedance of bipolar bootstrapped EHCS-GIC circuit with 10pF loading capacitance

| $R_L$ | *Frequency* (Hz) | | | | | |
|---|---|---|---|---|---|---|
| | ***100*** | ***1k*** | ***10k*** | ***100k*** | ***1M*** | ***10M*** |
| 5kΩ | 51M | 51M | 51M | 51.66M | 16.73M | 2.55M |
| 10kΩ | 12.74M | 25.49M | 25.63M | 25.69M | 8.39M | 12.17k |
| 15kΩ | 8.01M | 10.88M | 10.94M | 10.95M | 7.21M | 9.02k |
| 20kΩ | 3.31M | 3.75M | 3.70M | 3.70M | 3.16M | 7.99k |
| 25kΩ | 2.44M | 2.68M | 2.67M | 2.30M | 2.06M | 7.47k |
| 30kΩ | 2.07M | 2.25M | 2.26M | 2.10M | 1.99M | 7.16k |
| | ***Output Impedance $Z_o$(Ω)*** | | | | | |

Table 5.8: Output impedance of bipolar bootstrapped EHCS-GIC circuit with 30pF loading capacitance

| $R_L$ | *Frequency* (Hz) | | | | | |
|---|---|---|---|---|---|---|
| | ***100*** | ***1k*** | ***10k*** | ***100k*** | ***1M*** | ***10M*** |
| 5kΩ | 51M | 51M | 51M | 51.73M | 12.53M | 1.99M |
| 10kΩ | 12.74M | 25.49M | 25.63M | 25.71M | 7.17M | 11.88k |
| 15kΩ | 8.01M | 10.88M | 10.94M | 10.95M | 4.57M | 8.71k |
| 20kΩ | 3.31M | 3.75M | 3.70M | 3.17M | 2.76M | 7.69k |
| 25kΩ | 2.44M | 2.68M | 2.67M | 2.38M | 1.97M | 7.18k |
| 30kΩ | 2.07M | 2.25M | 2.24M | 1.80M | 1.49M | 6.88k |
| | ***Output Impedance $Z_o$(Ω)*** | | | | | |

Table 5.9: Output impedance of bipolar bootstrapped EHCS-GIC circuit with 50pF loading capacitance

| $R_L$ | *Frequency* (Hz) | | | | | |
|---|---|---|---|---|---|---|
| | ***100*** | ***1k*** | ***10k*** | ***100k*** | ***1M*** | ***10M*** |
| 5kΩ | 51M | 51M | 51.47M | 52.46M | 10.04M | 63.74k |
| 10kΩ | 12.74M | 25.49M | 20.50M | 20.83M | 6.71M | 9.09k |
| 15kΩ | 8.01M | 10.88M | 9.01M | 9.70M | 4.46M | 7.07k |
| 20kΩ | 3.31M | 3.75M | 3.51M | 3.07M | 2.67M | 6.36k |
| 25kΩ | 2.44M | 2.65M | 2.56M | 2.25M | 1.85M | 6.00k |
| 30kΩ | 2.09M | 2.23M | 2.18M | 1.64M | 1.45M | 5.78k |
| | ***Output Impedance $Z_o$(Ω)*** | | | | | |

Table 5.10: Output impedance of bipolar bootstrapped EHCS-GIC circuit with 100pF loading capacitance

| $R_L$ | *Frequency* (Hz) | | | | | |
|---|---|---|---|---|---|---|
| | ***100*** | ***1k*** | ***10k*** | ***100k*** | ***1M*** | ***10M*** |
| 5kΩ | 51M | 51M | 51.47M | 51.46M | 8.35M | 4.28k |
| 10kΩ | 7.84M | 8.49M | 25.63M | 14.56M | 5.57M | 3.05k |
| 15kΩ | 5.43M | 6.09M | 10.21M | 8.41M | 3.85M | 2.78k |
| 20kΩ | 2.77M | 2.93M | 3.63M | 2.67M | 2.36M | 2.67k |
| 25kΩ | 2.13M | 2.23M | 2.64M | 2.04M | 1.57M | 2.60k |
| 30kΩ | 1.84M | 1.93M | 2.23M | 1.53M | 1.24M | 2.56k |
| | ***Output Impedance $Z_o$(Ω)*** | | | | | |

Table 5.7 - Table 5.10 lists the calculated output impedance for the bipolar bootstrapped EHCS-GIC circuit at a specific frequency using Pspice® simulation. The result shows that the calculated output impedance gives an acceptable peak amplitude at different frequencies even at higher loads. The presented results show that the output impedance remains stable for a wider bandwidth as long as the loading capacitance remains minimum. For 5kΩ // 10pF loading, a stable output impedance (≈51MΩ) was observed for each tuned configuration (100Hz-1 kHz, 10kHz and 100kHz). The circuit tuned for 1MHz and 10MHz frequency gives a reduced output impedance of ≈17MΩ and ≈3MΩ respectively. It is noticed that the output impedance of the circuit shows a stable response for all tested frequencies with corresponding loading.

Above 5kΩ loading, the peak amplitude of the load current is clearer and resulted in a peak output impedance response for the corresponding tuned frequency. For 10kΩ // 10pF

loading, the bipolar circuit tuned for 100Hz to 1 kHz frequencies, gives a peak amplitude response (b/w 107Hz – 5kHz frequencies) of the output impedance and is ≈26MΩ. For 10 kHz tuned configuration, the circuit gives a peak amplitude response (b/w 9.5– 10kHz frequencies) of the output impedance and is ≈26MΩ, which is considered to be acceptable at this frequency. Above 100kHz, the circuit peak amplitude response was limited to a single frequency and reduction in the output impedance was observed for respective tuned frequency at a specific loading. At 100kHz and 1MHz, the output impedance of the circuit is ≈26MΩ and ≈8MΩ respectively. It dropped down rapidly after 1 MHz and reached a low value until 10MHz. This behaviour is noted in all tested loads (≤30kΩ). The maximum achievable output impedance by this bipolar circuit setup is ≈51MΩ with a 5kΩ and 10pF loading.

A similar response was observed for other RC loading combinations. The results show that the output impedance was effected due to the increase in loading capacitance. The output impedance was still high in MΩ's but its value was reduced due to amplitude decrease in the load current at a higher load. Graphical representation of the output impedance curve at a particular resistive and variable capacitive loading is given in Figure 5.33.

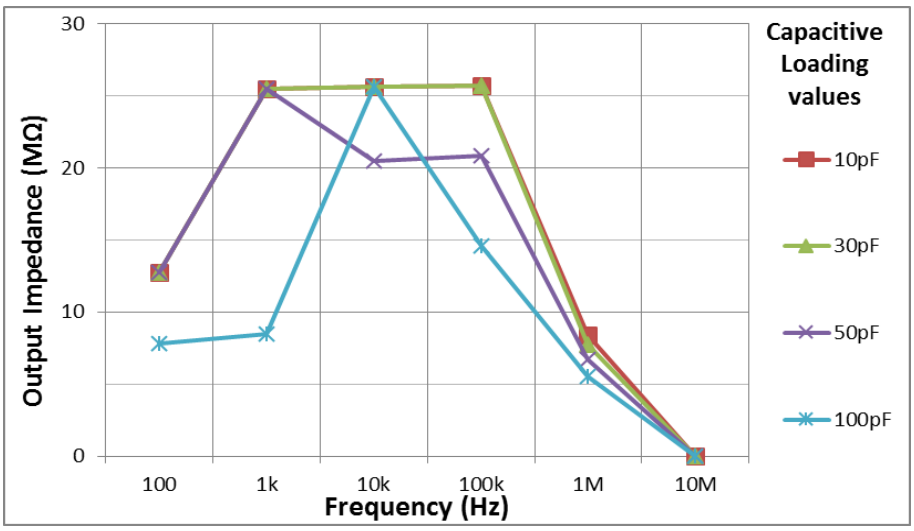



Figure 5.33: Bipolar bootstrapped EHCS-GIC circuit output impedance with 10kΩ resistive loading

## 5.6 High Frequency Discrete Component Current Source (DCCS)

The CS results presented earlier shows that it is difficult to achieve a high frequency bandwidth due to the non-linearity's involved with in the circuit. It can be seen that EHCS-GIC circuit can be used as a CS up to ≈2-3MHz and can be useful for low

frequency tuning system. The EIM system usually requires a high frequency and stable CS. The desired design specification for our high frequency CS was to work at 10MHz with the ability to deliver a 1mA current to large loads (>10kΩ). To achieve this performance, the voltage drop across the load and power supply to the circuitry must be >10V. It was also considered that the desired accuracy should be less than ±1% and the phase shift should be <1° regardless of the load attached with the CS. Considering the simulation results and from the literature review it is hard to use the EHCS principle and create a high frequency CS with this specification.

Another problem in using the EHCS circuit at this frequency is that it requires a high frequency op-amp. But most of the high speed amplifiers typically have a maximum ±5V for their power rails and will introduce the loading voltage problem in case of high load drive. By the use of a bootstrapping technique this problem can be overcome to some extent and the Howland based CS can achieve a frequency of ≈2–3MHz.

Therefore, a CS was designed using discrete components and uses a GA technique to achieve a high frequency and high output voltage signal. The principle is that the source will essentially create a voltage across a resistor and uses a GA of gain near one to maintain this voltage that results in a flow of 1mA current through the attached load. This principle is shown using an E-OrCAD component (used to simulate ideal op-amp response with selectable open loop gain) schematic shown in Figure 5.34, configured as follower op-amp.

In the first step, a voltage signal is directly applied between the terminal A and B (highlighted in Figure 5.34). The AC response showed a voltage drop of 10V across the load, which reflect a passage of 1mA current. The phase response of the circuit was observed to be very small for the frequencies >30Hz. In the next step, it was decided to choose an indirect way to make the oscillator appears as if it was floating and being driven by the GA (red rectangle highlighted in Figure 5.34). This entails having an oscillator referenced to earth and translating the voltage through a cascade circuit so that it appears across resistor (113R) that is being driven by the GA. The bottom of this 113R drives the 1 kΩ resistor that sets the current driven into the load. The amplitude and phase responses of the circuit after the floating oscillator circuitry also shows a very good response that can easily achieve a frequency bandwidth of >30MHz with very small phase shift above 30MHz, as shown in Figure 5.35. It can be concluded that a high open-loop gain and input

impedance amplifier designed using discrete components, can be used to design a constant high frequency CS (10MHz). In our actual used circuit, the E-part was replaced with a nearly equivalent part created with discrete components.

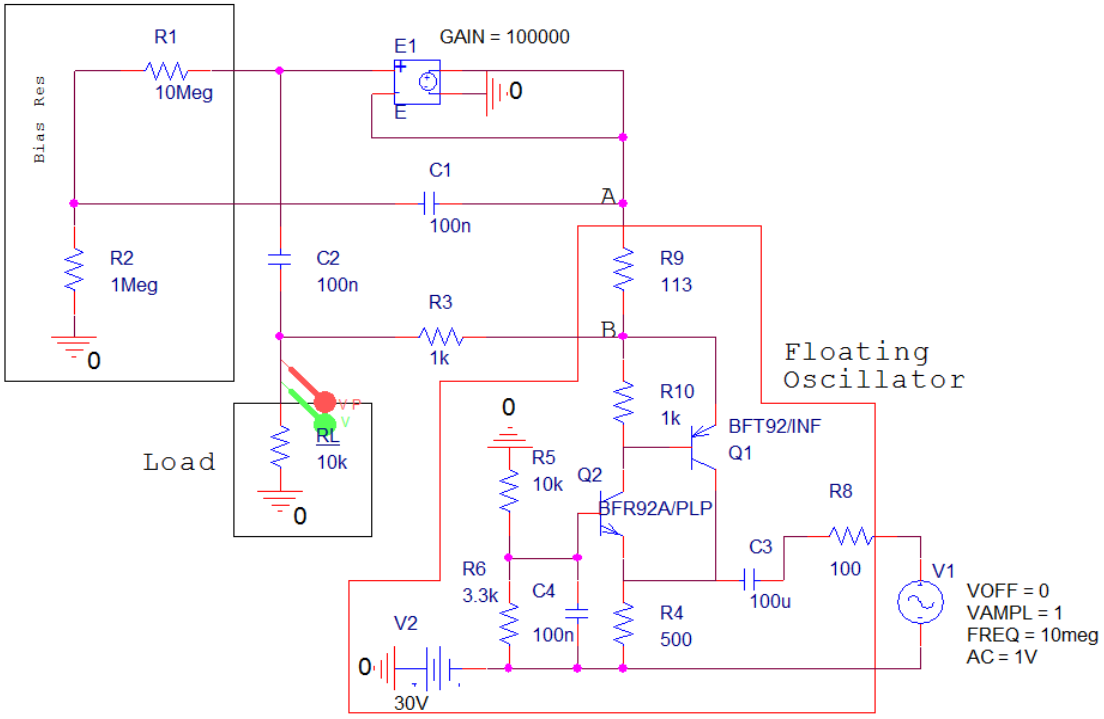



Figure 5.34: High frequency discrete component source principle

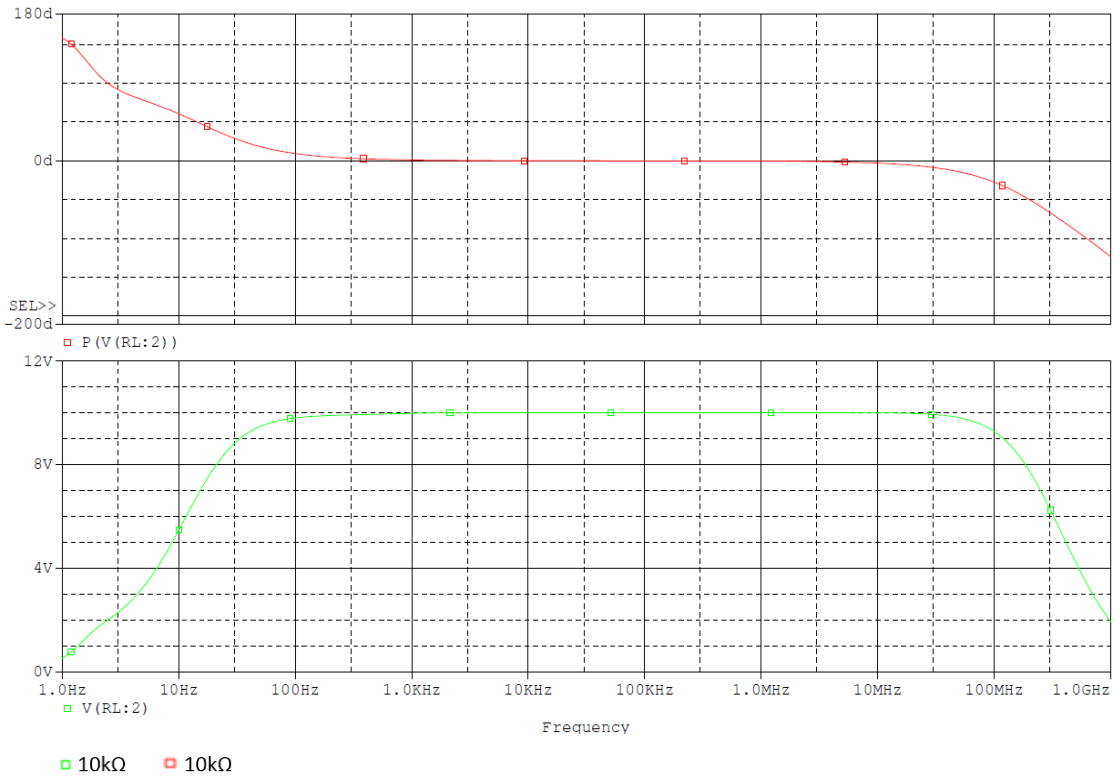



Figure 5.35: High frequency (10MHz) discrete component source with floating oscillator: Phase Response (top), Load voltage amplitude (bottom)

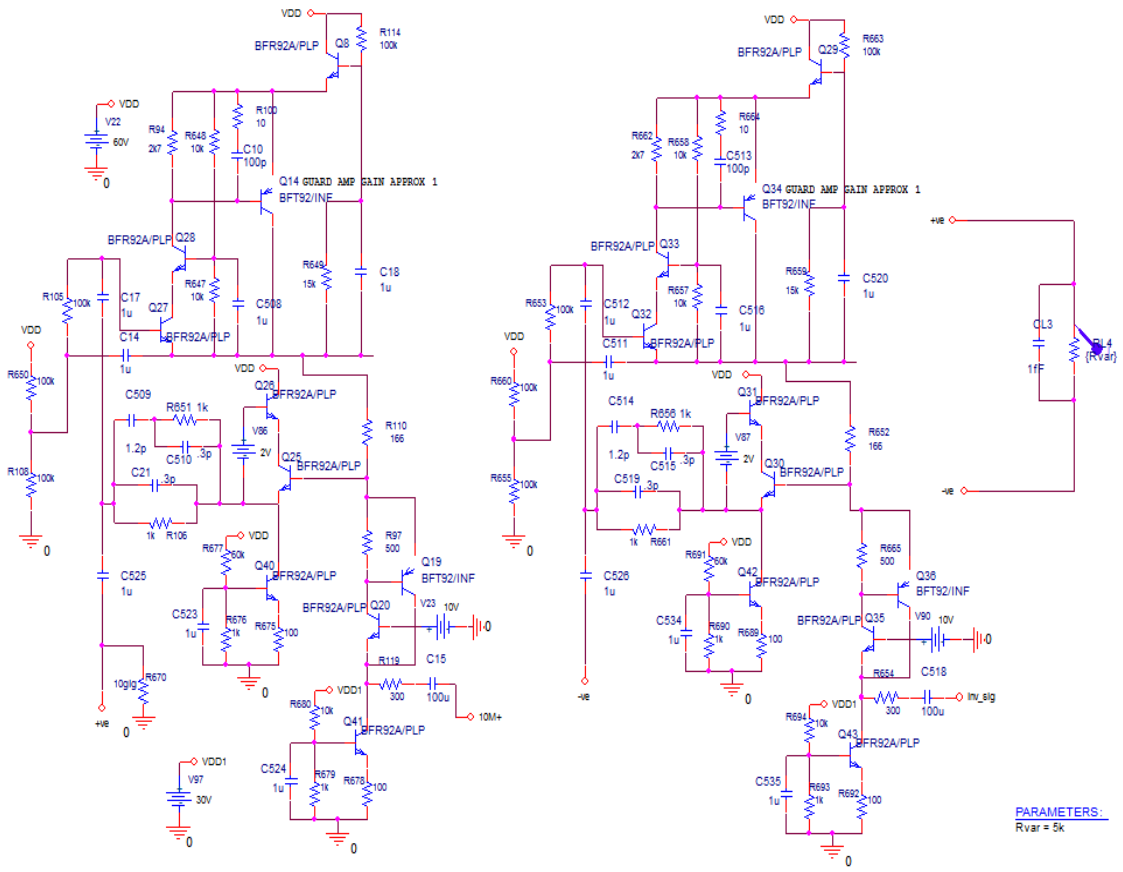



Figure 5.36: High frequency discrete component current source

Figure 5.36 shows the schematic of the high frequency CS with discrete components. This circuit is designed using a high frequency and high voltage transistor so that it can achieve a high amplitude output signal at higher frequency. The circuit simulation was performed to test a bipolar configuration. The inverted input signal was achieved by an inverting op-amp (OPA656) circuit. Both 0° and 180° signal were applied simultaneously to the load.

## 5.6.1 AC Response of DCCS Circuit

The circuit shown in Figure 5.36 was operated with an AC sweep analysis setup with a 2V AC-signal. The power rail *($V_{DD}$)* in the circuitry was set to 60V without any noise included. One internal bias voltage *($V_{DD1}$)* was set to 36V. The load resistance *($R_L$)* was changed from 5k-30kΩ. It was noticed that the Howland circuit generates some output capacitance, which affects the performance of the circuit in addition to the loading capacitance. It was expected that the DCCS will have minimum output capacitance and affect in the overall performance of the circuit. The circuit was simulated with possible loading capacitances of: 10pF, 30pF, 50pF and 100pF. To cancel the effect of loading capacitance, the circuit was simulated with a parallel inductor to observe its performance

at high frequency. The main focus was to see whether the DCCS can deliver an acceptable amplitude of output signal at high frequency or not?

The AC response of the bipolar DCCS circuit, shows a good performance with an acceptable amplitude of the load current. It was observed that the circuit can achieve a frequency bandwidth of >30MHz, with minimum circuit capacitance and can easily deliver 1mA load current at 10MHz. Alternatively, with any unwanted circuit capacitance along with its cancellation method, this circuit was still able to deliver 1mA current but over a narrow frequency bandwidth/specific frequency. A better output impedance response of the source was observed due to its ability to deliver 1mA current to all tested loads. The phase response of the circuit was observed and found to be very small (<2%) for all tested loads. The circuit was simulated in the same pattern and similar behaviour was expected and observed for 30pF, 50pF and 100pF loading capacitance. Hence it was concluded that a constant DCCS can be practically designed, which can deliver 1mA current up to ≈20MHz frequency. By applying a suitable capacitance cancellation method, the circuit will be able to deliver high amplitude current at 10MHz, which the Howland circuit was unable to achieve due to the op-amp bandwidth limitation and other non-linearities involved in the circuit. The amplitude and phase response are shown in Figure 5.37 & Figure 5.38, which describes the load current *($I_L$)* and the phase shift against its frequency sweep respectively.

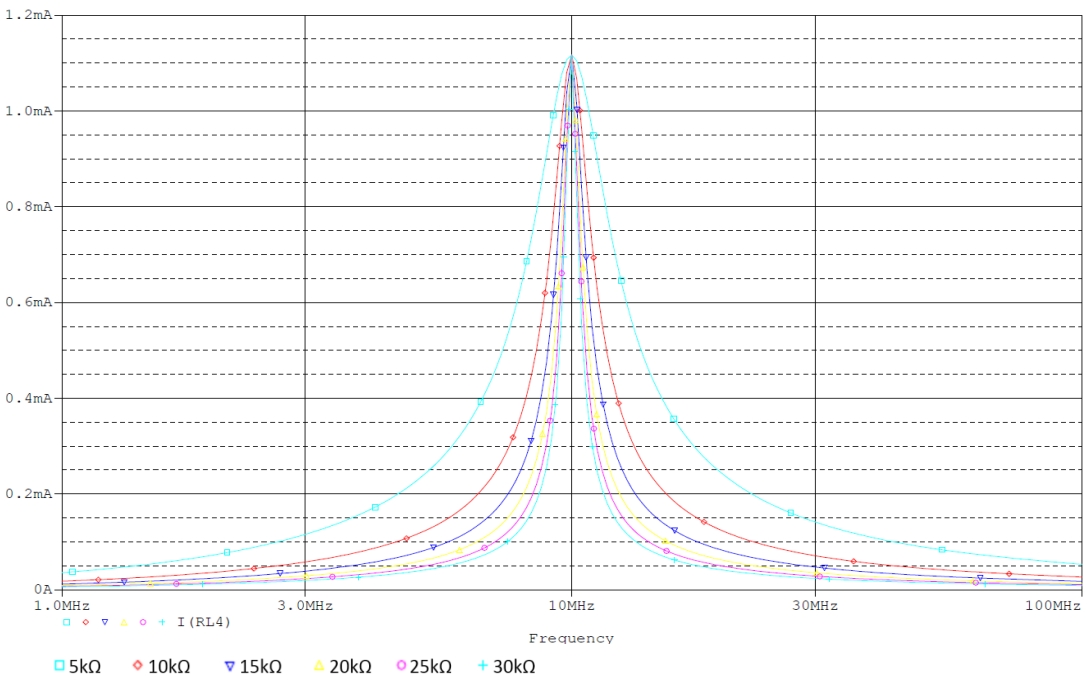



Figure 5.37: High frequency DCCS circuit AC response with 10pF loading capacitance

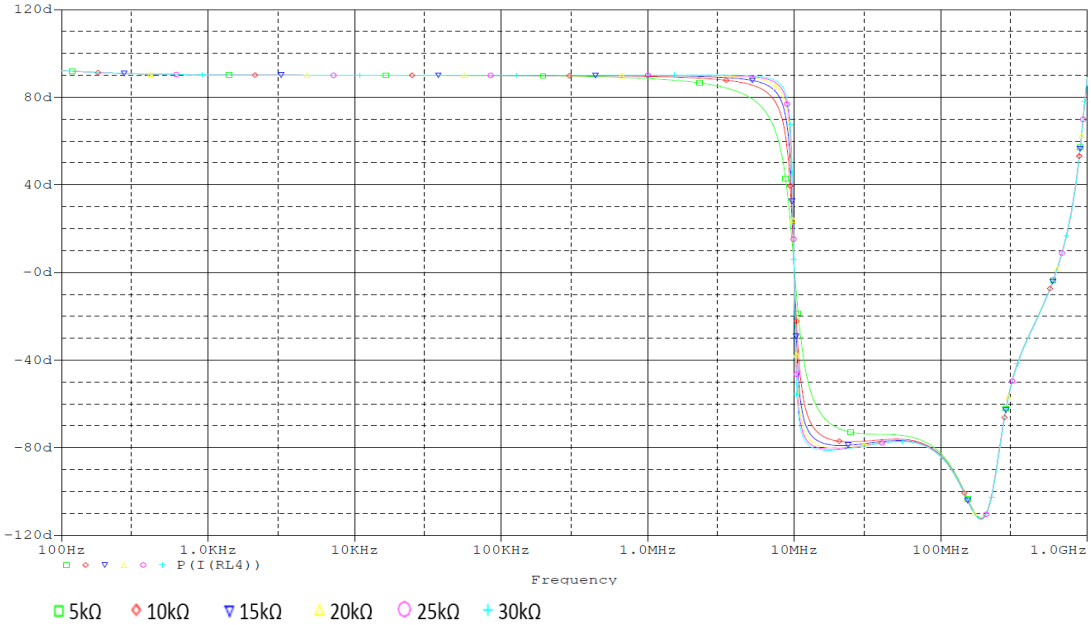



Figure 5.38: High frequency DCCS circuit phase response with 10pF loading capacitance

## 5.6.2 Transient Response of DCCS Circuit

The AC response of the bipolar DCCS was validated using a transient analysis setup. The tested loads were 5kΩ, 10kΩ, 15kΩ and 30kΩ with different loading capacitance. The simulation was applied with a 10MHz signal having a 2V amplitude and 0V offset voltage. The circuit was initially tested with a 10pF capacitive loading along with the above mentioned resistive loads. Using the capacitance compensation method, the circuit showed a good load current amplitude over a limited frequency bandwidth/specific frequency. The corresponding voltage drop across a wide range of tested loads indicate that 1mA current was passed through the load. It was observed that the DCCS can deliver 1mA current at higher load (30kΩ), demonstrated by ±30V load voltage amplitude shown in Figure 5.39. Therefore, this circuit can be considered as a good CS circuit at this frequency with a suitable capacitance cancellation method.

A similar transient response was observed at 10MHz for same resistive loads in parallel with 30pF, 50pF and 100pF loading capacitances. The reduction of the circuit's frequency bandwidth curve was observed with increase in loading capacitance. It can be concluded that a high frequency constant CS circuit can be implemented by careful selection of the discrete components. The transient response of the circuit with the corresponding loading capacitance is shown in Figure 5.39, which describe the load voltage at particular frequency.

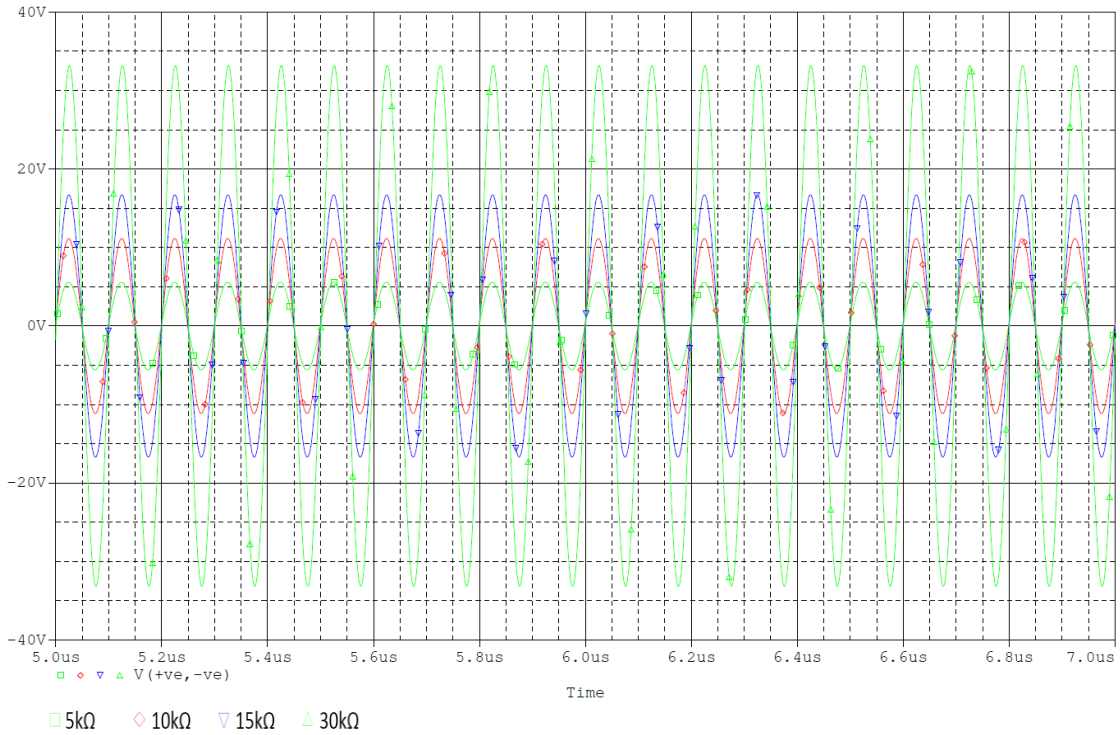



Figure 5.39: Transient response High frequency CS circuit at 10MHz with 10pF loading capacitance

## 5.6.3 Bandwidth and Output Impedance of DCCS Circuit

Like the Howland circuit, the DCCS circuit frequency bandwidth is also effected due to the loading capacitance but it still gives a good load current amplitude peak at 10MHz frequency. The DCCS circuit achieved a frequency bandwidth of >30MHz without any loading capacitance. In the presence of loading capacitance, the DCCS circuit showed a peak amplitude response of the load current over a limited frequency bandwidth. As long as the loading capacitance was small, the output amplitude peak achieved with the DCCS circuit can cover a wide band of high frequencies. With the increase in loading capacitance, the output amplitude peak reduced to a limited bandwidth and became sharper. The DCCS circuit bandwidth was observed with the loading capacitance in parallel with a fixed resistive load. The output impedance of the high frequency DCCS circuit was calculated from the same procedure explained earlier using Eq. (4.17). Table 5.11 gives the frequency bandwidth and output impedance performance of the high frequency DCCS circuit.

The result shows a reasonable output impedance response at high frequency even at higher load. It was noticed that the output impedance was stable at different loads irrespective of the loading capacitance effect. This shows that the circuit performance will not be effected by loading capacitance, with a precise compensation circuit. Graphical

representations of the output impedance curve at a particular load value is given in Figure 5.40 for different loading capacitances.

Table 5.11: Bandwidth and Output impedance Response of DCCS at 10MHz frequency

| $R_L$ | *Bandwidth (MHz)* | | *Loading Capacitance (F)* | | | |
|---|---|---|---|---|---|---|
| | *-3dB* | *-1dB* | *10p* | *30p* | *50p* | *100p* |
| 5kΩ | 3.17 | 1.61 | 56M | 56M | 56M | 56M |
| 10kΩ | 1.58 | 0.792 | 19M | 19M | 19M | 19M |
| 15kΩ | 1.06 | 0.528 | 17M | 17M | 17M | 17M |
| 20kΩ | 0.790 | 0.378 | 14M | 14M | 14M | 14M |
| 25kΩ | 0.636 | 0.259 | 12M | 12M | 12M | 12M |
| 30kΩ | 0.532 | 0.194 | 10M | 10M | 10M | 10M |
| | ***With 10pF loading capacitance*** | | ***Output Impedance $Z_o$(Ω)*** | | | |

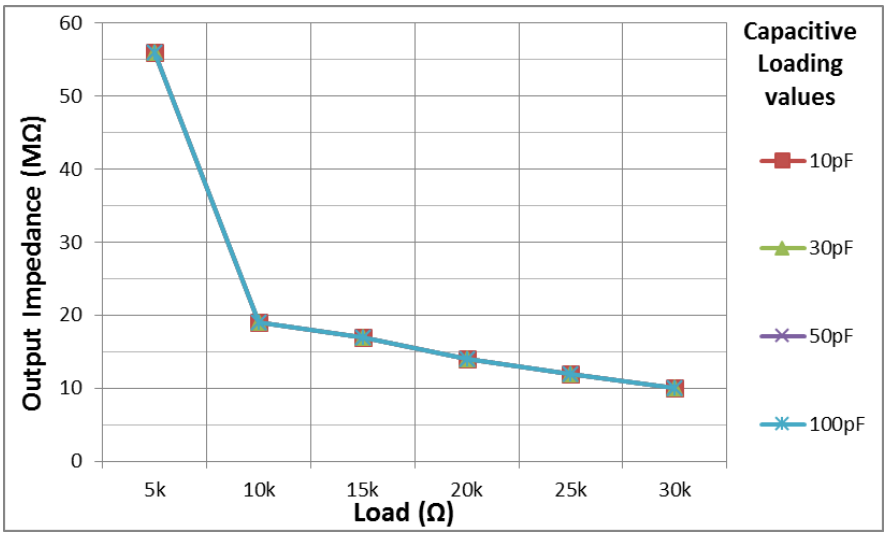



Figure 5.40: Bipolar DCCS circuit output impedance at 10MHz

## 5.7 Summary

This chapter was based on the problems identified in chapter 4. It was described in chapter 4 that the Howland circuit topologies were affected by the loading voltage and the circuit was not able to deliver a high amplitude output signal to the attached load. The circuit was also not able to achieve a high frequency bandwidth.

This chapter presented a bootstrapping technique to overcome the loading voltage problem. Upon application of the bootstrapping technique to the EHCS and EHCS-GIC

circuit, it was proven by simulation results that the circuit output doesn't clip even when a higher load is (up to 30kΩ) attached with both circuits. The bootstrapped improvement has resolved the lower driven load problem in both CS circuits.

This chapter further presented the GA technique to eliminate/minimise the unwanted capacitance introduced by the switches and multiplexer. The technique was explained and demonstrated by simulation to illustrate the concept. The GA simulation result showed that a voltage of ±30V was dropped across the load at 10MHz, which indicates that the technique had helped in cancelling the unwanted capacitance for 30kΩ load.

The design of the bootstrapped EHCS-GIC circuit was also presented in this chapter. The simulation presented for the circuit shows a good performance and can be considered as a good CS over a limited frequency bandwidth due to circuit tuning involved in the GIC part, to cancel the unwanted capacitance. This bipolar configuration was not able to achieve a high frequency bandwidth and was limited to ≈2-3MHz. The output impedance achieved by this circuit gave an acceptable value up to 1MHz and was unable to improve at high frequency (10MHz), which leads us to explore other options for high frequency CS design.

Finally, the chapter presented a high frequency DCCS. The simulation result showed that the DCCS circuit was able to achieve good performance. It showed that the voltage dropped across a 5kΩ and 30kΩ load was 5V and 30V, which proved that the CS was able to deliver 1mA current at 10MHz with phase response of <2% accuracy. The next step was to validate the simulation results of both circuits using experimental measurements.

Chapter 6 will address an excitation system based on a voltage source for the EIT system. The purpose of the VS design is to minimise the design complexity involved in the CS circuit and improve its performance parameters. The chapter will also present a design for a differential voltage measurement circuit.

# Chapter 6

# Development of Optimised Voltage Source Design for an EIT System

## 6.1 Introduction

In bio-impedance/EIM system, multiple frequencies are required for voltage and current measurement through which permittivity and conductivity of the observed region is reconstructed. Literature shows that breast tissues interesting features mostly can be found and can possibly be best explored above 1MHz (Jossinet, 1998). As a result, it leads the researcher to design a wide frequency bandwidth excitation source, which can cover higher frequencies (>1MHz). Therefore, to study tissue whose characteristics can be best explored at high frequencies, there impedance measurement system should be able to take measurements at high frequency (≤10MHz) to effectively distinguish the different breast tissues. The excitation source is an essential component in any impedance measurement system. If currents are injected, then voltages on some or all electrodes are measured. If voltages are applied, then current through the active electrodes are measured (Halter et al., 2004; Hartov et al., 2001). The EIM system requires an applied and measured signal with high precision. It was suggested in the literature that to maximize the distinguishability and SNR of an EIT imaging date set, a multiple and high-precision current sources are required (Saulnier et al., 2006; Isaacson, 1986). Many current sources of these kinds have been developed in the past for these bio-impedance systems (Ross et al., 2003; Hartov et al., 2000; Cook et al., 1994). Mostly these current sources had limited bandwidth, and were limited to apply only a sinusoidal excitation signal and high precision components were required. Further, due to additional complex trimming circuits, current source performance is degraded. As a result, it's difficult to achieve high precision and high output impedance (Tong et al., 2007; Ross et al., 2003). Over a wide frequency bandwidth, the system precision is also degraded. It was shown in chapter 4 & 5 that the CS design becomes more complex when additional loading capacitance was

minimised with additional circuitry. This has resulted in an electronics package having a large footprint, high component power and cooling costs.

Current source problems can be overcome and implemented by a high precision voltage controlled voltage source (VCVS) using a broadband op-amp (Yoo et al., 2010; Halter et al., 2008; Saulnier et al., 2006; Halter et al., 2004; Hartov et al., 2001). The VCVS circuit design mostly is easier to implement with less cost as compared to the current source. But it should be considered that a less optimal impedance measuring system will be achieved by voltage application and measuring its resulting current. To apply a desired optimal current pattern, an algorithm was developed for employing multiple voltage sources (Saulnier et al., 2006; Choi et al., 2003). While designing a voltage source it is desirable to know the applied voltage and its resulting current with a high precision. A low output impedance is expected from the voltage source while maintaining a constant voltage drop across the SUO and should be independent of the load impedance. The system, which requires specific current signals will use the iterative method of applied voltage adjustment to compensate the changes in load impedance. These systems require the ability of precise measurement of applied voltage and current rather than aiming to have a low output impedance of the voltage source.

This chapter presents three VCVS design circuitries. Based on initial voltage sources simulation results, the circuit with better acquired frequency bandwidth will be further researched to design and implement a differential voltage source for a bio-impedance system (Qureshi et al., 2012d). The research will also consider other performance parameters and effort will be made to achieve a high precision and stable excitation source based on VCVS. The proposed voltage source design will have the ability to sense current. The voltage source will be able to provide variable gain and controllable feedback current. Voltage gain of the system can be set as pre-requirement and will be used to acquire feedback current. The current passing through the load can be controlled through the feedback path (Qureshi et al., 2012b). This chapter mainly focuses on voltage source circuit frequency bandwidth with other circuit performance parameters: output impedance, SNR, phase response. The intended specification for voltage source design is to maintain a frequency bandwidth of >15MHz irrespective of the attached load in the presence of additional load capacitance. Another intention is to maintain low output impedance of the source at high frequencies without any oscillation in the circuit. Initial

simulation results will be presented to establish the frequency bandwidth of the voltage source with other circuit performance parameter.

This chapter also discusses the bipolar voltage source design based on a variable gain and controllable feedback current circuit. To avoid the loading problem like the current source, the bootstrapping technique will also be integrated with the voltage source circuit. This scenario may arise if an increase in the voltage gain or amplitude increase of the input signal can lead the circuit output signal to saturate. This additional circuit will prevent the output of the op-amp from saturation. The voltage source circuits are explained and their output is compared in terms of better frequency bandwidth and output impedance of the circuit based on Pspice® simulation. To measure the resulting voltage across the load, a differential amplifier circuit is also designed and presented in this chapter. A bootstrapped differential amplifier using an op-amp IC and with discrete components to measure high amplitude signals are also presented. This work takes into account the influence of different design parameters in the voltage source circuit over the frequency range of 100kHz to 15MHz. This will improve the implementations of practical voltage sources used in electrical bio-impedance systems.

## 6.2 Voltage Source Architecture

To implement a voltage source with an integrated current measurement capability, the most common architecture is to use an op-amp configured as a unity gain buffer with a current sensing resistor ($R_s$) included in the feedback path (Yoo et al., 2010; Halter et al., 2008; 2004; Saulnier et al., 2006). The proposed voltage source in this chapter is slightly different from the voltage source found in the literature. This source will have an ability to sense the injecting current into the object along with the ability to control the maximum amount of current passing through the load via feedback resistors ($R_f$ & $R_g$). The voltage source can give a voltage gain depending upon the requirements of the system. Three voltage source architectures were considered and based on their bandwidth comparison, the architecture, which will provide higher frequency bandwidth, will be considered for differential voltage source design and implementation (Qureshi et al., 2012b; Qureshi et al., 2012d). These voltage source architectures are shown in Figure 6.1.

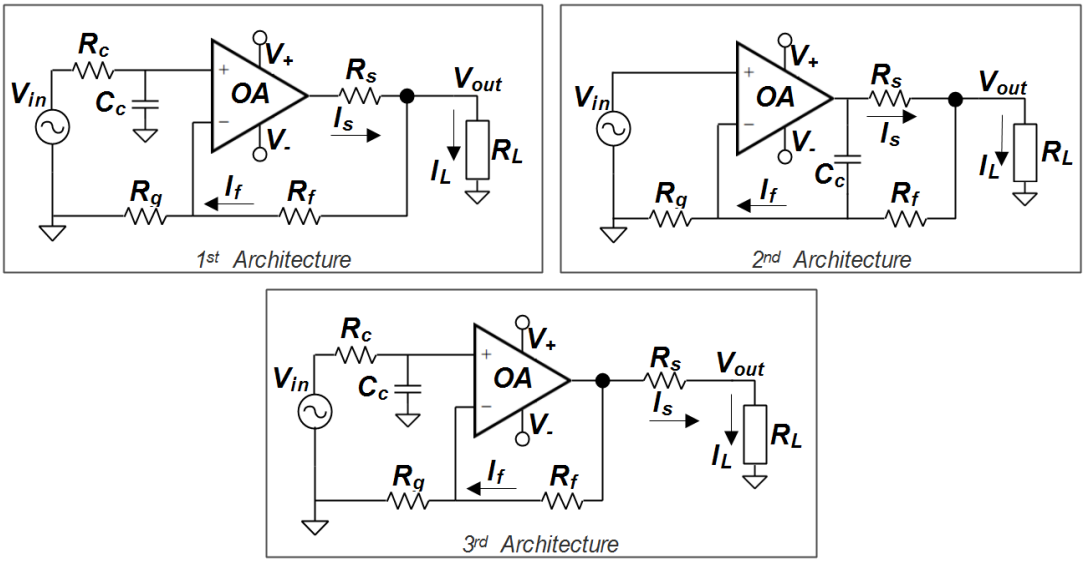



Figure 6.1: A Single-end voltage source circuit architectures

The architectures shown in Figure 6.1 were simulated with exactly the same circuit parameters and optimised until acceptable results were achieved. The circuits were simulated with a loading capacitance of 10pF, 30pF, 50pF and 100pF parallel with variable resistive load (5kΩ-30kΩ with ΔR=5kΩ). The initial bandwidth result using the above architectures show that the first architecture provides better performance over a wide range of frequency bandwidth as compared to the other two architectures. The detailed initial frequency bandwidth results achieved from the above architectures are given in the Table 6.1.

Table 6.1: Voltage Source Circuit Initial Frequency Bandwidth Response

| $R_L$ (kΩ) | -3dB Bandwidth (MHz) | | | Load Capacitance (pF) |
|---|---|---|---|---|
| | 1st Architecture | 2nd Architecture | 3rd Architecture | |
| 5 - 30 | 23.92 – 23.96 | 19.88 – 20.29 | 16.69 – 15.41 | 10 |
| 5 - 30 | 24.15 – 24.17 | 16.84 – 17.13 | 11.69 – 10.61 | 30 |
| 5 - 30 | 24.34 – 24.38 | 14.86 – 14.98 | 8.25 – 7.49 | 50 |
| 5 - 30 | 24.81 – 24.85 | 11.60 – 11.63 | 4.51 – 4.21 | 100 |

The results shown in Table 6.1 show that the 1st architecture of the voltage source gives a stable frequency bandwidth response across wide range of test resistive load irrespective of the loading capacitance effect. The average bandwidth was found to be ≈ 24–25MHz. Therefore, the 1st architecture shown in Figure 6.1 was selected to design the differential voltage source. The detailed source performance results were established, which are described in the simulation section of this chapter.

Circuit analysis of the voltage source circuit is done by initially considering that the shunt impedance ($Z_s$) is infinite. The op-amp is considered to be ideal with infinite input resistance, gain and zero input capacitance. Under this condition, the voltage dropped across attached load ($V_{out}$) will be an amplified signal and is equal to the input voltage ($V_{in}$) times the voltage gain of the circuit specified by feedback resistors. The load current ($I_L$) will be the difference of sense resistor current ($I_s$) and feedback resistor current ($I_f$). This load current can be determined by measuring the voltage across $R_s$ and $R_f$ and then evaluating Eq. 6.1.

$$I_L = I_s - I_f \qquad \text{Eq. (6.1)}$$

By ideal op-amp behaviour and by applying the voltage divider rule at node $V_{out}$, the following expression can be written,

$$I_f = I_g = \frac{V_{in}}{R_g} \qquad \text{Eq. (6.2)}$$

$$V_{out} = \left(1 + \frac{R_f}{R_g}\right) V_{in} \qquad \text{Eq. (6.3)}$$

Therefore, Eq. 6.1 can be expressed as,

$$I_L = \frac{V_{op_out} - V_{out}}{R_s} - \frac{V_{in}}{R_g} \qquad \text{Eq. (6.4)}$$

By solving Eq. 6.4, the load current ($I_L$) can be expressed as,

$$I_L = \frac{V_{op_out} R_g - V_{in}\left(R_s + R_g + R_f\right)}{R_s R_g} \qquad \text{Eq. (6.5)}$$

The unknown resistance / impedance can be found by evaluating the ratio of voltage dropped across load ($V_{out}$) and load current ($I_L$) and can be expressed as,

$$R_L = Z_L = \frac{V_{out}}{I_L} = \frac{\left(R_g + R_f\right) V_{in} R_s}{V_{op_out} R_g - V_{in}\left(R_s + R_g + R_f\right)} \qquad \text{Eq. (6.6)}$$

It can be seen from Eq. 6.5 & 6.6 that the load current ($I_L$) and unknown resistance ($R_L$) are both dependent on the op-amp output voltage. Therefore, solving Eq. 6.4, for op-amp output voltage gives,

$$V_{op_out} = \left[\frac{R_s R_L + (R_s + R_L)(R_g + R_f)}{R_g R_L}\right] V_{in} \qquad \text{Eq. (6.7)}$$

Eq. 6.7 shows that the op-amp output voltage is directly dependent upon the attached load. Its output amplitude varies with the change in attached load. This concludes that the load current $(I_L)$ is also dependent upon the attached load and will vary for different loads while maintaining a constant voltage drop due to the feedback path of the op-amp at the node where load is attached.

Practically, a differential amplifier will be used across the sense resistor $(R_s)$ to indirectly measure how much current was generated from the op-amp for the object. Another differential amplifier will be used across a feedback resistor $(R_f)$ to measure the amount of feedback current. The difference of $I_s$ and $I_f$ will be used to know the amount of current injected into the SUO. The op-amp output voltage varies with the change of the sense resistor $(R_s)$, as mentioned in Eq. 6.7. Firstly, the voltage gain of the system is set according to our requirement. Theoretically, the maximum current (i.e. 1mA) will pass through the load when the ratio of load and voltage gain becomes 1. That will be the case, which can be considered as the minimum value of load attached to the source with a maximum current of 1mA passing through it. The optimum value of $R_s$ can be found by fixed $V_{op_out}$ in Eq. 6.7 and can be expressed as,

$$R_s = \frac{V_{op_out} R_g R_L - (R_g + R_f) R_L V_{in}}{V_{in}(R_L + R_g + R_f)} \qquad \text{Eq. (6.8)}$$

Now consider the case in which the op-amp has a finite gain, which means that the output voltage will not be exactly equal to the applied input voltage. This requires measurement of the output voltage with a high precision. This problem arises due to the presence of unknown shunt impedance. Due to this shunt impedance, the load current $(I_L)$ will not be exactly the difference of $I_s$ and $I_f$ as it was in the ideal case. The shunt impedance $(Z_s)$ models the resistance/capacitance between the output of the voltage source and ground. This includes stray capacitance/resistance introduced by the PCB board, input impedance of the active devices, capacitance and finite shunt resistance introduced by the additional measuring circuit connected at the output etc. Due to this shunt impedance to ground, some of the current will flow through $Z_s$ to ground and will result in less current delivered

to the attached load $(R_L)$ as expected theoretically. The difference current $(I_{diff})$ can be denoted as,

$$I_{diff} = I_s - I_f - I_L \qquad \text{Eq. (6.9)}$$

Rearranging Eq. 6.9 for $I_L$ gives,

$$I_L = I_s - I_f - I_{diff} \qquad \text{Eq. (6.10)}$$

The voltage dropped across the shunt impedance node will be the same as the voltage dropped across the load. Therefore, it can be concluded that by the knowledge of $V_{out}$ , $I_s$ , $I_f$ and $Z_s$ , the actual amount of current delivered to the load can be computed. The voltage source circuit was further researched to implement a bipolar excitation source and its results are presented later in section 6.4 of this chapter.

## 6.3 Differential Amplifier Design for Voltage Measurement

A differential amplifier (DA) is also called a difference amplifier because it amplifies the difference between two signals. A multi-transistor amplifier is also considered to be a differential amplifier. It is considered as a fundamental block in any analogue circuit. This configuration virtually forms the differential amplifier of the input part of an op-amp. The configuration is used to provide high voltage gain and high common mode rejection ratio. Its other characteristics are very high input impedance, low offset voltage and low input bias current. DA can operate in two modes: common mode and differential mode. Common mode will result in zero output while differential mode will result in high output. The DA can be implemented with op-amp, BJTs, MOSFET and MESFETs.

The main purpose of a DA in this work is to measure a high amplitude output signal with high precision. Therefore, a DA was intended to measure a signal with ≈100$V_{p\text{-}p}$ at a high frequency (10MHz) with a phase shift of <1%. To obtain a high amplitude signal, the DA circuit was bootstrapped like the current source circuit in chapter 5. This research will focus on designing the differential amplifier with op-amp and through BJTs only to meet the system requirement. The differential amplifier using one op-amp is presented in Figure 6.2. The resistors $R_1$, $R_2$ and $R_f$ are the input resistors for the inverting, non-inverting terminal and feedback resistor of the op-amp.

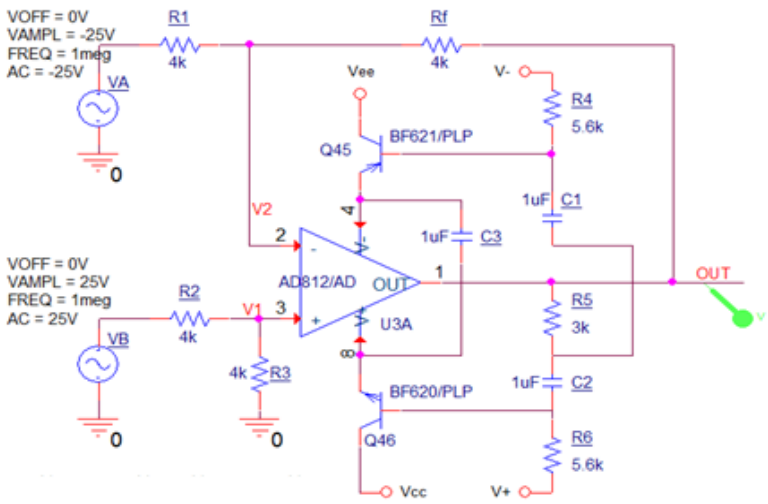



Figure 6.2: A single op-amp based differential amplifier

The voltage gain of the DA using one op-amp is derived as follows. The circuit shown in Figure 6.2 is a combination of inverting and non-inverting amplifier. By applying the superposition theorem, finding the output voltage of both configurations separately and then adding them together will give the output voltage of the DA. By eliminating $V_B$, the circuit will become an inverting amplifier, the output voltage due to $V_A$ can be expressed as,

$$V_{out_A} = -\left({R_f}/{R_1}\right)V_A \qquad \text{Eq. (6.11)}$$

By eliminating $V_A$, the circuit will become a non-inverting amplifier, the output voltage due to $V_B$ can be expressed as,

$$V_{out_B} = \left(1 + \frac{R_f}{R_1}\right)V_1 \qquad \text{Eq. (6.12)}$$

$V_1$ is the voltage at the non-inverting terminal. By applying the voltage divider rule at node $V_1$, Eq. 6.12 can be rewritten as,

$$V_{out_B} = \left(1 + \frac{R_f}{R_1}\right)\left(\frac{R_3}{R_2 + R_3}\right)V_B \qquad \text{Eq. (6.13)}$$

Assuming that $R_1 = R_2$ and $R_3 = R_f$ then,

$$V_{out_B} = -\left(\frac{R_f}{R_1}\right)V_B \qquad \text{Eq. (6.14)}$$

The overall output voltage and gain of the DA can be expressed as,

$$V_{out} = -\left(\frac{R_f}{R_1}\right)(V_A - V_B) \qquad \text{Eq. (6.15)}$$

$$A_v = \frac{V_{out}}{V_A - V_B} = -\left(\frac{R_f}{R_1}\right) \qquad \text{Eq. (6.16)}$$

**AC Response:** The circuit shown in Figure 6.2 was operated with an AC sweep analysis with two out of phase AC signals of amplitude ±25V. The power rails for all the active elements (AD812) in the circuitry were bootstrapped and will be a function of the op-amp output signal source without any noise included. The power rails ($V_{CC}$ and $V_{EE}$) of the bootstrapped circuit were set to ±200V. The bias voltages ($V_+$ and $V_-$) were set to ±36V DC. The output voltage was recorded at the output node (*OUT*) without any load resistance. The simulation results are shown in Figure 6.3, describing the output voltage amplitude and the phase response against frequency sweep respectively.

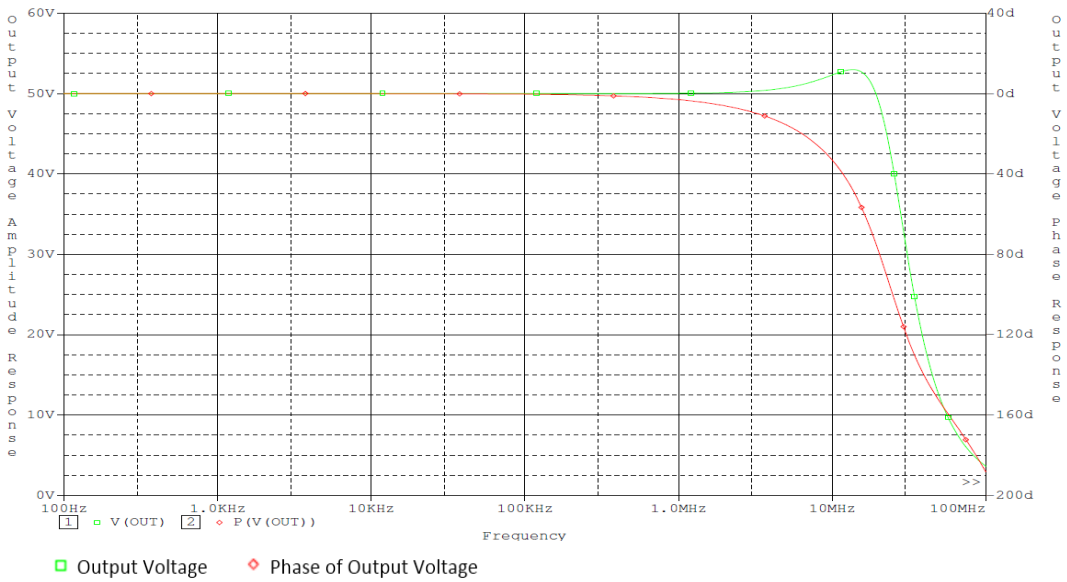



Figure 6.3: AC response based on differential amplifier using one op-amp

The AC response shows that the DA circuit gives good frequency bandwidth performance over a wide range ≈26.62MHz. The phase response of the circuit was also in an acceptable range. It was ≈0º till 500kHz and increases from -1º to -33º until the frequency reached at 10MHz.

**Transient Response:** The transient response was setup with two input signals with specified frequency, amplitude and 0V offset voltage. The simulation was applied as: 1) Two out-of-phase 100kHz frequency signals with ±25V amplitude, 2) Two in-phase

1MHz frequency signals with an amplitude of +25V and +10V and 3) Two out-of-phase 10MHz frequency signals with ±9V amplitude. The DA circuit was configured in two settings: 1) Addition of two signals to establish a maximum achieved output voltage swing, 2) Subtraction of the two signals to establish signal difference response. The transient responses of the DA circuit are shown in Figure 6.4 – Figure 6.6, which describe the output voltage at the node *OUT* at respective frequency.

The transient response of the circuit shows a good response till a certain frequency (i.e. 1MHz) and provides the theoretically expected amplitude of output signal at 10MHz. Figure 6.4 shows the circuit response when configured in a signal addition mode with two out-of-phase signals having the same amplitude at 100kHz. The response shows that the circuit can measure an output signal of $100V_{p\text{-}p.}$ Hence meeting the design requirement of this DA circuit.

Figure 6.5 shows the circuit response when configured in a signal subtraction mode with two in-phase signals having different amplitude at 1MHz. The response shows that the circuit can measure an output signal of $30V_{p\text{-}p}$ as expected.

Figure 6.6 shows the circuit response at 10MHz, which acts as signal addition when two same amplitude but out-of-phase signals were applied to the circuit. The response shows that the circuit can measure an output signal of $\approx 37V_{p\text{-}p}$ as expected. However, it was observed in simulation that when the amplitude of both signals increases ±9V or any combination which exceeds the amplitude of 18V either positive or negative, will result in a low output voltage dropped at the DA circuit output node *OUT*.

Based on the DA circuit using a single op-amp, it was concluded that with one set of gain settings; frequency between 1kHz to 1MHz can achieve an output voltage of $100V_{p\text{-}p.}$ The same gain setting can only provide an output voltage of $37V_{p\text{-}p}$ at 10MHz frequency. Above this amplitude, the output voltage drops and a greater phase shift was noticed in the simulation results.

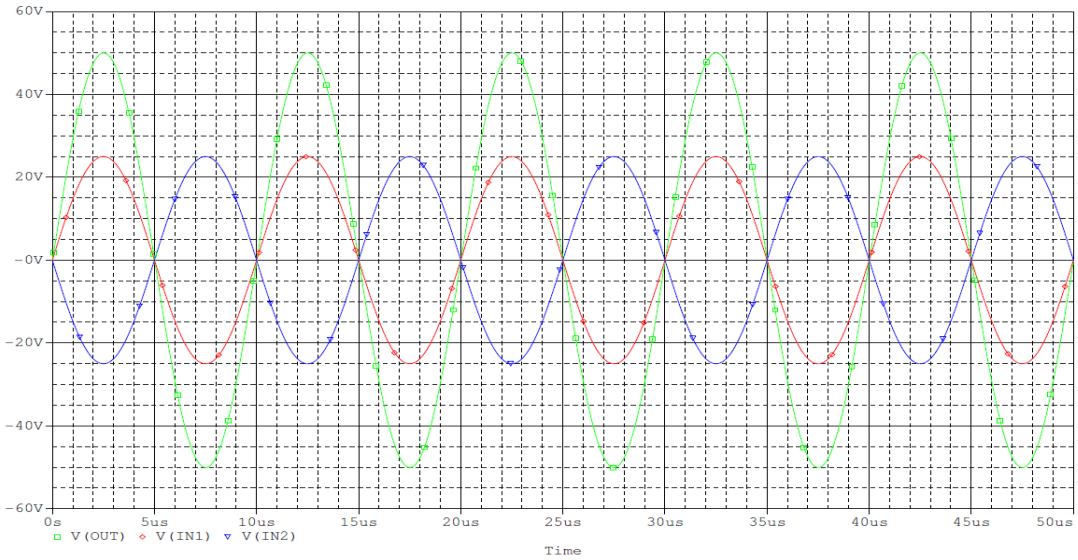



Figure 6.4: Transient response of DA at 100kHz

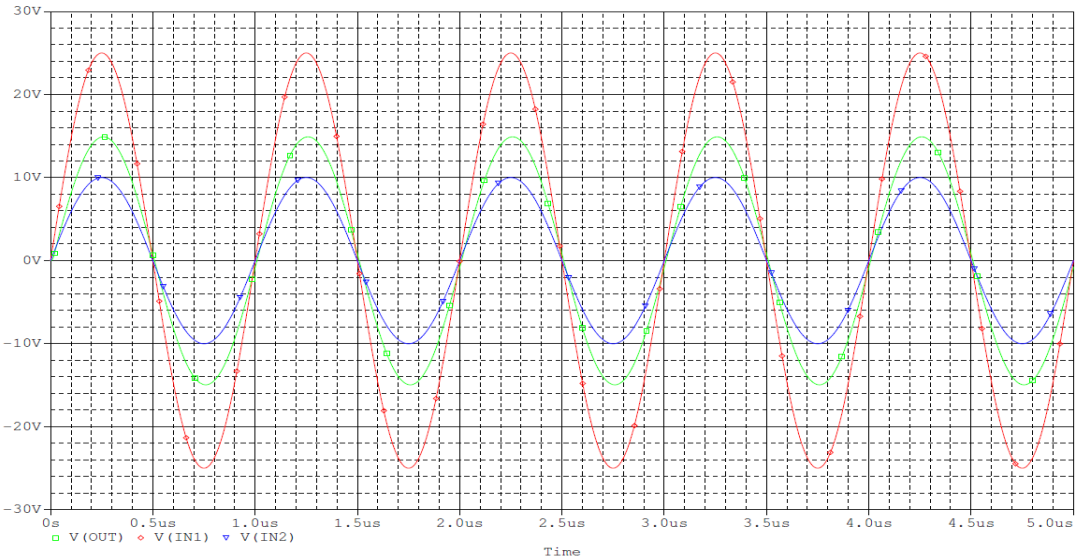



Figure 6.5: Transient response of DA at 1MHz

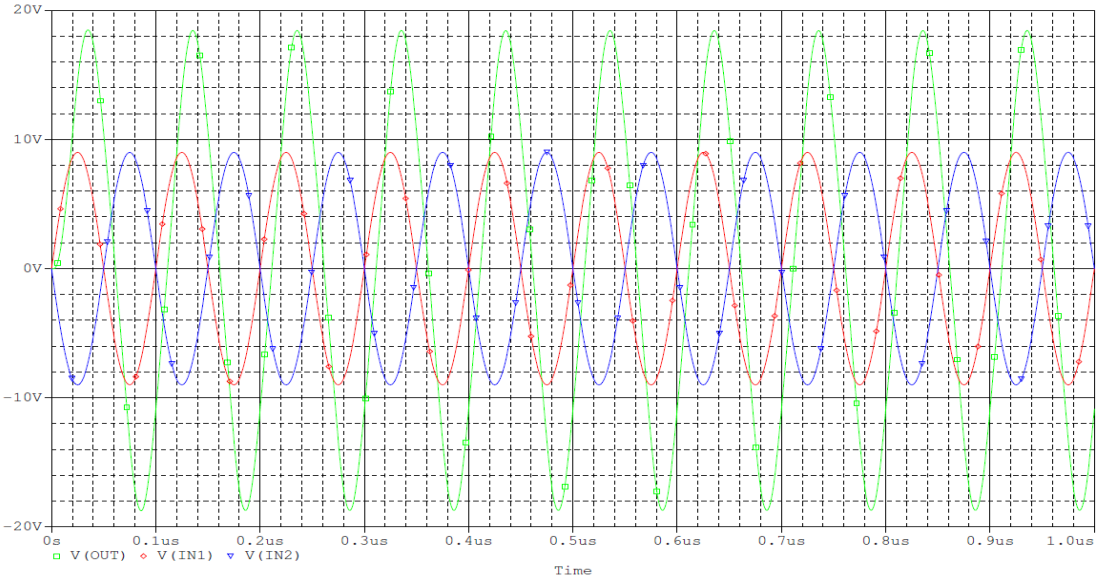



Figure 6.6: Transient response of DA at 10MHz

**Discrete Component DA:** The above problem leads to a requirement to design a DA circuit using discrete components, which can achieve a high amplitude output signal at higher frequencies (≤10MHz) and have a phase difference of <1%. A combination of high speed (BFR92 and BFT92) and high voltage transistors (BF620 and BF621) were chosen. The differential amplifier using discrete components is presented in Figure 6.7. The resistors $R_1$ and $R_2$ are the input resistors for the inverting and non-inverting terminal of the discrete op-amp. $R_f$ represents the feedback resistor. This DA circuit doesn't use any push-pull configurations and the amplifier will operate in a single ended output. This makes the circuit a simpler configuration and excludes the problems associated with crossover or switch-off distortion. The circuit was divided into different stages. The first stage is a typical differential transistor pair ($Q_1$, $Q_2$). The differential transistor pair can be loaded by a current mirror but it increases circuit complexity. The stage open-loop gain depends on the resistor connected directly to the emitters of $Q_1$ and $Q_2$, which provides a twofold change in gain. It can be helpful in optimisation of other circuit parameters. The second stage of the circuit is amplifying. This stage consists of transistor $Q_3$, which is dynamically loaded by an emitter follower transistor ($Q_4$). This follower is fed from a current generator on transistor $Q_5$. These two stages were bootstrapped by transistor $Q_6$ and $Q_7$, which will supply a high amplitude signal to the DA circuit. This compact amplifier configuration was expected to be excellent, featuring extremely low distortion and high frequency performance.

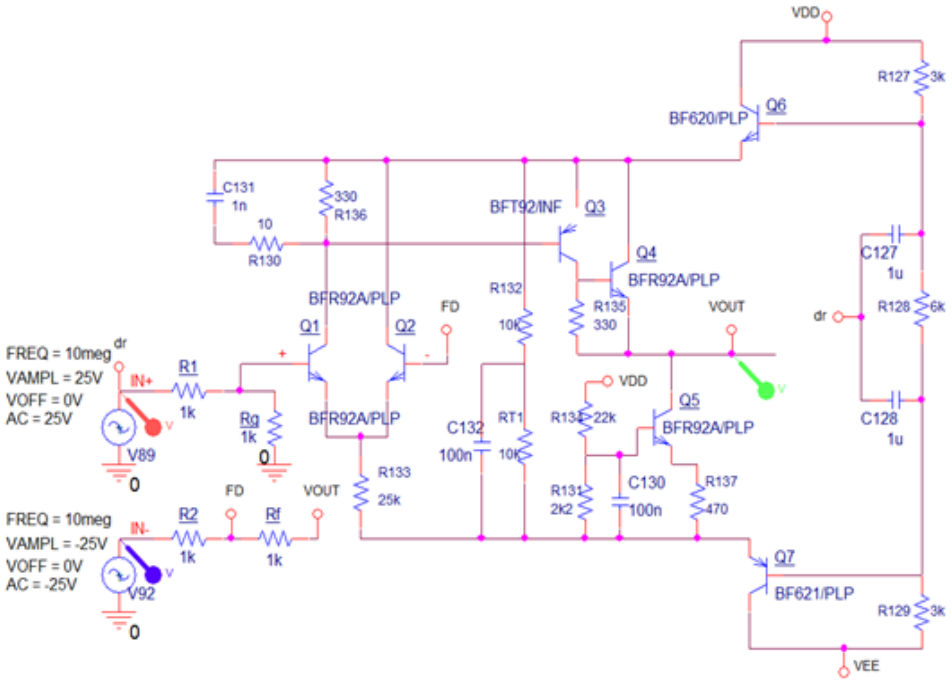



Figure 6.7: High voltage and high frequency discrete differential amplifier

**AC Response of discrete DA circuit:** The circuit shown in Figure 6.7 was operated with an AC sweep analysis with two out of phase AC signals of amplitude ±25V. The power rails of the DA circuit were bootstrapped. The power rails ($V_{CC}$ and $V_{EE}$) of the bootstrapped circuit was set to ±200V. The output voltage was recorded at the output node (*VOUT*) without any load resistance. The AC response of the circuit is shown in Figure 6.8, describing the output voltage amplitude and the phase response against frequency sweep respectively.

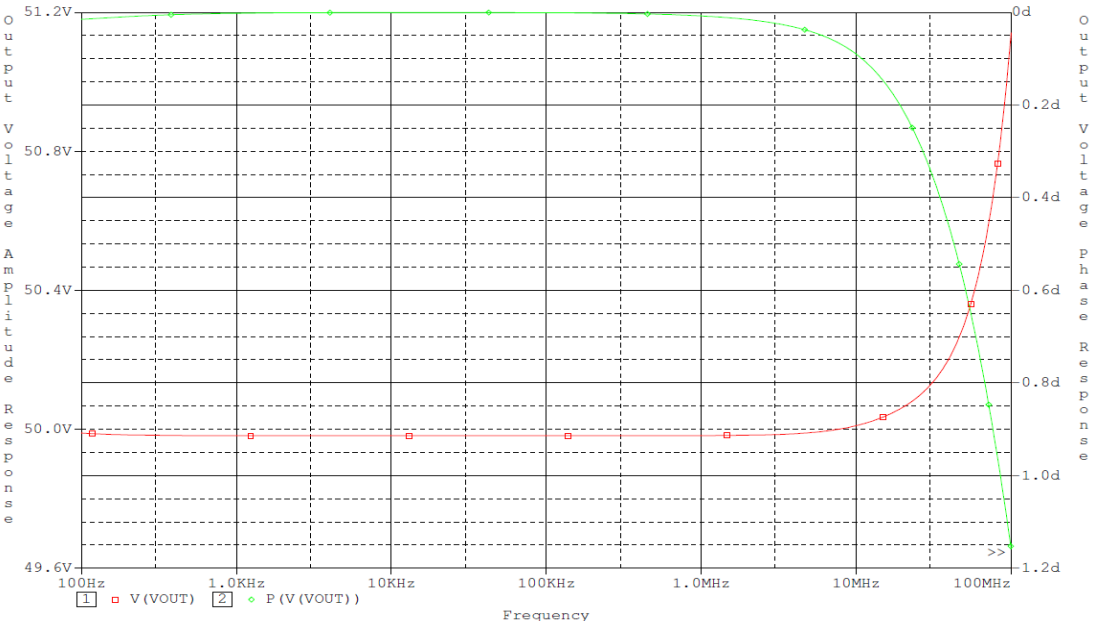



Figure 6.8: AC response based on discrete differential amplifier

The AC response shows that the DA circuit gives very good frequency bandwidth performance over a wide range of >30MHz. The circuit also gave a good phase response and was approx. 0º from 100Hz to 10MHz.

**Transient Response of discrete DA circuit:** The transient analysis was setup with two input signals using the intended frequency, amplitude and 0V offset voltage. The simulation was applied as: 1) Two out-of-phase 1MHz frequency signals with ±25V amplitude, 2) Two in-phase 5MHz frequency signals having an amplitude of +25V and +15V 3) Two in-phase 10MHz frequency signals with -15V & -10V amplitude simultaneously. The discrete DA circuit was configured in two settings: one setting showed the behaviour in which two signals were summed to establish a maximum achieved output voltage swing, while the second setting showed the behaviour in which the difference of two signals was propagated at the output of the DA.

The transient response of the circuit shows a very good response across a wide frequency bandwidth (up-to 10MHz). Figure 6.9 shows the circuit response of the circuit when configured as a signal subtraction circuit of two in-phase signals at 1MHz frequency. The response shows that the circuit can measure an output signal of -10$V_{p-p}$. Figure 6.10 represents the circuit response at 5MHz frequency, when configured as a signal subtraction circuit of two in-phase signals having different amplitudes. The response shows that the circuit can measure an output signal of 20$V_{p-p}$ as expected. Figure 6.11 shows the circuit response at 10MHz, when configured acts as a signal amplitude summation circuit of two out-of-phase signals having different amplitudes. The response shows that the circuit can measure an output signal of ≈100$V_{p-p}$ as desired. Hence, it meets the desired output amplitude of the discrete DA circuit design.

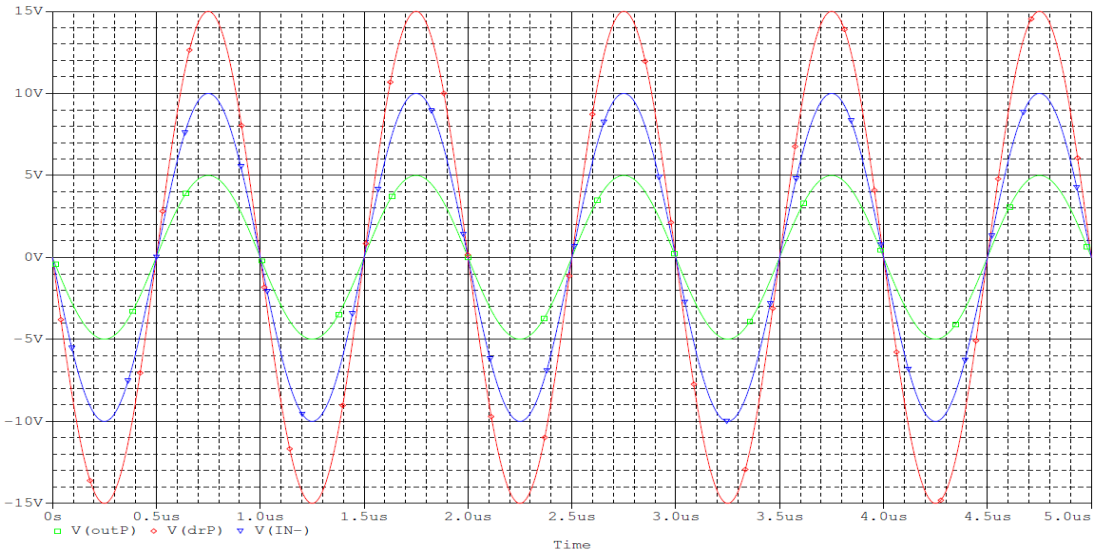



Figure 6.9: Transient response of discrete DA at 1MHz

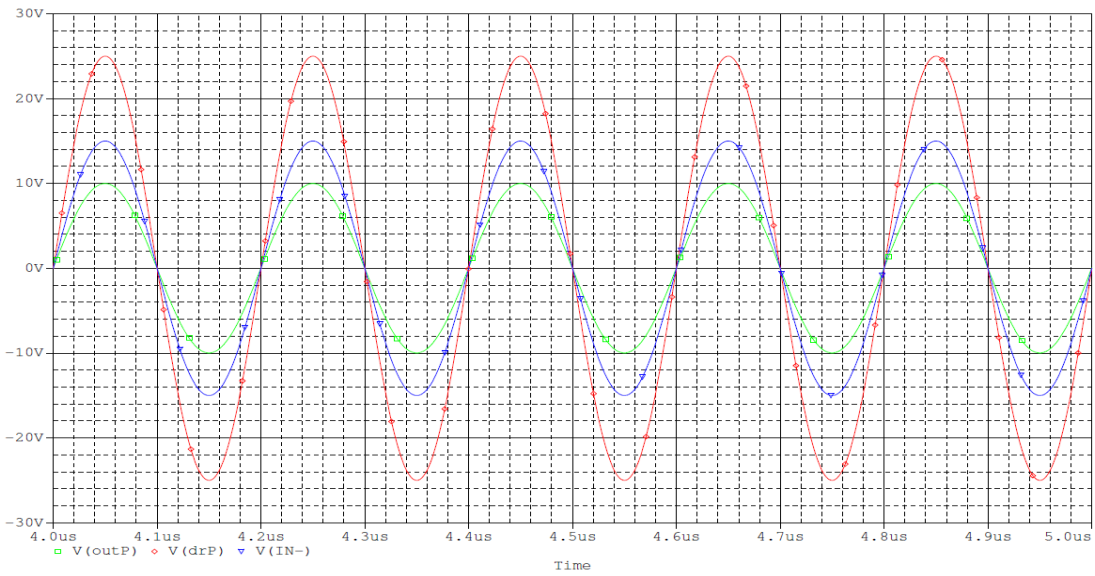



Figure 6.10: Transient response of discrete DA at 5MHz

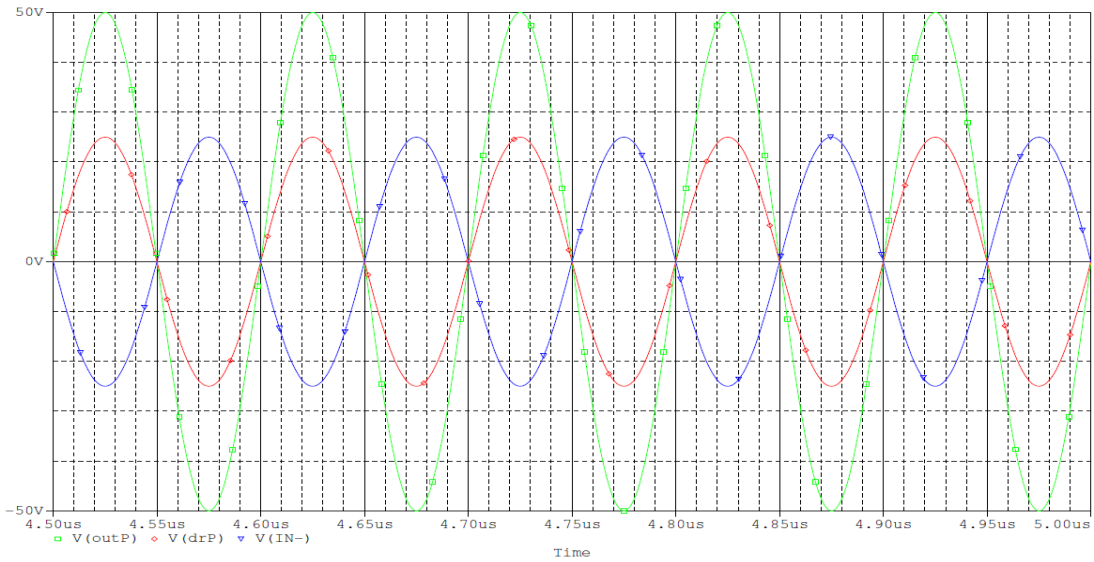



Figure 6.11: Transient response of discrete DA at 10MHz

Based on the AC and transient response of discrete DA circuit, it can be concluded that the circuitry can be used to measure differential signals having high amplitude at higher frequency with very little phase shift. A high precision DA circuit can be achieved by building a high quality PCB for the difference amplifier.

An enhanced circuit topology of the DA is an Instrumentation amplifier (IA) that is used for low-level amplification with high CMRR and input impedance to avoid loading. It is helpful for minor amplitude signal amplification, which requires high input resistance, low noise and precise closed-loop gain. For IA good performance, a low: power consumption, DC offset and noise are desirable along with; high: slew rate, CMMR, open-loop gain and input impedance. It is the front-end component of every measuring instrument, which improves the SNR of the electrical signal from the transducer.

The IA is equipped with input buffer amplifiers. This input buffering eliminates the need for input impedance matching of the DA and makes it suitable for testing/measurement of equipment that requires high accuracy, sensitivity and stability of the circuit. An internal signal or external resistor can set its gain. High CMMR of IA make it useful to recover a small signal buried in large common mode noise.

The IA is a closed loop circuit topology that consist of three op-amps. This topology consists of two stages: 1) the first input stage offers very high impedance to both input signals (non-inverting/buffer amplifier connected to DA inputs) and, 2) the second stage is the DA that forms the output stage of the IA (negative feedback and ground connections). Both stages consist of matched op-amp. The output of IA ($V_{out}$) will be the

amplified difference of the applied input signals. Assuming that the outputs of input buffering amplifiers are $V_{o1}$ and $V_{o2}$, then IA differential output (as per the DA given in Fig 6.2) is given by:

$$V_{out} = -\left(\frac{R_f}{R_1}\right)(V_{o1} - V_{o2}) \qquad \text{Eq. (6.17)}$$

By expressing the $V_{o1}$ and $V_{o2}$ voltages, in the form of input voltages and resistances, the final expressions for output voltage and gain of the IA are given by:

$$V_{out} = -\left(\frac{R_f}{R_1}\right)\left[\frac{(2R_i + R_{gain})}{R_{gain}}\right](V_A - V_B) \qquad \text{Eq. (6.18)}$$

$$Gain = A_v = -\left(\frac{R_f}{R_1}\right)\left[1 + \frac{2R_i}{R_{gain}}\right] \qquad \text{Eq. (6.19)}$$

It is clear from the gain equation that the differential operation doesn't depend on input resistor matching. Amplifier's input resistance is very high due to high input resistance of the op-amp and no current is drawn from the source. The gain resistor *($R_{gain}$)* or input resistor *($R_i$)* are used to control the voltage gain of the IA, while the DA stage provides the common-mode signal attenuation. It is clear from the above expression that the decrease in the value of $R_{gain}$ will increase the output voltage ($V_{out}$). Similarly, to increase the gain of the circuit, $R_{gain}$ has to be decreased. The metal film resistors can be helpful to achieve a precise and accurate high gain. The IA shows good linearity due to its large negative feedback (≈0.01% for <10 gain).

The IA could be beneficial in various ways. Some of the three op-amp based IA advantages are:

1. The adjustment of $R_{gain}$ resistor controls the gain without any significant change in the circuit and is dependent on external resistors that can be set by their careful selection.
2. The high input impedance is dependent on the input stage non-inverting amplifier.
3. The output impedance of the DA stage becomes IA output impedance and is generally very low.
4. The DA stage provides very high CMMR that significantly rejects the common mode signal.

5. IA does not require input impedance matching; hence make it suitable for testing and measuring various equipment with accuracy. It does not generate any noticeable noise along with having considerably low drift.
6. IA is very stable circuit configuration, hence ideal for long term as well as short-term use. It has a controlled circuit, which can be easily varied or adjusted by the $R_{gain}$ resistor.
7. IA usually works with the input. Hence, it doesn't really depend much on the various factors that influence the output at the latter stages. The output ability of an instrument depends on many factors, but to some extent, it can be understandable by good knowledge of its input.
8. Due to its highly scalable ability, even a relatively tiny input signal can be amplified largely but with a substantial input condition level.

The IA has a disadvantage of long-range transmission issues. Its only drawback is the superimposing of the original signal when the noise is transmitted over a long-range, which results in the system dependency on special cables that can cancel this superimposition or noise.

The IA can be used in variety of applications that require high differential gain accuracy, stability in a noisy environment and the presence of large common-mode signals. Some of the applications in which it is used are:

1. In data acquisition from low output transducers (i.e. thermocouples, Wheatstone bridge measurements etc.).
2. In medical instrumentation, Navigation and radar instrumentation.
3. In audio application that involves improvement of low amplitude signals in a noisy background by improving its SNR.
4. High speed signal conditioning for imaging and data acquisition.
5. Signal amplification in cable for RF systems.

The IA could be used in a variety of medical applications, to boost small amplitude signals that are overlapped with large common-mode voltages and DC potentials. High impedance along with high CMMR is a key parameter to many biomedical and sensor applications. EIT is considered to be one of these applications. Many researchers have used IA to measure the boundary voltages in the EIT system. This background literature review has been presented in the section 2.4.2.3 of this thesis. According to the scope of

this research, the differential measurement of the high amplitude signal at a high frequency was intended for use with an integrated circuit op-amp and discrete components based op-amp design. As a prototype design, the simulated performance parameters were established for both DA's design. Based on the simulated response of both DA's design, it can be concluded that the circuitry can be used to measure the differential signals having high amplitude at higher frequency. After validating the performance of the DA PCB and its subsequent precise testing, the design will be extended to achieve a high performance IA design, which will consider the additional parameters of high input impedance and CMMR for the IA circuit design.

## 6.4 Voltage Source Circuit Simulation Results

According to the initial frequency bandwidth test results presented in Table 6.1, the voltage source architecture with higher bandwidth acquired was considered for further testing as a single ended voltage source. The circuit design was extended to design a bipolar voltage source after achieving acceptable output from the voltage source.

Many available op-amp devices were explored to find a suitable op-amp device, which can be used in the voltage source circuit design (Qureshi et al., 2012c). At first instance, OPA656 device was selected to design and simulated the performance of the voltage source circuit. The simulation results showed that the voltage source design can provide good frequency bandwidth of >15MHz with a low output impedance along with good signal-to-noise ratio. These results were published in the 34$^{th}$ EMBS conference (Qureshi et al., 2012d). Later, it was decided to change the OPA656 op-amp with a high speed voltage feedback op-amp (THS4304) used in the Analog processing applications. Like the current source design in chapter 4 &5, it was decided to use the same op-amp device in the voltage source design.

Circuit simulation was performed using Pspice® model to demonstrate the performance of the op-amp in the voltage source circuit over the working bandwidth with a constant voltage amplitude. The power supply and voltage signal generator used in the simulation were considered to be ideal without any noise or other performance limitations. It was observed by simulating the 1$^{st}$ architecture based voltage source (shown in Figure 6.1) that the circuit output signal was saturated due to the low power rail supply of the op-amp. The power rail supply was initially set to ±2.5V as per the data sheet of the op-amp.

The simulation shows that the circuit can only deliver an output signal of amplitude ≈4-5$V_{p\text{-}p}$. This situation arose when the amplitude from the signal generator was increased or a higher voltage gain was required by the voltage source gain resistors. Therefore, to solve this signal saturation problem, it was decided to use the bootstrapping technique in the voltage source circuit. The bootstrapped voltage source circuit was optimised for the best achievable performance. The voltage dropped across the load was measured and the output impedance of the voltage source was calculated. The SNR of the voltage source circuit was also measured using Pspice®. The results achieved by the bootstrapped voltage source circuit are presented in this section later.

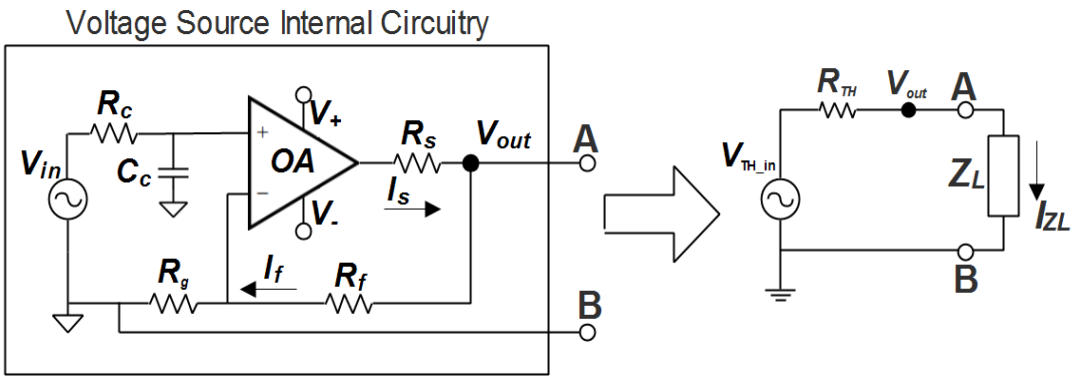



Figure 6.12: A VCVS and its Thevenin Equivalent circuit

The output impedance of the circuit was calculated using the same procedure discussed in chapter 4. It is known that any linear circuit can be represented by its Thevenin's equivalent to an equivalent circuit, which consists of a single voltage source ($V_{TH}$) with a series resistance ($R_{TH}$) connected to the load, regardless of the circuit complexity. It was assumed that voltage source circuit can be converted to its Thevenin equivalent and can be represented by its equivalent Thevenin voltage in series with its Thevenin resistance. In our case, the equivalent Thevenin voltage source will be the total theoretical voltage or ideally, generated voltage and Thevenin resistance will be referred as the output impedance of the voltage source circuit. This transformation is shown in Figure 6.12. It can be clearly seen that after the transformation of any circuit to its Thevenin equivalent, the circuit becomes a voltage divider circuit. Therefore, the output voltage at node $V_{OUT}$, which represents the output voltage generated by the voltage source can be expressed as,

$$V_{out} = \left(\frac{R_L}{R_{TH} + R_L}\right) V_{in} \qquad \text{Eq. (6.20)}$$

Rearranging Eq.6.20 to express the output impedance of the circuit,

$$Z_{out} = R_{TH} = \frac{V_{in}R_L - V_{out}R_L}{V_{out}} \qquad \text{Eq. (6.21)}$$

The SNR of the voltage source circuit was calculated using Pspice®. It can analyse the noise within the circuit. It calculates the total noise contribution from each element in the circuit and combines these noise sources with the various transfer functions in the circuit. The result of these calculations can be plotted to obtain the noise response over a range of frequencies like frequency response analysis. In Pspice®, the semiconductors devices and resisters contribute to the noise calculations. At each frequency, the total noise contribution was calculated in Pspice®. Probes were used to measure the total RMS noise across the band. The total noise is the overall variance of the combined noise fluctuations at each frequency. The total noise power was calculated by squaring the RMS-summed output noise for the entire circuit. The average signal power was assumed to be 2.5V ideally according to the set gain for the circuit. Signal-to-noise ratio can be expressed as,

$$SNR = 20\ \log_{10}\left(\frac{Signal}{Total\ noise}\right) \qquad \text{Eq. (6.22)}$$

The output impedance and SNR were calculated by the above procedure using Eq. 6.21 & Eq. 6.22 respectively and are recorded in the next section along with the frequency bandwidth *(-3dB and -1dB)* of the voltage source circuit. The detailed simulation performance of the single-end bootstrapped voltage source was performed and extended to a bipolar design. This section only represent the detailed simulation performance of the bipolar bootstrapped voltage source.

The voltage source circuit gain was defined to be 2.5. To obtain a specific gain, feedback resistors ($R_f$ and $R_g$) were specified. One of the feedback resistor ($R_g$) was fixed. The resistor $R_f$ was kept variable to change the circuit voltage gain during testing if required. The sense resistor ($R_S$) was also kept variable, which can be used to control the output voltage generated by the op-amp. Based on the predefined gain and one fixed resistor value, the value of other feedback resistors can be calculated by Eq. 6.23.

$$R_f = (Gain - 1)\ R_g \qquad \text{Eq. (6.23)}$$

The single-end voltage source circuit showed some oscillation/spikes in the output signal at higher frequency. To avoid the oscillation in the circuit a simple RC low pass filter (LPF) was used before the non-inverting terminal of the op-amp. This RC-LPF was made by connecting a resistor ($R_C$) in series with a capacitor ($C_C$) having one end of the capacitor referenced to ground. In this type of filter, the input signal is applied to the series combination of resistor and capacitor but the output is recorded across the capacitor. The value of the resistor remains constant with change in frequency, while the reactance of capacitor changes inversely with change in frequency. The capacitive reactance ($Xc$) of capacitor ($C_C$) will be very large at low frequencies as compared to the resistive value of $R_C$. This means that voltage dropped across the capacitor ($C_C$) will be larger than the voltage dropped across resistor ($R_C$). At higher frequencies, the effect is reversed due to the change in the capacitance reactance value ($X_C$). The capacitance reactance ($X_C$) and the impedance ($Z$) expression are given below followed by the RC-LPF output voltage.

$$X_C = \frac{1}{2\pi f C} \qquad \text{Eq. (6.24)}$$

$$Z = \sqrt{R^2 + X_C^2} \qquad \text{Eq. (6.25)}$$

$$V_{out_cap} = V_{in}\,\frac{X_C}{Z} \qquad \text{Eq. (6.26)}$$

The RC-LPF shows a flat behaviour at low frequencies and all the input signal is passed directly to the output of the filter until it reaches the filter's cut-off frequency ($f_C$). This is due to the high reactance of the capacitor at low frequencies, which blocks any current being passed through the capacitor. A high frequency signal when applied to the LPF above its $f_C$ point will rapidly decrease. This is due to the very low reactance of the capacitor at high frequency, which gives the effect of a short circuit on the output of the filter resulting in an almost zero output. By carefully selecting the $R_C$ and $C_C$ combination, a RC-LPF circuit can be created, which allows a range of frequencies below a certain value to pass through the circuit unaffected while rejecting other frequencies applied to the circuit above the defined cut-off frequency. The single-end voltage source circuit was able to pass frequencies till ≈78MHz while rejecting the frequencies above it, which were

causing oscillation in the circuit. The cut-off frequency for the voltage source circuit was defined by,

$$f_C = \frac{1}{2\pi RC} \qquad \text{Eq. (6.27)}$$

The AC and transient response of the single-end voltage circuit that showed a good response was extended to design a bipolar voltage source circuit. The single-end voltage source circuit was observed for different RC loading combinations (5kΩ to 30kΩ with ΔR=5kΩ and C=10pF, 30pF, 50pF and 100pF). To summarize using 10pF loading capacitance and variable resistive loading, the observed circuit performance parameter are: frequency bandwidth of 66MHz, the output impedance between 7Ω to 480Ω for frequencies between 100kHz to 10MHz, a phase shift of ≈0° to -18.23° for frequencies between 100kHz to 20MHz and an SNR in the range of 103-88dB for the frequency range of 1kHz to 30MHz.

### 6.4.1 Bipolar Bootstrapped Voltage Source Performance

Based on the performance and design of the single-end voltage source, the next step was to design a bipolar voltage source circuit. In other words, it is formed of two out-of-phase single end voltage sources working in parallel. Like the bipolar current source, the bipolar voltage sources were not found to be complex. The motive was to achieve good circuit performance of the bipolar voltage source at multiple frequencies, which can be used in any bio-impedance system with high frequency bandwidth, low output impedance, less phase shift and good SNR.

An experiment was setup to design a bipolar bootstrapped voltage source circuit schematics and its simulation was performed. Like the current source circuit, a single signal generator was used to test the voltage source circuitry. The generated signal was inverted using an inverting op-amp configuration. Both inverted and non-inverted signals were applied to the load simultaneously via a voltage source circuit and make the circuit a bipolar source for a bio-impedance system. All the op-amp components within the voltage source circuitry were bootstrapped to obtain a high amplitude output voltage signal.

The differential amplifier (DA) designed in section 6.3 was used to measure voltage across the intended resistor. The DA was connected across sense resistor ($R_s$), feedback resistor ($R_f$) and load to measure the voltage dropped across each component. The difference of $I_s$ and $I_f$ was used to calculate the amount of current injected in to the load. Once the injected current ($I_s$ - $I_f$) and dropped voltage ($V_L$) are known, the unknown impedance of the attached object can be calculated. This circuitry was tuned in a manner to achieve a wide frequency range and optimised until the maximum possible simulated performance was achieved from the circuitry. While optimizing the performance of the voltage source circuit, the RC filter components values were changed. Hence, the bipolar voltage source circuit was able to pass frequencies till ≈83MHz while rejecting the frequencies above it, which were causing oscillation in the circuit. The bipolar bootstrapped voltage source circuit simulation was performed with the circuit schematics shown in Figure 6.13.

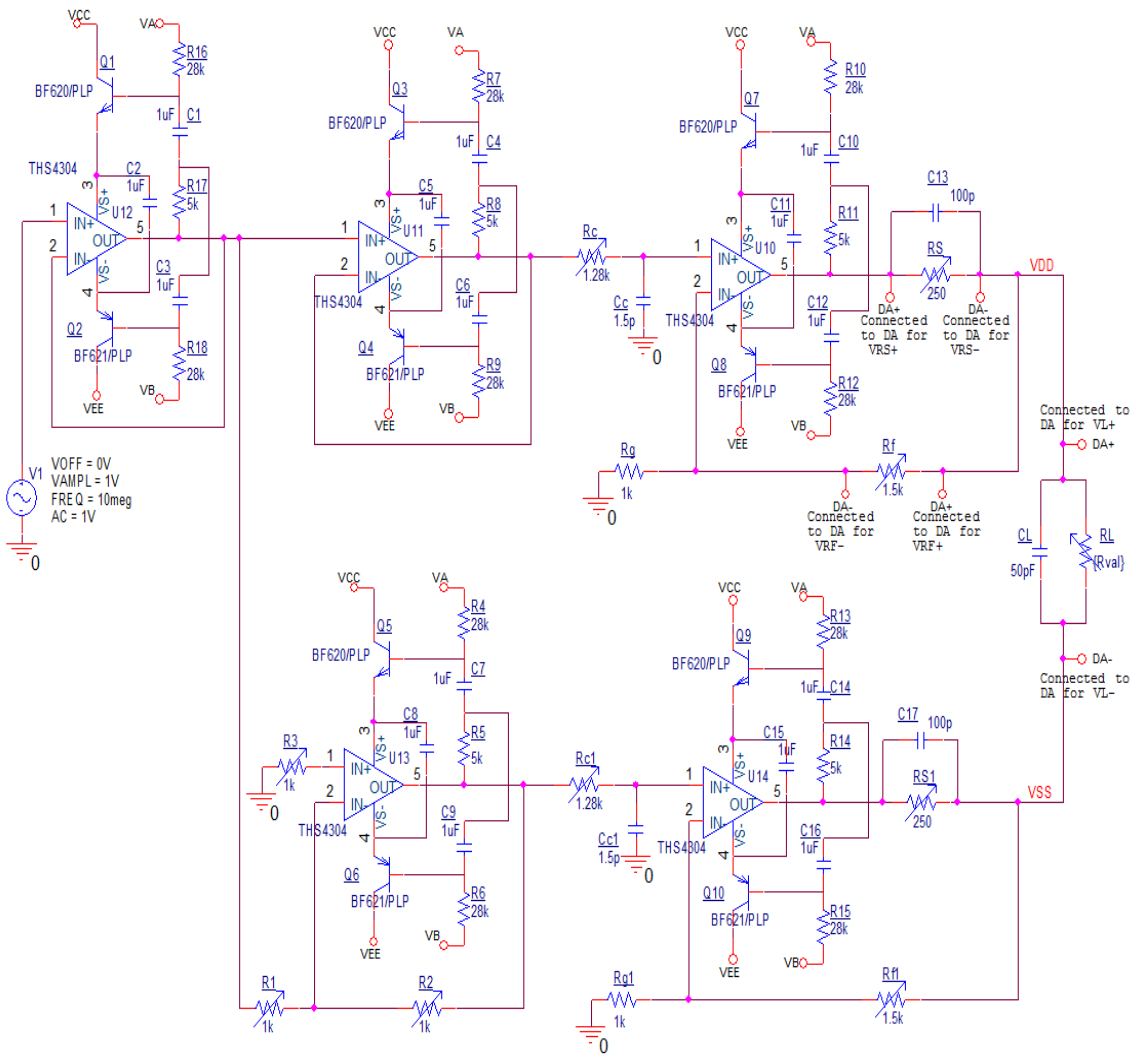



Figure 6.13: A bipolar bootstrapped voltage source circuit

### 6.4.1.1 AC Response of Bipolar Bootstrapped Voltage Source Circuit

The circuit shown in Figure 6.13 was operated with an AC sweep analysis from 100Hz to 1GHz frequency with a 1V AC signal. The power rails ($V_{CC}$ and $V_{EE}$) and the bias voltages ($V_A$ and $V_B$) of the bootstrapped circuit were set to ±36VDC and ±60VDC respectively. The circuitry voltage gain was set to be 2.5. The maximum amount of current, which can be injected to the load was specified to be 1mA. By knowing the voltage gain and injected current, the minimum value of load can be predicted and served as a minimum load condition to allow maximum current while maintaining a constant voltage drop across other load values. Therefore, on the basis of this assumption, the minimum value of the load was decided to be 5kΩ. The bipolar bootstrapped voltage source circuit setting was changed for different RC combinations to achieve the optimum performance of the source over a wide frequency bandwidth (R=5kΩ to 30kΩ with ΔR=5kΩ, C=10pF, 30pF, 50pF and 100pF). The simulation results are shown in Figure 6.14 & Figure 6.15, describing the output load voltage *($V_L$)* and phase of the output signal against its frequency sweep.

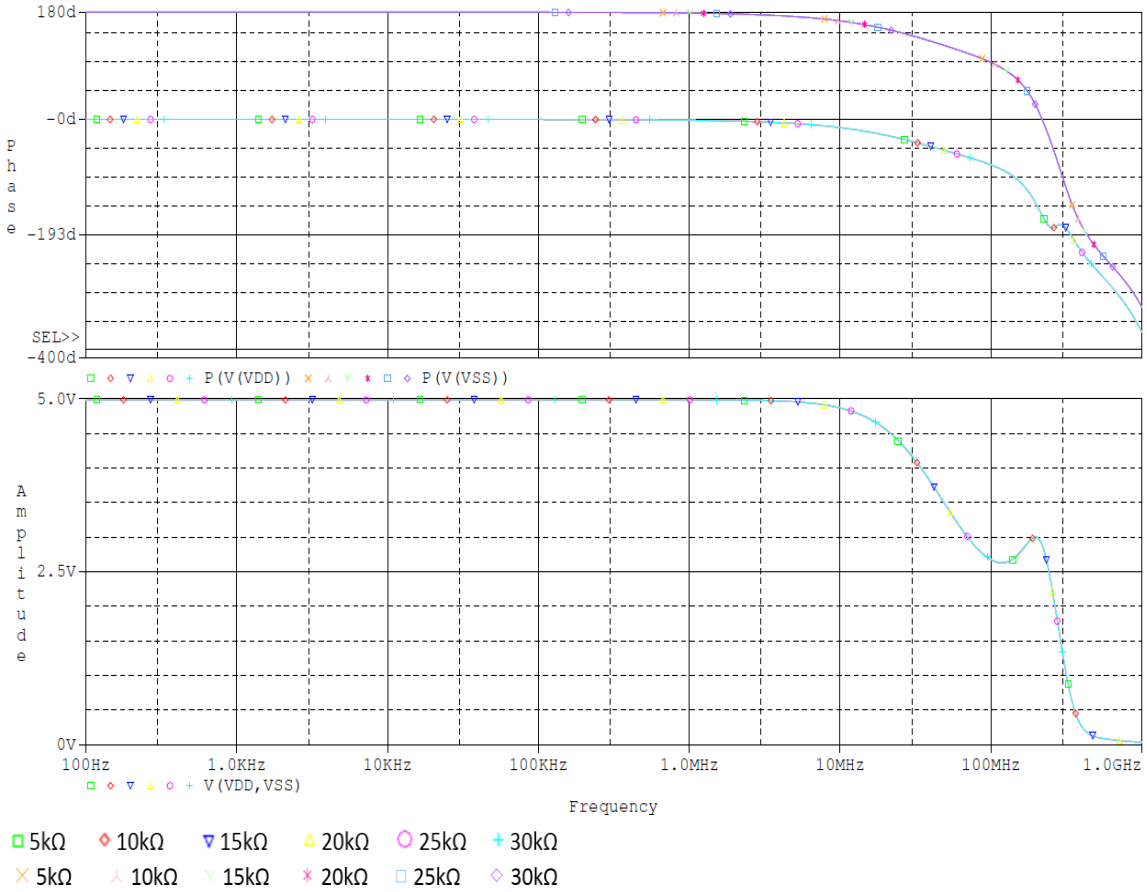



Figure 6.14:A bipolar bootstrapped voltage source circuit AC response with 10pF loading capacitance

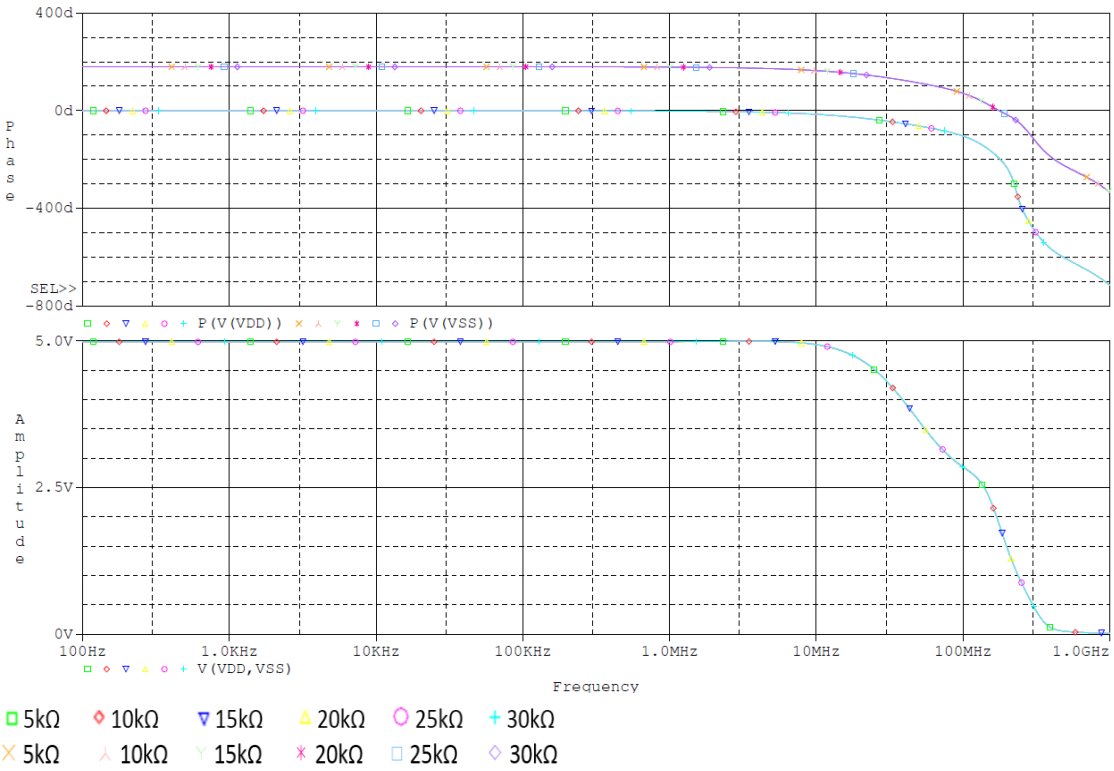



Figure 6.15: A bipolar bootstrapped voltage source circuit AC response with 50pF loading capacitance

The AC response of the bipolar bootstrapped voltage source circuit shown in Figure 6.13 shows a good performance with resistive loading in the presence of specific loading capacitance. The AC response reported above was taken using the voltage probes available in Pspice® instead of the DA output. It was also observed that the output taken from the DA output was almost equal to the output recorded by the voltage probe. The detailed results are presented in section 6.4.1.3. The results show that the output voltage dropped across the load gives an overall wide frequency bandwidth for the circuit at particular resistor network settings having a very small phase shift in the output voltage signal till ≈5MHz. This phase shift was noticed to be approximately <5º, which can be observed in the Figure 6.14 & Figure 6.15.

It was also observed in the AC response that by using low bias voltages ($V_A$ and $V_B$), a high amplitude peak in the output voltage was noticed with the increase in loading capacitance. The peak was noticed in the frequency range of 20-37MHz with different tested loading capacitance. This peak may result in oscillation of the circuit. Therefore, to overcome the peak amplitude response, the RC circuit was adjusted before the voltage source. It had helped to some extent to control this output amplitude peak but the shortcoming of reduced frequency bandwidth was observed. Although the low bias

voltages resulted in increased amplitude of the output signal up to 1MHz and dropped off rapidly above it, depending upon the cut-off frequency of the RC circuit. The increased amplitude resulted in a low output impedance of the circuit but also resulted in a low frequency bandwidth circuit, which was not compliant with the design requirement. A trade-off was done between very low output impedance of the circuit and high frequency bandwidth. Therefore, the circuit was further optimised to obtain a reasonable output signal amplitude having a wide frequency bandwidth. The bias voltages of the transistors were increased to ±60V and it was observed that the amplitude peaks were reduced. This was possibly due to the fact that a high voltage transistor was being used in the bootstrapped circuit, which requires a certain voltage to give its best performance as per its data sheet.

The circuit response was observed with different loading capacitance (30pF, 50pF and 100pF). A similar behaviour of the bootstrapped voltage source circuit was observed. Apart from a very slight difference in circuit parameters at frequencies >1MHz. The voltage source circuitry was slightly effected by the additional capacitance as compared to the current source. The circuit performance parameters are reported in detail later in this chapter in section 6.4.1.3.

#### *6.4.1.2 Transient Response of Bipolar Bootstrapped Voltage Source Circuit*

In the next step, the circuit's transient response was tested. The transient response of a bipolar bootstrapped voltage source circuit was setup with a specified signal frequency, amplitude and 0V offset voltage. The simulation was setup as: 1) For 100kHz and 10MHz frequency signals with 1V amplitude, 2) For 1MHz frequency signal with 2V amplitude and, 3) An additional simulation setup for 1MHz frequency signal with 3V amplitude in the presence of the DA connected across the attached load to demonstrate the capability of measuring a high amplitude signal using the designed DA circuit. The tested load resistance values were 5kΩ, 10kΩ and 15kΩ. The simulation was setup to run for 50µs, 0.5µs and 5µs respectively with a max step size of 0.001µs. The transient responses of the voltage source circuit shown in Figure 6.13 are shown in Figure 6.16 to Figure 6.19, which shows the output load voltage at respective frequency.

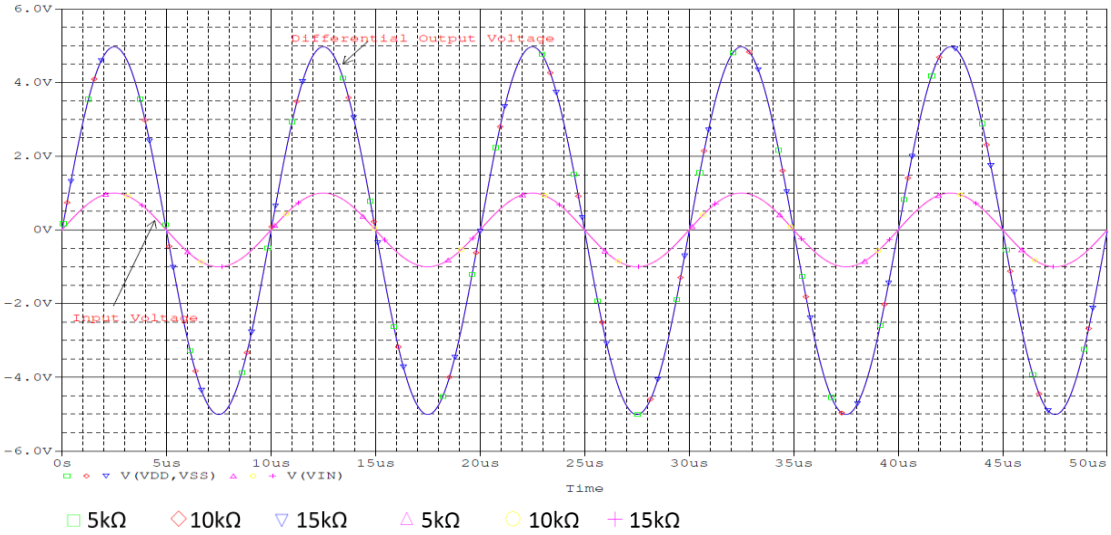



Figure 6.16: A bipolar bootstrapped voltage source circuit Transient response at 100kHz with 10pF loading capacitance

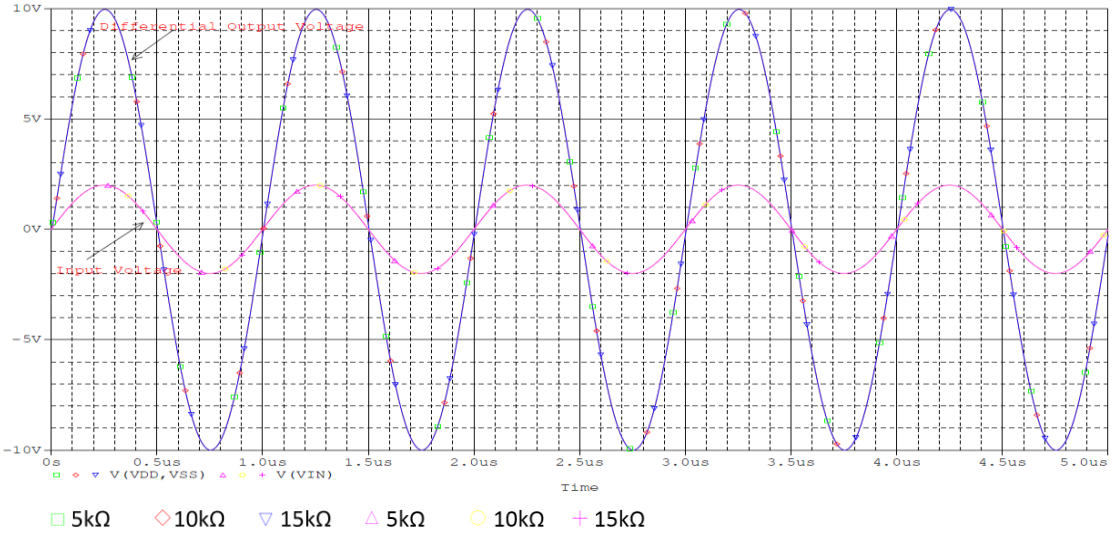



Figure 6.17: A bipolar bootstrapped voltage source circuit Transient response at 1MHz with 10pF loading capacitance

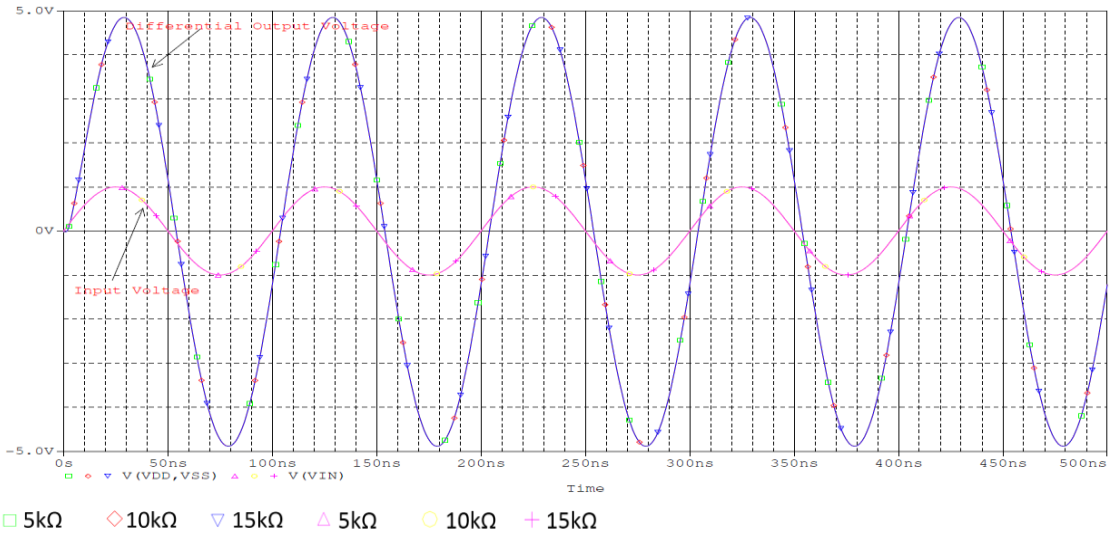



Figure 6.18: A bipolar bootstrapped voltage source circuit Transient response at 10MHz with 10pF loading capacitance

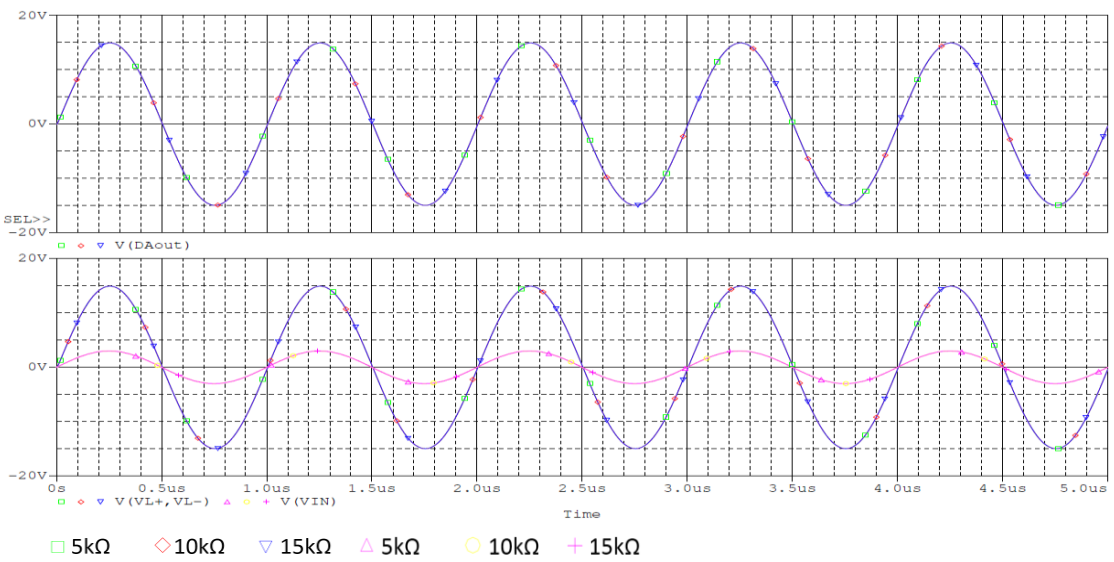



Figure 6.19: Differential voltage across load with 10pF loading capacitance: Output using Differential amplifier (top) & Output using Differential voltage probes (bottom)

The transient response of the circuit in Figure 6.13 shows a good behaviour in the presence of 10pF loading capacitance and verifies its AC response. The transient response shows that constant voltage was dropped across the attached load irrespective of its value and was equal to the voltage gain of the circuit until the cut-off frequency specified by the RC-LPF was reached. The transient response also showed that a high amplitude output signal was achieved without any saturated circuit output. The high amplitude behaviour was tested at 1MHz with ≈20$V_{p-p}$ output voltage across the load as shown in Figure 6.17. It was observed in the results that the phase shift was very small until 1MHz. According to the amplitude observed in the transient response, the output impedance of the source was expected to be very small due to the maximum voltage dropped across the load. The achieved output impedance for the above transient response is presented in detail in section 6.4.1.3. It was also observed that the voltage drop across the load at higher frequency (10MHz) was constant and irrespective of attached load but slightly decreased the amplitude. This was due to the RC-LPF cut-off frequency with an objective to control the unwanted amplitude peaks at high frequencies and maintain one RC-LPF configuration for tested loading capacitance. A very small phase shift was noticed at 10MHz and can be observed in Figure 6.18.

The transient response of the differential voltage measurement across the load is presented in the Figure 6.19. The response demonstrate that the designed DA circuit was capable of measuring a 30$V_{p-p}$ signal and was equal to the output achieved from the Pspice® voltage probe. The differential amplifier output measurement was tested at

different frequencies (10kHz, 100kHz, 10MHz) and it was observed that it can measure the voltage difference across a wide band of intended frequencies.

The simulation was setup to test the remaining loading capacitance effect. Nearly similar performance for transient response was noted for all tested frequencies (i.e. 100kHz, 1MHz and 10MHz) with 5kΩ, 10kΩ and 15kΩ resistive load in parallel with 30pF,50pF and 100pF loading capacitance. The only difference noted was a small change in circuit frequency bandwidth, phase shift with/without the involvement of the DA circuitry. The bipolar bootstrapped voltage source has also resolved the lower driven load problem without effecting the circuit performance parameters like: frequency bandwidth, output impedance, phase shift and SNR. The DA was able to precisely measure the differential voltage. Hence, after observing the transient response, it can be stated that the circuit can be used as a constant voltage source. Therefore, a PCB of this circuitry was designed for practical implementation and testing.

#### *6.4.1.3 Performance Parameter of Bipolar Bootstrapped Voltage Source Circuit*

A high frequency bandwidth circuit is one of the major objectives when designing an excitation source for a bio-impedance system. The bandwidth of the voltage source circuit was limited by the cut-off frequency of the RC circuit used before the voltage source circuit. The purpose of this cut-off frequency was to remove high amplitude peaks at higher frequency, which may lead the circuit to oscillate. The other purpose was to minimise the difference in the bandwidth of 0-deg and 180-deg voltages of the circuit. Like the current source circuit, the voltage source circuit was not affected by the additional loading capacitance of the circuit. Table 6.2 give the overall *-3dB* frequency bandwidth performance of the bootstrapped voltage source circuit shown in Figure 6.13.

Table 6.2: Bipolar Bootstrapped Voltage Source Circuit Bandwidth at corresponding RC loading

| $R_L$ (Ω) | *Load Capacitance (F)* | | | |
|---|---|---|---|---|
| | *10p* | *30p* | *50p* | *100p* |
| 5kΩ - 30kΩ | 47.67 - 47.90 | 50.93 – 51.20 | 53.53 – 53.80 | 53.71 – 53.88 |
| | ***-3dB Bandwidth (MHz)*** | | | |

Ideally, the voltage source should have zero output impedance. Due to non-linearity of the components, practically it is not possible. However, it should be as low as possible to get better performance. The voltage source circuit was simulated to evaluate the output impedance for various frequencies. The output impedance of the bipolar bootstrapped voltage source circuit was calculated using Eq. 6.21 and is mentioned in Table 6.3.

Table 6.3: Output impedance of Bipolar Bootstrapped Voltage Circuit with corresponding loading capacitance

| $R_L$ | *Frequency* (Hz) | | | *Frequency* (Hz) | | |
|---|---|---|---|---|---|---|
| | *100k* | *1M* | *10M* | *100k* | *1M* | *10M* |
| 5kΩ | 12.23 | 13.34 | 136.74 | 12.23 | 11.43 | 65.45 |
| 10kΩ | 23.86 | 25.87 | 265.89 | 23.86 | 22.05 | 123.30 |
| 15kΩ | 35.48 | 38.50 | 395.04 | 35.48 | 32.77 | 181.26 |
| 20kΩ | 46.91 | 50.93 | 524.19 | 46.91 | 43.29 | 239.23 |
| 25kΩ | 56.64 | 63.66 | 653.66 | 56.64 | 54.12 | 296.99 |
| 30kΩ | 70.37 | 76.39 | 783.12 | 70.37 | 64.34 | 354.54 |
| | ***Output Impedance $Z_o$(Ω) with 10pF*** | | | ***Output Impedance $Z_o$(Ω) with 50pF*** | | |

The phase shift between the input and output signal was also considered. The phase shift of the bipolar bootstrapped voltage source circuit was recorded from the voltage phase probe in Pspice®. The detailed phase shift of the output voltage signal dropped across load at corresponding frequency is reported in Table 6.4.

Table 6.4: Phase shift of Bipolar Bootstrapped Voltage Circuit with corresponding loading capacitance

| *Frequency (Hz)* | *Phase Shift (degree)* | | | | | |
|---|---|---|---|---|---|---|
| | *V+* | *V-* | *$DV_L$* | *V+* | *V-* | *$DV_L$* |
| 100k | ≈ 0º | 179.851º to 179.853º | ≈ 0º | ≈ 0º | 179.850º to 179.852º | ≈ 0º |
| 1M | -1.44º to -1.39º | 178.512º to 178.527º | -1.45º to -1.43º | -1.42º to -1.40º | 178.500º to 178.515º | -1.46º to -1.44º |
| 10M | -13.83º to -13.78º | 165.341º to 165.395º | -14.24º to -14.19º | -14.90º to -14.84º | 164.287º to 164.340º | -15.30º to -15.25º |
| 20M | -26.36º to -26.31º | 151.968º to 152.021º | -27.20º to -27.15º | -29.35º to -29.30º | 149.040º to 149.090º | -30.16º to -30.11º |
| | ***Output Impedance $Z_o$(Ω) with 10pF*** | | | ***Output Impedance $Z_o$(Ω) with 50pF*** | | |

The SNR of the bipolar bootstrapped voltage source circuit was obtained from the Pspice® noise analysis functions as recorded earlier for single-end source. The SNR was calculated for 0-deg and 180-deg voltage signal using Eq.6.22. The detailed SNR of the output voltage signal at corresponding frequencies is reported in Table 6.5.

Table 6.5: SNR of Bipolar Bootstrapped Voltage Circuit at corresponding loading capacitance

| *Frequency (Hz)* | *SNR (dB)* | | | |
|---|---|---|---|---|
| | *With 10pF* | | *With 50pF* | |
| | *V+* | *V-* | *V+* | *V-* |
| 1k to 100k | 101.08 – 96.20 | 95.59 – 90.72 | 101.08 – 96.20 | 95.59 – 90.72 |
| 100k to 1M | 96.20 – 94.32 | 90.72 – 88.84 | 96.20 – 94.32 | 90.72 – 88.84 |
| 1M to 10M | 94.32 – 90.17 | 88.84 – 84.71 | 94.32 – 90.15 | 88.84 – 84.69 |
| 10M to 30M | 90.17 – 86.95 | 84.71 – 81.60 | 90.15 – 86.87 | 84.69 – 81.54 |

Table 6.2 lists the frequency bandwidth achieved by the bipolar bootstrapped voltage source circuit at corresponding tested loads. The voltage source circuit results were observed using the voltage measurement probe in the Pspice®. Afterwards results were captured using the DA designed circuit. Results were compared and the precision of the captured results was quantified. Voltage probe results show that the voltage source circuit gives a wide frequency bandwidth even with an increase in the loading capacitance. It was observed that the bandwidth increases very minutely with the increase in load value, which can be neglected. It was also observed that the frequency bandwidth was stable and found to be ≈48MHz, for a wide range of tested loads with a fixed loading capacitance of 10pF. A similar pattern was observed at different loading capacitance with detailed information reported in Table 6.2. Later the DA circuit was applied across the load to measure the differential voltage and its corresponding frequency bandwidth was recorded. The results show that the loading of the differential amplifier didn't affect the performance of the voltage circuit too much. The average frequency bandwidth recorded with loading capacitances 10pF, 30pF, 50pF and 100pF was 47.02MHz, 50.11MHz, 52.68MHz and 53.09MHz respectively for load values from 5kΩ-30kΩ. It was reported in the literature that an EIT system had achieved a system bandwidth of between 10–12.5MHz (Halter et al., 2008). Hence, it can be concluded that if the design is fabricated with high accuracy and precision then the design will be less effected by stray capacitance and will result in a wider frequency bandwidth system.

Table 6.3 list the calculated output impedance of a bipolar bootstrapped VS circuit at selected frequencies. The output impedance performance was found to be similar to the results obtained using a single-end voltage source. Results were captured using the same pattern as discussed before i.e. without/with a DA connection. The voltage probe result show that the calculated output impedance value is in an acceptable range over a wide frequency bandwidth, even at higher load values. It was observed in the results that the output impedance of the circuit increases with the increase in the signal frequency. Alternatively, the output impedance was also noticed to increase with the increase in resistive load value. The results show that the output impedance was found to be ≈12Ω to 783Ω for the load value between 5kΩ to 30kΩ and frequencies between 100kHz to 10MHz having a fixed loading capacitance of 10pF. This shows that the circuit output voltage is less than the expected value at higher frequency but it is still in an acceptable range. It was further observed that the output impedance of the circuit was reduced with the increase in the loading capacitance. It still gave a pattern of increase in output impedance with the increase in load value and frequency, but it was found to be less than the results achieved with a loading capacitance of 10pF. The results show that it was between 12Ω to 567Ω, 12Ω to 354Ω and 12Ω to 165Ω with a loading capacitance of 30pF, 50pF and 100pF respectively for the tested frequencies. Later the DA circuit was applied across the load and the output impedance of the source was recorded. The output impedance was found to be between 14Ω to 924Ω, 14Ω to 710Ω, 14Ω to 498Ω and 14Ω to 19Ω with a loading capacitance of 10pF, 30pF, 50pF and 100pF respectively for frequencies between 100kHz to 10MHz. The results show that the differential amplifier loads the voltage source, which caused an amplitude drop of the output signal and ultimately a decrease in the output was noticed as compared to the result without DA connection. The output impedance of the voltage source was still in the acceptable range and the source was considered for practical implementation.

Table 6.4 demonstrate the phase shift of the bipolar bootstrapped voltage source circuit at its corresponding frequency in the presence of 10pF and 50pF loading capacitance with a variable resistive load between 5kΩ-30kΩ. The phase shift of 0-deg and 180-deg output signal are presented in a range format from lower to higher tested load. It was observed that phase shift was reduced with the increase of resistive load value. It was also observed that the phase shift of the differential voltage signal was an average of 0-deg and 180-deg signal. The results show that the phase shift was observed to be ≈0º till 100kHz frequency

for both 0-deg and 180-deg output signal. Above 100kHz to 20MHz, the phase shift varies between -1.39º to a maximum of -26.36º for 0-deg output signal and between -1.49º to -28.03º for 180-deg output signal. Similar phase shift behaviour was observed in other tested loading capacitances. For 30pF loading capacitance, the phase shift was observed to be between 0º to -27.84º, 0º to -29.48º and 0º to -28.66º for 0-deg, 180-deg and differential output voltage signal respectively for the frequency bandwidth of 100kHz to 20MHz. Similarly, for 100pF loading capacitance, the phase shift was observed to be between 0º to -33.30º, 0º to -34.84º and 0º to -34.07º for 0-deg, 180-deg and differential output voltage signal respectively for the frequency bandwidth of 100kHz to 20MHz. It was also observed that the phase shift was increased with the increase in loading capacitance. As frequency is increased, phase shift was decreased with the increase in load value.

Table 6.5 reports the SNR of the bipolar bootstrapped voltage source circuit within its corresponding frequency range. The SNR was calculated without and with the DA involvement in the circuit but it was observed that it didn't affect the SNR of the circuit significantly. It was observed in the results that the SNR remains within defined limits of design specification for different tested resistive and capacitive loading. The SNR of 0-deg and 180-deg voltage signals were observed to be in the range of 101dB to 87dB & 96dB to 82dB respectively for frequencies between 1kHz to 30MHz with different RC loading. A similar SNR response was observed when the DA is applied across the load. It was reported in the literature that a system with a SNR of >94dB up to 2MHz, 90dB up to 7MHz and 65dB at 10MHz (Halter et al., 2008). According to our findings, a SNR of 94dB up to 1MHz and between 94 to 90dB up to 10MHz can be achieved by good PCB fabrication. Hence it can be concluded that the circuit gives a stable SNR performance with different loading capacitance across a wide range of frequencies.

## 6.5 Summary

This chapter was based on the design complexity and performance issue of a bipolar current source when used as an excitation system. It was described in chapter 4 & 5 that the current source based on the Howland circuit topologies were greatly affected by the additional capacitance involved in the circuit. The current source circuit was not able to achieve high frequency bandwidth and was limited to either a single frequency or a very

small frequency bandwidth due to the complexity of design and output capacitance of the Howland circuit.

To solve the problem, this chapter presented a VCVS using op-amp for any bio-impedance system. Three different circuit architectures were presented and the one with the best possible performance was selected for further research. The bootstrapping technique was merged with the VCVS circuit to overcome the loading voltage problem. The VCVS circuit behaviour was described using theoretical equations. A high frequency/amplitude differential amplifier was also presented using op-amp and discrete components. The difference amplifier based on an op-amp was found helpful to some extent and its performance was degraded at 10MHz. While the discrete difference amplifier was able to measure a high amplitude ($100V_{p-p}$) signal at 10MHz frequency without any significant phase shift in its output.

The single-end and bipolar bootstrapped VCVS were simulated over a wide band of frequencies in the presence of loading capacitance. It was proved that the saturation of the VSVS circuit was removed by bootstrapping and high amplitude signal application was made possible to the attached load, without greatly effecting other circuit performance parameters. VCVS circuit performance parameters, namely: frequency bandwidth, output impedance, phase shift and SNR were presented. Efforts were made to achieve a VCVS circuit with a frequency bandwidth of >15MHz. The design and results of the bipolar VCVS was presented, which has achieved a low output impedance with an acceptable level of SNR. It can be concluded that a high frequency bandwidth VCVS with a precise voltage measurement circuit can be achieved by building a good quality printed circuit board with minimal on-board parasitic impedances.

Chapter 7 will address the practical implemented architectures of both excitation sources. The chapter will present the practical achieved results of an excitation system based on current source and voltage source for a bio-impedance system. The chapter will present the practical results achieved by the individual sub-circuits and its related performance parameters along with their integrated performance.

# Chapter 7

# Implementation & Testing of Excitation Source PCB Boards for an EIT System

## 7.1 Introduction

This chapter focuses on the practical implementation of the excitation sources discussed in chapter 5 & 6. Both excitation sources are implemented and tested using PCB boards. The composition of the PCB is described. It is a fibre reinforced epoxy FR4 board, made of material that doesn't conduct electricity. This board contain tracks and pads which electrically connect various points together. The PCB allows signals and power to be routed between electronic devices. A metal (called solder) makes the electrical connection between the electronic devices and PCB surface.

A PCB is composed of alternating layers of different material, which are laminated together with heat and adhesive, and result in a combined single object. These layers are: Silkscreen, Solder-mask, Copper and Substrate. The substrate is usually fiberglass and give the rigidity and thickness to the PCB. The PCB can have different thicknesses, which depend upon application requirement. The next layer is a thin copper foil laminated to the board with heat and adhesive. In commonly used double-sided PCB, the copper layer is applied on both sides of the substrate. An *N*-sided board normally refer to *N*-number of copper layers (i.e. 1-16). Copper thickness also varies and is specified by weight (i.e. ounce/square foot). Mostly 1 ounce/square foot copper is used in common PCB but PCB with high power may use 2-3 ounce copper. The next layer on top of copper foil is known as solder-mask layer. This layer is overlaid onto the copper layer to insulate the copper traces from accidental contact with other metal, solder etc. This layer helps solder to its correct place and prevents solder jumpers. This layer usually gives a green colour to PCB. The silkscreen is the top layer of PCB and is over solder-mask layer. This layer contains

component numbers, symbols, and names of the PCB for easy assembly and better user understanding. This layer is usually white in colour.

This chapter will present the block diagram of each excitation board along with its modules functionality description. The individual excitation board practical testing setup and results are presented in this chapter, which covers the following performance parameters: frequency bandwidth, output impedance, SNR, phase delay.

## 7.2 Block Diagram for the Excitation Source Board

It has been reported in the literature that the excitation source for a BI system can be a constant current or voltage source. Hence, the excitation source used in this research project is also categorised as current injection/voltage application source and was implemented on two separate PCBs, named as: current source board (CSB) and voltage source board (VSB). The intention was to use these PCB boards in the existing Sussex EIM system, but the scope of the project was changed to independent testing of the prototype PCB boards. Some additional circuits were designed and implemented to validate the performance of the individual excitation source PCB boards. This section presents the block diagram of both PCB's and describes the integrated sub-modules on each excitation source PCB board.

### 7.2.1 Current Source Board (CSB)

This PCB board is divided into eight sub-modules which are integrated together to form a complete single channel CSB. The PCB board is designed in such a manner that each sub-modules can be tested individually. The major sub-modules of the CSB are briefly described below:

***1. Internal Power Module (IPM):***

This module is responsible for generating all the internal power supplies needed for the PCB board. This module takes an external power supply and regulates it according to the requirements of the CSB.

*2.* ***Front-end Input Switching Module (FISM):***

This module takes an external sinusoidal signal from a function generator and transmit the signal to the corresponding output pin depending upon the instruction received from the microcontroller.

*3.* ***Current Source Module (CSM):***

This module is composed of two single-end (referenced to ground) current source circuits. The two single-end out-of-phase current sources are applied simultaneously to the load resulting in a bipolar CS. This module takes input signals from the FISM module and generates two output signals: 0° ($I^{+}$) and 180° ($I^{-}$) signals. This module consists of a GIC circuit attached at the output of a Howland circuit. Two of these parallel combinations are integrated within this module named as: HW-GIC 0°($I^{+}$) and HW-GIC 180°($I^{-}$). The input signal from the FISM module was inverted via an inverting amplifier and passed to the HW-GIC 180°. It was described earlier in chapters 4 & 5; different circuit configurations are required for different frequency ranges. The CSB was indented to test four different frequencies ranges: 0.1-1kHz, 10kHz, 100kHz and 1MHz frequencies, which require 4 different circuit configurations. Therefore, four CSMs were implemented to cover these frequencies. Precisely, eight HW-GIC CS circuits (i.e. four HW-GIC 0° and HW-GIC 180° each) were implemented on the PCB board.

*4.* ***High Frequency-Current Source Module (HF-CSM):***

The module is designed using discrete components to achieve a high frequency bandwidth CS. It was clear from the simulation results in chapter 5, that it is nearly impossible to tune the HW-GIC circuit at 10MHz frequency to give an optimum performance. Therefore, a new and separate CS was designed and implemented. The CSM circuit performance was limited due to the finite open loop gain and bandwidth problem of the used op-amp.

*5.* ***Signal Multiplexing Module (SMM):***

This module is used to propagate the 0° and 180° signal from the CSM to the attached load. Two levels of multiplexing is being involved in this excitation source PCB board. Level 1 multiplexing is used to propagate the signal at any of these frequencies (i.e. 100Hz/1kHz, 10kHz, 100kHz and 1MHz) to the Level 2 multiplexer. Level 2 multiplexing is used to propagate the signal to the attached load. This signal can be either the level 1 multiplexed signal or from the HF-CSM circuit. Each level of multiplexing

involves two MUX's. Level 1 consists of 4x1 MUX and level 2 consists of 2x1 MUX. One MUX in each multiplexing level is used to propagate 0° and the other is used for 180° signal transmission.

*6.* ***Guard Amplifier Module (GAM):***

This module consists of guard amplifiers, used to cancel the known capacitance introduced by four MUX's. This module is composed of two guard amplifiers, named as: Guard 0° and Guard 180°. Both guard amplifiers take its input from the attached load and generates three output voltages, which can be used to drive the power supply rails of MUX to cancel its capacitance. Guard 0° output voltages are used to drive two 0° MUX's power supplies to cancel its capacitance. Similarly, Guard 180° output voltages are used to drive other two 180° MUX's power supplies to cancel its capacitance.

*7.* ***Voltage Measurement Module (VMM):***

This module is used to measure the differential voltage drop across the load or it can be used to measure the voltage across any resistor on the PCB board. This module is composed of four differential amplifiers. First differential amplifier is based on an op-amp (AD812) whose power supplies are bootstrapped to give a high voltage differential measurement. Second differential amplifier is a discrete bootstrapped amplifier. An Op-amp based differential amplifier has some limitations at high frequency and can give good performance to a certain level. Therefore, a discrete component differential amplifier was designed and implemented to achieve voltage measurement at high frequency. Two separate discrete component differential amplifiers were implemented to measure 0° and 180° signal referenced to ground respectively.

*8.* ***Microcontroller and PC Interface Module (MPIM):***

A PIC microcontroller is used to control the selection lines of FISM and SMM blocks via a USB port interface. Software is written to control the transmission of the signal within the PCB board modules.

The integration of all the above modules will give a single channel CS excitation board, which can be used in any BI system. The whole system block diagram is shown in Figure 7.1.

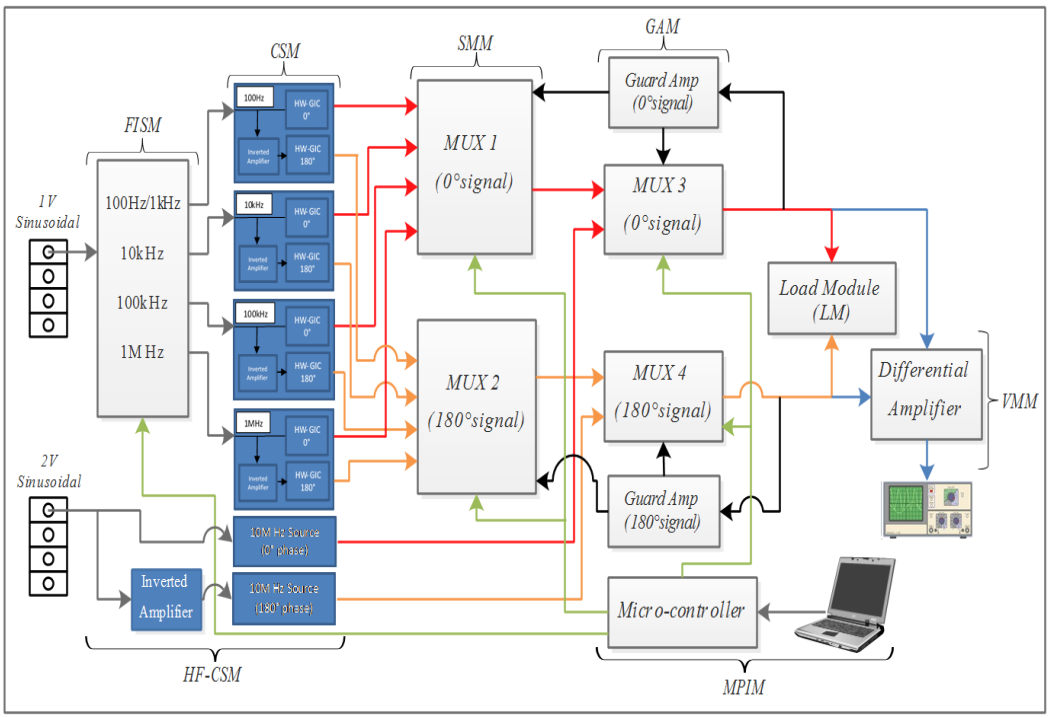



Figure 7.1: Block Diagram of CSB

## 7.2.2 Voltage Source Board (VSB)

This PCB is simple as compared to the CSB and involve fewer sub-modules. This board is divided into three sub-modules which are integrated together to acquire a single channel VSB measurement. The PCB is also designed with full flexibility to achieve each sub-modules individual testing. The major sub-modules of the VSB are briefly described below:

***1. Voltage Source Module (VSM):***

This module is composed of two out-of-phase single-end (reference to ground) voltage source circuit topologies. The two single-end circuit applied simultaneously to the load module resulted in a bipolar VS and are referred to in our design as: VS-0°($V^+$) and VS-180°($V^-$). The implemented voltage source circuit has an ability to generate a variable gain to the input signal along with ability to sense the total current generated by the source. The VSM module take an external sinusoidal input from a function generator (FG) and simultaneously passed it through a voltage buffer and a parallel inverting amplifier to generate an out-of-phase signal. Both the signals are passed through the voltage source circuits to generate VS-0°($V^+$) and VS-180°($V^-$) signals according to the predefined configuration. These two generated voltages are applied to the load module to obtain a differential measurement.

### 2. *Voltage Measurement Module (VMM):*

This module is responsible for measuring the differential voltage across the attached load or any other resistive component on the PCB. This module is designed and implemented to measure a high frequency and high voltage measurement within the VSB. The design presented in chapter 6 is implemented. The module consists of a discrete differential amplifier (DDA) and is replicated a few times on the PCB to measure differential voltages simultaneously or one at a time. Hence, the VMM is grouped into three divisions depending upon the type of voltage measurement. One group involves the voltage measurements across the load as: differential voltage, 0° and 180° load voltage signals. The other group combination are used to measure voltage across the current sense resistor and feedback resistor for the 0° voltage source circuit. The same measurement arrangements are replicated for 180° voltage source circuit.

### 3. *Load Module (LM):*

This module implements different combinations of RC components that can be selected practically to check the performance of the VSB. The module has implemented 24 combinations of RC components whose resistive element varies between 5kΩ to 30kΩ with a step size of 5kΩ along with capacitive element of 10pF, 30pF, 50pF and 100pF. This module has the flexibility to test the VSB in a bipolar as well as single-end RC combination attached to the VSB.

The integration of all the above modules will give a single channel VS excitation PCB, which can be used in a BI system. The whole system block diagram is shown in Figure 7.2.

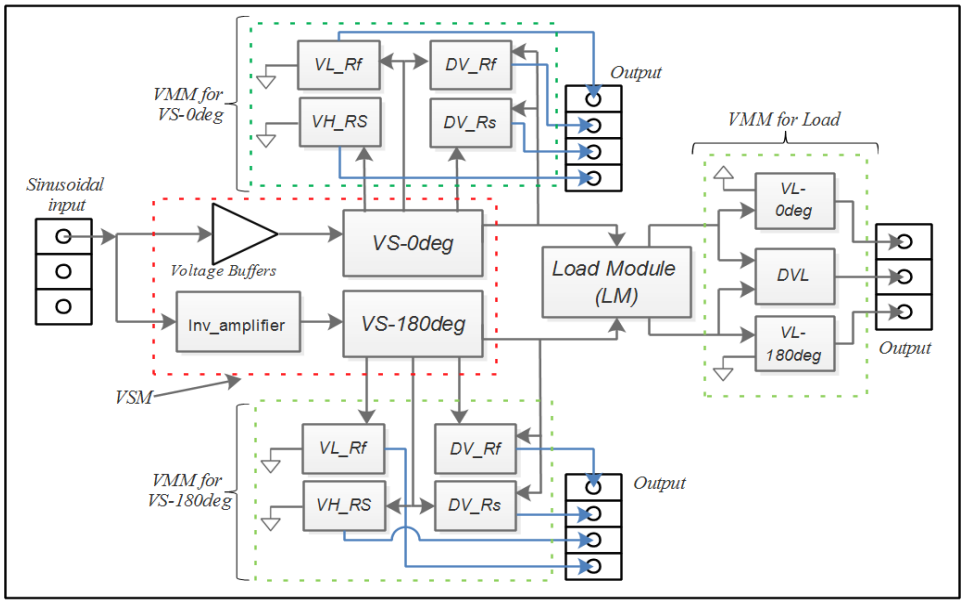



Figure 7.2: Block Diagram of VSB

## 7.3 Voltage Source PCB Board Performance

The differential voltage excitation source is implemented on a PCB as shown in Figure 7.3. The different modules described in section 7.2.2 are highlighted. The prototype PCB was designed with the flexibility to test the individual sub-circuits on the board without effecting other nearby circuits. This board can be used as a single-ended (reference to ground) source as well as a differential source.

The PCB schematic and layout were created using XL designer PCB creator from Seetrax CAD software. The final PCB is a two-layer board with components attached on the top layer and copper fill on the bottom layer.

To achieve better electrical performance and a small PCB package, the amplifiers used are small surface mount components (SMC) along with all other peripheral components on the PCB. The SMC are smaller, which can be placed/mounted directly on either side of the PCB and don't require any holes to mount the components. The SMC are preferred as compared to conventional through-hole components (THC) due to the advantages of: 1) Low resistance and inductance at the terminals, 2) high component density, 3) better electromagnetic compatibility due to smaller radiation area and lead inductance and 4) better mechanical performance under shake and vibration conditions.

The PCB is designed in such a manner that all the tracks within a single sub-circuit and nearby supporting circuits are arranged to be as short as possible and are connected to the nearest ground terminal. The PCB has a ground plane on the board to connect different components of the board to the nearest ground potential. Two different track widths are used for signal transmission. The tracks, which allow the flow of power are wider and of a size of 0.0200 inch while the normal tracks used to transmit signals between components of the circuit are 0.0120 inch wide. The PCB used six wire-to-board vertical connectors to take measurements from different parts of the board. The board tracks are routed in such a manner that the track lengths between each individual sub-circuits are also minimal.

The PCB also used the decoupling capacitors for each power supply of the op-amp used in the VS circuitry. The purpose of this bypassing is to supress high frequency noise in the power supply signals and must especially be used when driving current loads. The decoupling capacitors act as a small local power supply for respective IC. In case of a

temporary voltage drop in the power supply, the decoupling capacitor can briefly supply power at the correct voltage. Due to this feature, these capacitors are called bypass capacitors as they can act as a temporary power source, hence bypassing the main power supply of the circuit. In our voltage source PCB, a 100V SMD multilayer ceramic 1µF capacitor with ±10% tolerance is added to each of the power supply pins of the op-amp.

The resistors and capacitor used in the voltage source PCB are of component case size 0805. The voltage source PCB uses thick film resistors having a voltage rating of 150V, power rating of 100mW with ±1% tolerance. The resistors matching is approximately similar due to fact of coming from the same manufactured tape/reel. Similarly, the voltage source PCB uses SMD multilayer ceramic capacitors having a voltage rating of between 16-100V and ±5 to ±10% capacitance tolerance.

The points used on the PCB to take output measurement signal are AC coupled. It is also called capacitive coupling and is useful because the DC component of the signal act as a voltage offset and by its removal the resolution of measured signal can be increased. The simple implementation is achieved by placing capacitor between two nodes/circuits such that the AC signal from the first part is passed to the next circuit while blocking the DC component. In the voltage source PCB, the output nodes use DC-blocking capacitors of 100nF to implement AC coupling.

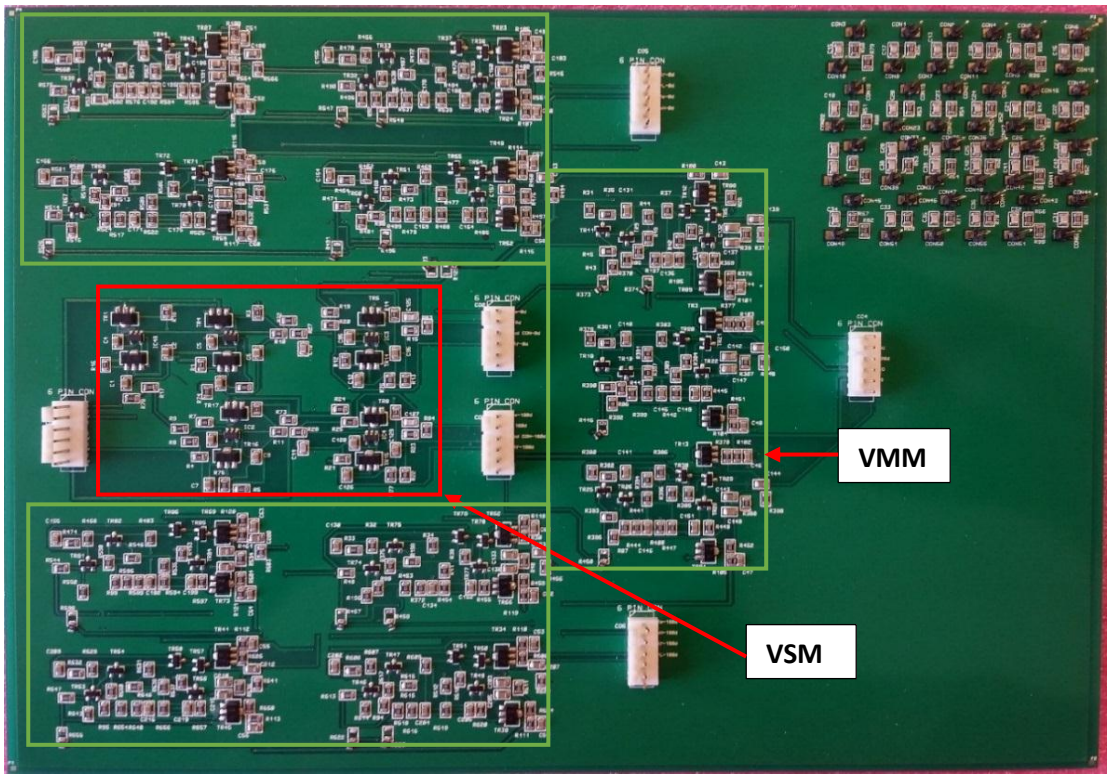



Figure 7.3: The Voltage Source PCB

### 7.3.1 Voltage Source (VS) Circuit Performance

To evaluate the performance of VSM, an experiment was setup using a FG, DC power supplies, oscilloscope and VSB PCB. The internal power supply module of the VSB is not complicated and requires only two external power supplies. A maximum of ±60V power supply voltages were configured by cascading two ±30V supply voltage from the equipment available in the laboratory. Initially the VSM was tested at a low power voltage (±15V) and later was extended to high voltage (±36V) for its performance evaluation.

A sinusoidal signal was generated using a built-in FG of a Schlumberger SI-1260 impedance/gain-phase analyser. It was used because of its flexibility to generate sinusoidal signals at high frequency (≥10MHz) and its availability in our laboratory. It uses microprocessor controlled digital/analogue techniques to provide a range of impedance and frequency response measurement facilities. In our experiments, it was mostly used as a signal generator. Its characteristics are summarised in Figure 7.4.

The output signals were captured using a Tektronix digital storage oscilloscope (TDS, 2014B), which can acquire four independent signals at a sampling rate of 1GS/s and 100MHz frequency bandwidth. Before taking any measurements, the scope probes were correctly compensated by attaching to an oscilloscope PROBE COMP ~5V connector and adjusted until a flat-top square signal was achieved. The scope probes (MI007) have various attenuation factors that affect the vertical scale (amplitude) of the signal. The probe attenuation should be matched with the attenuation level of the oscilloscope. The default oscilloscope setting for the probe is *10X* and was used in all our experimental measurements. The bandwidth of the oscilloscope will be limited with *1X* probe attenuation. Hence, to avail the full bandwidth of the oscilloscope, it should be set to *10X*. The detailed characteristics of the probe are given in Figure 7.5.

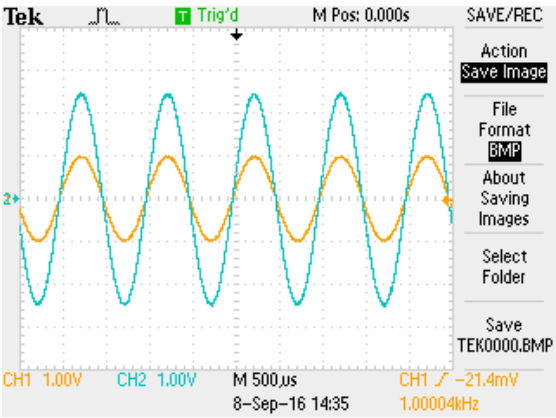
| | | | |
|---|---|---|---|
| GENERATOR | TYPE | **[voltage]** • current | |
| | FREQ | (+ ) **[Hz]** • kHz • MHz • pHz • mHz | 10μHz to 32 MHz<br>default = 100Hz |
| | V. AMPL | (+ ) **[V]** • mV | 0V to 3V ($f \leq$ 10MHz)<br>0V to 1V ($f >$ 10MHz) |
| | V. BIAS | (+ ) **[V]** • mV | -40.95V to +40.95V |
| [GENERATOR Cont.] | TYPE | **[voltage]** • current | |
| | FREQ | (+ ) **[Hz]** • kHz • MHz • pHz • mHz | 10μHz to 32 MHz<br>default = 100Hz |
| | I. AMPL | (+ ) **[mA]** • μA | 0mA to 60mA ($f \leq$ 10MHz)<br>0V to 1V ($f >$ 10MHz) |
| | I. BIAS | (+ ) **[mA]** • μA | -100mA to +100mA |

Figure 7.4: Function Generator operational characteristics

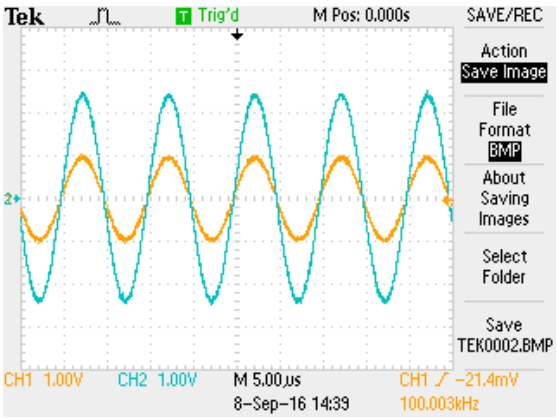
| *Attenuation Ratio* | *Probe Bandwidth* | *Input Resistance* | *Input Capacitance* | *Compensation Range* | *Maximum Working Voltage* |
|---|---|---|---|---|---|
| 1:1 (1X) | DC - 15MHz | 1 MΩ ± 2% | 70p - 120pF | N/A | 200$V_{p\text{-}p}$ (CAT II) |
| 10:1 (10X) | DC - 60MHz | 10 MΩ ± 2% | 14p -18pF | 15 – 45pF | 600$V_{p\text{-}p}$ (CAT II) |

Figure 7.5: MI007 probe characteristics

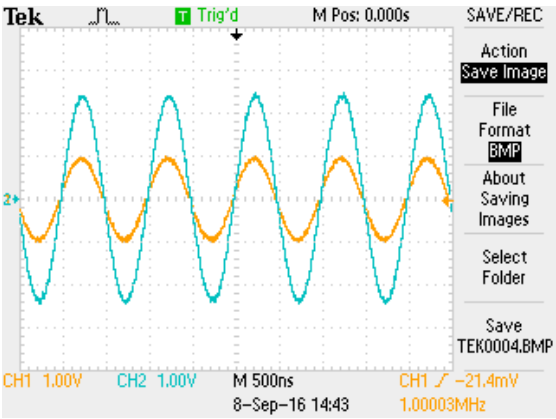
The VSM was tested using ±15V DC power supply rails attached with a load of 2kΩ, 5kΩ and 5kΩ‖10pF (loading capacitance). A sinusoidal signal of $2V_{p\text{-}p}$ was generated using a FG for the frequency range between 1kHz to 15MHz. To understand the performance level achieved by the VSM, a series of tests were conducted for: maximum operational frequency range, output impedance, maximum load amplitude, phase difference between the signals and SNR of the circuit. The results presented for VSM include an additional loading capacitance (≈15pF) for each probe. The experimental scope results obtained from VSM using a 2kΩ load are presented in Figure 7.6. The results show the amplitude of output signal (blue) with respect to the amplitude of input signal (yellow).



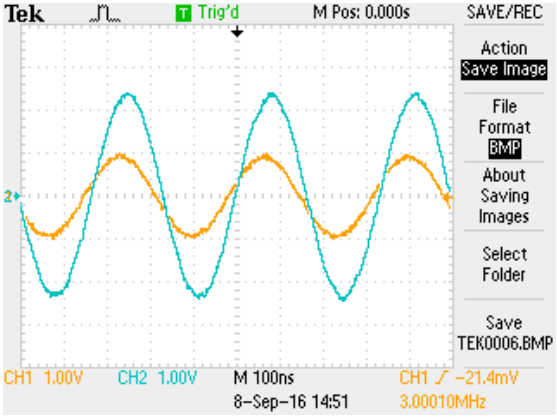

*(a)* Load voltage at 1kHz



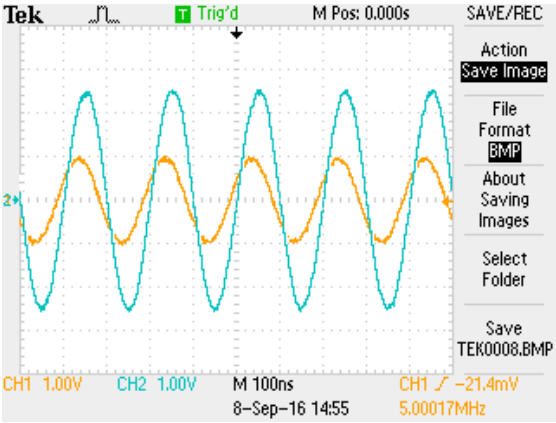

*(b)* Load voltage at 100kHz



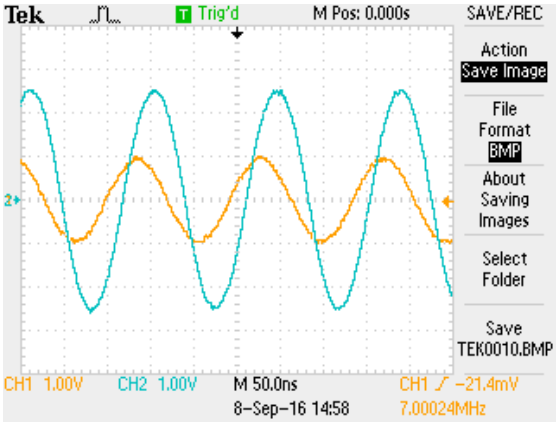

*(c)* Load voltage at 1MHz



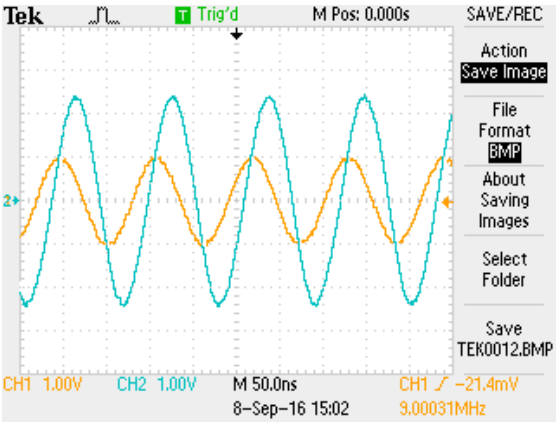

*(d)* Load voltage at 3MHz



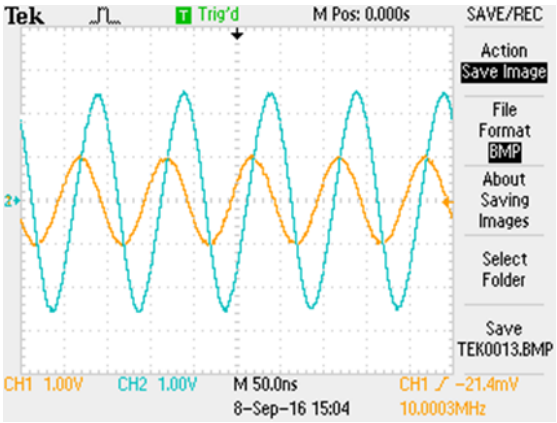

*(e)* Load voltage at 5MHz



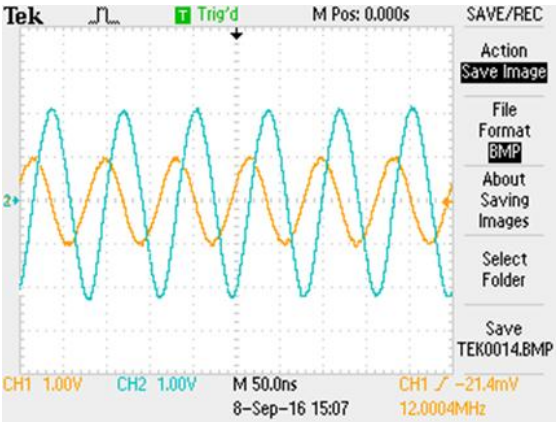

*(f)* Load voltage at 7MHz



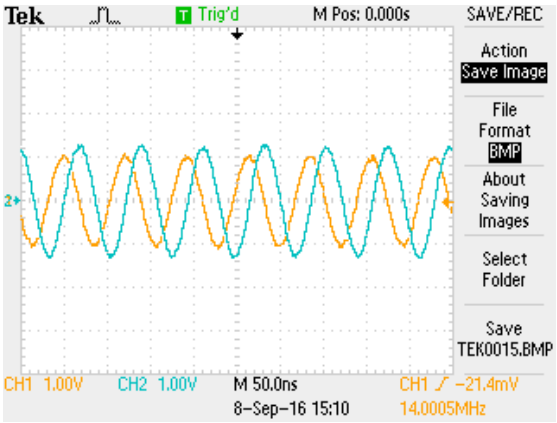

*(g)* Load voltage at 9MHz




*(h)* Load voltage at 10MHz




*(i)* Load voltage at 12MHz




*(j)* Load voltage at 14MHz

Figure 7.6: Voltage Source loading voltage at different frequencies

The experimental results show that the VS circuit has achieved a good performance level by providing the required signal amplitude at high frequency (i.e. 10MHz). The detailed performance parameters are presented in the next section. The VSM was also tested for other loading combinations mentioned earlier and achieved a similar performance level. These experimental oscilloscope results are presented in appendix E of this thesis.

### *7.3.1.1 Maximum Operational Frequency Test*

The purpose of this test is to calculate the frequency bandwidth of the VSM circuit while maintaining a constant output voltage. The VSM circuit was tested with a gain of 1.5 and was expected (theoretically) to deliver a constant voltage amplitude of 2.5V irrespective of the attached load for a wide frequency band. In this test, the VS circuit was attached with three different load combinations and the amplitude response of the output voltage was observed. The cut-off frequency point *(-3dB)* will be the point when the amplitude of the output voltage falls below 70.71% of the peak amplitude. In our case it will be a voltage amplitude of ≈1.77V (0.7071 x 2.5V). The experiment was repeated for multiple voltage measurements at various frequencies using different test load combinations. The plot for voltage measurements at different frequency levels with its corresponding loading is presented in the Figure 7.7.

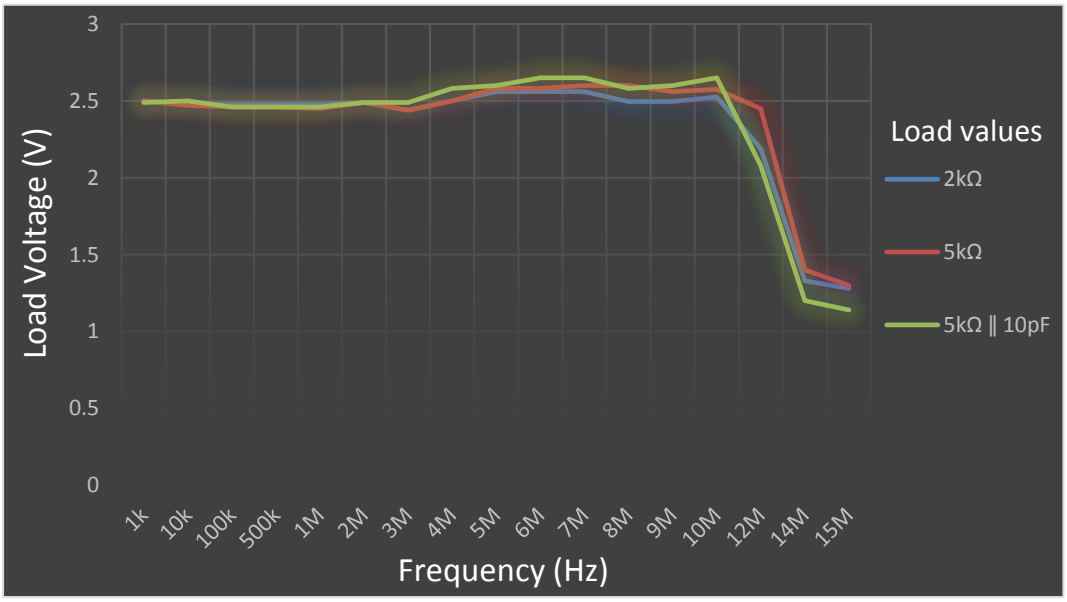



Figure 7.7: Load voltage versus Frequency

The experimental results in Figure 7.7 show that the VS circuit was able to maintain a constant voltage amplitude up to ≈3-4MHz. For frequencies >4MHz, the amplitude is still constant but is slightly increased. The amplitude remains constant until ≈10MHz and reduces afterwards. According to the achieved experimental results, the voltage source has achieved a cut-off frequency point of ≈12-13MHz and can be considered as a high frequency excitation source for an impedance measurement device. Based on these results, the performance of the prototype voltage source can be further optimised to achieve a precise constant amplitude over a wide frequency bandwidth.

### 7.3.1.2 Output Impedance Test

The purpose of this test is to identify the amount of generated voltage that is applied as loading voltage. As mentioned earlier in this thesis, any circuit can be represented by its equivalent Thevenin circuit (output resistance/impedance in series with a voltage source). This test is based on the same principle and will be implemented in two steps: 1) measure open circuit voltage $(V_{open})$ of the source, 2) then measure the output voltage of the source in the presence of a load$(V_{Load})$. The output impedance of the circuit is then calculated using Eq. 7.1. In this test, the circuit was also attached with three different load combinations and the loading voltage amplitude was observed. For a good performance of the VS, the output impedance of the circuit should be as low as possible so that the maximum voltage can be dropped across the attached load. The plot for output impedance of the voltage source at different tested frequencies with respect to its corresponding loading is presented in the Figure 7.8.

$$Z_{out} = R_L \left(\frac{V_{open}}{V_{Load}} - 1\right) \qquad \text{Eq. (7.1)}$$

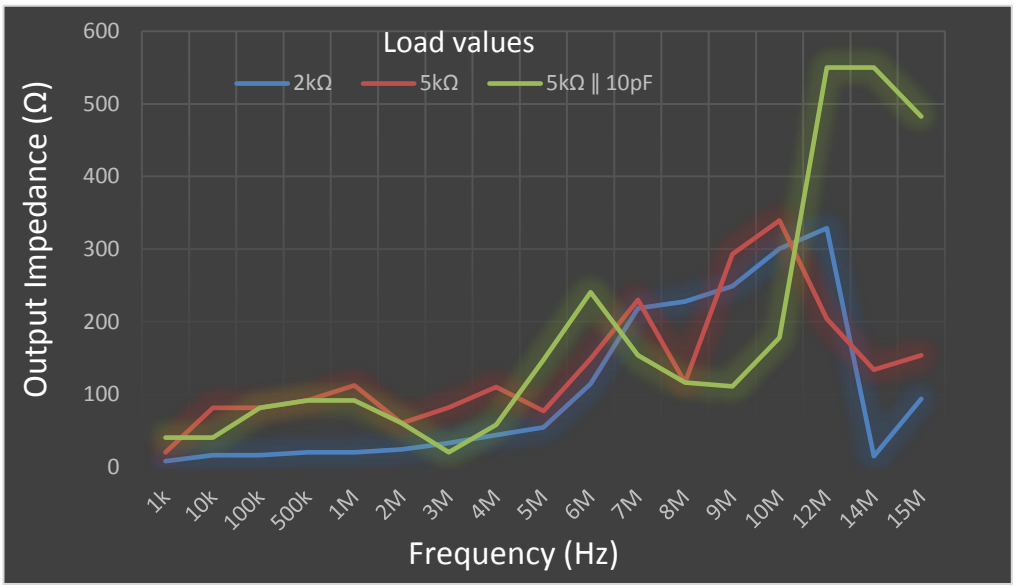



Figure 7.8: Output impedance versus Frequency

The experimental results in Figure 7.8 show that the VSM circuit has achieved a low output impedance (≈150Ω) until 5-6MHz. For frequencies >6M and ≤12MHz, the output impedance is found to be <350Ω. For 14-15MHz, the output impedance response is low due to the reduction in the amplitude of the output voltage to it corresponding input voltage. An impedance of >1kΩ is represented by graph point >500. The overall response of the output impedance is not steady but generally, it increases with frequency. The

unsteady response is due to slight difference in the voltage amplitude for different tested loadings. The optimization of this performance parameter can be achieved by a constant amplitude over a wide frequency band.

### *7.3.1.3 Phase Difference Test*

The purpose of this test is to find the phase change in loading voltage with respect to the input signal and its behaviour over a certain frequency range. The phase difference ($\phi$) was calculated using the oscilloscope measurements by adjusting the time scale until at least one full waveform of observed signals was displayed on the oscilloscope screen. The measurements were taken by: first by measuring the wavelength (λ) of the signals (time difference between the amplitude peak of input and output signal), followed by the period measurement of the signal. The $\phi$ of the circuit at corresponding frequency, is then calculated using Eq. 7.2.

$$\phi = \left(\frac{\lambda}{period}\right) x\ 360^{\circ} \qquad \text{Eq. (7.2)}$$

These test measurements were performed at various frequencies using different load combinations and the signal shifting was observed on the time scale. Based on phase information, the leading or lagging of a signal can be interpreted. The phase shift should be minimum between the signals but due the capacitive factor involved within the circuit/system, it is difficult to avoid this situation especially at high frequencies. The plot of phase difference of the VSM circuit at different frequency levels with its corresponding loading is presented in the Figure 7.9.

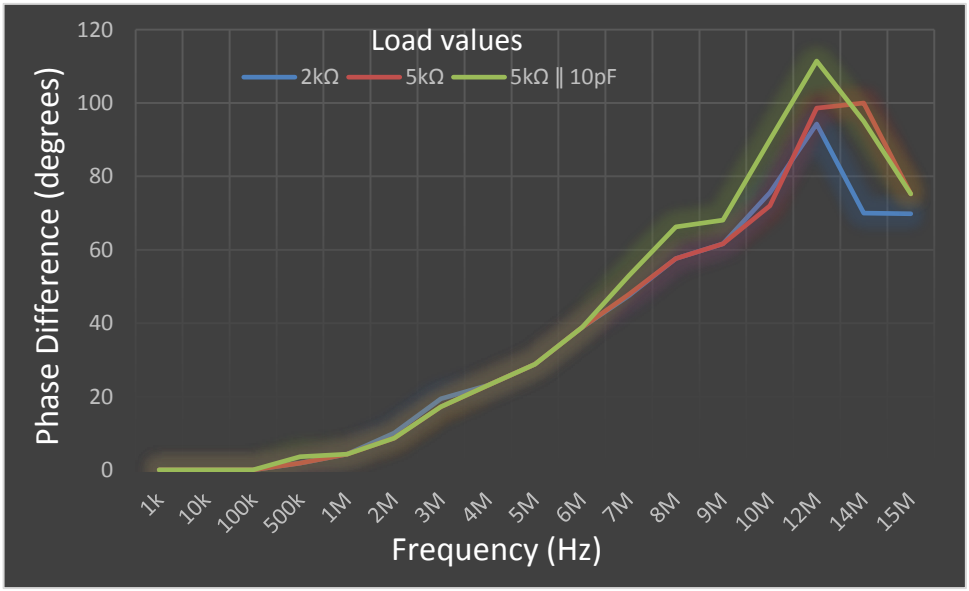


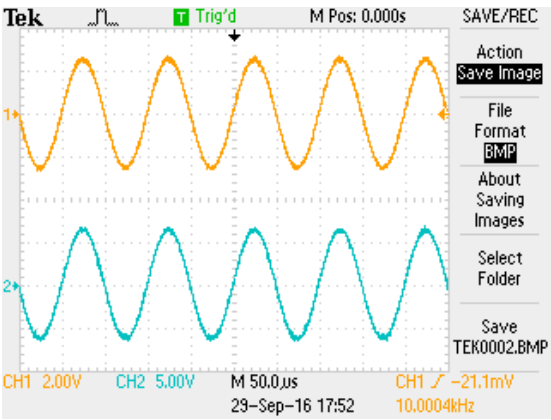

Figure 7.9: Phase difference plot versus Frequency

The experimental results in Figure 7.9 show that the VSM circuit was able to maintain a small phase shift (<40°) until ≈5-6MHz. For frequencies >6MHz, the phase shift is steady and increased with frequency having a maximum phase shift of 112° at 12MHz. The experimental results show that load voltage was leading the input signal at all tested frequencies.

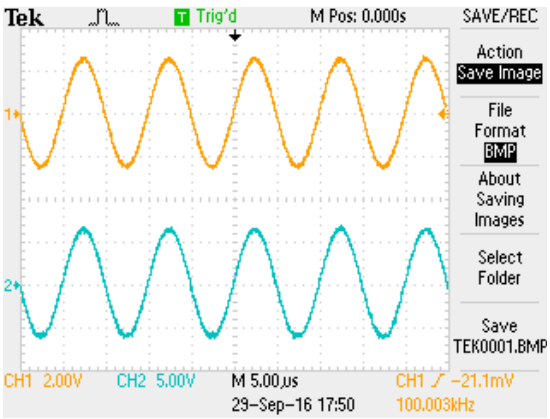
### *7.3.1.4 Circuit Maximum Loading Test*

The purpose of this test is to identify the maximum loading amplitude that can be achieved from the VSM without any saturated output signal. The voltage source was bootstrapped to achieve maximum voltage amplitude swing, closer to its applied power supply rails. Although the amplitude of output voltage will saturate when it reaches near its applied supply rails voltage but it gives the flexibility to adjust the amplitude by increasing the applied power supply rails, which is made possible due to the usage of a high voltage transistor in the bootstrapped circuitry.

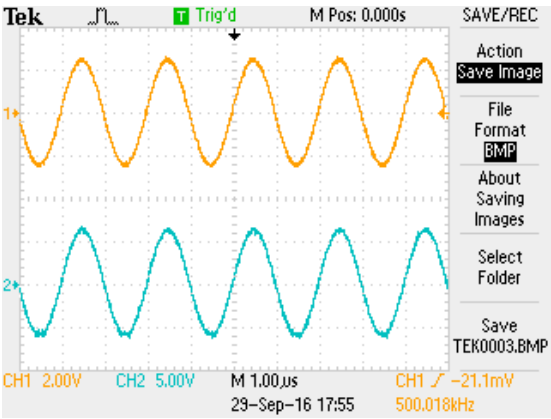
For our VS circuit, the amplitude of the voltage signal depends on the gain of the circuit that is constant for all tested loads. To evaluate this test, either the gain of the circuit or the amplitude of the input signal needs to be increased followed by the measurement of the resulting output voltage. The voltage source was initially tested with ±15V power supply rails with different loading combinations and the maximum achievable amplitude of output signal was measured. Later the supply rail voltages were increased to ±36V to demonstrate any increase in the amplitude of output voltage signal and its performance. The maximum loading amplitude of the VSM (±15V power supply) was tested and is presented in Figure 7.10.



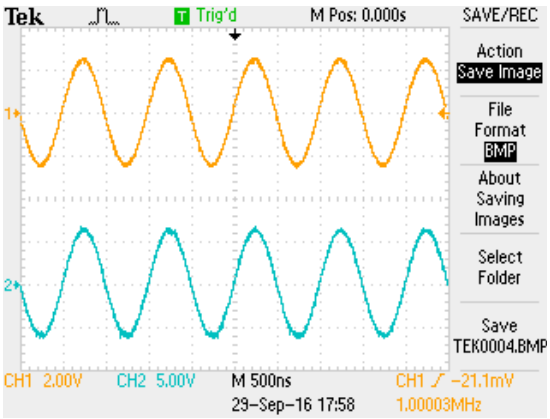

*(a)* Maximum load voltage at 10kHz



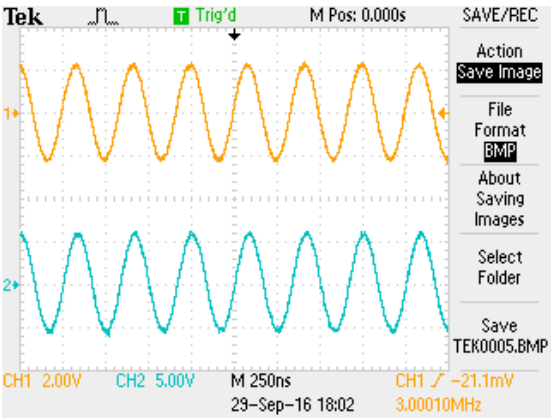

*(b)* Maximum load voltage at 100kHz



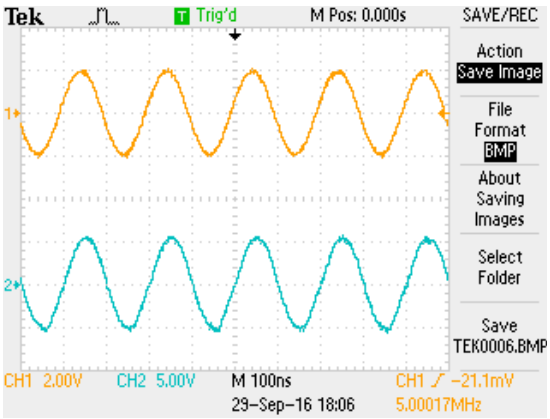

*(c)* Maximum load voltage at 500kHz



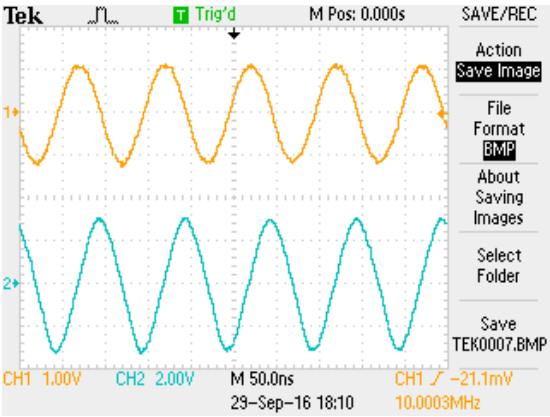

*(d)* Maximum load voltage at 1MHz




*(e)* Maximum load voltage at 3MHz




*(f)* Maximum load voltage at 5MHz




*(g)* Maximum load voltage at 10MHz

Figure 7.10: Maximum loading amplitude measured at different frequencies for 2kΩ loading

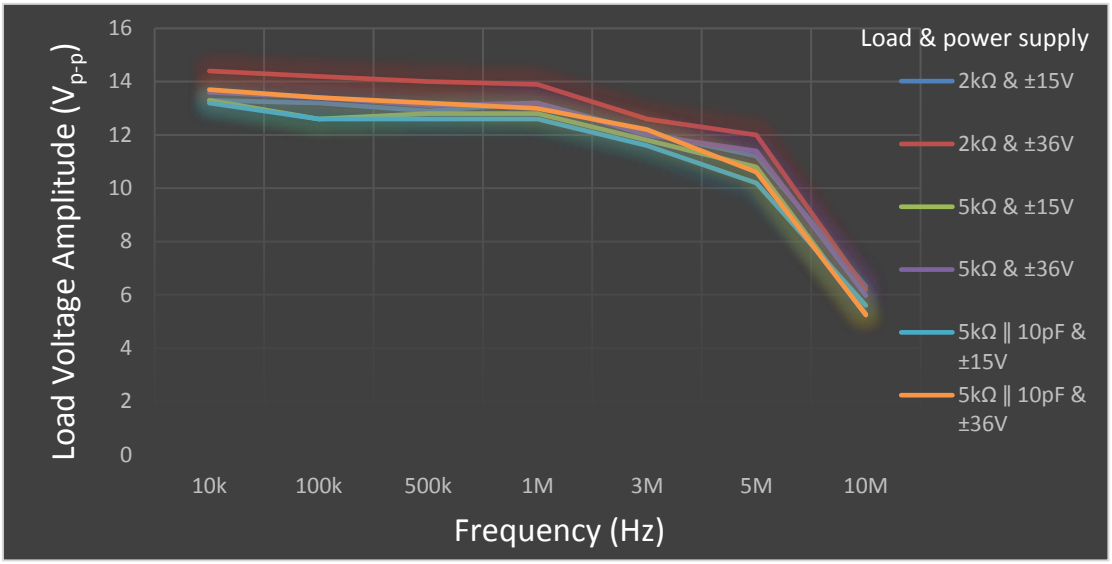



Figure 7.11: Maximum loading voltage at respective tested frequencies

The experimental results show that the VSM circuit was able to maintain the expected amplitude of the output voltage signal without output saturation for certain power supply rail. The experimental measurements for different tested loading are plotted in the Figure 7.11. At ±15V DC power supply, an AC input between 2.64 to 1.04V can be applied to the source for a frequency range of 10k to 10MHz under different loading. A maximum of ≈13.3$V_{p-p}$ output voltage was achieved for this particular power rail setting as shown in Figure 7.11.

The power supply rails were increased to ±36VDC and a slight improvement in the circuit was achieved. At this power rail setting, an AC input of amplitude between 3V to 1.42V can be applied to the source for the same frequency range and loading described earlier. At this setting, a maximum of ≈14.4$V_{p-p}$ output voltage was achieved. Above this input amplitude, the output was saturated and didn't achieve the required amplitude even with an increase in power supply rails. The experimental results show that the amplitude of the output signal was decreased with an increase in circuit gain and has also affected the frequency bandwidth of the VS circuit.

Based on these experimental results, the VS performance was restricted to an output voltage signal of ≈15$V_{p-p}$ regardless of the high voltage power supply rails in the bootstrapped circuitry. This leads an opportunity to further investigate the VS circuitry for an increase in the maximum loading amplitude capacity. Similar experimental results (shown in Figure 7.10) were observed for other test loadings.

### 7.3.1.5 SNR Test

The purpose of this test is to identify the strength of the desired signal with respect to its background unwanted interference. This test involves two level measurements: 1) the VS circuit was tested with $0V_{p\text{-}p}$ input signal and the amplitude of the output signal was measured, 2) then the VS circuit was applied with an AC voltage of $2V_{p\text{-}p}$ followed by the amplitude measurement of the output signal. The peak-to-peak voltage amplitude of both signals were measured using the oscilloscope and there root mean square (RMS) value is calculated as: $V_{RMS} = V_{amplitude} * 0.7071$. The calculated RMS amplitudes were used in the Eq. 7.3 to calculate the SNR of the output signal. The voltage source was tested with the ±15V power supply rails with different loading combinations and the SNR was calculated at a specified frequency with respect to its input RMS voltage. The SNR of the voltage source for different frequency range is presented in Figure 7.12.

$$SNR = 20 \log_{10}\left[\frac{(Load\ Voltage)_{RMS}}{(Noise\ Voltage)_{RMS}}\right] \qquad \text{Eq. (7.3)}$$

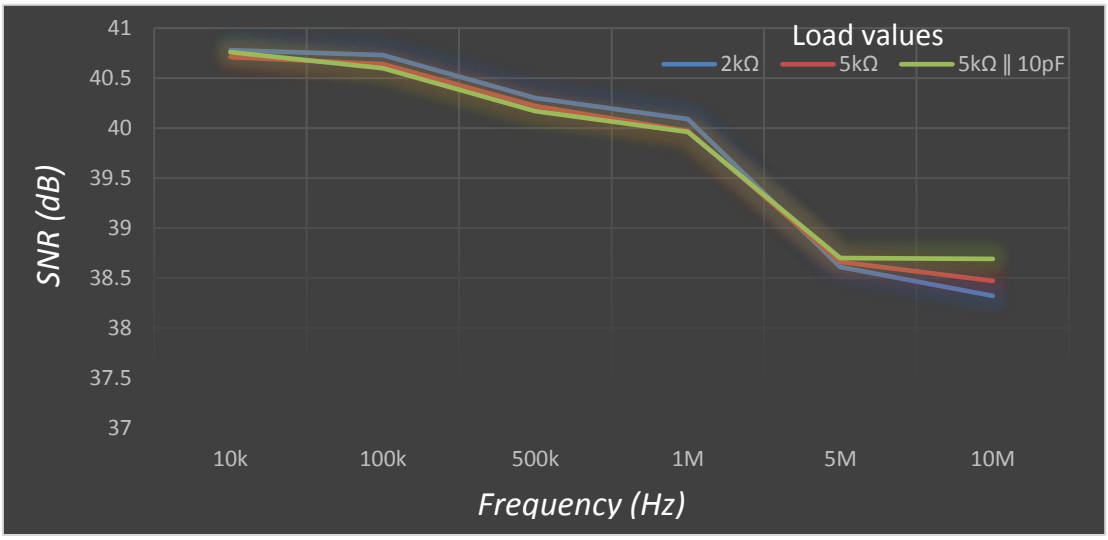



Figure 7.12: Voltage source SNR at different frequencies

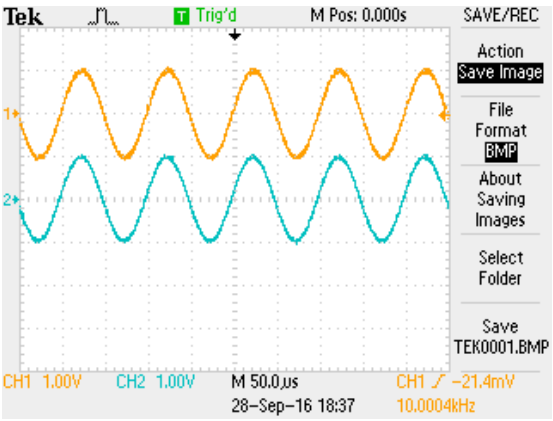
The calculated SNR value based on the experimental measurement in Figure 7.12 shows that the VS circuit was able to maintain an approximate SNR of 41dB to 38dB for a RMS voltage range of $3.47V_{p\text{-}p}$ to $3.57V_{p\text{-}p}$ at different tested loads. The overall SNR response for the frequencies range between 10k - 1MHz, is steady and decreased after this frequency with an achieved SNR of ≈38dB at 10MHz. The experimental results of voltage amplitude obtained from the oscilloscope were based on the average measurements and give an opportunity to further improve the SNR by a precise amplitude reading obtained from the oscilloscope.

## 7.3.2 Differential Amplifier Circuit Performance

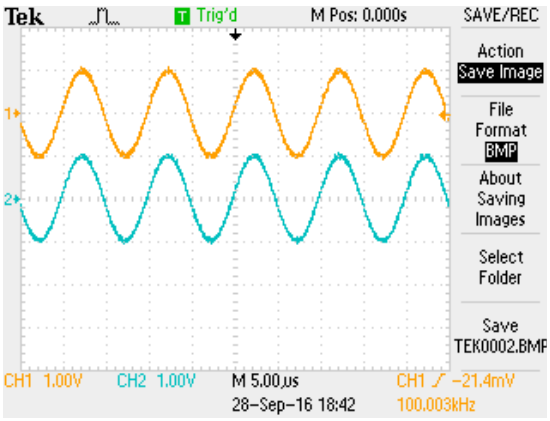
The performance of the prototype DA circuit of the VSB is evaluated independently with the intension of applying it to the VSB measurements upon achieving reasonable performance. All DA's on the VSB are a replica of each other, hence it was decided to first evaluate the performance of one DA independently and then extended later to other parts of the VSB for voltage measurements. This part of the board is also referred to as VVM. The power supply of the DA module can be applied independently or can be integrated from the main power supply of the VSB. The DA circuit was tested at a power supply voltage of ±36V by cascading two power supplies available in the laboratory.

A sinusoidal signal was generated using a FG with variable amplitude for the frequency range between 10kHz to 10MHz. To understand the performance level achieved by the DA module, multiple measurements were conducted to check the maximum operational frequency range of the DA without reduction in the output voltage amplitude. The results presented for the DA includes an additional loading capacitance (≈15pF) for testing the probe.

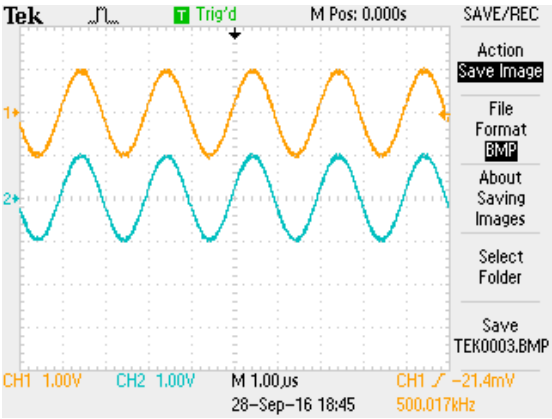
The experimental oscilloscope results obtained from the DA circuit using $2V_{p\text{-}p}$ input signal are presented in Figure 7.13 (a-g). The results show the output signal amplitude (blue) with respect to the input signal amplitude (yellow). The DA circuit was also tested to evaluate the maximum achievable output amplitude for a particular circuit setting and results are plotted in Figure 7.14.



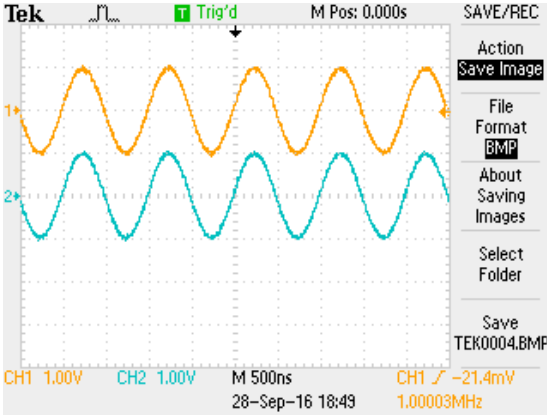

*(a)* DA output voltage at 10kHz



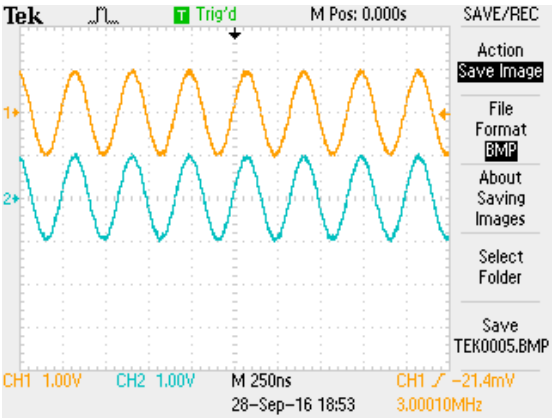

*(b)* DA output voltage at 100kHz



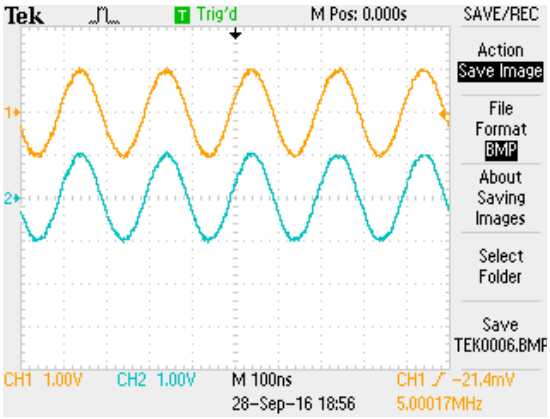

*(c)* DA output voltage at 500kHz



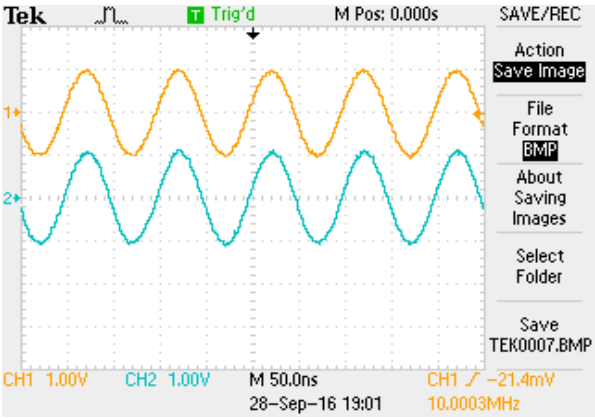

*(d)* DA output voltage at 1MHz




*(e)* DA output voltage at 3MHz




*(f)* DA output voltage at 5MHz




*(g)* DA output voltage at 10MHz

Figure 7.13: DA Output voltage using $2V_{p\text{-}p}$ input at different frequencies

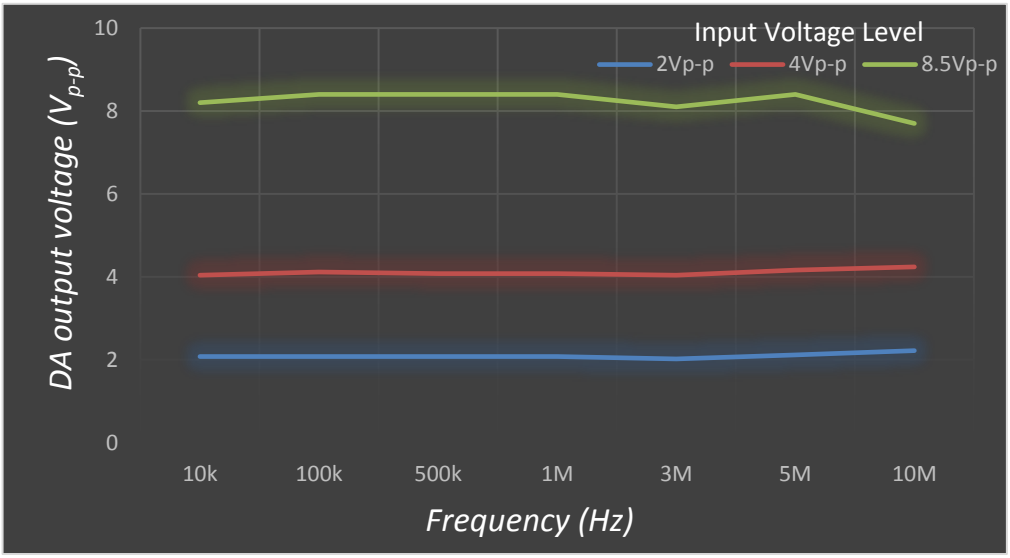



Figure 7.14: DA output voltage using different input voltages at respective frequency

The plotted experimental results show that the DA circuit was able to measure a constant voltage signal amplitude up to 10MHz until the input amplitude is 2V. For an amplitude of >2V, the DA was able to measure the required output amplitude up to 5MHz with an amplitude reduction in output signal at 10MHz. This shows that the frequency bandwidth of the DA circuit was reduced with an increase in the signal output voltage level. This is possibly due to stray capacitance involved in the PCB and slight mismatching of the analogue component characteristics. Using an impedance analyser FG, the maximum achievable results are shown in Figure 7.14. At 10MHz, the output voltage signal is slightly distorted with an input amplitude of 4.25V. This limits the performance of the DA circuit to an input amplitude of ≈3-3.5V for a wide frequency bandwidth measurement (i.e. 10k – 10MHz). The phase difference was measured to be negligibly small for the whole range of tested frequencies.

Another FG (Jupiter-2000) was also used to generate a high amplitude input voltage but was limited to only 1MHz frequency. For the same DA circuit setting, a 5V signal amplitude was applied to the DA circuit and it was able to measure $10V_{p-p}$ output signal for 10kHz, 100kHz and 1MHz frequency. It was observed that the DA circuit was able to measure a maximum of $\approx 12V_{p-p}$ signal for a specific power supply rail setting (±36V). This shows the ability of the DA circuit to measure the same output signal amplitude at ≈5-6MHz. According to the achieved experimental results, it can be generally interpreted that the DA circuit has achieved a cut-off frequency point of 10MHz and can be used as a high frequency voltage measurement circuit for impedance measurement device. Based

on these results, the performance of the prototype DA circuit can be further optimised to acquire precise high amplitude signal at high frequency.

## 7.4 Current Source PCB Board Performance

The PCB implementation of a differential current excitation source along with its other supporting modules is shown in Figure 7.16. The detailed description of the CSB was presented earlier in section 7.2.1. Like VSB, the prototype CSB also has the flexibility to test all individual sub-modules. The CSB has also followed the similar implementation standards as used for VSB.

All the components used on the CSB are SMC with closest possible placement within a respective submodule to keep the respective module track as short as possible. The CSB also has a ground plane throughout under the PCB and uses different tracks size for normal and power supply transmission lines. The 0805 case size was used for passive components having the following performance rating: 150V, 0.1W and ±1% tolerance (resistance) and 25V-100V, ±5 to ±10% tolerance (capacitance). The CSB also uses decoupling capacitors at all the power supply nodes along with AC coupling on all the nodes which are used to take output measurements. The CSB has used an eight wire-to-board connector to provide or acquire electrical signals from the PCB. A brief description of each module is presented along with its implemented components.

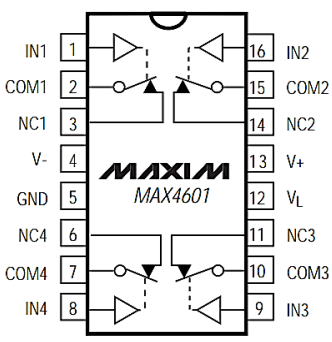
The FISM is implemented using a MAX4601 chip. It is a quad analogue switch, which features low on-resistance of maximum 2.5Ω and low off-leakage current of maximum 2.5nA. Each switch can acquire analogue signals until its rail-to-rail supply. This switch is suitable for low distortion applications and is preferred over mechanical relays in automatic test equipment or applications, which require current switching. It has four closed switches with a low power requirement and can be operated by either a single supply (+4.5 to +36V) or dual supplies (±4.5V to ±20V). The IC was operated at ±15V in our CSB. The FISM is controlled by the MPIM to route the external signal to its assigned module (CSM) (Datasheet MAX4601, 2016).

The CSM is the implementation of a CS along with capacitance cancellation (GIC) circuit. The CS and GIC circuit are implemented with an AD812 and THS4304 op-amp respectively. This module used high voltage transistors (BF620 & BF621) to bootstrap the CS and GIC circuitry for a high amplitude signal measurement.

The output of the CSM is routed to the load (LM) through the SMM. The SMM consists of two level multiplexing and was implemented using ADG1204 and ADG1219 multiplexers.

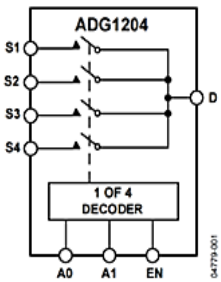
The ADG1204 is a CMOS analogue multiplexer comprised of 4-channels designed on a modular manufacturing process that combines high voltage CMOS and bipolar technologies (iCMOS®). It has an off-source capacitance of 1.5pF, on-resistance of 120Ω and <1 pC charge injection fully specified at ±15V power supply. Its ultralow capacitance and charge injection makes it suitable for data acquisition application having low glitch and fast switching requirement. It is useful for video signal switching due to its fast switching speed together with high signal bandwidth. The ADG1219 is a SPDT switch based on the same technology with off-source capacitance of 2.5pF, on-resistance of 120Ω and <0.5 pC charge injection over fully specified at ±15V power supply (Datasheet ADG1204 & ADG1219, 2016).

Both multiplexers use 3V logic-compatible inputs. The power supplies of the SMM is dependent on the GAM that generates the voltage signals according to the attached loading. The ADG1204 implements level 1 multiplexing to route any of the four signals generated from the CSM. While the ADG1209 implements the level 2 multiplexing to either route level 1 signals to the respective load or route the signal from the HF-CSM unit. The functional diagram and logic table of the devices used in FISM and SMM are presented in Figure 7.15. The pin packing used for these devices are: SSOP-16 (MAX4601), TSSOP-14 (ADG1204) and SOT-23 (ADG1219).



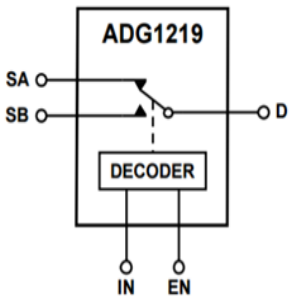

| MAX4601 | |
|---|---|
| LOGIC | SWITCH |
| 0 | ON |
| 1 | OFF |

(a)




| EN (LOGIC) | A1 | A0 | SWITCH | | | |
|---|---|---|---|---|---|---|
| | | | S1 | S2 | S3 | S4 |
| 0 | X | X | OFF | OFF | OFF | OFF |
| 1 | 0 | 0 | ON | OFF | OFF | OFF |
| 1 | 0 | 1 | OFF | ON | OFF | OFF |
| 1 | 1 | 0 | OFF | OFF | ON | OFF |
| 1 | 1 | 1 | OFF | OFF | OFF | ON |

(b)




| EN (LOGIC) | IN | SWITCH | |
|---|---|---|---|
| | | SA | SB |
| 0 | X | OFF | OFF |
| 1 | 0 | ON | OFF |
| 1 | 1 | OFF | ON |

(c)

Figure 7.15: Functional block diagram and logic table of FISM and SMM devices

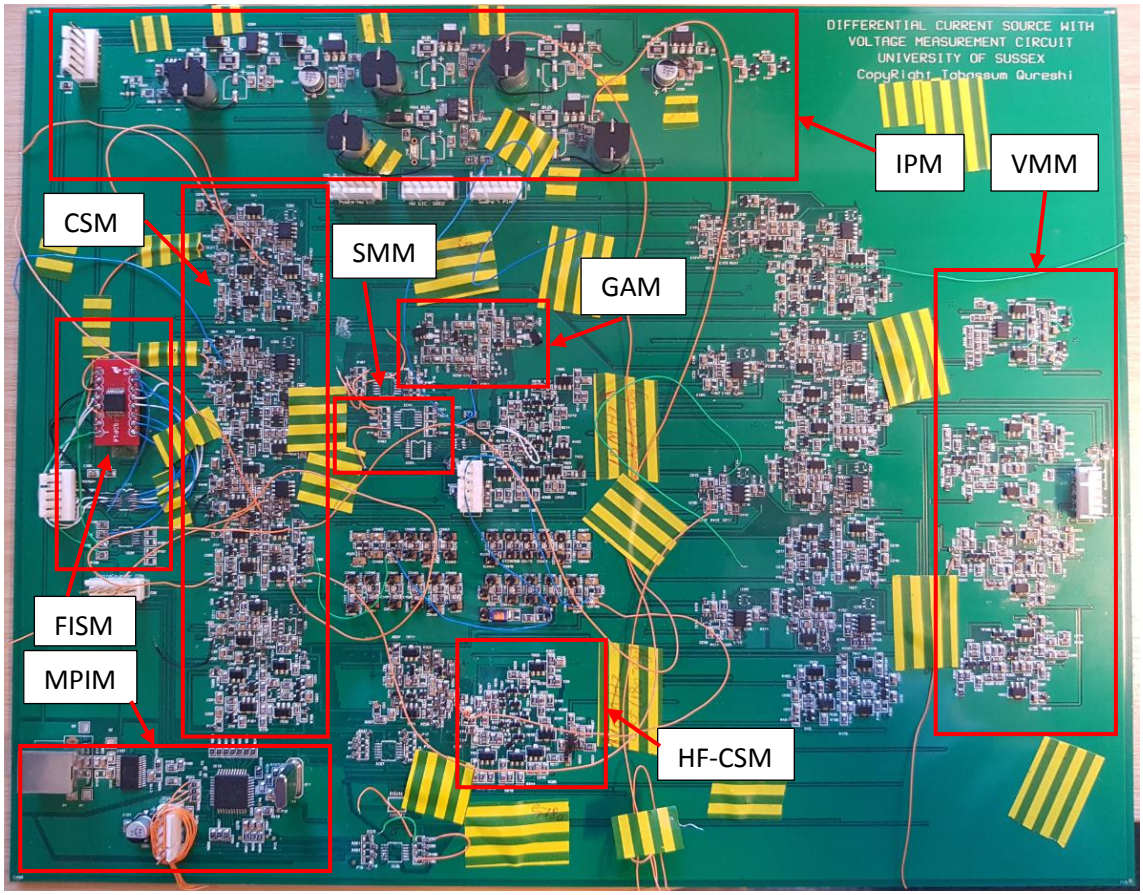



Figure 7.16: The current source PCB

### 7.4.1 Internal Power Module of the CSB

The IPM of the CSB is important circuitry of the PCB. The power supply of every electronic circuitry is noise sensitive. Hence, it is important to precisely achieve the power supply condition for a high performance circuit. This module takes a few external power supplies and generates on-board DC power supply voltages. The on-board power supply generation of the CSB is divided into two levels: 1) <10V DC voltage and 2) ≥10V DC voltage.

Hence, to meet these two level, four external power supplies (±10V and ±40V) were required from an external DC voltage source. The CSB requires ten power supplies: ±40V, ±18V, ±15V, ±5V and ±2.5V. Each on-board power supply unit for different CSB sub-modules are designed separately to avoid power supply perturbation of sub-modules. Most of the modules on CSB are powered from the maximum applied external power supply but there are some modules on the CSB, which require less power supply voltage. The circuit schematics of the IPM is presented in Figure 7.17.

The IPM used three types of voltage regulators (LM317, LM337 and LM7805) to generate the required power supply voltages. The regulator takes variable input voltage and maintains a constant stable output voltage. Eight voltage regulators were used in the CSB to step down the input voltage to the required level.

The LM317 and LM337 devices are 3-terminal adjustable positive/negative voltage regulators with an ability to supply ±1.5A current over an output voltage range of ±1.25V to ±37V respectively. The output voltage level for both regulators is set by two external resistors followed by a simple calculation using Eq. 7.4. The "+" and "-" symbols in Eq. 7.4 are referred to LM317 and LM337 regulator output voltage polarity respectively (Datasheet LM317 & LM337, 2016). Another regulator used in our design is LM78L05, which is also a 3-terminal positive regulator and is available to generate fixed +5V output voltage with a maximum of 100mA output current. An output capacitor is also used with the regulator for frequency compensation and acts as a load balancer by smoothing out any fluctuations that may appear on the regulator output (Datasheet LM78L05, 2013).

The external power supply inputs of the CSB are passed through rectifiers to ensure the DC behaviour of the transmitted signal before its application to any sub-module. A general purpose (GF1G) rectifier was used in each power transmission line featuring high surge current capability and low forward voltage drop. The rectified signal is applied to the voltage regulator via power supply filter capacitors (generally tantalum) that provides necessary bypassing due to the usage of an output capacitor. These capacitors act to smooth out fluctuations in the signal and create a smoother waveform. The resistor combinations for respective output power supply voltages are mentioned in the schematics shown in Figure 7.17. The pin packaging used for the regulators are SOIC-8 and SOT-223.

$$V_{OUT} = \pm 1.25 \left(1 + \frac{R_2}{R_1}\right) \qquad \text{Eq. (7.4)}$$

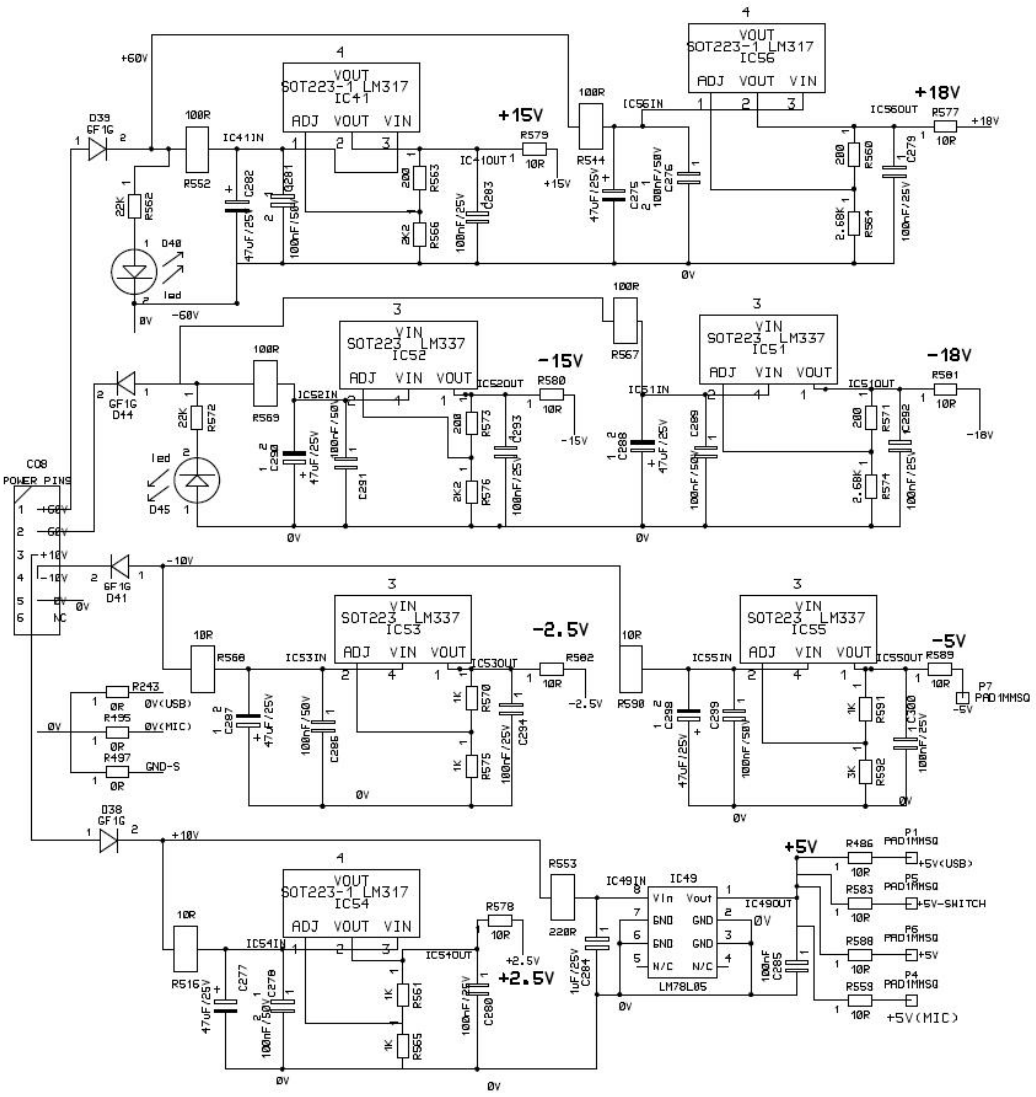



Figure 7.17: Power supply schematics for the CSB

## 7.4.2 Microcontroller & USB Interface of the CSB

To control the signal transmission lines of the CSB from its input to output level, an interface was required. The interface was implemented using a microcontroller with a PC connection. A microcontroller from Microchip (PIC18F4523) was selected for this implementation, which is a 44-pin enhanced flash device having 36 input/output (I/O) pins and 12-bit ADC. These I/O pins are used to control signal routing through the CSB.

The PIC microcontroller requires an internal clock (CLK) module to perform all synchronization between its internal and external modules. The CLK module for the PIC controller was implemented using an AELX005L series external crystal with a 3.69MHz frequency. The CLK crystal was connected with two parallel 22pF capacitors to stabilise the frequency generated by the crystal. The PIC sends a command to the targeted device

via the TX (transmitter) pin in response to the command received on the RX (receiver) pin from the PC via the USB port. This PC to board connection was implemented using an FT232RL IC, which follows a USB to serial UART transmission protocol. The PIC was programmed to perform dedicated tasks for the CSB using a computer program written in the C-language and complied using the MPLAB C18 compiler. The command program was uploaded to the microcontroller using MPLAB IDE v8.92. Different codes for the corresponding task were assigned for signal routing through the CSB and are presented in the appendix F. The schematic for the interface connection devices are presented in Figure 7.18.

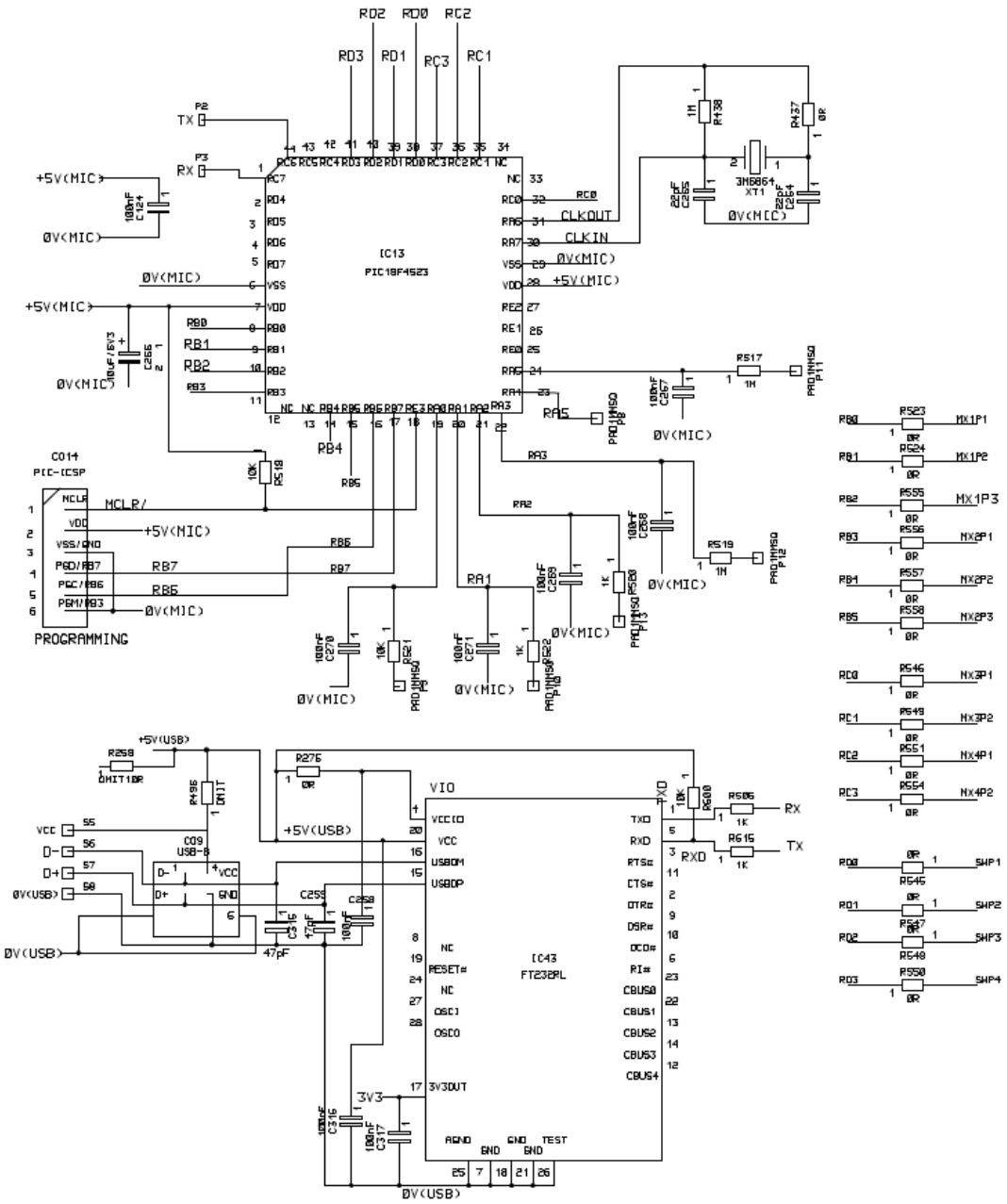



Figure 7.18: Board to PC interface schematic

Interface software was required to communicate with the PIC microcontroller via PC to perform the required tasks. Control software was written in visual basic 6.0 to facilitate this control procedure. The software is required to open a serial port of the PC before starting any communication with the PIC. Once the port is open, the required task can be selected through the interface software and instructions are sent to the PIC in different combinations. The software also provides the updated value of PIC microcontroller internal registers along with the information of the recent transmitted commands. The interface software for the CSB is presented in Figure 7.19.

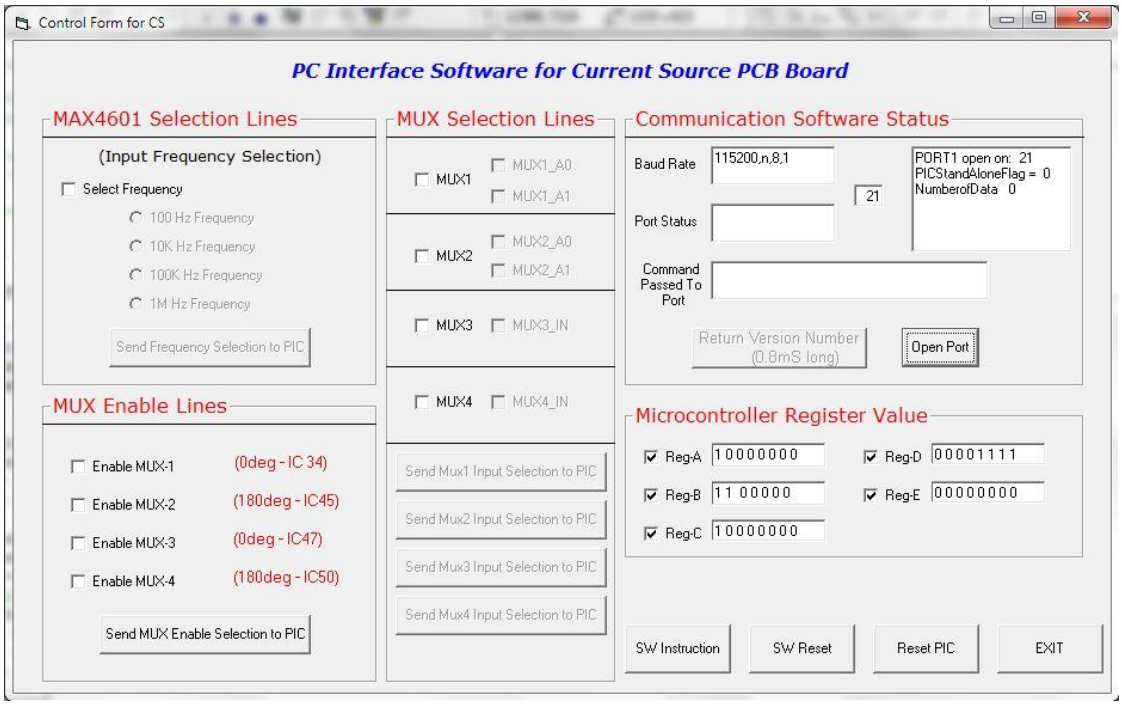



Figure 7.19: Control interface software for CSB

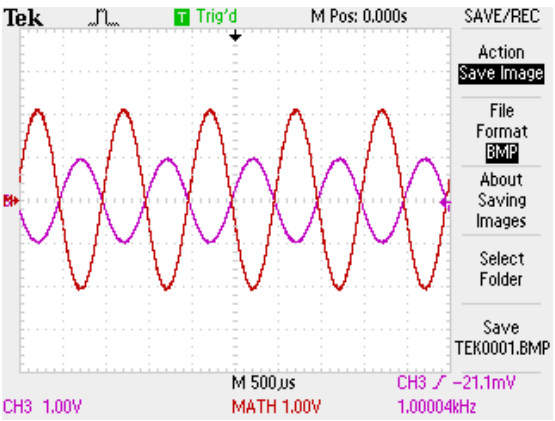
## 7.4.3 Current Source Circuit Performance

To evaluate the performance of the CSM, an experiment was setup in a similar manner to the VSB (FG, DC power supplies, oscilloscope and CSB PCB). The internal power supply module of the CSB is complicated and less external power supply voltage inputs were required to minimise external dependency. The CSM was tested using a power supply voltage of ±36V by cascading two DC power supplies. The input signal was generated using the impedance analyser FG and the output signal was acquired using the same digital oscilloscope. All the measurements were acquired using 10X attenuation

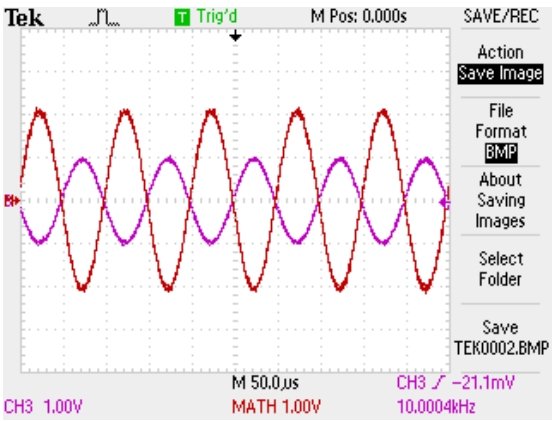
level. The CSM input signals were routed through two level multiplexing to show the performance of the CSM.

The CSM was tested using a load of 2kΩ, 5kΩ and 10kΩ, attached in parallel at the output of the CSM. A sinusoidal signal was generated using a FG with an amplitude of $2V_{p\text{-}p}$ for a frequency range between 1kHz to 3MHz. To understand the performance level achieved by the CSM, a series of tests were conducted for: maximum operational frequency range, output impedance, maximum load amplitude, phase difference between the signals of the circuit.

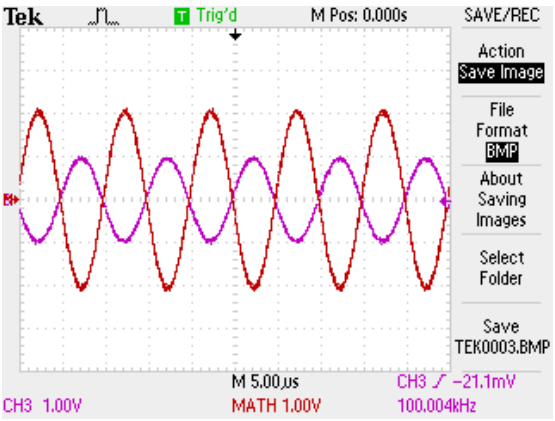
The results presented for the CSM include an additional loading capacitance (≈30pF = 15pF x 2) for two probes to measure the differential signal. The experimental scope results obtained from CSM using a 2kΩ load are presented in Figure 7.20. The results show the amplitude of the output differential signal (red) with respect to the amplitude of the input signal (purple).



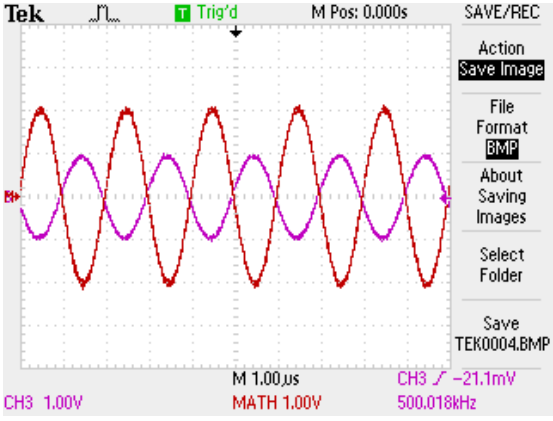

*(a)* Differential load voltage at 1kHz



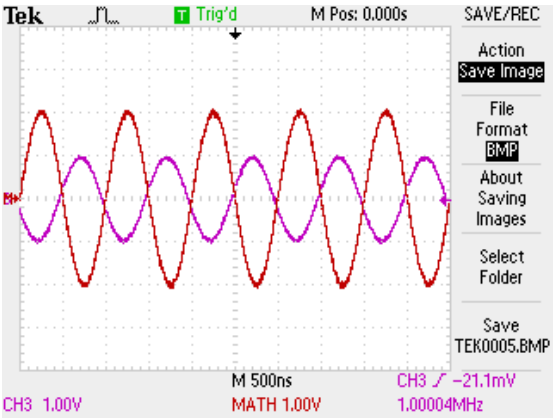

*(b)* Differential load voltage at 10kHz



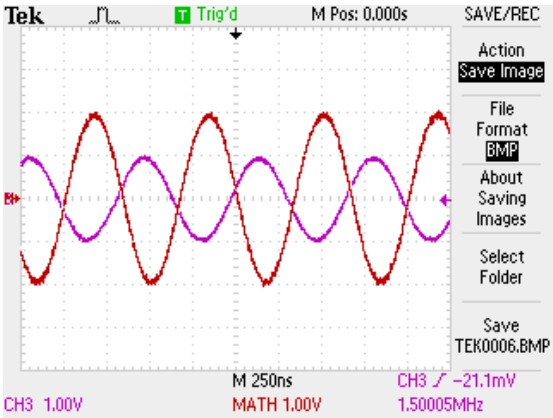

*(c)* Differential load voltage at 100kHz



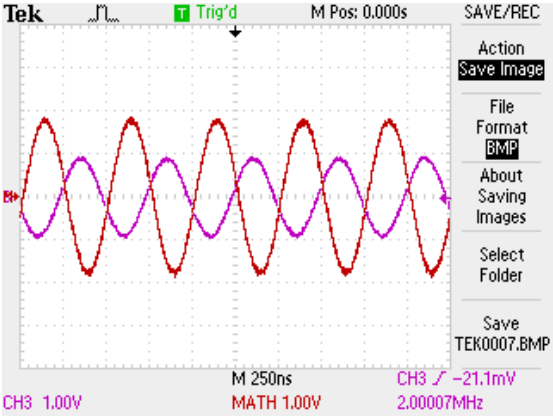

*(d)* Differential load voltage at 500kHz



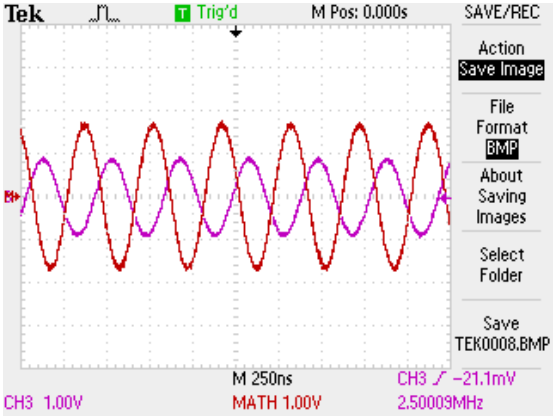

*(e)* Differential load voltage at 1MHz



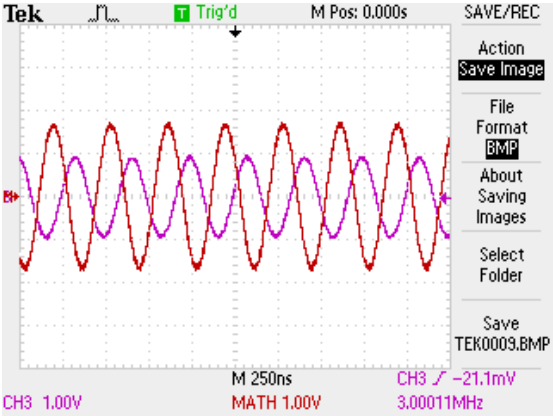

*(f)* Differential load voltage at 1.5MHz




*(g)* Differential load voltage at 2MHz




*(h)* Differential load voltage at 2.5MHz




*(i)* Differential load voltage at 3MHz

Figure 7.20: Differential load voltage using $2V_{p\text{-}p}$ input at different frequencies

The above experimental results show that the CSM circuit has achieved a good performance level by providing the required signal amplitude without any saturation at high frequency (i.e. 3MHz). The voltage amplitude is ≈ $4V_{p\text{-}p}$ up to 2MHz, which shows that CSM is able to deliver 1mA of current up to this frequency. The detailed performance parameters are presented in the next section. The CSM was also tested for other loading combinations mentioned earlier and achieved a similar performance level. These experimental oscilloscope results are presented in appendix G.

### 7.4.3.1 Maximum Operational Frequency and Phase Difference Test

The purpose of this test is to calculate the frequency bandwidth of the CSM while maintaining a constant output voltage that in turn will ensure delivery of a constant current amplitude. The CSM circuit was tested with a gain of 1 and was expected (theoretically) to deliver a constant current amplitude of 1mA (i.e. 2V amplitude for 2kΩ) irrespective of the attached load for the tested frequency band. In this test, the CSM was attached to three different load combinations and the amplitude response of the output voltage was observed. The cut-off frequency point *(-3dB)* of the CSM was observed which gave 70.71% of the initial peak amplitude. In our case it is a voltage amplitude of ≈1.42V (0.7071 x 2V) or ≈707µA (0.7071 x 1mA). The phase difference ($\phi$) was also measured in this test using the same procedure described earlier using Eq. 7.2. The experiment was repeated for multiple measurements at various frequencies using different test load combinations and the frequency bandwidth along with phase shift was observed. The plot for voltage measurements and phase difference, at different frequency levels with its corresponding loading is presented in Figure 7.21.

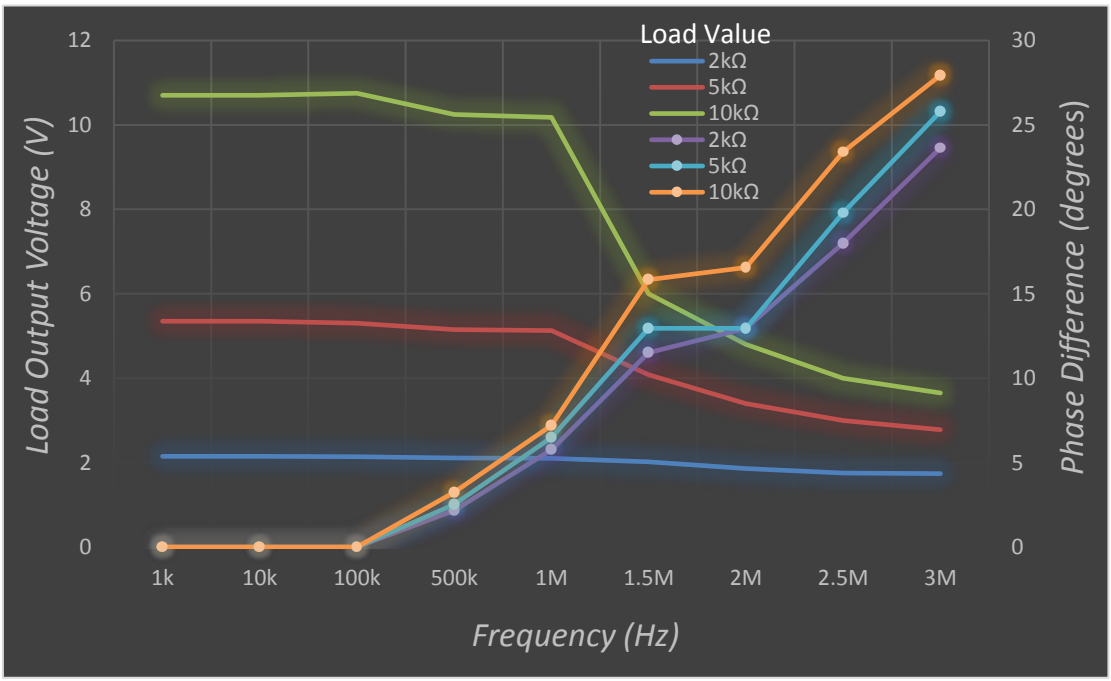



Figure 7.21: Load voltage frequency bandwidth (-3dB) and phase shift for CSM

The experimental results show that the CSM was able to maintain a constant voltage amplitude at low load (≤2kΩ) through-out the tested frequency band. The voltage amplitude dropped after a certain frequency for a load >2kΩ, this result in a reduction of useful operational frequency over the tested frequency band. As the load increases, the

voltage amplitude is still constant but is limited to low frequency operation. This is due to the stray capacitance involved in the system which the capacitance cancellation circuit was not able to minimise due to mismatching of the circuit configuration, or/and characterises of the components used. The experimental results in Figure 7.21, also show that the CSM circuit was able to maintain a phase shift of <30° until 3MHz at a maximum loading of 10kΩ. The phase shift response is steady and increased in the tested frequency range but with an out-of-polarity signal at the output. The experimental results show that the load voltage was leading the input signal at all tested frequencies.

According to the obtained plotted experimental results, it can be interpreted that the CSM circuit has achieved a frequency bandwidth (*-3dB*) of between ≈3-1MHz with a low-to-high loading. Hence it can be considered, to be a useful current excitation source for an impedance measurement device which requires frequencies of ≤3MHz. Based on these results, the performance of the prototype CSM can be further optimised to achieve a further enhanced CSM with precise constant amplitude over a frequency bandwidth of >3MHz.

### *7.4.3.2 Output and Input Impedance Test*

The purpose of this test is to identify the amount of current delivered to the attached load by knowing the voltage dropped across it and solving the voltage-to-resistance ratio for current measurement. The output impedance of the CS can be realised as its parallel combination with the load at the output node. In this test, the output impedance of the CSM is determined by the measurement of loading voltage on two different loads represented as $V_1$ and $V_2$ with respect to tested $R_1$ and $R_2$ loads. Hence, mathematically the relationship between the output current and output impedance can be interpreted as shown in Eq. 7.5 and its solution for the output impedance ($Z_o$) in Eq. 7.6.

$$I = \frac{V_1}{(Z_o \parallel R_1)} = \frac{V_2}{(Z_o \parallel R_2)} \qquad \text{Eq. (7.5)}$$

$$Z_o = \frac{R_1 R_2 (V_1 - V_2)}{R_1 V_2 - R_2 V_1} \qquad \text{Eq. (7.6)}$$

In this test, the circuit was attached with 5kΩ and 10kΩ load in the presence of parallel ≈30pF loading capacitance (probes) and the loading voltage amplitude was observed using a digital oscilloscope at different frequencies. A high output impedance is required

for a good performance of the CS that ensures the maximum amount of current is delivered to the attached load.

The input impedance of the CSM unit was also determined at different tested loads and frequency range. It was observed during the experiment that the amplitude of the input was dropped when the power supply was applied to the CSM. Hence, it is useful to know the input impedance of the circuit. The input impedance of the circuit was determined by measuring the input voltage signal amplitude before connecting the power supply to the circuit, followed by the input amplitude measurement with the power supply connected. The input impedance is determined by the ratio of voltage amplitude difference and input current generator by the FG. The plots for the output and input impedance of the CSM at different frequency levels with its corresponding loading are presented in Figure 7.22.

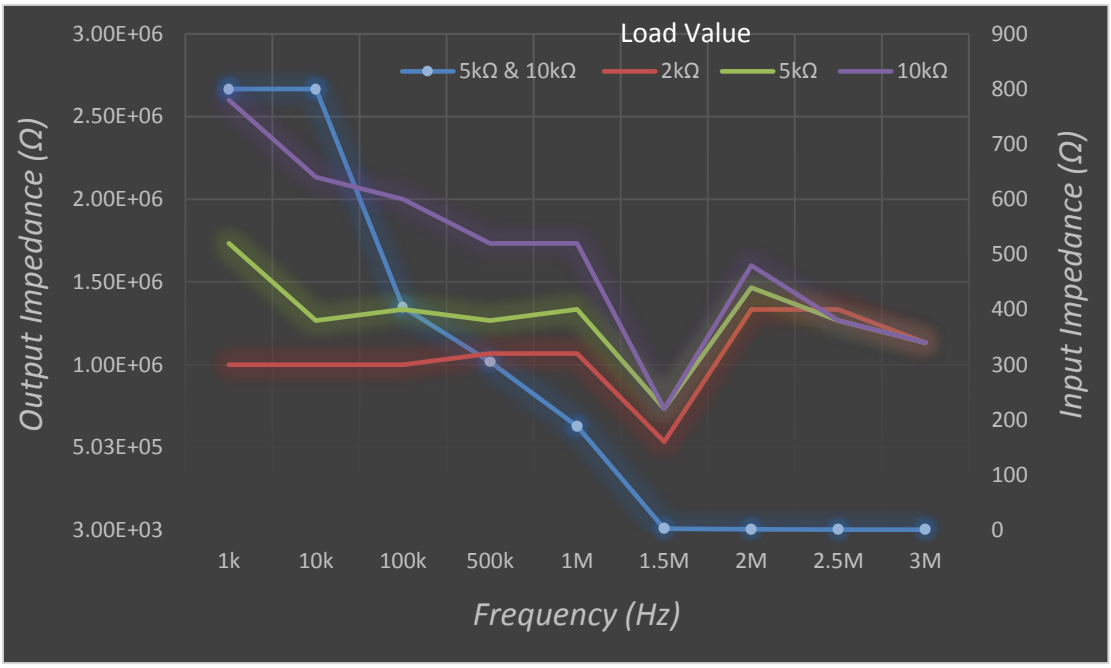



Figure 7.22: Output & Input Impedance of the CSM at respective tested frequency

The experimental results in Figure 7.22 show that the CSM hasn't achieved as high an output impedance as predicted by the simulation results. The CSM is able to achieve an output impedance of ≈2.7-1.2MΩ, for frequencies up to 500kHz. The circuit is not able to maintain the output impedance, which drops to ≈631kΩ to 5kΩ for the frequency range of 1MHz to 3MHz respectively. This is possibly due to: the bandwidth of the op-amp used, which has reached its limit, and the stray capacitance of the PCB has affected the performance of the circuit limiting it to <1MHz.

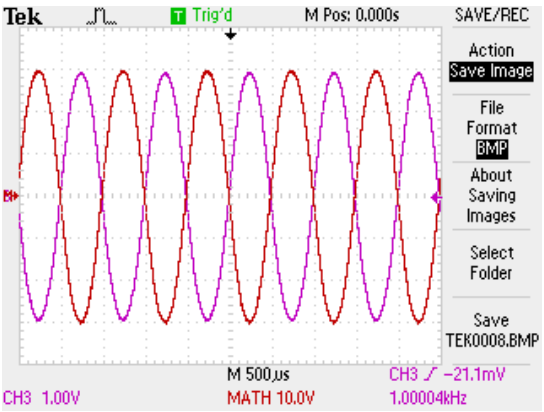
The input impedance of the CSM increased, as the loading and frequency increases. It shows an almost steady response up to 1MHz and drops to a low value at 1.5MHz followed by a rise and gradual fall up to 3MHz. It has possibly affected the output impedance of the circuit that resulted in a low voltage amplitude dropped across the load.

Based on these results, it gives an opportunity to further research the performance of the CS circuit to achieve a high output impedance and reduce the input impedance of the circuit that can result in a high frequency bandwidth excitation source based on current injection. These parameters are still a research topic, especially at high frequency for an impedance measurement device.

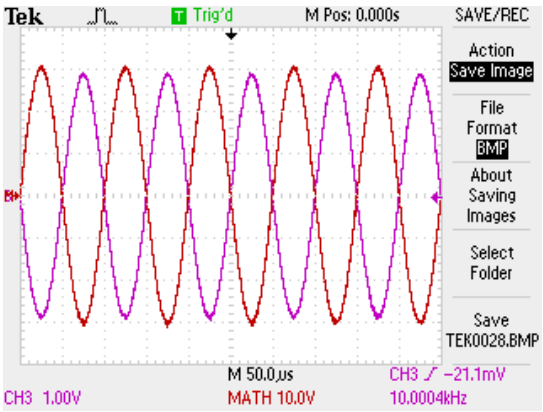
### *7.4.3.3 Maximum Loading Test*

The purpose of this test is to identify the maximum loading that can be attached to the CSM without any saturated output signal at a certain power supply voltage. The amplitude of loading voltage depends on the gain of the circuit, which is one and is constant for all the tested loads. To evaluate this test at a certain power supply voltage, the input signal amplitude was gradually increased and the loading voltage was observed to check its saturation point.

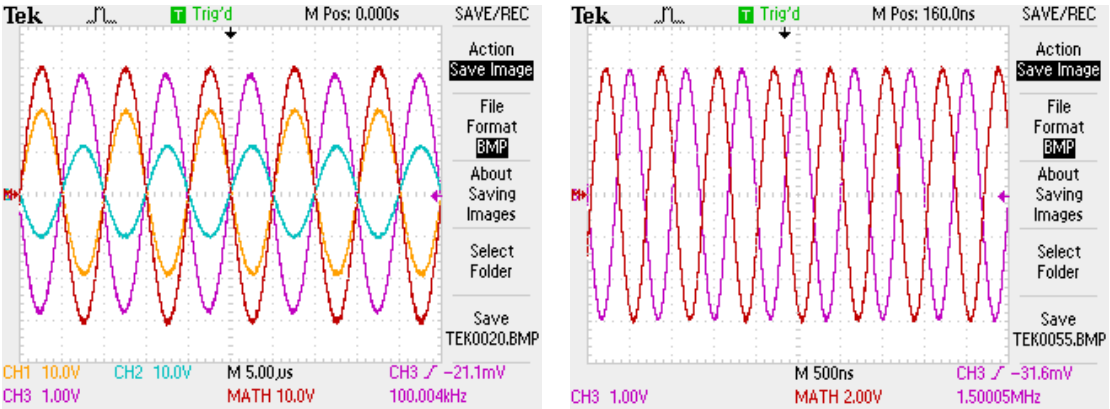
The CSM was initially tested using the ±36V power supply rails with 2kΩ, 5kΩ and 10kΩ loading with a parallel loading capacitance of ≈ 30pF (probes). The maximum achievable amplitude of output signal was measured at randomly selected frequencies and some are presented in Figure 7.23 (differential output signal amplitude: red and the input signal amplitude: purple).




*(a)* 30V loading amplitude at 1kHz using 10kΩ load




*(b)* 30V loading amplitude at 10kHz using 10kΩ load




*(c)* 30V loading amplitude at 100kHz using 10kΩ load

*(d)* 6V loading amplitude at 1.5MHz using 2kΩ load

Figure 7.23: Maximum loading at different tested frequencies

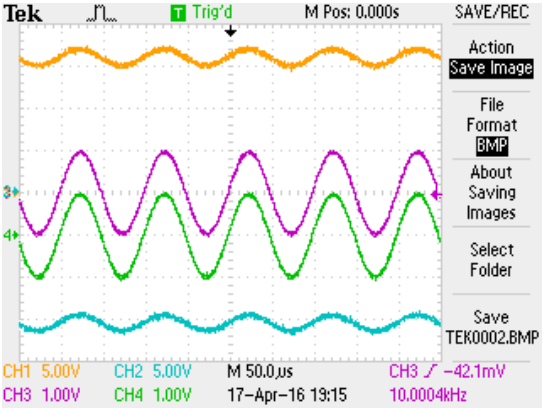
The experimental result showed that using an input amplitude of 3V for a 2kΩ load, the CSM was able to achieve a loading voltage amplitude of 6V at 1kHz, 10kHz, 100kHz, 500kHz, 1MHz and 1.5MHz frequencies followed by amplitude reduction above this frequency. Under the same circuit conditions, the CSM was able to achieve 15V and 20V loading amplitude at 1kHz, 10kHz and 100kHz frequency using 5kΩ (3V input amplitude) and 10kΩ (2V input amplitude) respectively. The loading voltage saturates with an input amplitude of 3V at 10kΩ loading. Hence, the power supply rail voltages were increased to utilise the bootstrapping benefit. The power supply was increased to ±45V and the CSM was able to achieve a loading voltage amplitude of 30V over the tested frequency range. These experiment results show that the CSM was capable to handle a load up to 10kΩ demonstrating the effectiveness of the bootstrapping technique.

### 7.4.4 Guard Amplifier Circuit Performance

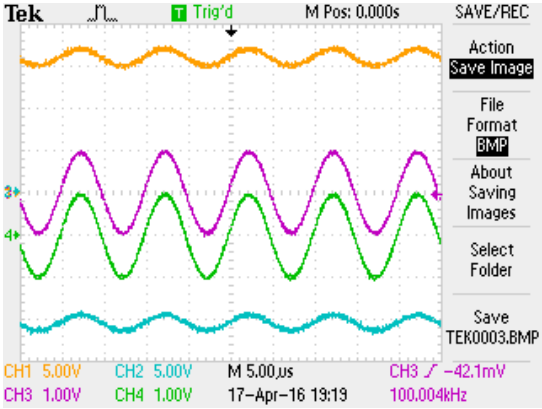
This circuit is referred to as GAM on the CSB. The performance of GAM was tested in two steps: GAM individual testing followed by its application to the respective MUX's to see its capacitance cancellation/minimisation affect.

Like other CSB modules, the GAM can also be configured for standalone prototype testing. To evaluate its performance, a similar experimental setup was established with available laboratory equipment. The GAM was tested using a ±36V DC power supplies. A sinusoidal signal of $2V_{p\text{-}p}$ was generated using a FG for the frequencies range between 1kHz to 3MHz. To understand the GAM performance level, its three output voltages ($V_{dd\text{-}GAM}$, $V_{ss\text{-}GAM}$ & $V_{gnd\text{-}GAM}$) were measured for the tested frequency range. For a better GAM performance, $V_{dd\text{-}GAM}$ & $V_{ss\text{-}GAM}$ should swing to half of the DC power supply on positive

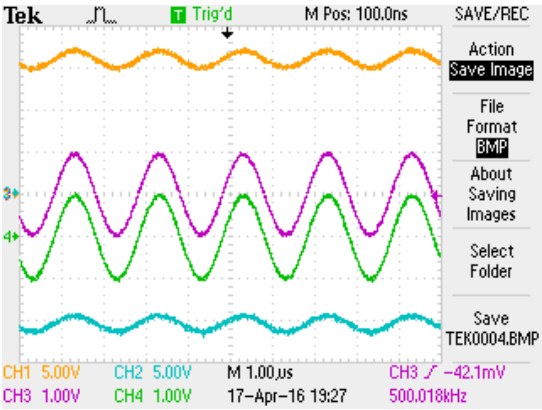
& negative peak respectively with an amplitude equal to its input signal. The $V_{gnd\text{-}GAM}$ signal should follow the input signal nearly with the same amplitude. The experimental scope results obtained using GAM without any loading along with probes (10X attenuation) capacitance are presented in Figure 7.24. The results show that the amplitude of the generated output voltages by GAM (yellow, green, blue) with respect to the amplitude of input signal (purple).



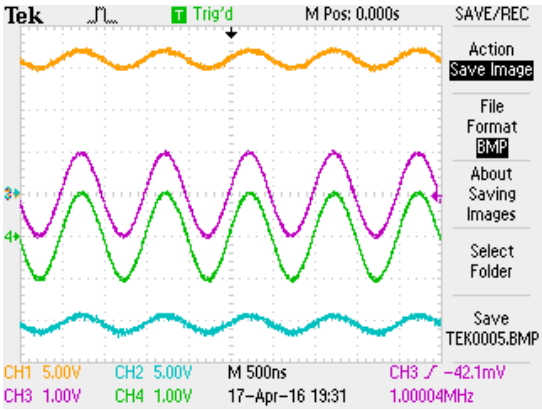

*(a)* GAM output voltages at 10kHz



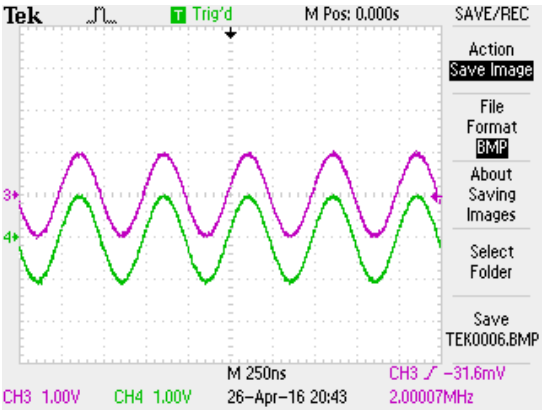

*(b)* GAM output voltages at 100kHz



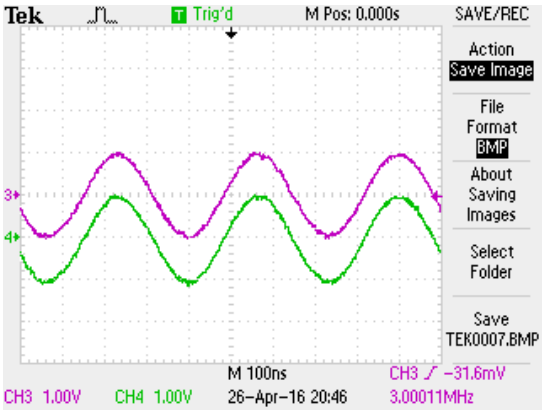

*(c)* GAM output voltages at 500kHz




*(d)* GAM output voltages at 1MHz




*(e)* GAM output voltage at 2MHz




*(f)* GAM output voltage at 3MHz

Figure 7.24: GAM output voltages at different tested frequencies

The experimental results of the GAM show that the circuit was able to achieve a power supply voltage shift of ≈16V towards the positive and negative peak for a 1V amplitude. The signal was shifted one division down to demonstrate a clear follow up of $V_{gnd\text{-}GAM}$ with respect to the input signal. The GAM achieved a good performance up to a 3MHz frequency.

In next phase, the GAM circuit performance was evaluated by driving the power rail of the MUX's used in the CSB. The GAM takes the load voltage as an input and generates three corresponding output voltages. These three generated GAM voltages were applied to the power supply pins of both the MUX's (level 1 & 2). This testing was evaluated in 3 steps: 1) the CSM was directly connected to the load and the resulting load voltage amplitude was measured, 2) the CSM output was routed to the load via two MUX's and the resulting load voltage amplitude was measured, 3) the GAM output voltages were used to drive the MUX's along with the circuit configuration in step 2 followed by the measurement of loading voltage.

These circuit setups were tested using ±36V DC power supplies, a $2V_{p\text{-}p}$ input signal in the frequencies range between 1kHz to 3MHz and a 2kΩ load. The experiment was repeated to measure the loading voltage for the three steps described above. The experimental oscilloscope result for this test is presented in the appendix H. The experimental results for this test are plotted at different tested frequencies against their voltage amplitudes in Figure 7.25.

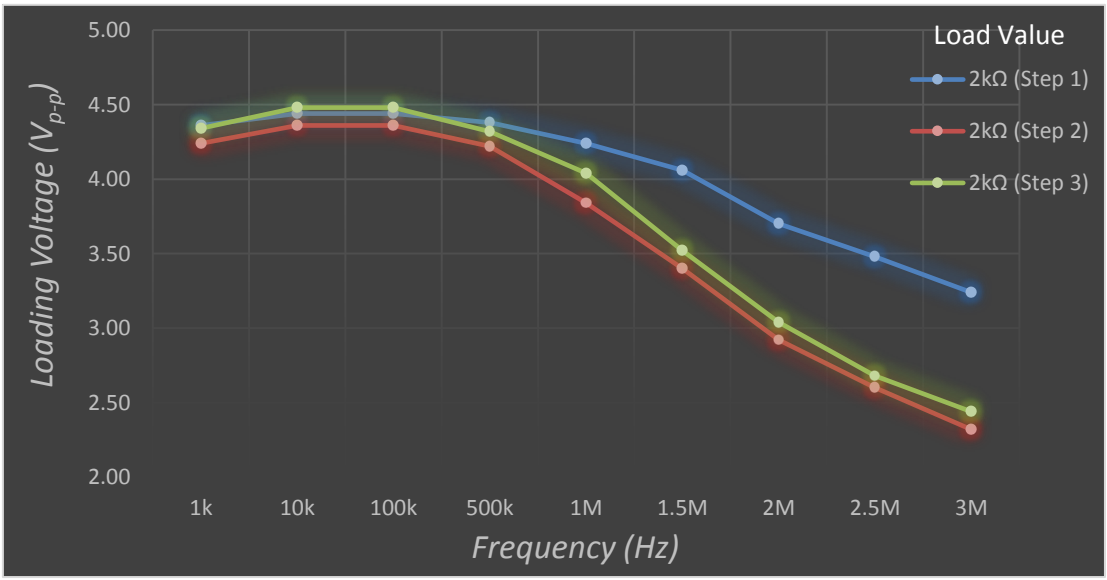



Figure 7.25: Load voltage using CSM and GAM at tested frequency band with 2kΩ loading

The experiments show that the GAM was able to minimise the capacitance effect of the MUX to some extent and has slightly increased the amplitude of the voltage dropped across the load. It can be noticed that up to 500kHz, the capacitance is effectively minimised and the amplitude of the load voltage is approximately equal to the amplitude as connected directly to the load. Although the GAM has helped in minimising the capacitance effect for frequencies >1MHz the improvement is not that significant. Based on these experimental results it can be determined that the GAM has a potential to minimise the unwanted capacitance effect and provides an opportunity for further circuit improvement to achieve optimum results for frequencies >1MHz.

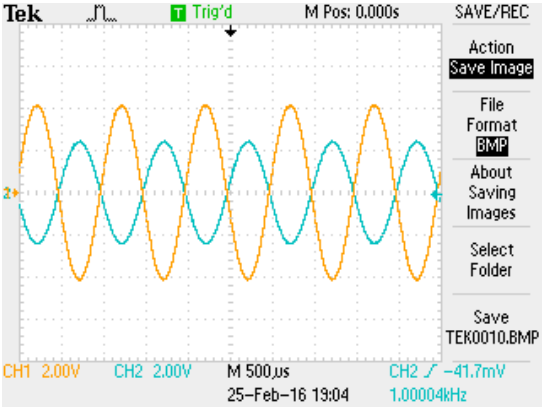
### 7.4.5 Differential Amplifier Circuit Performance

This circuit is referred as VMM on the CSB. The performance of the VMM circuitry based on the op-amp was only evaluated in this test. The VMM circuitry based on discrete components are similar to the one used in VSB and its performance has already been presented in section 7.3.2. This VMM can also be configured for standalone testing. The testing of this VMM was evaluated in two steps: 1) VMM was individually tested, 2) VMM was applied to the CSM and the resulting load voltage was observed.

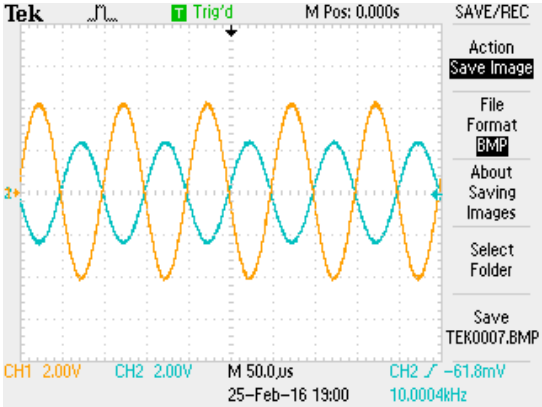
To evaluate its performance, an experimental setup was established with available laboratory equipment. Initially the VMM was tested using ±36V DC power supplies, sinusoidal signal of amplitude 2V, 5V and 10V for frequencies: 100kHz, 1MHz, 5MHz and 10MHz. The experiment was repeated for the noted amplitudes and frequencies and results were observed to establish a relationship for maximum achievable amplitude at the respective frequency. The experimental results showed that the VMM was able to measure a 10V amplitude up to 1MHz. At 5MHz, the maximum achievable amplitude was reduced and limited to 5V. At 10MHz, the VMM was not able to deliver any significant performance and hence limited the operational frequency of VMM based on the selected op-amp to ≤5MHz.

In the next testing level, the loading voltage measurement was taken at the VMM output by its integration with the CSM circuit. To evaluate this circuit setup performance, an experimental setup was established for a sinusoidal signal of amplitude 1V, 2V and 3V for frequencies: 1kHz, 10kHz, 100kHz, 500kHz, 1MHz and 2MHz. The experiment was repeated with these amplitudes & frequencies and results were observed to measure the loading voltage at the respective frequency. The experimental scope results obtained from

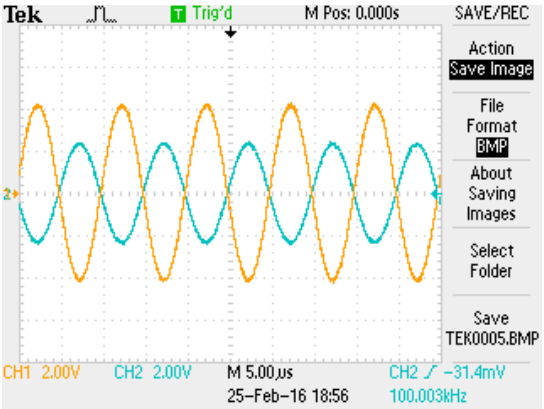
VMM using a 2V input amplitude at 2kΩ loading are presented in Figure 7.26. The results present the loading voltage amplitude measured by VMM (yellow) with respect to the amplitude of input signal (blue).



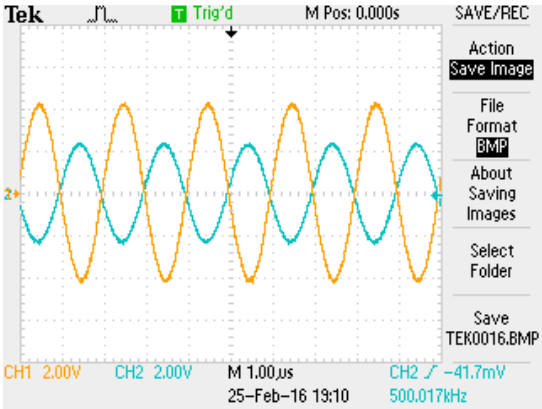

*(a)* VMM Load voltage at 1kHz



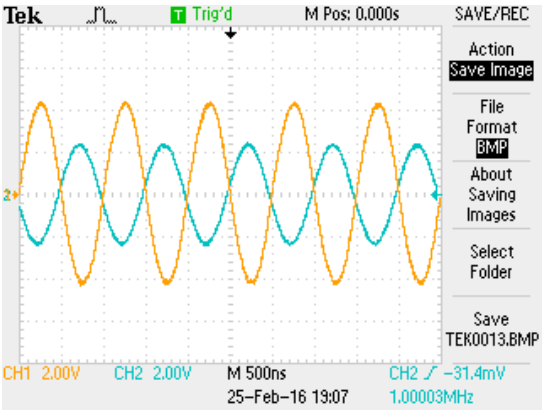

*(b)* VMM Load voltage at 10kHz



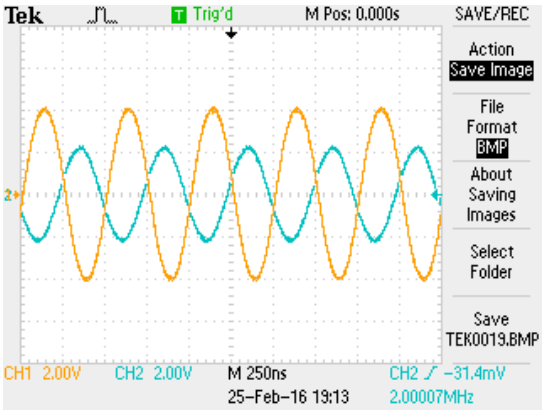

*(c)* VMM Load voltage at 100kHz




*(d)* VMM Load voltage at 500kHz




*(e)* VMM Load voltage at 1MHz




*(f)* VMM Load voltage at 2MHz

Figure 7.26: VMM Load voltages measured at different tested frequencies

The experimental results show that the VMM based on the op-amp (AD812) was able to achieve a frequency bandwidth of 2MHz with the required amplitude measurement for 2kΩ loading. The experimental results observed for other tested input amplitudes are plotted in Figure 7.27. The plotted experimental results show that the VMM circuit was

able to measure a constant voltage signal amplitude up to 2MHz for input amplitude ≤3V. Above a 2MHz frequency, the VMM was not able to measure the required output amplitude and was reduced to low amplitude. Hence, it shows that the frequency bandwidth of the VMM was reduced, possibility due to: the operational frequency limit of the op amp, stray capacitance of the PCB or slight mismatching of the analogue component characteristics. The conclusion is that this VMM circuit is useful for frequencies ≤2MHz. The phase difference was also observed and was small for the whole range of tested frequencies with an out-of-polarity signal.

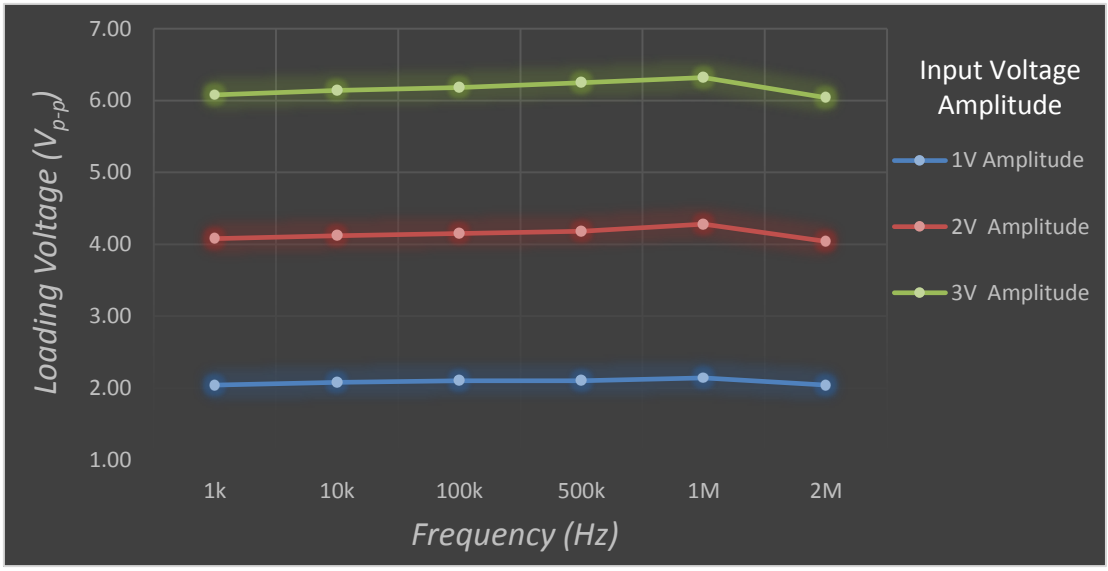



Figure 7.27: Load Voltage using CSM and VMM at respective tested frequency with 2kΩ loading against variable input amplitude

## 7.5 Summary

This chapter was based on the PCB implementation of the excitation source based on current/voltage application. The chapter provides a brief overview of the PCB terminologies and its construction mechanism. The chapter presented the block diagram of the current and voltage source PCB that showed main modules of the both PCBs along with working dependencies, a description of each module, and both PCBs performance based on their submodules.

The chapter initially presented the VSB performance along with its PCB configuration. It described the type of components used on the PCB with their electrical characteristics. The VSB routing pattern, track sizes and decoupling/capacitive coupling were presented. The VSB practical performance was determined by evaluating VSM and VMM

performance independently. The performance parameters of maximum operational frequency, output impedance, phase difference, maximum achievable loading amplitude and SNR for VSM were presented. The VSM achieved a frequency bandwidth of ≈ 13MHz, an output impedance and phase shift of <350Ω and <112° respectively for frequencies ≤12MHz. The VSM reported a SNR of 41-38dB. The chapter also presented the performance of the VMM based on a discrete DA and reported a frequency bandwidth of 10MHz for an input signal amplitude of 3.5V. It also reported that the circuit was able to measure ≈6V amplitude over a reduced frequency bandwidth (i.e. ≈5-6MHz).

The chapter also presented the CSB performance along with its PCB arrangement. The characteristics and functionality of the IC's used in the respective CSB modules were briefly described. The on-board power supply system, switching control module and interface software for the CSB were presented. The practical performance of the CSB was determined by evaluating the performance of the CSM, GAM and VMM separately as well as with their integration. The CSM was able to achieve a frequency bandwidth of ≤3MHz with a phase shift of <30°. The output impedance of the CSM was not found to be extremely high as obtained in simulation results. It reported a maximum output impedance of ≈3MHz for <500 kHz frequency. An independent performance of the GAM until 3MHz was presented. A circuit setup was presented to minimise the capacitance effect and was reported to be effectively minimised for frequencies ≤500kHz. The capacitance minimisation was also reported for >1MHz but its effect was not significant. An op-amp based VMM was also tested. The performance of the VMM was presented and reported a signal measurement up to ≤3V amplitude for frequencies ≤2MHz. The experimental results for the prototype HF-CSM didn't produce any significant outcome due to oscillation at high frequency (10MHz). Hence, an improvement is needed for this module that leads to an opportunity for future research work.

Chapter 8 will present the conclusion of the research work along with its findings and limitations. The chapter will also address the areas for further optimization of the excitation system and improvement opportunities via further research work.

# Chapter 8

# Conclusions and Future Work

Electrical impedance measurement using tomographic imaging can produce the internal impedance distribution of the biological tissue and lesions within the body. This technique is non-invasive and non-destructive that has broad application in the clinical area. In this thesis, an in-depth study of this technique has been investigated with a focus on developing improved hardware for the Sussex EIM system. This chapter gives the discussion on the research work covered in this thesis along with a conclusion based on the attained experimental results. It also present areas of research, which includes further optimization for its future implementation.

## 8.1 Thesis Review

The thesis started with a literature review that will help to understand cancer terminologies for a non-technical person. Cancer types, staging and grading system were briefly presented for general understanding. The main scope of this research work was based on breast cancer, hence it also presented the literature for breast cancer, its different types and details of cancer stages. Breast cancer has significantly attracted attention in western world due to its high mortality rate, but in developing countries people don't have much awareness about its terminologies and symptoms. Therefore, the section intention is to educate the reader about cancer (especially breast cancer) and its symptoms. It presents the diagnosis methods for cancer detection with a precise focus on the imaging based diagnosis tools along with its advantages and limitations. The imaging technique based on impedance distribution was investigated in depth in the thesis and is generally referred as Electrical Impedance Tomography or Electrical Impedance Mammography for breast cancer diagnosis.

A detailed literature and methodology for a bio-impedance measurement is discussed along with its tissue/cell impedance interpretation using the Cole-Cole model. Two bio-

impedance measurement protocols are presented describing its benefits and limitations along with its extension to the EIT technique for medical application. The EIT imaging technique is introduced along with its potential application in different areas and its brief history for medical application. The theory and mathematical model for the EIT method is discussed. The primary focus of this research work is on the hardware modules involved in the EIT system. Hence, the hardware components are discussed in detail along with a brief description of the EIT image reconstruction algorithms. The advantages and limitations for the imaging technique is presented along with the areas for possible improvement. The precise focus of this research work is based on the improvement of the excitation power source for the EIM system at Sussex. Hence, techniques are proposed for the performance improvement of the present excitation source of the Sussex EIM system.

The hardware modules of the EIT system are primarily investigated in this research work. The EIT system signal measurement protocols are discussed. These protocols describe the pattern of excitation signal application and its resulting signal measurements. Irrespective of the system measurement pattern, the EIT system should maintain health and safety standards and satisfy the electrical safety limit. The excitation signal safety limits are introduced along with benefits and limitations of excitation source based on either the current or voltage source. The pros and cons of multi-frequency EIT measurements are also discussed. The precise focus of the research work is limited to the excitation power source development, therefore a literature review of prominent existing EIT systems is presented and they are categorized by their type of excitation signal generator. The respective EIT systems are presented along with their system architecture and performance parameters. The performance parameter of: operating frequency range, number of electrodes and system SNR are presented as reported by their authors. The Sussex EIM system is presented along with its development history. The detailed Sussex EIM system architecture is presented, the description includes the information from its mechanical assembly to its electronic data acquisition module. The existing operating frequency range for the EIM system is presented along with the proposed system specification. The most unique part of the Sussex EIM system is its hexagonal planar electrode arrangement along with hexagonal voltage acquisition measurement. The image reconstruction method of this EIM system is based on voltage differences and uses the logarithm of the voltage ratios to reconstruct the conductivity. The frequency bandwidth

of the excitation system for the latest Sussex EIM system is presented along with the limitation factor involved in system frequency performance degradation.

The improvement of the power excitation source for the Sussex EIM system is investigated. The previous excitation source of the EIM system is a voltage-to-current convertor/voltage controlled current source (VCCS) named as the Enhanced Howland current source (EHCS). Two VCCS circuits are investigated for an improvement of the excitation source. The detailed circuit analysis of the EHCS and GIC circuit are presented followed by the simulated performance of both VCCS circuits for variable resistive and capacitive loading. The performance parameters of: maximum operational frequency range and the output impedance of both VCCS circuit are established and presented along with its limitations.

The two VCCS circuits are further investigated to overcome the limitation achieved. A bootstrapping technique is presented along with simulation demonstration to establish a high amplitude output signal performance. Both VCCS circuits are bootstrapped to achieve a high amplitude voltage that resulted in a solution to the loading voltage problem. Another technique of Guard amplifier is presented to cancel/minimise the additional capacitance introduced by the multiplexing devices. The performance of this technique is demonstrated by simulation and presents its maximum operating frequency with respect to its loading. A bipolar VCCS circuit is also presented with a simulation demonstration to establish a set of performance parameters. The frequency bandwidth and the output impedance of the bipolar VCCS is presented. The VCCS circuit shows an inability for a good performance at a high frequency. Hence, a discrete component current source (DCCS) using high frequency and voltage transistors, is presented to demonstrate a high frequency excitation signal generator. The performance of the DCCS is demonstrated using simulation and the performance parameters are established to show it’s achieved frequency bandwidth, output impedance and phase difference.

Another type of excitation source referred as voltage controlled voltage source (VCVS), is also investigated in the thesis. The voltage source investigation is done to overcome the limitations that occurred using the current injection excitation source. Three VCVS architectures are presented and based on the initial frequency response, the one that demonstrates the better frequency response is selected for a detailed investigation and design. The presented voltage source has an ability to generate a variable gain with a

controllable feedback current. A bootstrapped voltage source design is presented to avoid the loading effect for high amplitude output signals. The circuit analysis of the voltage source is presented to model the amount of current generated/injected by the source to the attached load. The performance of the VCVS is demonstrated by simulation while presenting its maximum operating frequency and low output impedance at different loading. A bipolar VCVS circuit is also presented with a simulation demonstration to establish a set of performance parameters. The presented performance parameters are: frequency bandwidth, output impedance, phase difference and SNR.

Analogue circuitry is presented for a differential voltage measurement. Two analogue circuits are presented to measure differential voltages. A bootstrapped differential amplifier (DA) circuit is presented to measure a high amplitude voltage signal. The performance of the DA is demonstrated by simulation and performance parameters are reported along with its limitations. A discrete component DA (DCDA) device is also presented to overcome the limitation that occurred in the op-amp based DA. The performance of the DCDA is demonstrated with a high amplitude measurement at high frequency and has resolved the limitations of the simple DA. The performance of the DA is also presented with its application to the bipolar VCVS circuitry and differential measurements are acquired.

The PCB implementation of both excitation sources are presented in this thesis. The PCBs architecture are represented by their block diagram to provide information about the PCB's implemented modules and their interconnection with other modules. Both excitation sources are implemented on a separate PCB and their practical performance is evaluated independently. The voltage source module is practically tested and the performance parameters data set are evaluated and demonstrated for: maximum operational frequency, output impedance, maximum achievable amplitude, phase difference and SNR. The DA designed using discrete components, is practically tested for signal amplitude measurement of the voltage source. Its performance is evaluated in terms of maximum measured amplitude and achieved operating frequency. The PCB performance of the current source is also presented along with its supporting modules. The practical test presented the measured data sets for maximum operating frequency, its output impedance, phase difference and maximum loading of the current source. Other modules of the current source PCB are also practically tested and their performance parameters are established and presented. The DA measurements on the current source

PCB are acquired using an op-amp based DA. The performance of the guard amplifier circuitry is also presented which demonstrates the principle to minimise the capacitance introduced by the multiplexers.

## 8.2 Thesis Conclusion

The achievement of the thesis includes following:

1. A comparison of two current excitation source circuits: The Enhanced Howland Current Source (EHCS) and the EHCS-GIC (Generalized Impedance Converter) has been presented.
2. The introduction of a bootstrapping technique for the excitation source circuit. This technique can improve the loading voltage problem of the circuit by providing a high amplitude signal according to the supplied power rails.
3. A performance comparison of bootstrapped current excitation source circuits: The EHCS and the EHCS-GIC.
4. A design for a bipolar bootstrapped current excitation source with a signal transmission via multiplexers.
5. The introduction of a Guard amplifier design to cancel/minimise the capacitance introduced by multiplexers. This is an alternative approach investigated in addition to the GIC circuit.
6. A design for a high frequency current source excitation source based on discrete components (i.e. high speed and high voltage transistor).
7. A voltage application excitation source circuit with the ability to provide variable gain and controllable feedback current. Bootstrapped technique is integrated with the voltage source for a high amplitude signal generator.
8. A design and comparison of a differential amplifier (DA) circuits: op-amp and discrete components based DA. Bootstrapping is integrated with DA to measure high amplitude signals according to the supplied power rails.
9. A design of on-board power supply circuitry for a current source excitation PCB. This circuitry helps to minimise the external power supply connections by internally generating the required DC voltages.
10. An interface designed to control the signal multiplexing for current source excitation PCB. This is implemented using interface software on a PC that communicates with the PCB by a microcontroller via USB serial port.

11. Both types of power excitation sources have achieved substantial frequency bandwidth performance. The voltage application excitation source has achieved a frequency bandwidth of ≤13MHz, while the current injection excitation source has achieved an overall frequency bandwidth of ≤3MHz, tuned for different frequency range configurations. The differential amplifier based on op-amp has achieved a frequency bandwidth of ≤2MHz. The DA based on discrete components has achieved a bandwidth of ≤10MHz and showed a reduced bandwidth (≈6MHz) at high input amplitude.

The above mentioned research work is evaluated by its implementation on two separate PCB boards named as: Current source (CS) and voltage source (VS) board. Both PCBs have different modules that have different testing requirements. The CS board has a complex architecture due to its greater number of modules as compared to the VS board. Hence, the on-board power supply circuitry is implemented on the CS board. The on-board power supply module is a high performance module having least effect on nearby analogue circuitry. The designed on-board module has the ability to generate a precise DC output voltage determined by the ratio of the two feedback resistors that form a potential divider across its output terminal according to our project requirement. Ten DC power supply voltages are required by the CS board that is generated from two external DC voltage source (±10V and ±40V). The individual testing of power supply modules showed that it can generate the required DC voltage level with ±1% accuracy. A slight mismatching of on-board feedback resistors due to its tolerance causes the accuracy difference. The on-board power circuitry for the EIT system has an advantage of minimum noise and is more convenient as compared to external power supply systems. The power isolation is also considered and designed for user safety.

A single sinusoidal input (external) generated from a function generator is used for testing the excitation source. The differential source testing requires two out-of-phase (180°) signals applied simultaneously to the tested load. Hence, to keep the external input dependency at a minimum level, an on-board inverted signal is generated using an inverting op-amp configuration with a gain of one. The inverting op-amp configuration is precisely designed to ensure that the amplitude of the inverted signal is equal to the signal generated by the FG.

The EIT system requires multiple measurements using multiple channels. A dedicated excitation source for a single channel will result in a complex and costly instrument. Therefore, most of the systems prefer multiplexing of a single excitation source with a multiple electrode interface. Although it will reduce the complexity and cost of the instrument but alternatively the instrument will suffer from the capacitance introduced by the multiplexer. A multiplexed single excitation source with proper calibration has a tendency to achieve stable results as compared to a multiple excitation source system. In our designed prototype PCBs, a single channel CS board has been implemented which involves cascading multiplexing between low and high frequency current source circuits to ensure minimum capacitance. The CS circuit is implemented for set of different frequency ranges hence its multiplexing is needed to route the respective signal to corresponding load/electrode. In the case of the VS board, the single channel voltage source circuit is implemented and doesn't require any multiplexing in its prototype testing over different frequency ranges. The research work has investigated the ways to minimise the capacitance and has reported its performance results.

Two circuit configurations for VCCS are investigated as a current source. Both VCCS circuits are sensitive in resistor matching. High the tolerance on resistors will result in resistor matching difficulties, hence a ±1% tolerance resistors are used for implementation. First, the EHCS was tested and its performance was recorded. The EHCS showed a stable response for multiple frequencies until its performance was degraded due to the output capacitance produced by the EHCS circuit, due to the finite open loop gain of the op-amp used in the EHCS circuit and the additional loading capacitance introduced by the multiplexers. Secondly, the GIC circuit was integrated in parallel with the EHCS circuit to minimise the unwanted capacitance introduced in the circuit. The EHCS-GIC showed a stable response but was limited to either small frequency band or single frequency. This resulted in multiple tuning of the EHCS-GIC for different frequencies.

The simulated performance showed that the EHCS circuit frequency bandwidth was limited to <1MHz in the presence of different tested RC load combinations. A maximum output impedance of ≈33MΩ was found for frequencies ≤100kHz with a drop off to a low value when it reaches 10MHz frequency. The EHCS-GIC simulated performance showed a reduced frequency bandwidth for a certain tuned configuration. It was observed that with an increase in the resistive part of the RC load combination, the frequency bandwidth of the respective tuned configuration is reduced. This limited frequency bandwidth

response of the circuit is expected and alternatively the improvement in the output impedance is needed. The output impedance of the EHCS-GIC circuit was not fully achieved as expected but it showed a stable and steady response up to ≤1MHz and drops off to a low value above this frequency until it reaches 10MHz. This stability is due to the precise circuit tuning for a narrow frequency bandwidth. Both VCCS circuits showed an output signal saturation due to the usage of low power op-amps, this limits its usage to a very low RC loading combination. The comparison concludes that both VCCS circuit configurations can be used as a current source by solving the op-amp loading voltage problem and precise selection of a resistor network to improve its output impedance.

Bootstrapping is introduced in the research work to overcome the loading voltage problem for the EHCS & EHCS-GIC circuits. Its circuit analysis and some common mode input range conditions are presented. Independent testing of this technique with ±60V power rails resulted in an output amplitude measurement of ≈100$V_{p-p}$. The application of this technique to both VCCS circuits demonstrated that the output voltage doesn't saturate at higher resistive load (≤30kΩ). This concludes that this technique has overcome the loading/saturation problem in both VCCS circuits without affecting other performance parameters with an expectation to achieve similar experimental performance.

Due to the presence of unwanted capacitance of the current source, the bootstrapped EHCS-GIC circuit was focused for performance parameter evaluation. The bootstrapped EHCS-GIC also showed a similar limited frequency bandwidth response due to GIC circuit tuning. The circuit was able to achieve a frequency bandwidth of between 2.6MHz to 418kHz for a RC loading combination of fixed 10pF capacitance and variable resistance (5k-30kΩ with ΔR=5kΩ) for the circuit configuration between 1kHz to 1MHz. The output impedance response for the bootstrapped EHCS-GIC showed a stable response up to ≤1MHz with a drop off above this frequency up to 10MHz due to precise circuit tuning for multiple narrow frequency bandwidth. The circuit showed an output impedance between 50M-3.64kΩ using the same RC loading combination for circuit configuration between 1kHz to 10MHz.

The bipolar bootstrapped EHCS-GIC circuit is also tested with signals routed through multiplexers. The bipolar configuration showed a similar behaviour over a very limited frequency bandwidth for a certain tuned configuration. The circuit was able to achieve a frequency bandwidth between 349kHz to 62 kHz & 1.82-1.61MHz using an RC loading

combination of fixed capacitance (10pF) and variable resistance (5k-30kΩ with ΔR=5kΩ) for circuit configuration between 1kHz to 1MHz & 10MHz respectively. The output impedance of the bipolar configuration shows a similar response between 51MΩ to 7.16kΩ for the same RC loading combination and frequency range as mentioned above.

Based on the results it concludes that bootstrapped bipolar EHCS-GIC circuit has overcome the output saturation problem. The circuit can be used as a current source for the instrument that requires limited multiple frequency bandwidth or single excitation frequency. The overall tested frequency and output impedance response were limited to ≤1MHz for different tuned circuit configurations but was expected to maintain a similar performance level up to ≈2-3MHz. These responses were further reduced with an increase in the RC loading combination. The bipolar configuration of the circuit does not provide good performance at 10MHz frequency and provides an opportunity to further investigate the ideas for high frequency current source design using a different approach.

A high frequency current source design using discrete components is presented to overcome the frequency bandwidth limitation that occurred in the EHCS based current source. This source design was tested at 10MHz frequency with a large loading (30kΩ). The simulation result demonstrated that it achieved a good performance with a voltage drop of 30V at this frequency. It showed that the source was able to deliver 1mA of current at 10MHz with <2% accuracy of phase response.

Besides the GIC technique, another technique for capacitance minimisation is also presented in the thesis and referred as Guard amplifier. It is based on the principle of driving a resistor (effectively large) or capacitor (effectively small) using a high input impedance amplifier with gain nearly but <1. The multiplexer analogue switch models were designed (using $C_{ON}/C_{OFF}$ and $R_{ON}$) and tested with/without guard amplifier circuits using a 30kΩ load for a frequency range between 10kHz to 10MHz. In the presence of a guard circuit, the voltage dropped across the load is 30V (1mA being delivered) and indicates that the circuit has helped in minimising the capacitance for the tested frequency range.

The VCVS/voltage source circuit is also considered as an excitation source in many impedance measurement instruments. The presented bootstrapped voltage source design was tested and its performance was evaluated as a single-end and bipolar source. The result demonstrated a high amplitude output signal without any saturation over a wide

frequency bandwidth as reported in chapter 6. The result of only bipolar VCVS are discussed here. The bipolar circuit was able to achieve a frequency bandwidth of ≈48MHz using an RC loading combination of fixed capacitance (10pF) and variable resistance (5k-30kΩ with ΔR=5kΩ). A low output impedance of the bipolar circuit was observed. It is found to be between 12Ω to 783Ω for 100kHz, 1MHz and 10MHz frequency using the above mentioned RC loading combination. The bipolar source reported a phase difference and SNR of ≈14° (in differential load voltage) and 85-90dB respectively at 10MHz. This concludes that the bipolar VCVS design can practically achieve a frequency bandwidth of >15MHz along with other performance parameters, by building a good quality PCB and precise experimental data measurements.

A DA design is presented for voltage measurement across different passive components. The DA is designed using two different circuits: based on op-amp and discrete components. The performance of the op-amp based DA was limited to a certain amplitude at high frequency (10MHz) using a single resistor gain of DA. The result showed that this DA design was able to measure a high amplitude of ±25V until ≤1MHz. At 10MHz, the DA signal measurement was restricted to an amplitude of ±9V. Above this input amplitude level, it resulted in a low output signal amplitude with a significant phase difference in the output signal. To achieve the required level of amplitude measurement, a discrete component DA is presented based on high speed and high voltage transistors. The performance of this DA is tested at frequencies ≥1MHz to ≤10MHz with variable input amplitude. The result showed that the DA can measure a differential signal of ±25V amplitude at 10MHz without any significant phase difference. Based on the above result, it can be concluded that the DA based on an op-amp has the ability to measure a differential signal at a required amplitude (±25V) up to ≈2-3MHz. Alternatively, the discrete component DA has the ability to measure the required input amplitude for a wide frequency bandwidth. The DA design was applied to the excitation source for voltage measurement and the results were observed to be as per expectation and in-accordance to the above mentioned performance.

The two excitation sources are implemented on two separate PCBs. Their sub-modules are tested and results are compared with the simulation results. The practical results for the VS board are presented. The VS board performance was evaluated with the testing of the voltage source module and discrete component DA. The on-board circuit is slightly optimized according to the practical measurements. The voltage source module was tested

and its performance is presented. According to the measurements, the voltage source was able to achieve a frequency bandwidth of ≈13MHz, an output impedance and phase shift of <350Ω and <112° respectively. The source reported a SNR of 38-41dB. The DA was also tested and reported a frequency bandwidth of 10MHz for a maximum input amplitude of 3.5V. A high input amplitude (≈6V) was also measured but over a reduced frequency bandwidth (≈6MHz). Based on the experimental results for the voltage source PCB, it can be concluded that it has achieved a good performance and can be considered as a good replacement module for the Sussex EIM system along with further optimization in the circuit design.

The experimental results for the current source (CS) board are also tested and presented. The CS board is more complex than the VS board and required testing of large sub-modules. The CS board performance was evaluated by the testing of current source module, guard amplifier module, voltage measurement module and power supply module along with slight optimization of the on-board circuits for practical measurements. The on-board power supply was tested with an output accuracy of ≈1%. The current source module was able to achieve an overall frequency bandwidth of ≤3MHz for different tuned circuit configurations. The generated output voltage for this module gives a phase shift <30°. The experimental output impedance of this module doesn't achieve a high value and was limited to ≤3MΩ for <500kHz frequency and drop to <500kΩ above this frequency. The guard amplifier performance was tested by applying the current source signal to the load through the multiplexers. The load voltage was observed with/without the application of guard amplifier circuit. The experimental result showed that the capacitance was minimised for ≤500kHz frequencies with an increase in the amplitude of the load voltage. The guard amplifier has minimised the capacitance for >1MHz frequencies but its effect was not very significant. The op-amp based DA performance was experimentally tested on the current source board for differential voltage measurement. The results reported a frequency bandwidth of ≤2MHz for a signal amplitude of ≤3V using an op-amp based DA. Considering the experimental result for current source PCB, it can be concluded that it has achieved a satisfactory performance and needs to be considered for further improvement. Although the current source module has achieved a frequency bandwidth of ≤3MHz, its output impedance is not able to maintain the same value up to this frequency.

Based on the experimental results for the DA circuit, it can be concluded that the voltage measurement module can be further optimised and its performance can be enhanced using an IA instead of simple DA circuit. Most of the medical devices connected to sensors in hospitals uses IA at the backend with the benefit of precision gain devices. These devices contain laser-trimmed feedback resistors onto the IC and only require one external gain resistor for amplification, hence eliminating the mismatch factor in the resistors. High impedance small amplitude signals are generated by most of the biomedical sensors. The characteristics of these sensors can show a variable loading effect and can cause signal distortion. As a result, it requires a high impedance from the IA. The IA also requires a high noise rejection level. Due to many wireless devices working in parallel, the medical centres are considered to be an electrically noisy environment. These noise signals are mostly of higher magnitude in contrast to the original signal from the sensor ((typically in mV). Hence, the IA are preferred because the biomedical electrodes pickup unwanted electrical noise, which needs to be excluded for an accurate measurement. IA are used in nearly every field of electronics, by fulfilling the above mentioned circuit requirements, it can be concluded that this device is an important tool for medical devices and should be considered for precise measurements. Hence, this leads an opportunity for further optimisation of the voltage measurement module.

A difference in the experimental and simulated result has been observed as expected for both type of excitation sources. The performance difference is due to any of these possibilities: the stray capacitance introduced by PCB tracks/leads/switches, a slight mismatching in the characteristics of components used, the practical bandwidth of the op-amp used has reached, and finite open-loop gain of the op-amp. Based on the experimental results, the performance of the designed PCB can be further improved by a compact design of board layout with closer component placement so that the stray capacitance can be significantly minimised. Apart from this, the performance can be improved by precisely matching of the circuit components, usage of op-amp with high gain-bandwidth product, precise calibration of the capacitance cancelation circuit, some more precise measurements to determine the output impedance and SNR of the excitation sources.

## 8.3 Future Work

In continuation of the research work investigated and completed in this thesis, there are some suggestions, which can be further explored to achieve better performance of the excitation power source. These possibilities are:

1. One possible source of stray capacitance can be the connection leads used with external devices. In our case, the sinusoidal input was generated using a function generator. The signal generated by the function generator is applied to the input connector of the PCB, which involves a long cable and has resulted in stray capacitance. Hence, one aspect of this project can be the generation of an on-board sinusoidal signal according to the requirements of the instrument. In order to improve the precision and quality of the signal, it is preferred to generate the signal digitally. In this process, the digital samples are generated by direct digital synthesis that are passed through digital-to-analogue convertor followed by a reconstruction filter to generate an analogue signal which can be used to drive the excitation source. The implementation of this waveform generator can be done using an FPGA. The implementation of this module will have a good impact on the performance of the excitation as well as the EIT system.
2. An integrated excitation source can be a future aspect for this research work. It can be achieved by the combination of both current and voltage source on a single PCB for a high frequency excitation signal. The current source tested in this research work is limited to a narrow bandwidth or single frequency due to its frequent circuit tuning for the GIC. Alternatively, the voltage source can change its output signal instantly for any input frequency change. By the integration of these two sources together, it may be useful to achieve a multi-frequency excitation source. A predefined auto-frequency selection module can be designed to select the corresponding source with a change in input frequency (i.e. for ≤2MHz the current source acts as a signal generator and voltage source for >2MHz).
3. Presently the current source module (CSM) consists of an EHCS with a parallel GIC circuit. The CSM was replicated to cover different frequencies and has resulted in a complex PCB. A future aspect for investigation can be multiplexing a single EHCS circuit with multiple GIC circuits. The multiplexing will introduce some additional capacitance but if it is tackled by the GIC itself or any other

supporting cancellation technique then a possibility for good performance can be expected.

4. For patient safety, a current limiting circuit should be introduced in the design. In the case of the voltage source, in which a constant voltage amplitude is applied to the subject irrespective to the load current. The resulting load current varies and depends upon the attached loading value. To maintain the safety standard described earlier in the thesis, a current limiter circuit should be integrated with the excitation source especially for the voltage source design.
5. Presently, the on-board power module is taking four external power supplies. This module can be further optimised in terms of a precise on-board DC power supply generation and reducing to two external inputs.
6. Presently, the experimental performance of the guard amplifier capacitance cancellation technique is limited to 500kHz frequency. The minimisation above this frequency is not very significant. Hence, it leads an opportunity to further investigate this circuit to achieve a better performance and extend its operational frequency range to at least 4-5MHz.
7. Presently, the voltage source module provided a high frequency bandwidth of 10MHz but improvement is needed to precisely maintain a constant amplitude for frequencies >3MHz and ≤10MHz. At high frequency, the amplitude was fluctuating with the increase in the loading. Therefore, this leads to an opportunity to further optimise the voltage source module for its improved performance. A possible solution can be an amplitude comparator, which drops the voltage down to a required amplitude when needed.
8. Voltage measurement module (differential amplifier) performance can also be improved because its performance was not compliant with the simulated performance. The future focus can be the experimental measurement of >15V amplitude up to ≤10MHz frequency. A more compact design of this module can be implemented using op-amp/discrete components. Currently, the DA design is replicated to acquire the voltage measurement on the CS and VS PCB board. A multiplexing of this module can also be implemented in future to further optimize the entire design.
9. In addition to (8), a few other problems were observed during the testing of the voltage measurement module and should be considered for future improvement. The current measurement module is based on a simple DA design using a single

op-amp and discrete op-amp design. This configuration could be beneficial for a few differential measurement applications (i.e. bridged signal) showing a good CMMR. However, a non-infinity input impedance of the circuit is observed, which shows low and unmatched input impedance on the inverting input terminal. As a result, a large difference in input impedance can be observed as compared to the non-inverting terminal. The simple circuit configuration also requires precise resistor matching and source impedance balancing. The input impedance of the circuit can be increased by making the feedback resistors very large. If the input resistors of the DA are set to 1MΩ then the feedback resistors should be 100MΩ (for an approximate gain of 100). However, amplification of small amplitude signals usually requires higher than this gain. On the other hand, usage of high value resistors also raises problems. It can be noisy, difficult to accurately match large resistors and sources of stray capacitance at high frequencies affecting the device CMMR. The IA can be one of the possible solutions, in which the non-inverting buffers before the input terminals will provide infinite input impedance along with gain, while the DA provides an additional gain level along with a single-ended output. A future aspect of this research is to further improve the performance of the voltage measurement module by the integration of IA within the PCB either with the market available IC's or by designing a high performance IA based on a high speed op-amp IC or a discrete component based IA. The improved module will have the expected performance of very high: CMMR, gain and input impedance.

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# Appendices

## A: HCS Circuit Analysis

Prof. Bradford Howland of MIT invented HCS in 1962. This circuit was not patented at that time. The HCS circuit was first published in January 1964. Studies have shown that HCS has comparable performance as compared to other complicated sources. There may be some application, which requires a unidirectional current source. Unidirectional current source is easier to make with a high output impedance and wide frequency range using an op-amp and some other discrete components. However, there can be some applications like the EIT system, which requires current to be put in either direction or even AC currents. HCS are excellent for those applications. Current sources are mostly used to test another devices performance. They can be used to inject current into sensors or other materials, can be used in experiments, and can be used to bias up diodes or transistors. In short, when you need a current source, HCS are always useful.

A differential V-I converter / differential VCCS can be obtained by applying two input voltage signals. The circuit consists of one operational amplifier and a resistive network, which consists of five resistors. A load is connected between the resistors attached to the non-inverting terminal of the operational amplifier. Current passing through each resistor are identified as $I_1$ to $I_4$ and $I_L$. Node voltages ($V_a$, $V_b$ and $V_o$) are identified in the circuit to perform circuit analysis and output equations for the HCS circuit are derived. Figure A.1 shows the circuit setup of a HCS.

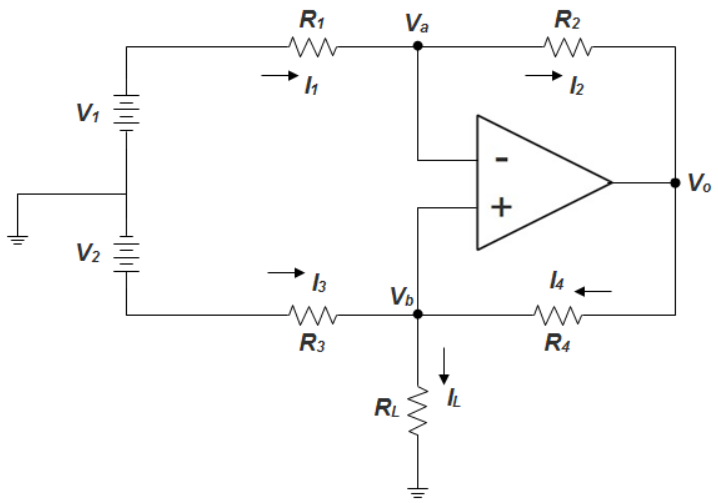



Figure A.1: A differential VCCS using Howland circuit

To find the amount of current passing through $R_L$, the Kirchhoff current law is applied at node $V_b$. It can be seen that the load current can be found once we know the amount of current passing through resistor $R_3$ and $R_4$. Therefore, the load current ($I_L$) can be rewritten as:

$$I_L = \frac{V_2 - V_b}{R_3} + \frac{V_o - V_b}{R_4} \qquad \text{Eq. (A.1)}$$

After rearranging, the above equation can be written as;

$$I_L = \frac{V_2}{R_3} + \frac{V_o}{R_4} - V_b\left(\frac{R_3 + R_4}{R_3 R_4}\right) \qquad \text{Eq. (A.2)}$$

We need to find $V_o$ and $V_b$ in order to find the current passing through the load. The output voltage equation of the HCS circuit can be derived with the help of the Superposition Theorem. If $V_2$ is disconnected first then it can be seen that the circuit configuration becomes an inverter having its non-inverting terminals connected to ground through resistor $R_3$ and $R_4$. Therefore, the output voltage ($V_{o2}$) will be given by the following equation:

$$V_{o2} = -V_1\left(\frac{R_2}{R_1}\right) \qquad \text{Eq. (A.3)}$$

If $V_1$ is disconnected then it can be seen that the circuit configuration becomes a non-inverting amplifier. Therefore, the output voltage ($V_{o1}$) will be given by the following equation:

$$V_{o1} = V_b\left(1 + \frac{R_2}{R_1}\right) \qquad \text{Eq. (A.4)}$$

Applying the voltage divider rule at node $V_b$ to find its value it is given by:

$$V_b = V_2\left(\frac{R_4}{R_3 + R_4}\right) \qquad \text{Eq. (A.5)}$$

$V_{o1}$ can be rewritten as:

$$V_{o1} = V_2\left(\frac{R_4}{R_3 + R_4}\right)\left(1 + \frac{R_2}{R_1}\right) \qquad \text{Eq. (A.6)}$$

Therefore, the output voltage ($V_o$) equation for the op-amp will be:

$$V_o = V_{o1} + V_{o2} \qquad \text{Eq. (A.7)}$$

$$V_o = V_b\left(1 + \frac{R_2}{R_1}\right) + \left[-V_1\left(\frac{R_2}{R_1}\right)\right] \qquad \text{Eq. (A.8)}$$

Substituting the value of $V_0$ in the Eq. (A.2), the equation for $I_L$ can be expressed as:

$$I_L = \frac{V_2}{R_3} - \frac{V_1 R_2}{R_1 R_4} + V_b \left[\frac{R_2}{R_1 R_4} - \frac{1}{R_3}\right] \quad \text{Eq. (A.9)}$$

In order to make the HCS circuit as a single signal supply source, $V_2$ can be eliminated by shorting to ground and the resulting output current expression becomes the total amount of current passing through the load. It can be described by:

$$I_L = -\frac{V_1 R_2}{R_1 R_4} + V_b \left[\frac{R_2}{R_1 R_4} - \frac{1}{R_3}\right] \quad \text{Eq. (A.10)}$$

The above expression shows that the amount of current passing through load is independent of the load value. This circuit can be considered as a constant current source with the following conditions:

- $R_1$ should be equal to $R_2$ and $R_3$ should be equal to $R_4$.
- It should also verify the following ratio:

$$\frac{R_2}{R_1} = \frac{R_4}{R_3} \quad \text{Eq. (A.11)}$$

If the above conditions are satisfied, then the load current equation becomes:

$$I_L = -\frac{V_1}{R_3} \quad \text{Eq. (A.12)}$$

The output impedance of the HCS can be found by the following procedure. Assuming that $V_1 = 0$ in Eq. A.10 and solving it for the ratio $V_b / I_L$, will give an expression for the output impedance and can be expressed as:

$$Z_o = \frac{V_b}{I_L} = \left[\frac{R_1 R_3 R_4}{R_2 R_3 - R_1 R_4}\right] \quad \text{Eq. (A.13)}$$

When the ratio condition is satisfied, the HCS circuit will perform as an ideal current source and the output impedance of the circuit will be infinite.

# B: EHCS Circuit Analysis

According to the Figure 4.2, the output current delivered to the load can be calculated by evaluating the respective current at node $V_o$. Applying the Kirchhoff current law at node $V_o$ to describe load current:

$$I_3 + I_L = I_4 \qquad \text{Eq. (B.1)}$$

$$I_L = I_4 - I_3 \qquad \text{Eq. (B.2)}$$

Above equation shows that the load current can be found once the current passing through resistor $R_4$, $R_3$ and $R_5$ are found. Figure 4.2 shows that current passing through resistor $R_5$ and $R_3$ is same and is denoted by $I_3$. To find these currents, ohm's law can be applied on the above equation and can be described as:

$$I_L = \frac{V_z - V_o}{R_4} - I_3 \qquad \text{Eq. (B.3)}$$

Rearranging above equation:

$$I_L = \frac{(V_z - V_x) - (V_o - V_y)}{R_4} - \frac{I_3 R_4}{R_4} \qquad \text{Eq. (B.4)}$$

$$I_L = \frac{-V_{R2} - V_{R5}}{R_4} - \frac{I_3 R_4}{R_4} \qquad \text{Eq. (B.5)}$$

$$I_L = \frac{-I_1 R_2 - I_3 R_5}{R_4} - \frac{I_3 R_4}{R_4} \qquad \text{Eq. (B.6)}$$

Rearranging above equation:

$$I_L = -\frac{I_1 R_2}{R_4} - I_3\left(\frac{R_4 + R_5}{R_4}\right) \qquad \text{Eq. (B.7)}$$

$I_1$ and $I_3$ can be expressed as:

$$I_1 = \frac{V_1 - V_x}{R_1} \qquad \text{Eq. (B.8)}$$

$$I_3 = \frac{V_y}{R_3} \qquad \text{Eq. (B.9)}$$

Substituting the above values into the above equation, it can be expressed as:

$$I_L = -\frac{(V_1 - V_x)R_2}{R_1R_4} - \frac{V_y}{R_3}\left(\frac{R_4 + R_5}{R_4}\right) \qquad \text{Eq. (B.10)}$$

$$I_L = -\frac{V_1R_2}{R_1R_4} + \frac{V_xR_2}{R_1R_4} - \frac{V_y}{R_3}\left(\frac{R_4 + R_5}{R_4}\right) \qquad \text{Eq. (B.11)}$$

Since $V_x = V_y$ then above equation can be rearranged as:

$$I_L = -\frac{V_1R_2}{R_1R_4} + \frac{V_y}{R_4}\left[\frac{R_2}{R_1} - \frac{(R_4 + R_5)}{R_3}\right] \qquad \text{Eq. (B.12)}$$

Applying the voltage divider rule at node $V_y$ to find its value:

$$V_y = \frac{V_o\, R_3}{R_3 + R_5} \qquad \text{Eq. (B.13)}$$

Therefore, the final equation for the output current becomes:

$$I_L = -\frac{V_1R_2}{R_1R_4} + \frac{V_oR_3}{R_4(R_3 + R_5)}\left[\frac{R_2}{R_1} - \frac{(R_4 + R_5)}{R_3}\right] \qquad \text{Eq. (B.14)}$$

The above expression can be used to find the amount of current delivered to the attached load. It can be seen that the expression is independent to the load value and depends on the resistor network settings along with applied input voltage.

# C: GIC Circuit Analysis

The circuit analysis of the GIC circuit shown in Figure 4.3 is based on the assumption that the op-amp used in the circuit are ideal. To analyse the GIC circuit, all possible node voltages were identified: $V_1$, $V_2$, $V_3$ and $V_4$ as shown in Figure 4.3. Using an ideal op-amp fact, that op-amp keeps its $V_n = V_p$, we can write the nodes voltages defined in Figure 4.3 as:

$$V_i = V_2 = V_4 \qquad \text{Eq. (C.1)}$$

Ideally, the op-amp doesn't draw any current. Therefore, the current at node $V_4$ can be expressed as:

$$I_4 = I_5 = \frac{V_4}{Z_5} = \frac{V_i}{Z_5} \qquad \text{Eq. (C.2)}$$

Voltage at node $V_3$ can be written as:

$$V_3 = V_4 + I_4 Z_4 \qquad \text{Eq. (C.3)}$$

Substituting value of $I_4$ and $V_4$ into $V_3$ equation gives:

$$V_3 = V_i + \frac{V_i Z_4}{Z_5} \qquad \text{Eq. (C.4)}$$

Current passing through $Z_3$ ($I_3$) can be expressed using ohm's law as:

$$I_3 = \frac{V_2 - V_3}{Z_3} \qquad \text{Eq. (C.5)}$$

Substituting the value of $V_2$ and $V_3$ into $I_3$ equation gives:

$$I_3 = \frac{V_i}{Z_3} - \frac{\left(V_i + \frac{V_i Z_4}{Z_5}\right)}{Z_3} \qquad \text{Eq. (C.6)}$$

Rearranging Eq. C.6 for $I_3$:

$$I_3 = \frac{-V_i Z_4}{Z_3 Z_5} \qquad \text{Eq. (C.7)}$$

The voltage at node $V_1$ can be written as:

$$V_1 = V_2 + I_2 Z_2 \qquad \because \quad I_2 = I_3 \qquad \text{Eq. (C.8)}$$

Substituting the value of $V_2$ and $I_2$ in $V_1$ equation gives:

$$V_1 = V_i - \frac{V_i Z_4 Z_2}{Z_3 Z_5} \qquad \text{Eq. (C.9)}$$

Finally, the last current ($I_1$) in the circuit can be calculated as:

$$I_1 = \frac{V_i - V_1}{Z_1} \qquad \text{Eq. (C.10)}$$

Substituting the value of $V_1$ into $I_1$ equation gives:

$$I_1 = \frac{V_i - \left[V_i - \frac{V_i Z_4 Z_2}{Z_3 Z_5}\right]}{Z_1} \qquad \text{Eq. (C.11)}$$

Rearranging the above equation gives:

$$I_1 = \frac{V_i Z_4 Z_2}{Z_1 Z_3 Z_5} \qquad \text{Eq. (C.12)}$$

Solving Eq. C.12 for $V / I$ ratio, the input impedance of the GIC circuit can be described as:

$$Z_i = \frac{V_i}{I_1} = \frac{Z_1 Z_3 Z_5}{Z_2 Z_4} \qquad \text{Eq. (C.13)}$$

# D: Guard Amplifier Circuit Testing

An experiment was setup with a 1V AC signal source driving a simple FET follower amplifier through a 10M resistor. Initially the follower amplifier circuit was checked with a simple configuration in which the output signal is taken off the source with respect to ground and the drain is connected directly to $V_{DD}$. Two bias resistors were connected with the gate of the FET transistor. The AC simulation of this circuit configuration showed that the circuit amplifier output was not able to follow the 1V input signal due to the potential division formed between the bias resistors and the 10M source resistor. The output voltage was ≈0.9V of input voltage and the circuit shows a band pass characteristics having a cut off frequency at ≈120 kHz frequency. Therefore, modification was required in the circuit so that it can closely follow the input signal.

The first step in this achievement was to bootstrap the bias resistor (connected with source of FET) larger by driving it with the output signal of the amplifier. This is highlighted as step 1 in the Figure D.1. The AC simulation of this configuration showed a slightly improved output signal following but over a narrow frequency bandwidth. This can be possibly due to a small capacitance between the drain and gate of the FET amplifier, which forms an RC potential divider circuit. R is being referred to the 10M source resistor and C is referred to the gate-drain capacitance. Results show that the output voltage signal is ≈0.95V of the input signal and the amplifier still shows band pass characteristics of 20 kHz having 2 kHz as the lower 0.5 amplitude frequency and 95 kHz as the upper 0.5 amplitude frequency. To further improve the signal follower the gate-drain capacitance needs to be minimised. This was done by bootstrapping the drain of the FET transistor and is shown as step 2 in Figure D.1.

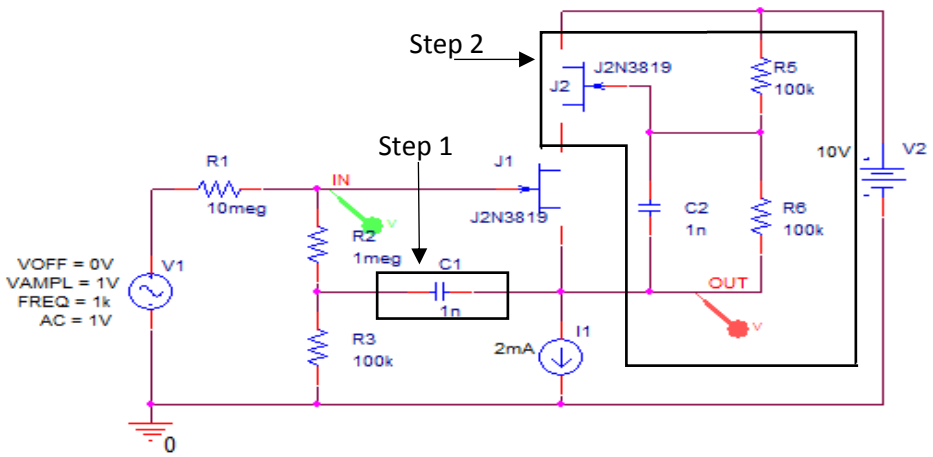



Figure D.1: Guard Amplifier schematic with bootstrapped bias resistor and FET drain

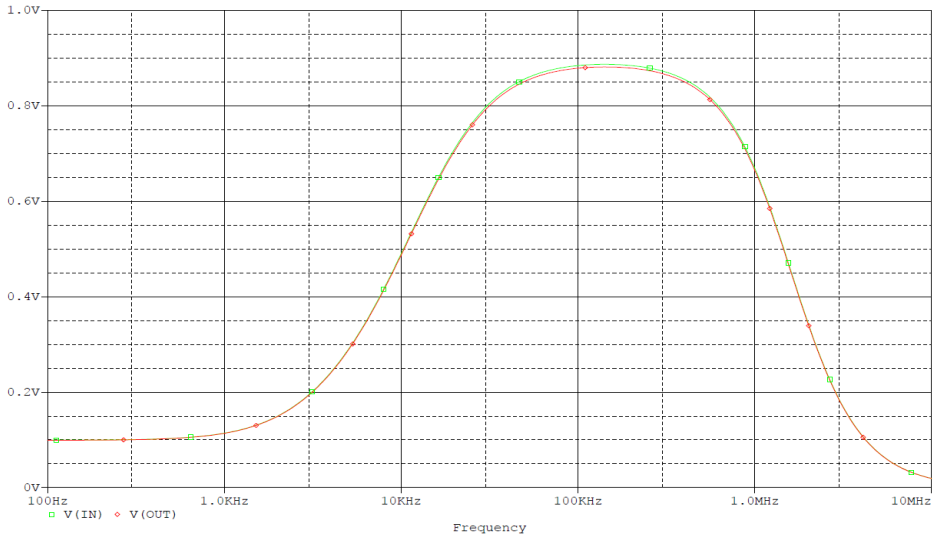



Figure D.2: Guard Amplifier AC response with bootstrapped bias resistor and FET drain

The overall AC response of the circuit shown in Figure D.2, reports the improvement gained by this final bootstrapping step. It was seen that the output signal closely follows the input signal and both are close over a wide frequency range. This gate-drain capacitance bootstrapping has reduced the input capacitance of the follower amplifier and as a result the band pass characteristics of the circuit has widened. The improved guard amplifier schematic is shown in Figure D.1, which highlights all the important steps of the circuit in achieving a better follower amplifier.

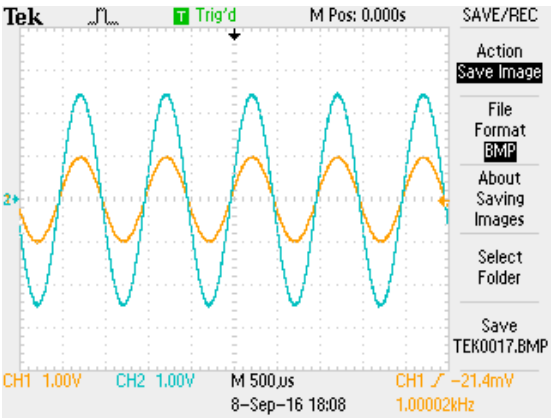
Having considered the benefits of the guard amplifiers there are also some defects of guard amplifiers usage within a circuit. A trade-off has to be made between the advantages and disadvantages of the guard amplifier. The first defect of guard amplifiers is that it amplifies the circuit internal noise, which is done by the increase in the input impedance of the bias resistor due to bootstrapping. Mostly this is not a problem because there is large signal, which is the resultant of a resistor charging and discharging the input capacitance to be measured and results in a good signal to noise ratio.

A problem may arise when the first stage of the guard amplifier is a BJT. If that is the case then a FET should be used instead. A second defect can be the tendency of oscillation especially when there is a long co-axial interface in between the circuitry or when the input capacitance becomes more than the capacitance between input and guard output. A third defect relates to the gain of the amplifier. The guard amplifier technique is mostly useable at the lower frequencies (i.e. ≈1MHz). This is due to the difficulties in achieving a gain near to but less than one at higher frequencies. If the required gain can be achieved at higher frequencies then the guard amplifier can be used to cancel unwanted capacitance at higher frequency.

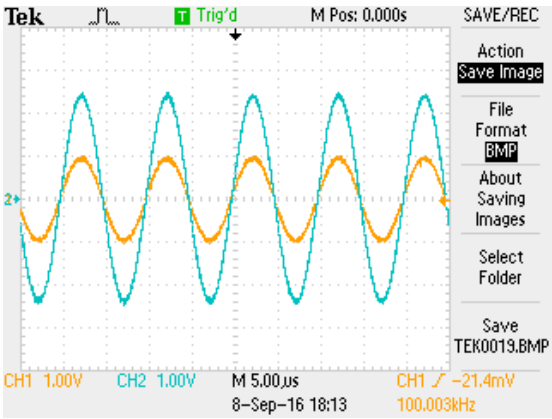
# E: VSM Circuit Performance

This appendix represents the VSM experimental result attached with a load of 5kΩ and 5kΩ‖10pF (loading capacitance) using ±15V DC power supply rails. A $2V_{p\text{-}p}$ sinusoidal signal was generated using a function generator for the frequencies range between 1kHz to 15MHz. Different performance parameters are evaluated for the VSM circuit using the above mentioned loading, and are presented in chapter 7 of this thesis.

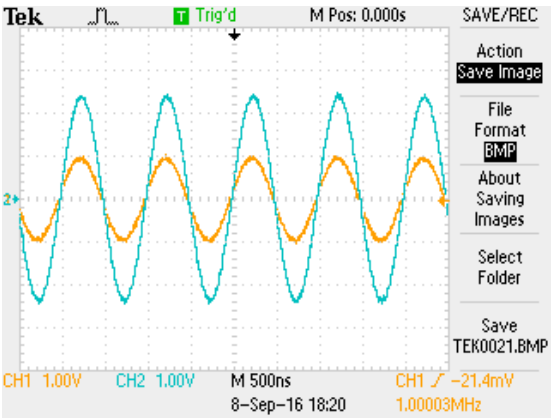
The experimental results show that the voltage source circuit has achieved good performance level by providing the required signal amplitude at high frequency (i.e. 10MHz). It maintains an amplitude of $5V_{p\text{-}p}$ for the tested load across a wide frequency bandwidth. The experimental results presented for the VSM include an additional loading capacitance of ≈15pF for the measurement probe and are presented in Figure E.1 and Figure E.2. The results show the amplitude of output signal (blue) with respect to the amplitude of input signal (yellow).



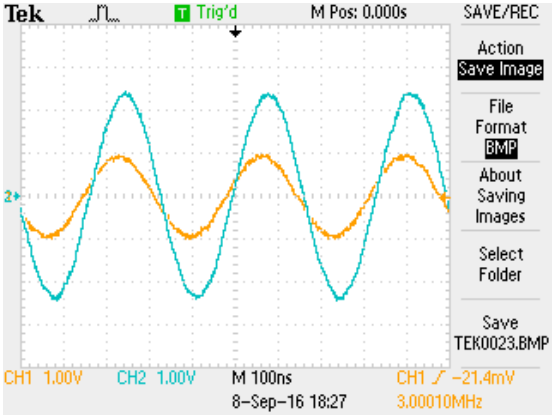

*(a)* Load voltage at 1kHz: approximately $5V_{p\text{-}p}$ amplitude and 0°phase shift



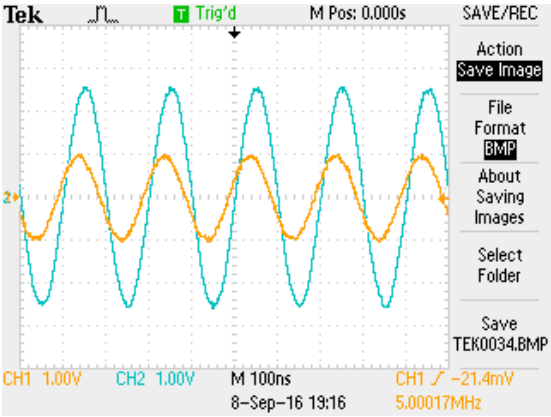

*(b)* Load voltage at 100kHz: approximately $5V_{p\text{-}p}$ amplitude and 0°phase shift



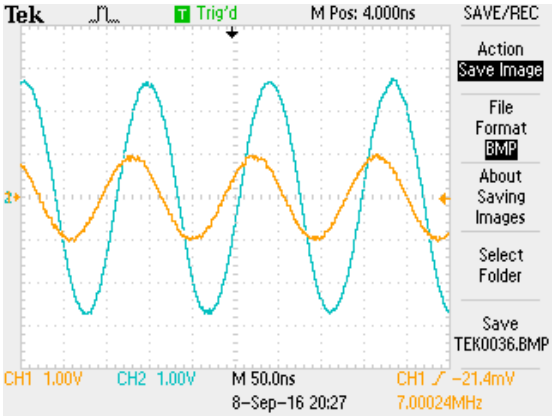

*(c)* Load voltage at 1MHz: approximately $5V_{p\text{-}p}$ amplitude and 4.32°phase shift



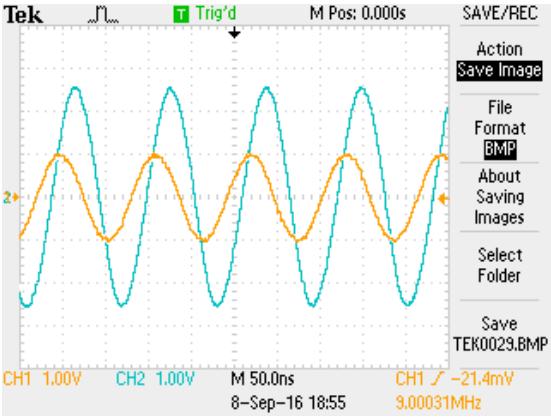

*(d)* Load voltage at 3MHz: approximately $5V_{p\text{-}p}$ amplitude and 17.19°phase shift



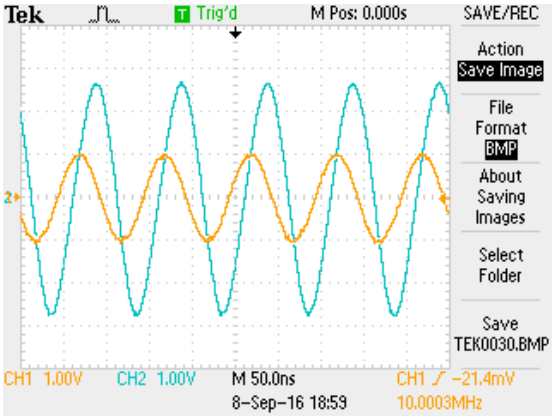

*(e)* Load voltage at 5MHz: approximately 5.16$V_{p\text{-}p}$ amplitude and 28.8°phase shift



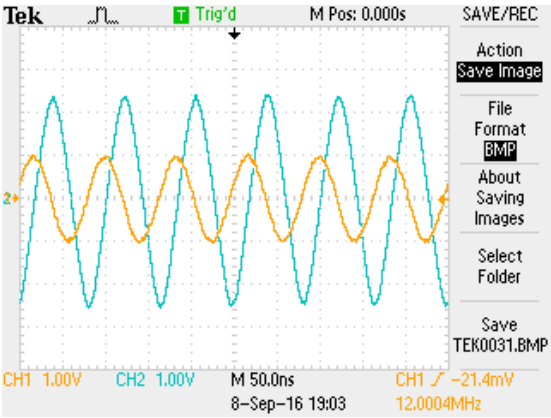

*(f)* Load voltage at 7MHz: approximately 5.20$V_{p\text{-}p}$ amplitude and 47.83°phase shift



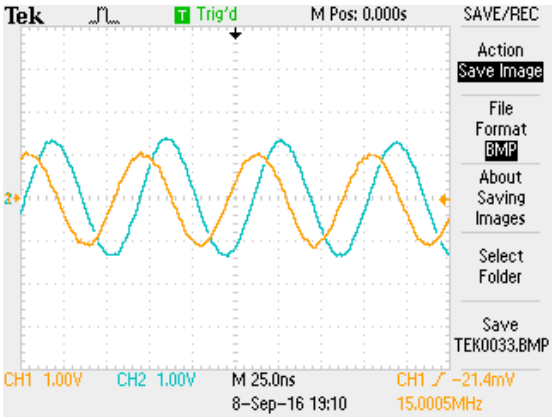

*(g)* Load voltage at 9MHz: approximately 5.12$V_{p\text{-}p}$ amplitude and 61.62°phase shift




*(h)* Load voltage at 10MHz: approximately 5.12$V_{p\text{-}p}$ amplitude and 72°phase shift

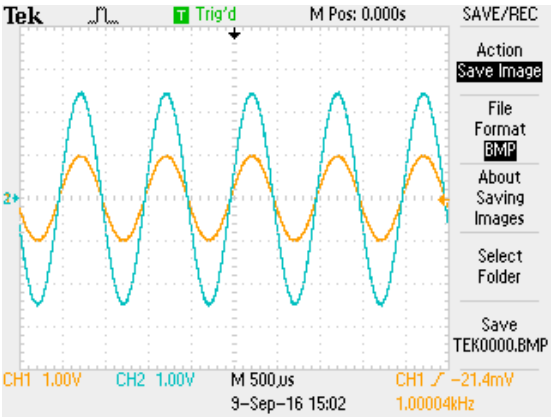



*(i)* Load voltage at 12MHz: approximately 4.9$V_{p\text{-}p}$ amplitude and 98.57°phase shift

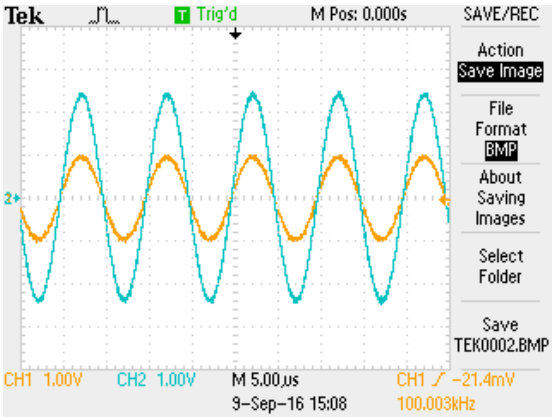



*(j)* Load voltage at 15MHz: approximately 2.6$V_{p\text{-}p}$ amplitude and 75.22°phase shift

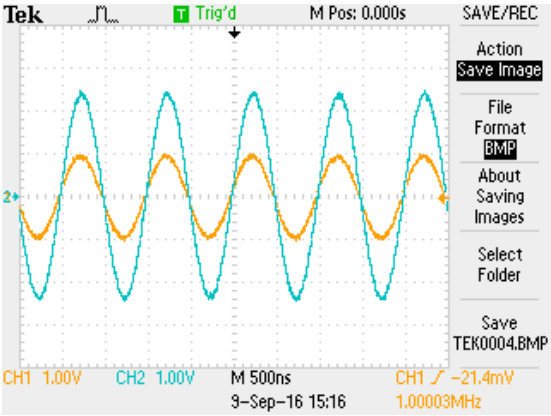
Figure E.1: Voltage Source loading voltage at different frequencies for 5kΩ loading



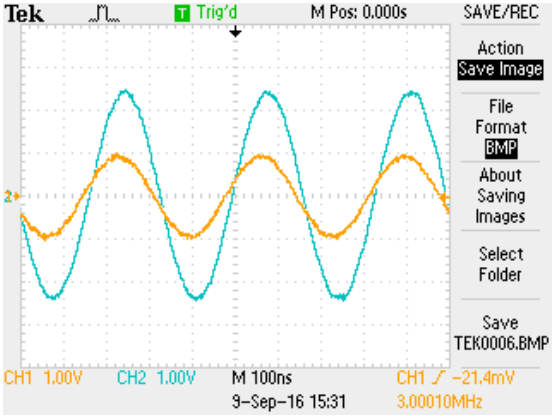

*(a)* Load voltage at 1kHz: approximately $5V_{p\text{-}p}$ amplitude and 0°phase shift



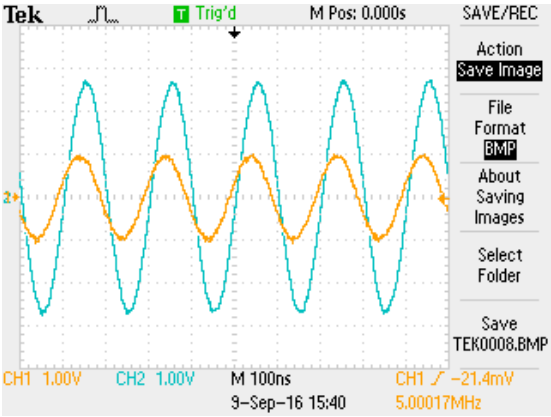

*(b)* Load voltage at 100kHz: approximately $5V_{p\text{-}p}$ amplitude and 0°phase shift



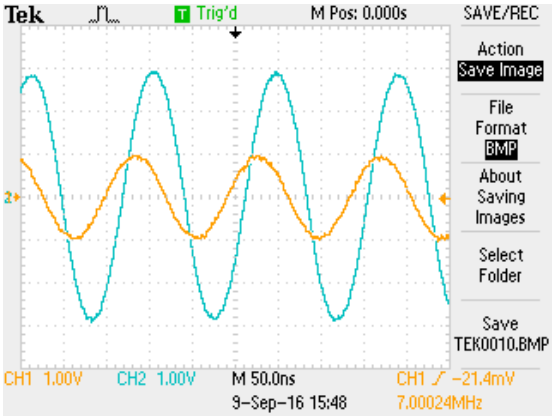

*(c)* Load voltage at 1MHz: approximately $5V_{p\text{-}p}$ amplitude and 4.32°phase shift



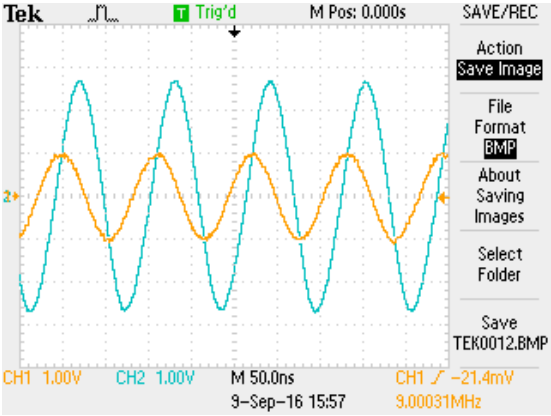

*(d)* Load voltage at 3MHz: approximately $5V_{p\text{-}p}$ amplitude and 17.19°phase shift



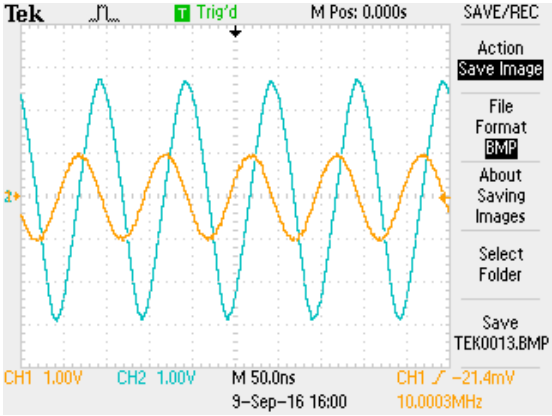

*(e)* Load voltage at 5MHz: approximately $5.20V_{p\text{-}p}$ amplitude and 28.8°phase shift



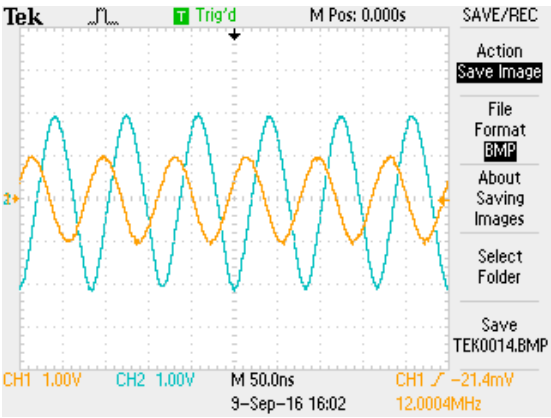

*(f)* Load voltage at 7MHz: approximately $5.80V_{p\text{-}p}$ amplitude and 52.87°phase shift



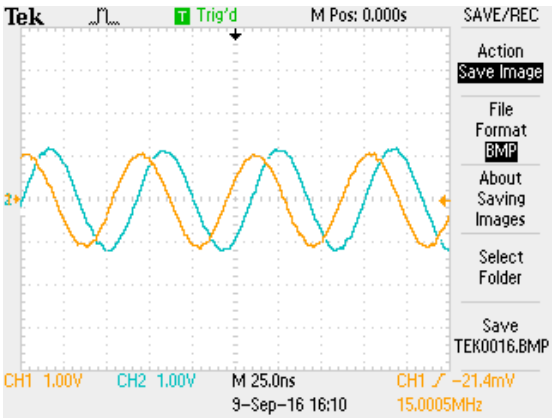

*(g)* Load voltage at 9MHz: approximately $5.20V_{p\text{-}p}$ amplitude and 68.11°phase shift




*(h)* Load voltage at 10MHz: approximately $5.30V_{p\text{-}p}$ amplitude and 90°phase shift




*(i)* Load voltage at 12MHz: approximately $4.16V_{p\text{-}p}$ amplitude and 111.5°phase shift




*(j)* Load voltage at 15MHz: approximately $2.28V_{p\text{-}p}$ amplitude and 75.22°phase shift

Figure E.2:Voltage Source loading voltage at different frequencies for 5kΩ‖10pF loading

# F: Microcontroller Ports Configuration

This appendix presents the microcontroller 8-bit wide, bidirectional I/O ports (A-E) configuration, used for signal multiplexing on the current source board.

**Register A:** ***Not Used, I: input, O: output**

| Register bit (with data direction) | A7(I) | A6(O) | A5(I) | A4(I) | A3(I) | A2(I) | A1(I) | A0(I) |
|---|---|---|---|---|---|---|---|---|
| Pin description | CLK IN | CLK OUT | * | * | * | * | * | * |

**Register B:** *Level 1 Multiplexing: MUX-1(B0 – B2), MUX-2(B3-B5), I (input), O (output), **Not Used*

| Register bit (with data direction) | B7(I) | B6(I) | B5(O) | B4(O) | B3(O) | B2(O) | B1(O) | B0(O) |
|---|---|---|---|---|---|---|---|---|
| Pin description | PGD | PGC | EN | A0 | A1 | EN | A0 | A1 |
| 1kHz CSM circuit selected | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 10kHz CSM circuit selected | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 100kHz CSM circuit selected | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1MHz CSM circuit selected | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Register C:** *Level 2 Multiplexing: MUX-3(C0 – C1), MUX-4(C2-C3), I (input), O (output), **Not Used*

| Register bit (with data direction) | C7(I) | C6(O) | C5(O) | C4(O) | C3(O) | C2(O) | C1(O) | C0(O) |
|---|---|---|---|---|---|---|---|---|
| Pin description | RX | TX | * | * | EN | IN | EN | IN |
| 1kHz-1MHz CSM output passed to load | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 10MHz CSM output passed to load | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

**Register D:** *Front-end signal multiplexing (D0 – D3), I (input), O (output), **Not Used*

| Register bit (with data direction) | D7(O) | D6(O) | D5(O) | D4(O) | D3(O) | D2(O) | D1(O) | D0(O) |
|---|---|---|---|---|---|---|---|---|
| Pin description (frequency selection) | * | * | * | * | 1k | 10k | 100k | 1M |
| 1kHz input signal passed to CSM | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 10kHz input signal passed to CSM | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 100kHz input signal passed to CSM | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1MHz input signal passed to CSM | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

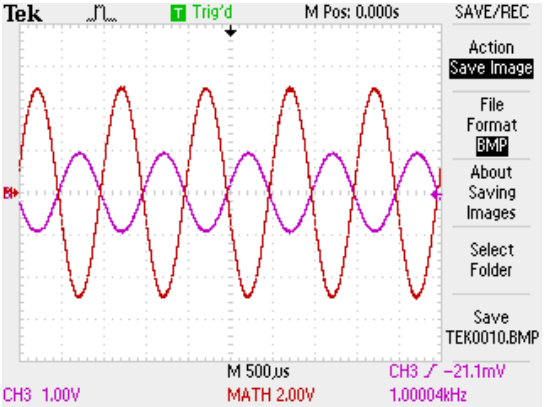
**Register E:** ***Not Used, I (input), O (output)**

| Register bit (with data direction) | E7(O) | E6(O) | E5(O) | E4(O) | E3(I) | E2(O) | E1(O) | E0(O) |
|---|---|---|---|---|---|---|---|---|
| Pin description | * | * | * | * | MCLR_ | * | * | * |

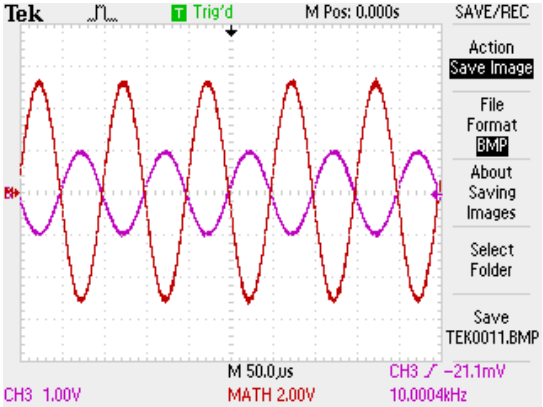
# G: CSM Circuit Performance

This appendix presents the CSM experimental result attached with a load of 5kΩ and 10kΩ loading using ±36V DC power supply rails. Different performance parameters are evaluated for the CSM circuit using the above mentioned loading, and are presented earlier in chapter 7 of this thesis.

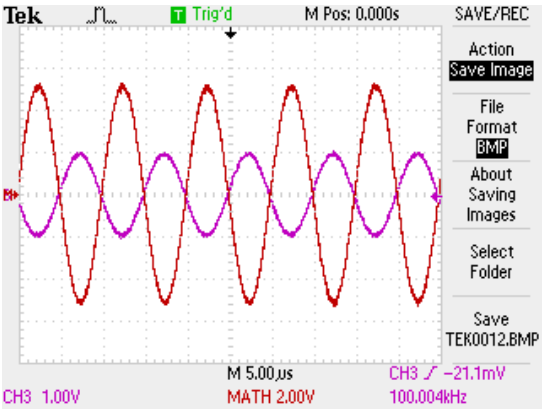
The experimental results show that the current source circuit has achieved a good performance level by providing the required signal amplitude until 3MHz frequency without any signal saturation. It maintains an amplitude of $10V_{p\text{-}p}$ & $20V_{p\text{-}p}$ for the tested load across the tested frequency range. The experimental results presented for the CSM include an additional loading capacitance of ≈30pF for the measurement probes and are presented in Figure G.1 and Figure G.2. The results show the amplitude of output signal (red) with respect to the amplitude of input signal (purple).



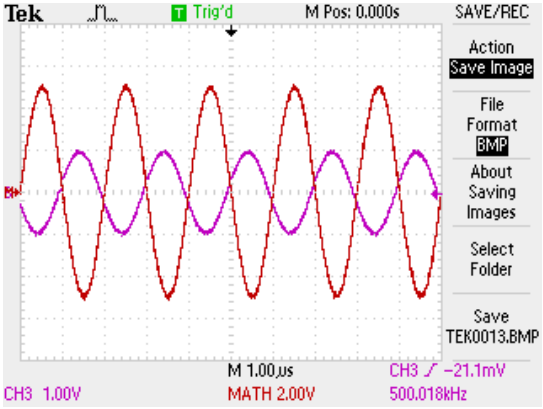

*(a)* Differential load voltage at 1kHz: approximately $10V_{p\text{-}p}$ amplitude



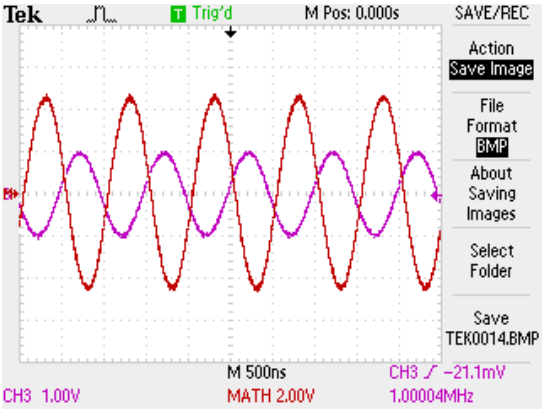

*(b)* Differential load voltage at10kHz: approximately $10.7V_{p\text{-}p}$ amplitude



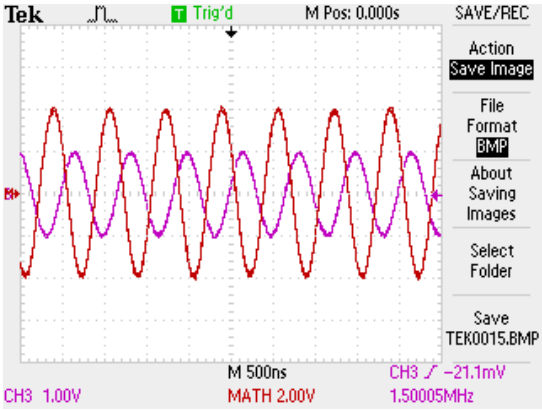

*(c)* Differential load voltage at 100kHz: approximately $10.6V_{p\text{-}p}$ amplitude



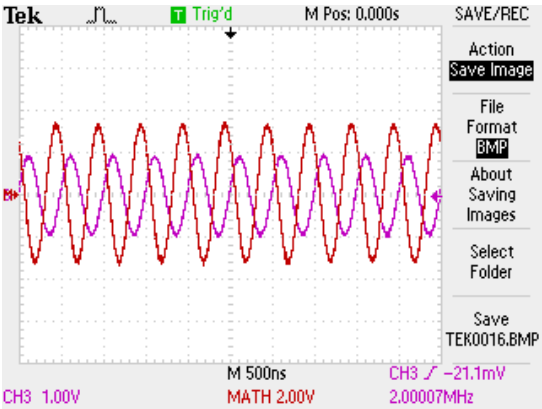

*(d)* Differential load voltage at 500kHz: approximately $10.3V_{p\text{-}p}$ amplitude



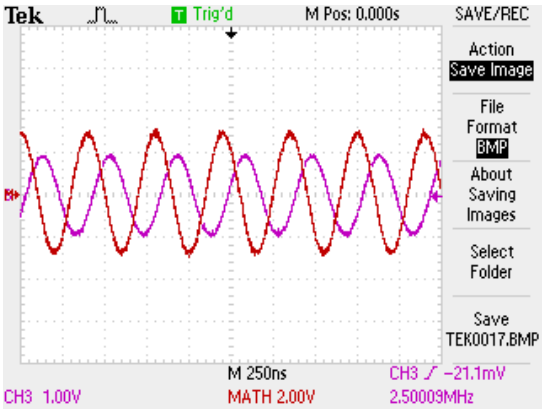

*(e)* Differential load voltage at 1MHz: approximately 9.36$V_{p\text{-}p}$ amplitude



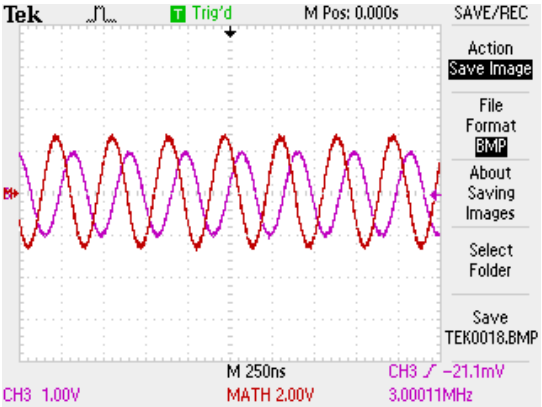

*(f)* Differential load voltage at 1.5MHz: approximately 8.16$V_{p\text{-}p}$ amplitude




*(g)* Differential load voltage at 2MHz: approximately 6.80$V_{p\text{-}p}$ amplitude

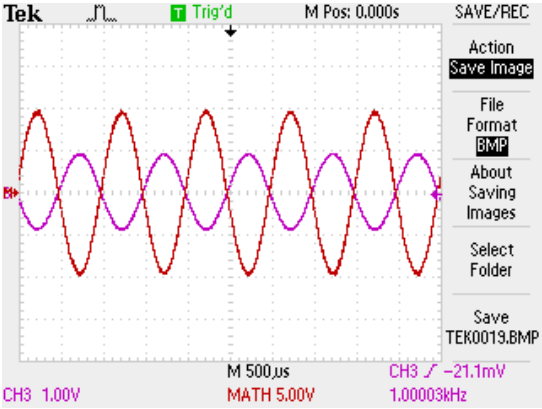



*(h)* Differential load voltage at 2.5MHz: approximately 6$V_{p\text{-}p}$ amplitude

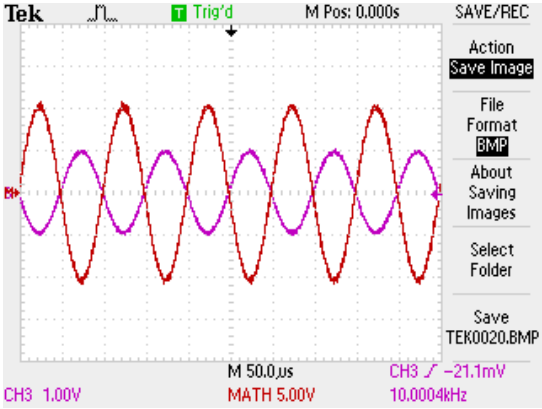



*(i)* Differential load voltage at 3MHz: approximately 5.56$V_{p\text{-}p}$ amplitude

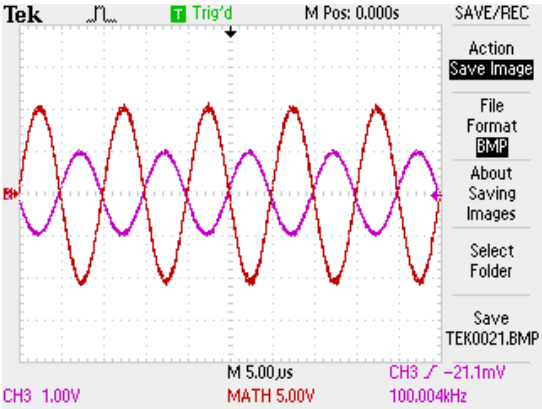
Figure G.1: Differential Load Voltage using 2$V_{p\text{-}p}$ input at different frequencies for5kΩ loading



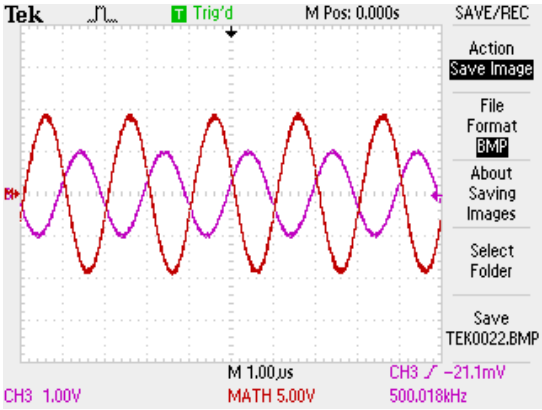

*(a)* Differential load voltage at 1kHz: approximately 20$V_{p\text{-}p}$ amplitude



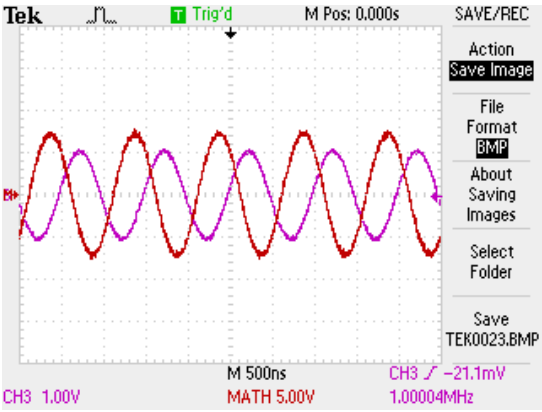

*(b)* Differential load voltage at10kHz: approximately 21$V_{p\text{-}p}$ amplitude



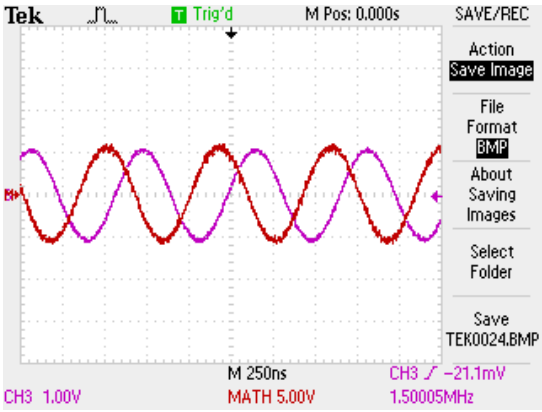

*(c)* Differential load voltage at 100kHz: approximately 21$V_{p\text{-}p}$ amplitude



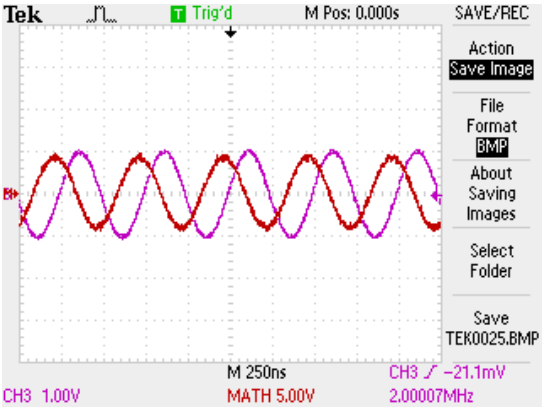

*(d)* Differential load voltage at 500kHz: approximately 19.40$V_{p\text{-}p}$ amplitude



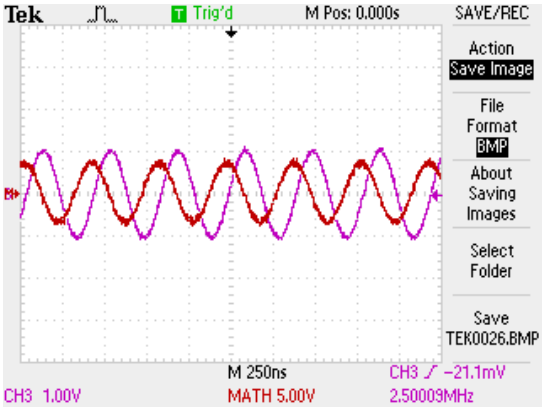

*(e)* Differential load voltage at 1MHz: approximately 15.20$V_{p\text{-}p}$ amplitude



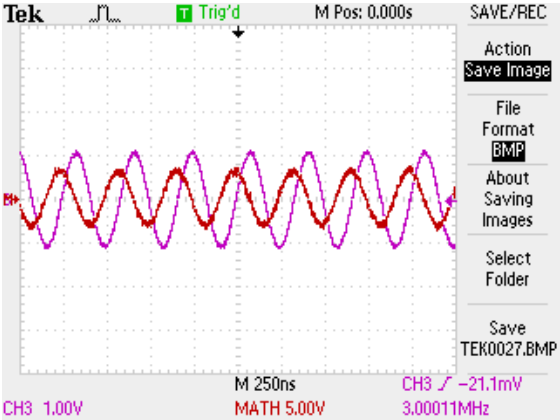

*(f)* Differential load voltage at 1.5MHz: approximately 12$V_{p\text{-}p}$ amplitude




*(g)* Differential load voltage at 2MHz: approximately 9.55$V_{p\text{-}p}$ amplitude




*(h)* Differential load voltage at 2.5MHz: approximately 8$V_{p\text{-}p}$ amplitude



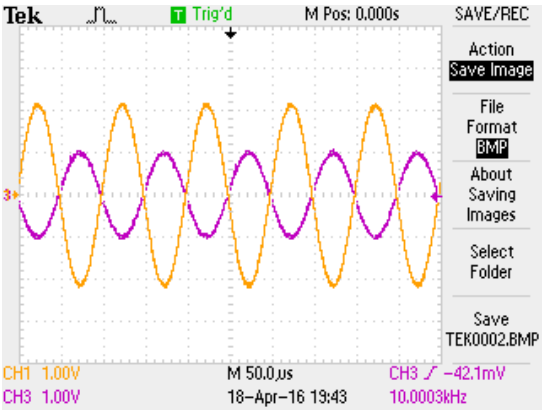

*(i)* Differential load voltage at 3MHz: approximately 7.30$V_{p\text{-}p}$ amplitude

Figure G.2: Differential Load Voltage using 2$V_{p\text{-}p}$ input at different frequencies for10kΩ loading

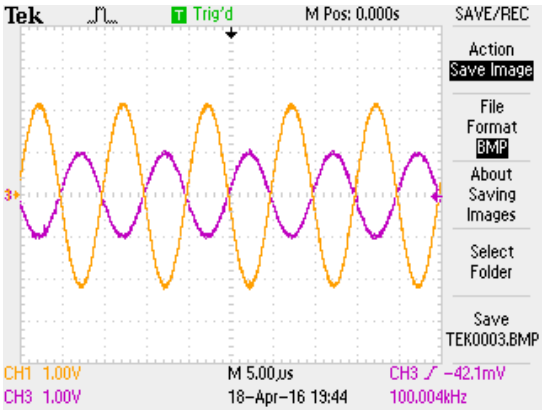
# H: GAM Circuit Performance

This appendix presents the GAM experimental result attached with a load of 2kΩ using ±36V DC power supply rails.

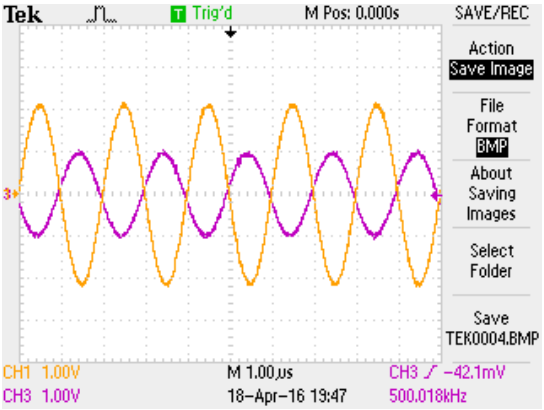
Step 1: The load voltage amplitude was measured when the CSM output was directly connected to the load (shown in Figure H.1).



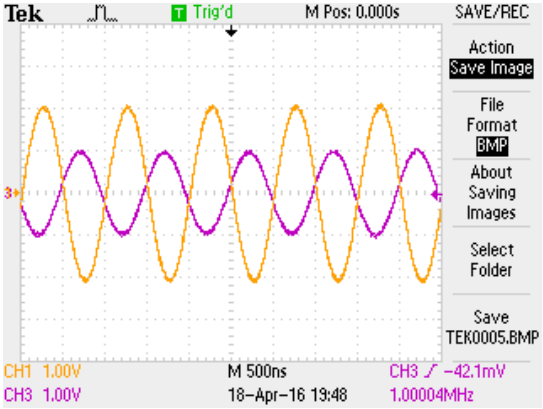

*(a)* Differential Load voltage at 10kHz: approximately 4.44$V_{p\text{-}p}$ amplitude



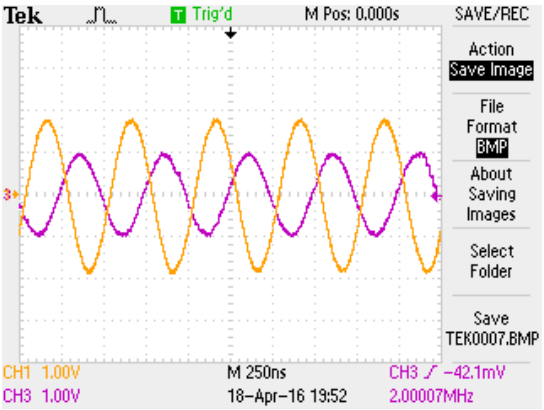

*(b)* Differential load voltage at100kHz: approximately 4.44$V_{p\text{-}p}$ amplitude



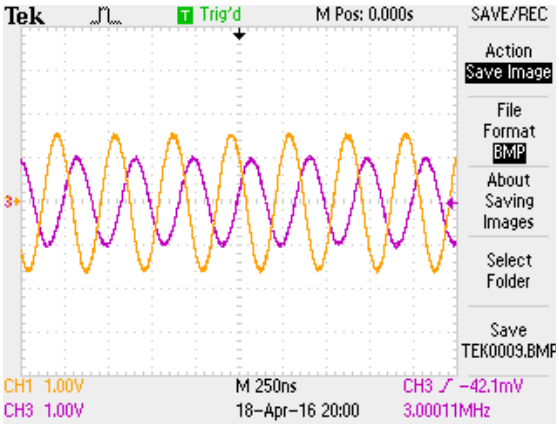

*(c)* Differential load voltage at 500kHz: approximately 4.38$V_{p\text{-}p}$ amplitude




*(d)* Differential load voltage at 1MHz: approximately 4.24$V_{p\text{-}p}$ amplitude



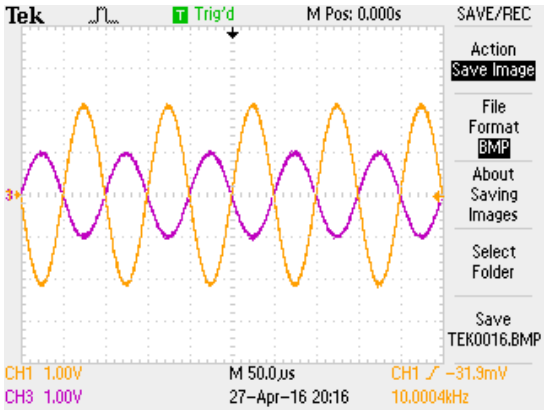

*(e)* Differential load voltage at 2MHz: approximately 3.70$V_{p\text{-}p}$ amplitude



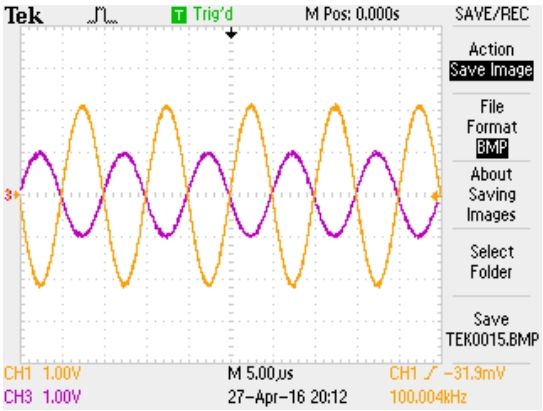

*(f)* Differential load voltage at 3MHz: approximately 3.24$V_{p\text{-}p}$ amplitude

Figure H.1: CSM Load Voltage using 2$V_{p\text{-}p}$ input at different frequencies for2kΩ loading (Step 1)

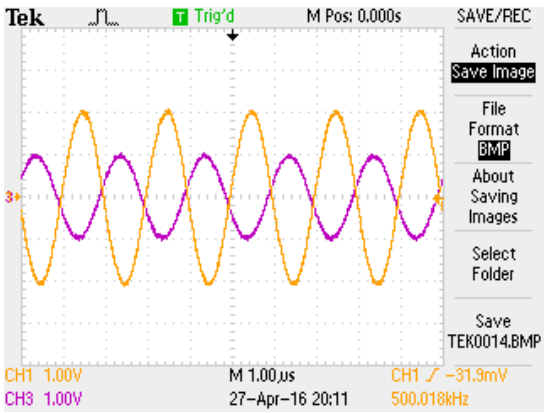
Step 2: The load voltage amplitude was measured when the CSM output was routed to the load via two MUX's (shown in Figure H.2).



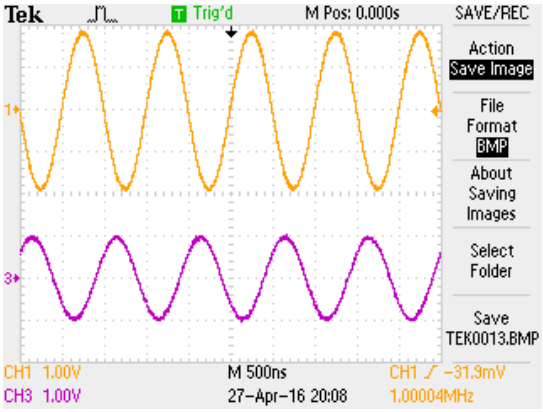

*(a)* Differential Load voltage at 10kHz: approximately 4.36$V_{p\text{-}p}$ amplitude



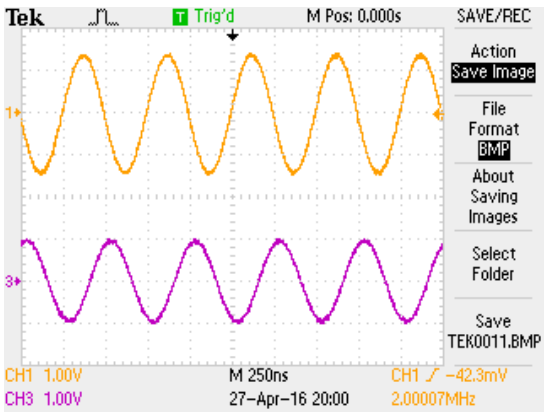

*(b)* Differential load voltage at100kHz: approximately 4.36$V_{p\text{-}p}$ amplitude



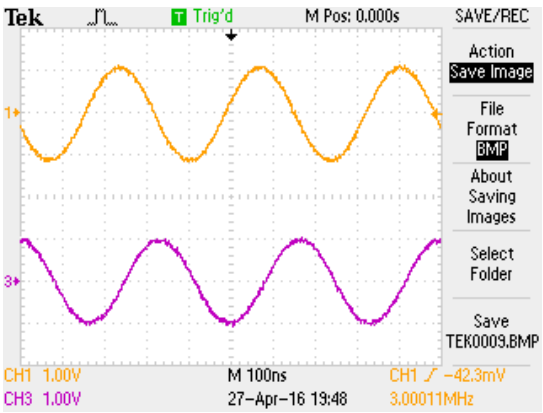

*(c)* Differential load voltage at 500kHz: approximately 4.22$V_{p\text{-}p}$ amplitude




*(d)* Differential load voltage at 1MHz: approximately 3.84$V_{p\text{-}p}$ amplitude



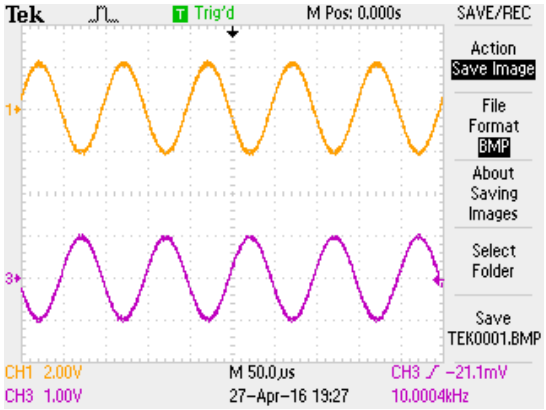

*(e)* Differential load voltage at 2MHz: approximately 2.92$V_{p\text{-}p}$ amplitude



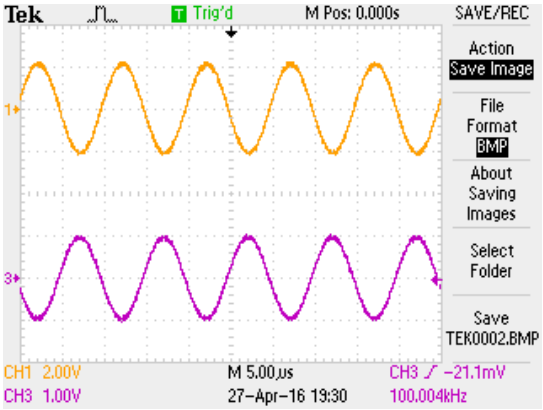

*(f)* Differential load voltage at 3MHz: approximately 2.32$V_{p\text{-}p}$ amplitude

Figure H.2: CSM Load Voltage using 2$V_{p\text{-}p}$ input at different frequencies for2kΩ loading (Step 2)

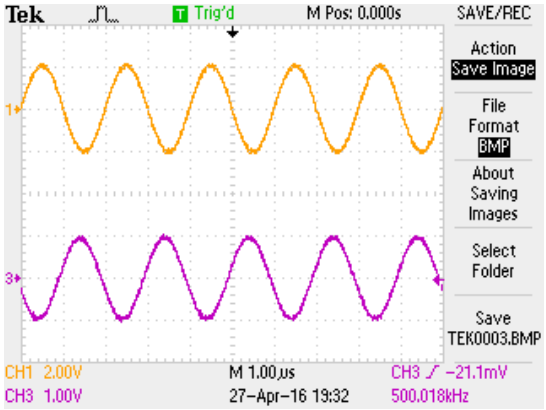
Step 3: The load voltage amplitude was measured when the CSM output was routed to the load via two MUX's along with MUX power supplies pin driven by the GAM output voltages (shown in Figure H.3).



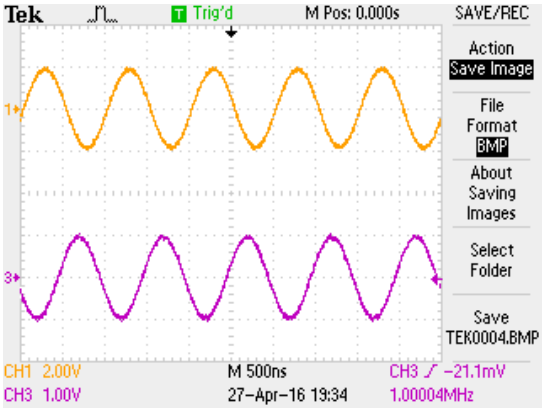

*(a)* Differential Load voltage at 10kHz: approximately 4.48$V_{p\text{-}p}$ amplitude



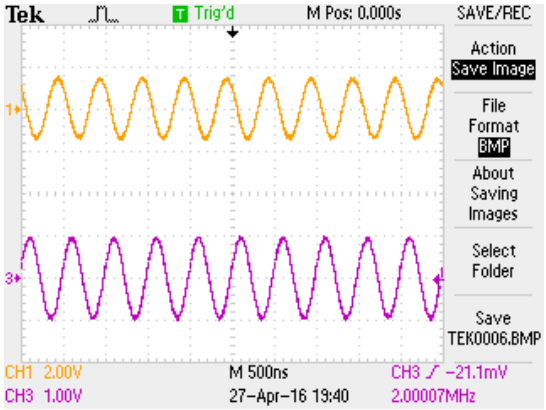

*(b)* Differential load voltage at100kHz: approximately 4.48$V_{p\text{-}p}$ amplitude



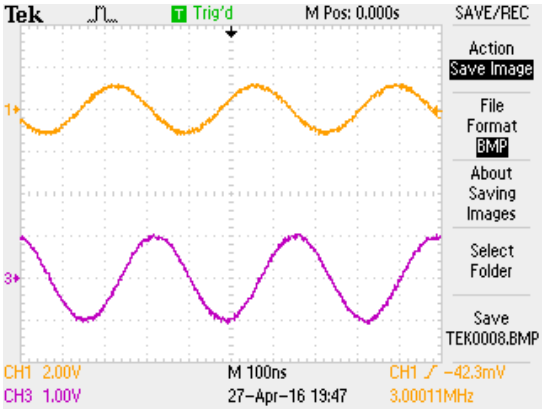

*(c)* Differential load voltage at 500kHz: approximately 4.32$V_{p\text{-}p}$ amplitude




*(d)* Differential load voltage at 1MHz: approximately 4.04$V_{p\text{-}p}$ amplitude




*(e)* Differential load voltage at 2MHz: approximately 3.04$V_{p\text{-}p}$ amplitude




*(f)* Differential load voltage at 3MHz: approximately 2.44$V_{p\text{-}p}$ amplitude

Figure H.3: CSM Load Voltage using 2$V_{p\text{-}p}$ input at different frequencies for2kΩ loading (Step 3)