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Design and Fabrication of Ion Traps for a Scalable Microwave Quantum Computer

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Declaration

I hereby declare that this thesis has not been and will not be submitted in whole or in part to another University for the award of any other degree.

Signature:

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Weikang Fan, Doctor of Philosophy

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Abstract

This thesis describes the experimental work towards the development of a scalable quantum computer based on microfabricated ion trap using long-wavelength radiation and magnetic field gradient.

There are three key elements in implementing such a quantum computer: the junction trap to shuttle ions, the structure to generate high gradient magnetic field and the structure to induce strong microwave coupling to the ions. A new dynamic simulation tool was developed addressing the problems faced by static solvers. This tool was used to aid the design and optimisation of an X junction geometry allowing the ions to be shuttled with minimised motional heating gain. The design and fabrication techniques were reported on the structure to generate a high gradient magnetic field. A discussion was given on the design of producing microwave and maximise the coupling to the cold ions. A review was given on the far-field methods and near-field methods. A novel design was reported where the single-qubit gate is predicted to be 45 times faster than a conventional setup.

Two essential topics on the microfabrication of a reliable scalable quantum computer unit were discussed: breakdown and RF loss. Investigation using numerical simulations showed that dielectric can breakdown due to high voltage and local heating which are results of impedance mismatch. Microfabrication processes were improved, high-quality films were reported to have twice as much breakdown voltages. The mechanisms of RF loss were reviewed. Novel structures and smooth electroplating technique were developed to minimise the loss. A low loss ion trap was produced and tested. An experimentally observed anomalous glow discharge phenomenon was reported and investigated.

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Contents

List of Tables

List of Figures

Chapter 1

Introduction

In 1965, Gordon Moore published his famous paper [1] describing that the number of components per integrated circuits (ICs) doubles every year, also known as Moore's law. Before the 2000s, the clock speeds of ICs grew exponentially as well, but in the early 2000s, it was stopped due to the limits of efficient cooling. To maintain the increase in computational power, the size of transistors was decreased and many other technologies including multi-core integration emerged. But eventually, the size of a single transistor will reach and terminates at its fundamental barrier, atomic levels.

One way to further meet the demand for computation power is to develop quantum computation technologies. Quantum computation, by making use of quantum mechanical properties including quantum superposition and entanglement, can speed up computations and execute quantum algorithms. A widely known algorithm was Shor's algorithm [2] which allows factoring large numbers exponentially faster than a classical algorithm, ground-shaking modern cryptosystems. Other algorithms allow the implementation of fast searches in databases [3], the simulation of other quantum systems [4, 5] and the implementation of an oracle machine [6], etc.

Based on the classical mathematical model of computation, Turing machine [7], David Deutsch [8] proposed a universal quantum computer model, also known as a quantum Turing machine. Over the past few decades, many basic quantum simulations [5,9,10] were realised and many different applications of quantum systems [11–14] were investigated. The tremendous potential of quantum computation motivated the community to develop and optimise a universal quantum simulator, a computational platform that can efficiently solve many different problems.

The quantum mechanical systems for information storage are subject to decoherence, efficient quantum error correction has to be performed to allow a fault-tolerant computation. The quantum system has to be of a large scale to meet the ever-increasing demand for computational power. To help identify the goals for developing a quantum computer (QC), D. P. DiVincenzo presented a discussion [15] summing up the requirements a system must fulfil to become a universal quantum system. The system has to be able to initiate the quantum bit (qubit) in a simple fiducial state. The decoherence time of qubits need to be longer than the gate times to allow one or multiple complete gate operations. A set of universal gates is needed for constructing any other operations. The qubits require a readout operation at its arbitrary states. Last but not least importantly, the system needs to be physically scalable with well- characterised qubits.

Many research groups have made great efforts in different fields of physics. Among them, the most promising approaches [16] are superconducting circuit quantum electrodynamics systems and trapped ions. They faced difficulties among which scalability is the most challenging one.

Google, Intel and IBM have successfully demonstrated their superconducting qubits based prototype machines with online interactive quantum algorithm composers but faces scalability problems. Google and IBM announced 53 qubits and 16 qubits superconducting quantum computing chips in 2019 [17, 18] however, due to the architecture used, only up to 4 neighbours were coupled to each qubit limiting the implementation of the algorithms, and due to intertalks between qubits, the fidelity of quantum gates are poor unless a complicated error correction algorithm is employed. The superconducting systems also require a dilute fridge and microwave amplifiers with ultralow noise to operate properly making them very expensive to be scalable.

Ion trap system meets all the required criteria and multiple scalable blueprints [19, 20] were proposed in recent years. Robust and high fidelity state preparation [21] and readout [22,23] were performed. Long coherence time [24], efficient error correction schemes [25,26] and fast universal gates [27] have been demonstrated.

Ion trap was first developed for electrodynamic mass spectrometer by W. Paul in 1953 [28] and was adapted to trap ions [29, 30] shortly after. The development of laser cooling techniques [31, 32] made high-resolution spectroscopy and study of ultracold atom collisions possible, resulting in the first experimental demonstration of a two-qubit quantum gate [33] and the first-ever theoretical work towards the realisation of large-scale ion trap

architectures [34].

Several realistic architectures [19,35] were proposed consisting of an ion trap array incorporating storage and gate regions interconnected with either photonic connections or direct ion shuttling protocols. Both architectures require the ion trap with versatile dedicated regions of functions to be fabricated on micrometre scales with high electrode geometry precision. The key to miniaturising ion traps is through the state-of-art microfabrication technologies. Methods like photolithography allow the fabrication of very large scale arrays. Multiple conductive and insulating layers of different materials can be patterned and stacked up with interconnections to create the interconnection ports required by the architectures. Wafer bonding and die bonding techniques can further integrate individual ion trap units with devices such as digital-analogue-converter, photon counter and bandpass filters.

A scalable quantum computer will require that a massive number of quantum gates be operated at the same time with individual addressing and readout. When using conventional qubit gates where the entanglement is realised by lasers interacting with the ions, the number of lasers required is substantial for a scalable quantum computer. The lasers need to be stable, precisely aligned and real-time controlled. This is challenging to realise in the engineering point of view and not practical economically. An alternative method, known as MAgnetic Gradient Induced Coupling (MAGIC) scheme, was proposed by Mintert and Wunderlich [36] in 2001 where the internal and motional dynamics of the ions are coupled using microwave radiation with an additional spatially varying magnetic field. Upon the excitation with microwave radiation, an effective Lamb Dicke parameter arises through MAGIC. The individual addressing of atoms is realised by driving the radiation field at a frequency specific for each individual ion due to the Zeeman effect.

In this thesis, the microwave ion trap quantum computer architecture proposed by B. Lekitsch [19] is followed. Very high fidelity single and two-qubit gates were realised [37] paving the way for a practical application. However, Chapter 3 reviews the challenges in realising the scalable system. The key component to the scalable quantum computer blueprint is a versatile quantum computing unit where the ions are cooled, transported, flopped and readout. This unit consists of a junction trap with multiple functional regions. The junction itself requires the ion to shuttle through with little to no motional heat gain. In Chapter 4, a junction geometry with optimal motional heat gain is delivered together with the simulation method that correctly models the RF trapping potential.

The MAGIC scheme requires a microwave field radiation delivered at the ion where a high static magnetic gradient exists. Currently, the devices and components delivering both fields are done using external horns and sources. No work has been reported on the effort to integrate them in a monolithic quantum computing unit which is essential to its scalability. In Chapter 4, methods and designs to integrate both the microwave and static magnetic fields sources are discussed. The integration of static magnetic field generation is studied, developed and demonstrated using advanced microfabrication techniques. A design with integrated microwave cavity reports a very high Rabi frequency of 45 times higher than the conventional methods.

Chapter 5 looks into the electrical breakdowns in a microfabricated ion trap. Designs and optimised fabrication processes were developed to achieve a high breakdown voltage of 1500 V_{PP} , significantly higher than its peers of typically 500 V_{PP} . Chapter 6 discusses the RF loss in an ion trap which helps researchers to design and fabricate reliable devices.

Also in this thesis, minor topics including the simulation study of failed traps which gives the community insights on how to improve the reliability of ion traps, study on the dielectric loss and impedance matching in MEMS devices and the development of the smooth electroplating technique, etc.

Chapter 2

Ion trapping with microfabricated ion traps

2.1 Paul ion trap

It has long been desired to isolate single atoms in order to study atomic properties and the interaction between atoms and light. Based on earlier developments of linear Radio Frequency (RF) quadrupole mass filters, Prof. Wolfgang Paul [38], H.P. Reinhard, U. Zahn [39] and E. Fisher [40] described a technique to confine a charged particle with specific charge-to-mass ratio.

Earnshaw's theorem [41] states that a point charge or a collection of them cannot be stably confined in local space in equilibrium solely with an electrostatic interaction of the charges. From Gauss's law, the divergence of an electric field force is zero in free space and it must satisfy Laplace's equation. This means that only saddle-shaped static potentials can be generated, as shown in Fig. 2.1. The electrostatic force produced by such an electric potential cannot maintain charges in a stable equilibrium. However, if the potential rotates with time then it leads to a net force on the charges that always points towards the centre of the saddle as shown in Fig. 2.2.

To better understand how such an electric potential is formed and how a charged particle interacts and can be trapped in such a potential, it is necessary to look at the equations of motion.

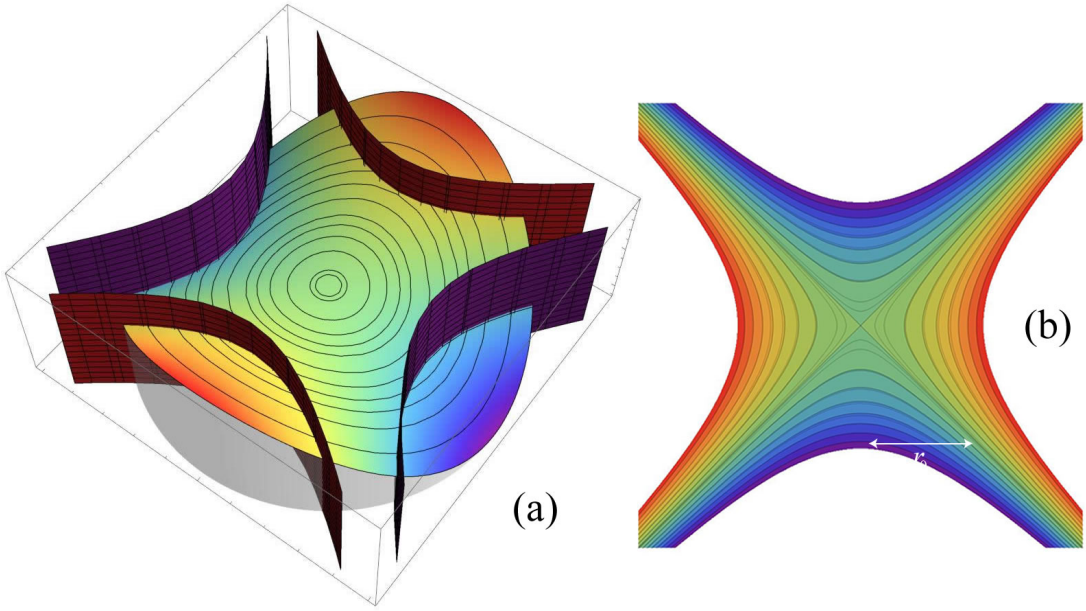

Figure 2.1: **(a)** Combined images of a set of hyperbolic shaped electrodes and the saddle potential produced when opposite plates have the same potential ϕ and obverse plates have the same potential with inverse polarity $-\phi$. **(b)** Two-dimensional static saddle potential with ion-electrode distance r_0 with stable trapping along one direction.

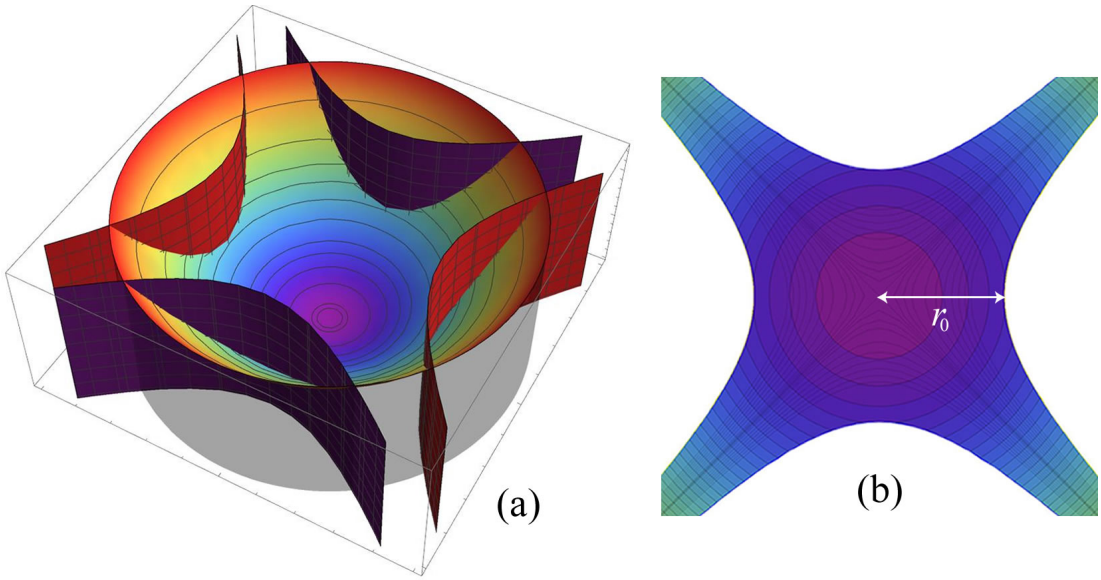

Figure 2.2: **(a)** Combined images of a set of hyperbolic shaped electrodes and the saddle potential produced when alternating potentials are applied to the electrodes. The opposite plates have the same potential ϕ and obverse plates have the same potential with 180° phase delay. **(b)** Two-dimensional time averaged saddle potential with ion-electrode distance r_0 with stable trapping along one direction.

2.1.1 Ponderomotive pseudopotential approximation

To describe the motion of the ion in a time-varying field, the average force on an ion is calculated. The equivalent field resulting from such an inhomogeneous RF field is the ponderomotive pseudopotential. Following the discussion by H.G. Dehmelt [42], the derivation is as follows.

First, consider a charged particles with a mass m and a charge e in a homogeneous electric RF field with a frequency Ω, such as that produced between the parallel plates of a capacitor. The equation of motion in this field E_h is described by

$$m\ddot{x} = eE_h\cos(\Omega t) - eE_s \tag{2.1}$$

where E_s is a result of the static voltage offset, U, and is kept at 0 in most ion trapping experiments. The solution to the equation above with E_s being 0 is gained via direct integration

$$x(t) = x_0 - a\,\cos(\Omega t) \tag{2.2}$$

where $a = eE_h/m\Omega^2$ and x_0 is the initial position of the particle.

The motion of the particle described by $x(t)$ indicates that averaged over time, there is no force is acting on the ion as it oscillates back and forth around the starting point x_0.

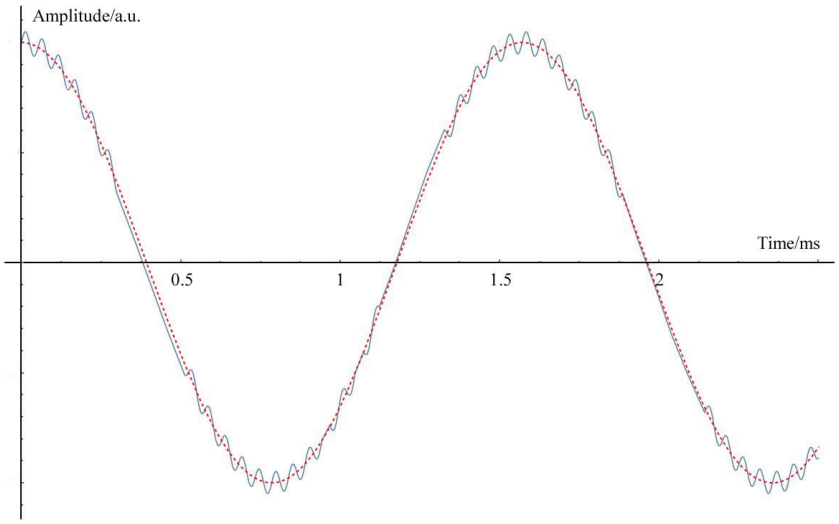

Figure 2.3: Ion motion along x axis over time. The large oscillation is carrying a higher frequency type of motion known as micromotion.

When the plates are hyperbolic, a non-zero time-averaged force acts on the particle, and the generated electric field becomes inhomogeneous $E_i(x)$. Under such conditions, the

solution to equation 2.1 is often not solved analytically but requires numerical solutions. However, in the presence of a slightly inhomogeneous field, with a few assumptions and approximations, an analytical solution can be derived.

Using the Taylor expansion on the electric field $E_i(x)$ around x_0 gives,

$$E_i(x) = E_i(x_0) + \frac{\partial E_i(x_0)}{\partial x}(x - x_0) + ... \tag{2.3}$$

Ignoring higher order terms and substituting $x(t)$ for $(x - x_0)$ gives,

$$E_i(x) = E_i(x_0) + \frac{\partial E_i(x_0)}{\partial x}(a\ \cos(\Omega t) - x_0). \tag{2.4}$$

Substituting the equation above into equation 2.1, gives an equation describing the force acting upon the particle

$$m\ddot{x}(t) = eE_i(x_0)\cos(\Omega t) - e\ \cos(\Omega t)(a\frac{\partial E_i(x_0)}{\partial x}\cos(\Omega t) - x_0). \tag{2.5}$$

Assuming that the motion of the ion is local, the amplitude of motion $a = eE_i(x)/m\Omega^2$ can be replaced by $a(x_0) = eE_i(x_0)/m\Omega^2$. Averaging both sides of equation 2.5,

$$\langle m\ddot{x}\rangle = -\frac{1}{2}ea(x_0)\frac{\partial E_i(x_0)}{\partial x} \tag{2.6}$$

which can be further simplified to give

$$\langle m\ddot{x}\rangle = -\frac{e^2}{4m\Omega^2}\frac{\partial E_i^2}{\partial x}. \tag{2.7}$$

By substituting $\Phi = e^2E_i^2/4m\Omega^2$, the equation becomes

$$\langle m\ddot{x}\rangle = -\frac{\partial \phi(x_0)}{\partial x}. \tag{2.8}$$

Such an equation describes a force $F = m\ddot{x}$ arising from the alternating inhomogeneous electric field E_i whose direction is determined by the gradient $\partial E_i^2/\partial x$. The time independent potential $\Phi(x_0)$ is the effective electric potential describing the time-averaged ion motion in the electric field E_i. Such a potential is called a pseudopotential in which the ion motion can be approximated as a secular harmonic motion. The secular frequency of

the ion is then

$$\omega_s = \sqrt{\frac{e^2}{4m\Omega^2}\frac{\partial^2|\nabla E_i|^2}{\partial x^2}}. \tag{2.9}$$

Furthermore, this solution can be generalised to three dimensions.

2.1.2 Mathieu equations and stability parameters

Whilst the ponderomotive pseudopotential gives an approximated description, a full description of the ion can be found which includes both secular and micromotion of the ion.

Given a quadrupole trap with ion-electrode separation r_0 and applied potential φ_0, the free space potential can be described by

$$\varphi = \frac{\varphi_0}{2r_0^2}(\lambda x^2 + \sigma y^2 + \gamma z^2) \tag{2.10}$$

where λ, σ and γ are constants set by the geometry of the electrodes and which satisfies $\lambda + \sigma + \gamma = 0$ and $\nabla^2\varphi = 0$ as required.

To simplify calculations, set $\lambda = 1$, $\sigma = -1$ and $\gamma = 0$. This gives us a two-dimensional inhomogeneous hyperbolic potential:

$$\varphi = \frac{\varphi_0}{2r_0^2}(x^2 - y^2). \tag{2.11}$$

The applied potential can be written as $\varphi_0 = U + V\cos(\Omega t)$ where V is the RF voltage amplitude, U the static offset, and Ω the drive frequency. Since the movement of the ion in different directions is uncoupled, decouple the equation and rewrite it into

$$\ddot{x} + \frac{e}{mr_0^2}(U - V\cos(\Omega t))x = 0 \tag{2.12}$$

and

$$\ddot{y} + \frac{e}{mr_0^2}(U - V\cos(\Omega t))y = 0. \tag{2.13}$$

By substituting $a = 4eU/mr_0^2\Omega^2$, $q = 4eV/mr_0^2\Omega^2$ and $\epsilon = \Omega t/2$,

$$\frac{\mathrm{d}^2x}{\mathrm{d}\epsilon^2} + (a - 2q\cos(2\epsilon))x = 0 \tag{2.14}$$

and

$$\frac{\mathrm{d}^2 y}{\mathrm{d}\epsilon^2} + (a - 2q\cos(2\epsilon))y = 0 \tag{2.15}$$

They are uncoupled linear second order differential equations with a periodic coefficient $\cos(2\epsilon)$ which fall into the category of Mathieu equations. The general solution to Mathieu equations were found to be classified in two cases, the first type has the following term:

$$r_{\pm}(t) = e^{\mu t}\phi(t) \pm e^{-\mu t}\phi(-t) \tag{2.16}$$

where two periodicity exponent are present. The Floquet theorem can be used to obtain this type of solution.

The second solution type, however, takes a non-periodic form:

$$r_2(t) = \pi r_2(\pi) t r_1(t) + u(t) \tag{2.17}$$

where $r_1(t)$ is a periodic solution of the first type, and $u(t)$ is a periodic function with period π. Solutions of this type are not stable as there are a non-linear term $tr_1(t)$.

The Mathieu equations have an infinite number of solutions, only part of which are stable periodic solutions. To trap an ion, a stable solution is required.

Fig. 2.4 shows the stable solutions mapped on a stability diagram against parameters a and q. By assuming that the ion travels freely in the z direction, then, for the ion to remain stable the a and q parameters must fall within the stable region on both x and y stability diagram.

The solution to Mathieu equations is given by [43]

$$u(t) = A\cos(\omega t + \phi_i)(1 + \frac{q}{2}\cos(\Omega t) + \frac{q^2}{32}\cos(2\Omega t)) + A\frac{q}{2}\sin(\omega t + \phi)\sin(\omega t) \tag{2.18}$$

where $u(t)$ is either $x(t)$ or $y(t)$, A is a constant depending on initial conditions and $\omega = \beta\Omega/2$ where $\beta \sim \sqrt{a + q^2/2}$.

This shows that the ion motion has two distinct frequencies, the secular and the micromotion. The ion oscillates around the starting point at its secular frequency ω and is superimposed with a micromotion of RF drive frequency Ω.

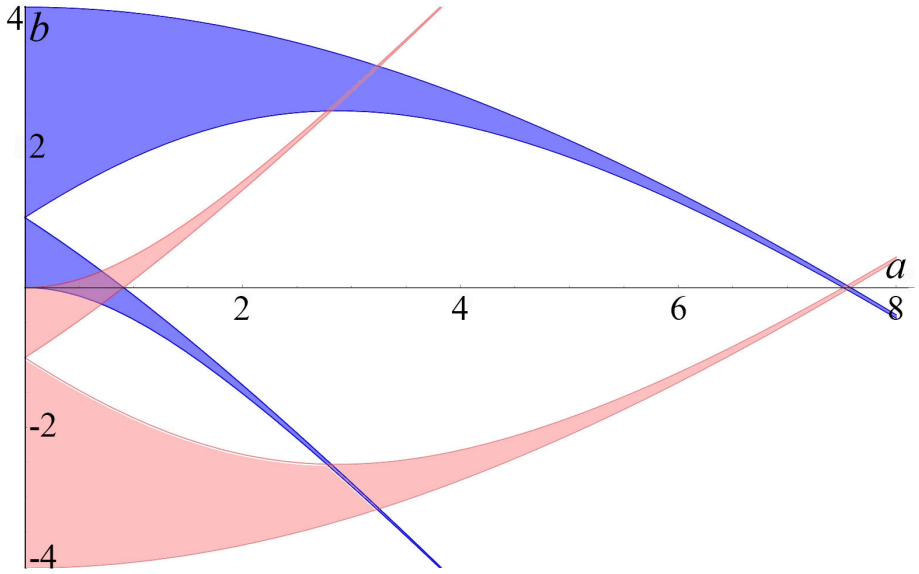

Figure 2.4: Mathieu stability diagram. The blue and red areas represent motions that are stable along the x-axis and y-axis respectively.

2.2 Analytical description of the trapping potential

So far the ion motion in an alternating field is discussed. To generate the alternating field, W. Paul [38] invented what is known as the quadrupole ion trap which is consisted of four hyperbolic electrodes with different polarities on opposite electrodes. Linear ion trap is formed by replacing the electrodes with a set of quadrupole rods to confine the ions radially and a static electrical potential on end electrodes to confine ions axially, first demonstrated by D.A. Church [44]. Linear ion traps offered an increased ion storage capacity and simpler construction. The electric field in such geometries is described by multipole expansion.

To further make ion traps compact hence suitable for quantum information processing, planar ion traps or surface traps, are created by unfolding the electrodes of a linear ion trap on a plane. The electric field generated by the unfolded electrodes cannot be described by multipole expansion. In this section, approximations are made such that the electric field produced by a surface ion trap can be described analytically. Mathieu equations in surface traps are modified due to the inhomogeneity of the RF field generated by the geometry.

2.2.1 Analytical approach for modelling electric fields in a surface trap

The first approximation is that the electrodes occupy the entire surface, which means that the electrodes may extend infinitely in the plane, and the gaps between different electrodes

are infinitely small. This approximation holds only when the gaps are much smaller than the electrode sizes which often is fulfilled in a microfabricated ion trap. For example, a typical gap size in a chip used in this group is 5 µm which when compared to a typical electrode size of ~ 200 µm is very small.

The second approximation is that all electrodes are rectangular. A non-rectangular electrode can be subdivided into smaller elements, but this is not necessary as complicated geometries were often numerically simulated.

The third approximation is that the RF field can be seen as an electrostatic field in an ion trap. This is possible as a typical ion trap will operate with an RF field of $1 \sim 100$ MHz, and therefore a minimum wavelength of 3×10^6 µm, which is far larger than the length of the electrode which is $10 \sim 100 \times 10^3$ µm. This allows us to use analytical approaches based on electrostatic fields at a cost of not detailing the micromotion.

The electrostatic potential of a rectangular electrode of arbitrary size was derived by M.G. House [45]. Given a rectangular electrode of width $x_2 - x_1$ and height $y_2 - y_1$ with voltage U applied, the electrostatic potential generated is

$$\begin{aligned}\phi(x,y,z) &= \frac{U}{2\pi}\Big(\arctan\Big(\frac{(x_2-x)(y_2-y)}{z\sqrt{z^2+(x_2-x)^2+(y_2-y)^2}}\Big)\\ &\quad - \arctan\Big(\frac{(x_1-x)(y_2-y)}{z\sqrt{z^2+(x_1-x)^2+(y_2-y)^2}}\Big)\\ &\quad - \arctan\Big(\frac{(x_2-x)(y_1-y)}{z\sqrt{z^2+(x_2-x)^2+(y_1-y)^2}}\Big)\\ &\quad + \arctan\Big(\frac{(x_1-x)(y_1-y)}{z\sqrt{z^2+(x_1-x)^2+(y_1-y)^2}}\Big)\Big)\end{aligned} \tag{2.19}$$

To acquire a solution for the entire electrode geometry, simply sum up all individual electrode potentials since electrostatic fields are linearly additive in free space.

The electric potential can be expressed as a volume integral minus surface integral by solving Laplace's equation with Dirichlet boundary condition

$$\phi(x) = \frac{1}{4\pi\epsilon_0}\int_V \rho(x')G(x,x')\mathrm{d}^3x' - \frac{1}{4\pi}\oint_V \phi(x',y',z')\frac{\partial G(x-x',y-y',z)}{\partial n'}\mathrm{d}a \tag{2.20}$$

where G is Green's function, a is a unit area and n' the surface normal. Since Laplace's equation is satisfied in vacuum, $\rho(x') = 0$, only the second term remains. With the surface potential $\varphi(x,y) = \phi(x,y,0)$ and Green's function [46]

$$G(x,y,z) = \frac{|z|}{2\pi(x^2+y^2+z^2)^{3/2}}, \tag{2.21}$$

Based on the approximations of infinite electrodes and no gaps, the electric potential over the entire space can be calculated once $\varphi(x, y)$ is known. This is known as basis function technique or Green function method. It will be used again in the numerical simulations described later in this thesis.

With a typical ion trap geometry shown in Fig. 2.5. The motion of a trapped ion is confined by two categories of electrodes. The static electric potential from the DC electrodes dictates the ion's position in the imaginary plane parallel to the trap surface. The time-varying potential emitted from the RF electrodes confines the ion along the line perpendicular to the trap surface. The height above the electrode surface at which an ion is trapped is at the minimum of the RF potential. This height is known as the trapped ion height. The height of the ion is an important parameter in experiments. The ion suffers from heating and the heating effect is dependent on the ion-electrode distance [47–50]. The lasers need to be aligned to avoid shining on the electrode surfaces but centred at the ion for the maximum intensity. When an ion travels vertically beyond the escaping point z_e, the electric potential can no longer pull the ion back.

The trapping and escaping positions, as well as the ion height above the trap surface, are studied using the assumptions discussed above. The trapped ion's position is

$$(\frac{ac}{b+c}, 0, \frac{\sqrt{abc(a+b+c)}}{b+c}). \tag{2.22}$$

The escaping position is

$$(\frac{ac}{b+c}, 0, \sqrt{2ab+a^2+2(a+b)\sqrt{2ab+a^2/2}}). \tag{2.23}$$

The trap depth is defined as the difference in potential between the trapping position and escaping position

$$\Xi = \frac{e^2V^2\kappa}{\pi^2 m\Omega^2 h^2} \tag{2.24}$$

where $h = \sqrt{abc(a+b+c)/(b+c)}$ and $\kappa = 2\sqrt{abc(a+b+c)}/((2a+b+c)(2a+b+c+2\sqrt{a(a+b+c)}))$.

A surface trap, compared to a linear quadrupole trap, has a much lower trap depth. For symmetric RF electrodes, $b = c$, maximum depth can be achieved given a constant ion height h when $b/a = 3.7$. However, such a ratio gives rise to large RF rail separation and leads to a higher RF rail capacitance which is not always desired as it becomes hard to

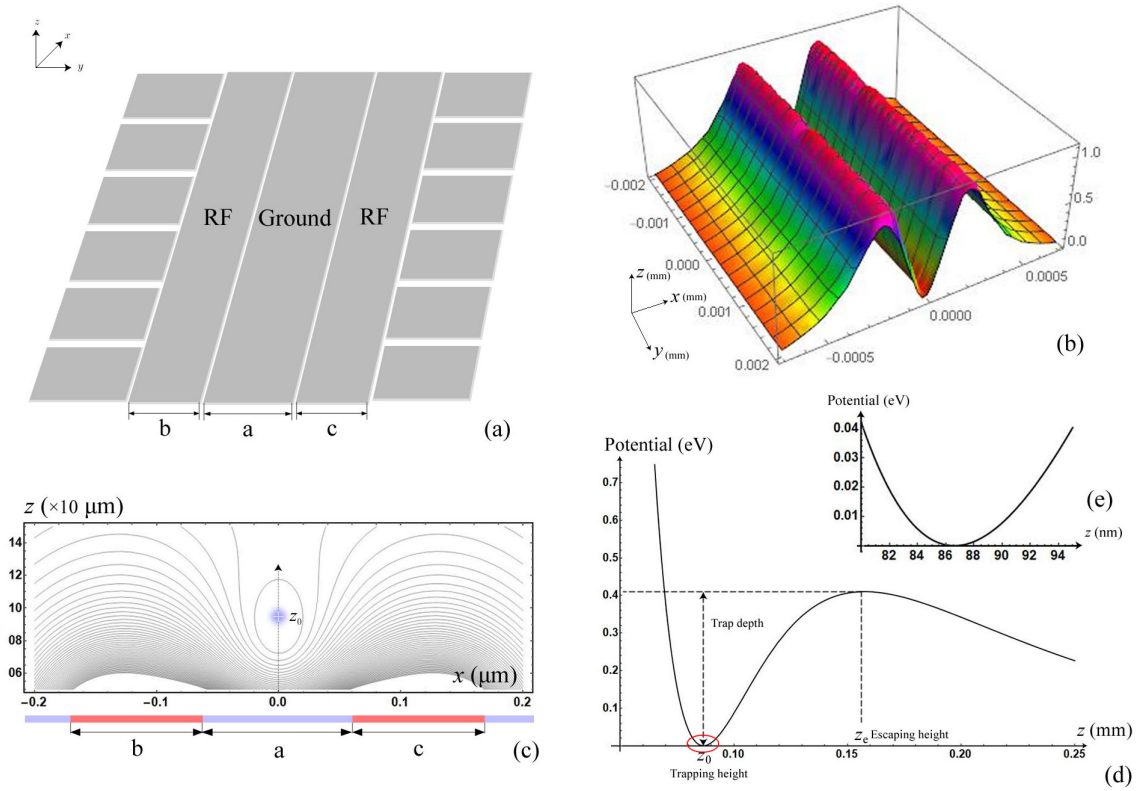

Figure 2.5: **(a)** A typical surface trap electrode geometry, with RF electrodes of width b, c and central ground electrode of width a. The small segmented electrodes on both sides are DC electrodes which are also ground to RF signals. The RF and central ground electrodes extend to infinity along the $\pm x$ axis and the DC electrodes extend to infinity along the $\pm y$ axis. **(b)** 3D representation of an equipotential surface of the pseudopotential produced by the trap described in (a) with an arbitrary RF frequency and voltage. **(c)** Field contour plot of the trapping field with $y = 0$ in x-z plane. The coloured blocks below show the dimension of the electrodes and the blue area with a white cross marks the trapping position. **(d)** Plot of trapping potential along z axis with $x = 0, y = 0$. Ion height, escaping height and trap depth are marked. **(e)** A zoom-in view of the trapping potential near the ion height along z axis shows that locally it is very similar to a harmonic potential.

drive an RF resonator. RF resonators are built to supply low-noise high voltage onto RF rails. A. Nizamani *et al.* [51] presented a detailed discussion on how trapping potential changes with geometry. They outlined what values of the ratio b/a should be used for different applications such as long trapping time and better control over an ion shuttling process.

Besides trap depth, ion height and secular frequencies, the angle between the principal axis of the trapping potential and the trap surface normal needs to be investigated as they are critical in laser cooling. Principal axes are the axes of secular motion of the ion in the trap. For example, with symmetric electrodes, normal and parallel to the trap surface are principal axes.

To cool all uncoupled ion motions, a component of the laser cooling beam has to present on each axis of the motion. Cooling beams are usually parallel to the trap surface to avoid scattering photons from the trap surface. There is no component of the beam in the axis normal to the trap surface. Therefore rotation of the potential in this principal axis is required so that all axes of motions can be cooled.

There are two ways of rotating, first, one can use asymmetric RF rails to make the pseudopotential asymmetric as shown in Fig. 2.6, or, by applying a DC quadrupole potential which combines with the RF quadrupole. By varying the DC voltages, arbitrary rotation can be achieved.

To calculate the exact rotation angle, the Hessian matrix $\mathcal{H}$ for a given pseudopotential ϕ is introduced:

$$\mathcal{H}(\phi(x,z)) = \begin{bmatrix} \frac{\partial^2\phi}{\partial^2 x}(x_0,z_0) & \frac{\partial^2\phi}{\partial x\partial z}(x_0,z_0) \\ \frac{\partial^2\phi}{\partial x\partial z}(x_0,z_0) & \frac{\partial^2\phi}{\partial^2 x}(x_0,z_0) \end{bmatrix} \tag{2.25}$$

where (x_0, z_0) is the minimum potential position.

The Hessian matrix describes the potential curvature at the RF minimum (also known as RF nil) position where the ion sits. Locally, the pondermotive potential is a quadratic with a form $F(x,z) = ax^2 + bxz + z^2$, where a, b and c are constants. When axes of motion lay along x and z, $b = 0$. The eigenvectors represent the trap principal axes. The eigenvalues λ_i give the curvature of the field in the direction of the corresponding eigenvector $\boldsymbol{e}_i$. Since the Hessian matrix is a real symmetric matrix, the eigenvectors are orthogonal to each other and aligned with the principal axes of motion [52]. The secular motion frequency ω_i can be calculated from the eigenvalues by [52]

$$\omega_i = \sqrt{\frac{m}{\lambda_i}}. \tag{2.26}$$

Angle α between the surface normal $\boldsymbol{n}$ and the eigenvector $\boldsymbol{e}_i$ which is known as the principal axis rotation angle is calculated by the dot product of the two vectors

$$\cos\alpha = \frac{\boldsymbol{n}\dot{\boldsymbol{e}}_i}{\|\boldsymbol{n}\|\|\boldsymbol{e}_i\|} \tag{2.27}$$

For example, in the trap described by Fig. 2.5, the RF electrodes are symmetric, resulting in a quadrupole potential of the form $F(x,z) = ax^2 + cz^2$. The Hessian matrix of $F(x,z)$

is

$$\begin{pmatrix} 2a & 0 \\ 0 & 2c \end{pmatrix}. \tag{2.28}$$

The eigenvectors of this matrix are

$$\begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix}. \tag{2.29}$$

The angle of rotation is $\alpha = \arccos 1 = 0$.

Assume that the pseudopotential is $F(x, z) = x^2 + 0.5xz + z^2$, the Hessian matrix is

$$\begin{pmatrix} 2 & 0.5 \\ 0.5 & 2 \end{pmatrix}. \tag{2.30}$$

Calculating the eigenvectors will give

$$\begin{pmatrix} 1/\sqrt{2} & 1/\sqrt{2} \\ -1/\sqrt{2} & 1/\sqrt{2} \end{pmatrix}. \tag{2.31}$$

The angle of rotation is found $\alpha = \arccos(1/\sqrt{2}) = 45°$. In practice, researchers do not try to find the quadratic at the centre of the trap. Instead, they find the Hessian matrix of the simulated pseudopotential (represented by an interpolated function) at the centre of the trap. The calculated rotation angle indicates the principal axes.

2.2.2 Inhomogeneous RF field

In the discussion above, the local potential is assumed to be quadratic. However, in a surface trap, the potential very quickly becomes near exponential below the trapping height along z axis as shown in Fig. 2.7.

In a non-harmonic potential, the electric field is no longer homogeneous, as discussed in section 2.1, a charged particle will no longer maintain a stable position but follows a trajectory towards an electrode. In an ion trap, the possible instability caused by this trajectory is highly undesired.

To describe the inhomogeneous RF field produced by a surface ion trap, the surface trap

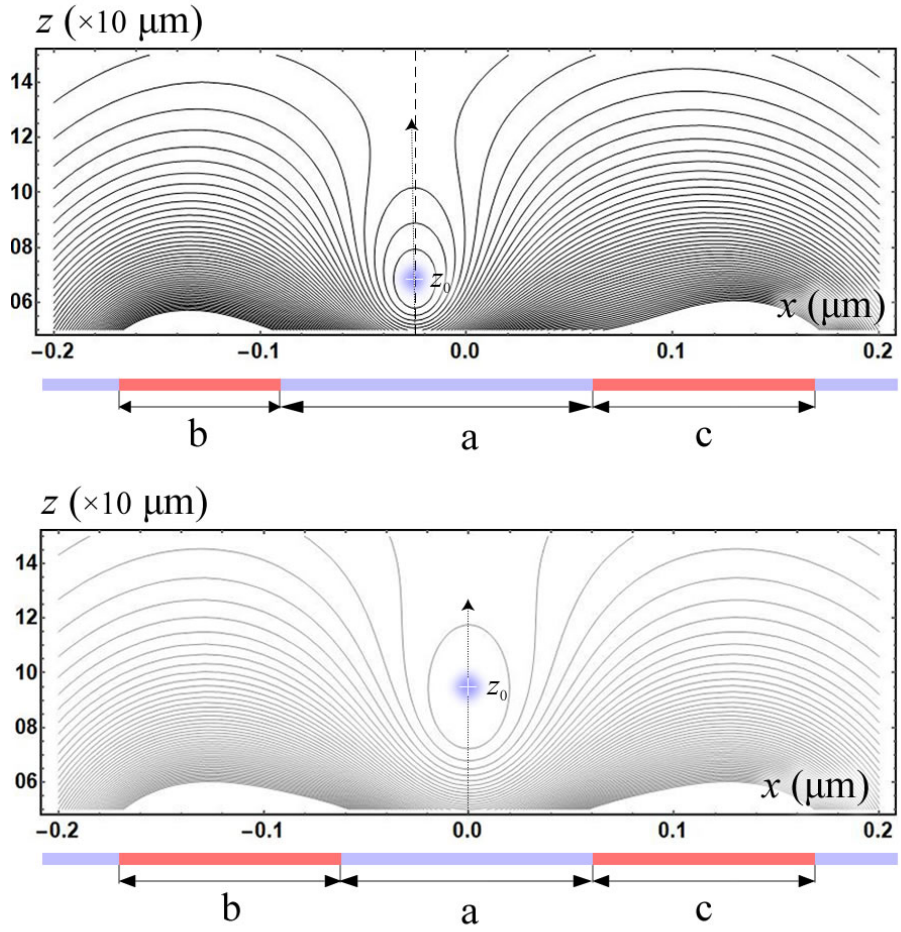

Figure 2.6: The principal axes are rotated by decreasing the width of one of the RF rails. Dotted lines with arrowheads show the principal axes, dashed lines shows the norm of the surface.

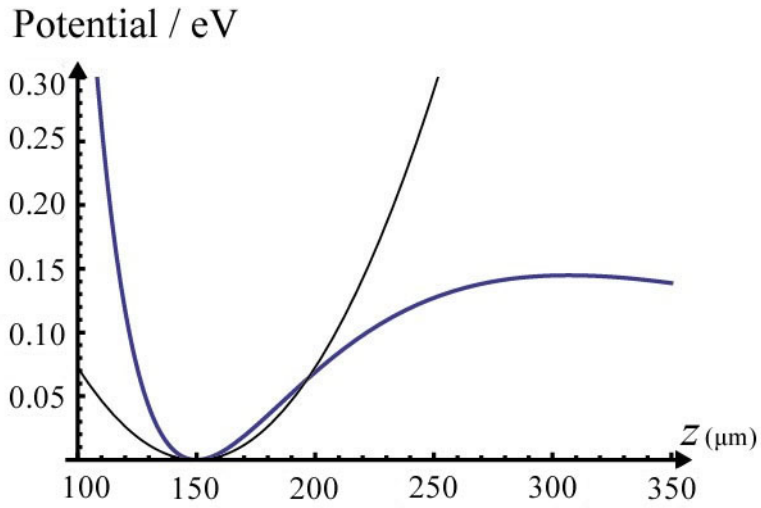

Figure 2.7: Fitting an harmonic potential to a surface trap potential.

field potential is compared with a perfectly homogeneous field. It can be quantified using the adiabaticity parameter θ which is dependent on the gradient of the electric field, the mass of the ion and the RF driving frequency [53]:

$$\theta = \frac{2e\,|\nabla E(x,y,z)|}{m\Omega^2}. \tag{2.32}$$

In a perfectly homogeneous field, $\theta = 0$. In a quadrupole trap, it is a none-zone constant. However, in a given surface trap with constant RF source parameters and ion mass, it is a function of spatial position (x, y, z).

As discussed above, at RF nil (x_0, z_0), the potential is a perfect quadratic. The adiabaticity parameter is normalised, $\theta_i(x,z) = \theta(x,z)/\theta(x_0,z_0)$ so that θ_i describes how inhomogeneous the field is compared to a quadratic field. $\theta_i(x_0,z_0)$ is defined as the inhomogeneity parameter.

As discussed earlier, the trap is stable only if the combination of the Mathieu stability parameters a and q are within certain regions in the Mathieu stability diagram (Fig. 2.4). The Mathieu stability diagram describes the motion of ions in a quadratic field. The trapping field is no longer quadratic in a surface trap, a new set of parameters is needed to describe the stability of trapped ions. Inspired by D. Gerlich [53], the Mathieu stability parameters in a none-quadratic field can be 'mapped' to these in a quadratic field using conformal mapping technique[1]. The relationship between the corrected q value or mapped q value in an inhomogeneous (none-quadratic) field q_c and that in a quadratic q_quad is [53]

$$q_\mathrm{c}(x,z) = \theta_i(x,z) q_\mathrm{quad}. \tag{2.33}$$

z_min is introduced where this height is below the ion height along the z axis and the potential at this height has the same potential as the escaping height as marked in Fig. 2.8. The ion becomes unstable at this height if the deviation from a perfect quadruple field is too large. It has been shown both theoretically [51, 53] and experimentally [54] that ion trajectories become unstable when $q_\mathrm{c}(x_0,z_0)$ or $q_\mathrm{c}(x_0,z_0) > 0.4$.

When designing an ion trap, it is important that the $q_\mathrm{c}(x_0, z_\mathrm{min})$ and $q_\mathrm{c}(x_0,z_0)$ remains below 0.4. By varying the widths of RF electrodes and the ground electrodes, fields with different degrees of inhomogeneity are produced.

[1] Conformal mapping is a mathematical transformation where a function is transformed to a target function preserving the angles between any directed curves.

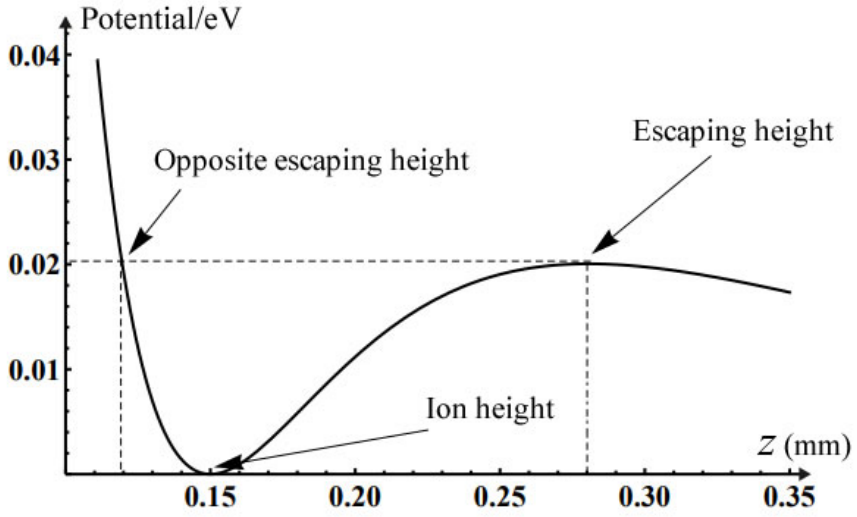

Figure 2.8: Potential along z axis in a surface trap with 150 μm ion height.

In a symmetric ion trap design, the ratio of the RF electrode width w_{RF} to the spacing between the RF rails w_{GND} is:

$$\mathcal{A} = w_{\mathrm{RF}}/w_{\mathrm{GND}}. \tag{2.34}$$

In Fig. 2.9 the inhomogeneity parameter and trap depth are plotted as a function of $\mathcal{A}$ at a fixed ion height and both are seen to increase with increasing $\mathcal{A}$. Typically $\mathcal{A} = 1.5$ is an ideal compromise between trap depth, inhomogeneity and large capacitance that comes with a small $\mathcal{A}$.

In an asymmetric ion trap design, the ratio between the width of the two RF electrodes β is introduced, $\beta < 1$. Given a constant ion height and RF spacing, by changing β it is found that the field produced becomes very inhomogeneous as β approaches 0 as shown in Fig. 2.10.

Using equation 2.22, the electrode widths of an ion trap given a specific ion height are produced. When $\mathcal{A}$ and β are fixed, the inhomogeneity parameter $\theta_i(x_0, z_0)$ stays almost constant as can be seen in Fig. 2.11.

Based on the discussion above, an optimised geometry can be found for a given ion height. For example, for an ion height of 150 μm, $V_{\mathrm{RF}} = 220$ Vpp [2]is desired. It is required to work at 20 MHz, it is aimed to deliver a geometry whose trap depth is higher than 0.1 eV and $q_c < 0.386$. A set of Mathematica scripts[3] was written to automatically search

[2]Vpp stands for peak to peak voltage in volts. In this thesis, Vpp rather than root-mean-squared voltage is used for all breakdown voltages.

[3]Available on https://github.com/ww9980/IonTrapNotebooks.

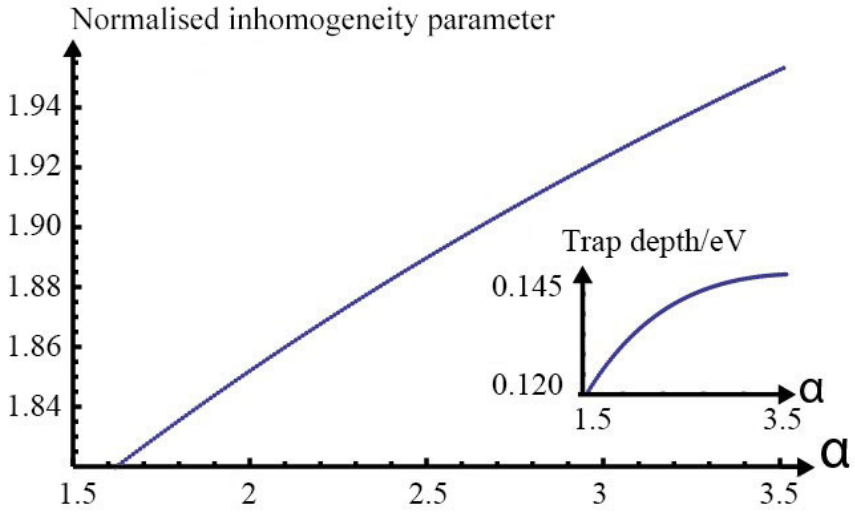

Figure 2.9: Normalised inhomogeneity parameter with different $\mathcal{A}$. Inset: trap depth with different $\mathcal{A}$.

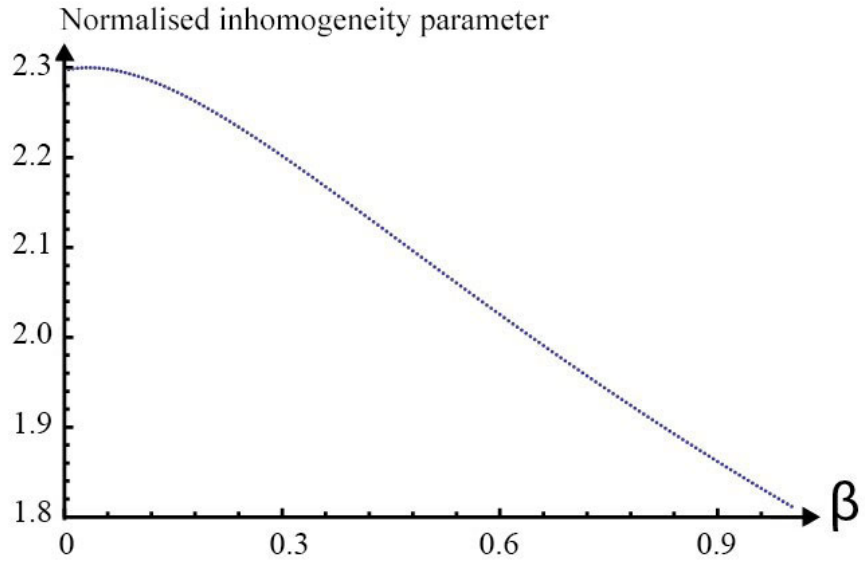

Figure 2.10: Normalised inhomogeneity parameter with different β.

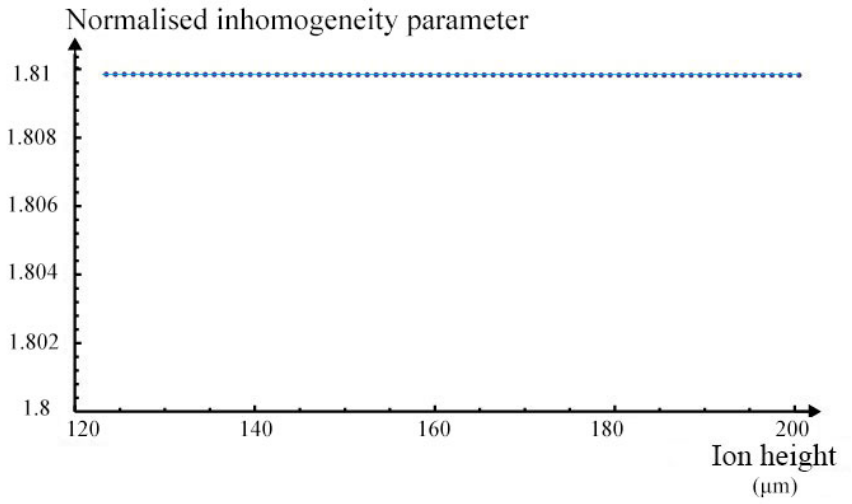

Figure 2.11: Normalised inhomogeneity parameter with different ion height with fixed α and β. The change in inhomogeneity parameter is less than 0.0001 in the range from 120 μm to 200 μm ion height.

for optimised geometries with maximum trap depth based on these inputs. The script demonstrates a trap geometry of 150 μm ion height, 0.1383 eV trap depth, 1.508 MHz secular frequency and $q_c = 0.386$, $q_{\text{quad}} = 0.213$ at a driving frequency 20 MHz.

2.3 Manipulation of motional states of trapped ions

As discussed, the local potential can be approximated by a harmonic potential well for ions with low motional energy. Therefore, the motion of an uncoupled ion along a single axis of motion is described by a one-dimensional quantum harmonic oscillator. The Hamiltonian of such an oscillator is

$$H = \hbar\omega(a^\dagger a + \frac{1}{2}) = \hbar\omega(N + \frac{1}{2}) \tag{2.35}$$

where ω is the secular frequency along this axis, $a^\dagger$ and a are operators which raise and lower the motional state of the ion respectively, $a^\dagger |n\rangle = \sqrt{n+1}\,|n+1\rangle$, $a\,|n\rangle = \sqrt{n}\,|n-1\rangle$, and N denotes the total motional quanta of an ion. Thus, when an ion absorbs a motional phonon with kinetic energy $\hbar\omega$ it moves up one motional level.

The mechanism of lowering motional quanta is known as cooling as the ion loses motional energy. Doppler laser cooling is the most commonly known cooling technique. It is remarkable because a hot ion (for example, at room temperature) can be cooled to μK in microseconds which is on the order of 10^5 times gravity acceleration constant.

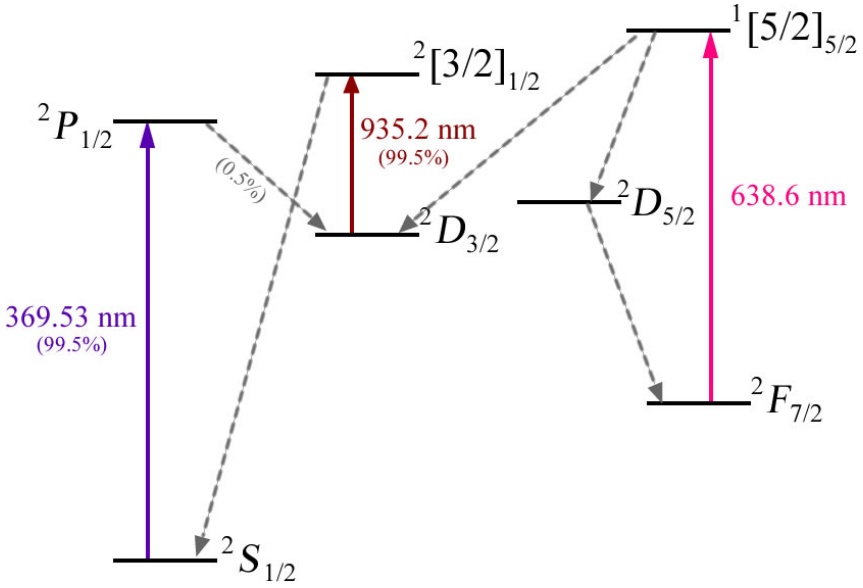

Figure 2.12: Relevant internal states of $^{174}Yb^+$ Doppler cooling. Laser-driven dipole transitions are shown as solid lines with the corresponding wavelength and the decays shown as dashed lines with branching ratios. The main cooling cycle is the $^2S_{1/2}$ to $^2P_{1/2}$ transition. The 638 nm laser repopulates the ions that are in $^2F_{7/2}$ state due to background gas collisions back into the cooling cycle. This laser is not critical especially in a cryogenic system where the chance of collisions is negligible.

A semi-classic description of laser cooling is based on the momentum transfer of photons to the ion [55]. Assuming that a two-level system with a dipole transition frequency ν_{dipole}. The decay time τ is on the order of 10^{-6}s. The cooling laser has a frequency of ν_{laser}. When an ion moves towards the laser source, the ion can only absorb photons which are red detuned from the resonance of the transition of the atom due to Doppler effect. So the laser needs to be at a frequency of $\nu_{\text{laser}} = \nu_{\text{dipole}} + \Delta\nu$ where $\Delta\nu$ is the detune frequency due to Doppler effect. When the ion absorbs a photon, it goes from lower to upper state gaining the photon's momentum p. The upper state will decay due to spontaneous emission after time τ. A photon in an arbitrary direction will be released during the process resulting in a loss of momentum in that direction. Due to the isotropic nature of the random scattering, the average momentum transfer over time is zero. The relevant internal states and laser-driven transitions are shown in Fig. 2.12 and this process is described in Fig. 2.13.

The minimum motional temperature achievable by Doppler cooling is the Doppler temperature T_D:

$$k_B T_D = \frac{\hbar\Gamma}{2} \tag{2.36}$$

where $\Gamma = 1/\tau$ is the decay rate.

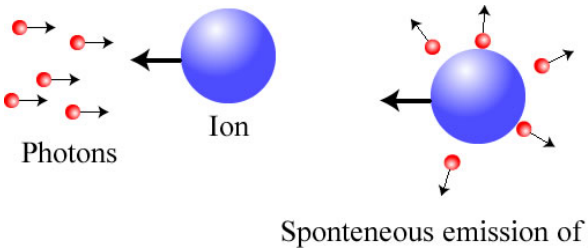

Figure 2.13: The cooling process of an ion due to the photons of a Doppler cooling laser.

Further cooling techniques on Yb^+ ion below Doppler temperature include side-band cooling [56] and Sisyphus cooling [57].

The ion gains motional energy during periods without cooling, this is known as motional heating. Coherent quantum manipulations and operations can only be performed if the heating is efficiently removed by cooling lasers.

The increase in motional quanta $\mathrm{d}N/\mathrm{d}t$ is described by electric field noise power spectral density $S_E(\omega)$ using perturbation theory [48, 58]:

$$\frac{\mathrm{d}N}{\mathrm{d}t} = \frac{q^2}{4m\hbar\omega}(S_E(\omega) + \frac{\omega^2}{2\Omega^2}S_E(\Omega \pm \omega)) \tag{2.37}$$

where the second term with $S_E(\Omega \pm \omega)$ is caused by the perturbations of the RF source.

The electrical noise $S_E(\omega)$ at frequency ω consists of several parts:

$$S_E(\omega) = S_j(\omega) + S_s(\omega) + S_e(\omega) + S_a(\omega, r). \tag{2.38}$$

The first term, known as Johnson noise[4], describes the electrical noise $S_j(\omega) = 4k_BTR(\omega)$ where $R(\omega)$ is the frequency-dependent resistance of the circuit, k_B the Boltzmann's constant and T the temperature of the conductor at equilibrium. Noise densities $S_s(\omega)$ and $S_e(\omega)$ correspond to noise inherent to the voltage source and electrical pick-up from the external wiring and circuits. The last term, $S_a(\omega, r)$, represents the anomalous heating. This phenomenon has been widely observed and studied experimentally and theoretically but as yet has not been explained definitively [47–50]. Anomalous heating scales as r^{-n}, where r is the distance between the ion and nearest electrode and n varies from 2 to 4. Studies have indicated that $S_a(\omega, r)$ is independent of the supplied voltage and depends on the trap electrode temperature and the surface properties of the electrode [47,49,50,59–62].

[4] Also known as Johnson-Nyquist noise or thermal noise. It describes the electronic noise generated by the thermal agitation of the charge carriers inside a conductor at equilibrium.

A well-studied microscopic model of anomalous heating is the fluctuating dipole model [63, 64] where such noise is assumed to arise from adsorbate dipole fluctuations. In this model, it is suggested that the anomalous heating is dependent on the species of the surface atoms and adatoms, the surface roughness of nanometre scales and distribution of surface adatoms. Based on this, surface roughness was measured and optimised in the works presented in this thesis.

2.4 Internal states of Yb ions and quantum information processing

J.I Cirac and P. Zoller proposed [34] that trapped cold ions can be used in quantum computing by coupling multiple ions through collective quantised motion. Impressive progress were made in realising quantum gates using various species of ions [27,33,65–68].

In recent years, ytterbium won a popularity in the ion trap community and atomic clock field. Ytterbium has the advantage of its relatively simple energy levels being easily addressable by commercially available lasers and the spin 1/2 nucleus of $^{171}Yb^{+}$ resulting in a hyperfine structure that can be used as qubit states with a long lifetime. Furthermore, ytterbium has been demonstrated in creating entanglement both in the case of using only lasers [69] as well as lasers in combination with microwave radiation [70]. In addition, ytterbium ions can be Sisyphus-cooled [57] to enable a subsequent sideband cooling. For these reasons, ytterbium is chosen for the experiments in this work.

Two different isotopes of ytterbium, $^{171}Yb^{+}$ and $^{174}Yb^{+}$ were used in this work. $^{171}Yb^{+}$ is used for coherent manipulation for its magnetically sensitive hyperfine structure in the $^{2}S_{1/2}$ manifold. The separation between the upper and the lower levels is 12.6 GHz making it ideal for microwave-driven quantum gates. $^{174}Yb^{+}$ is used for verification of trapping parameters for it is easier to get trapped due to its rich natural abundance of 32% while that of $^{171}Yb^{+}$ is 14% [71].

The ytterbium is injected into the experimental space in the form of a neutral atom flux by thermally heating a small piece of ytterbium metal in an atomic oven. The atomic oven is constructed from a $\sim$ 20 mm long stainless steel tube which is crimped flat at one end and welded shut with a constantan foil[5]. A high current of 5-7 A passes through the constantan foil via copper wires and after several minutes, the oven heats up to 400°C

[5] A copperCnickel alloy.

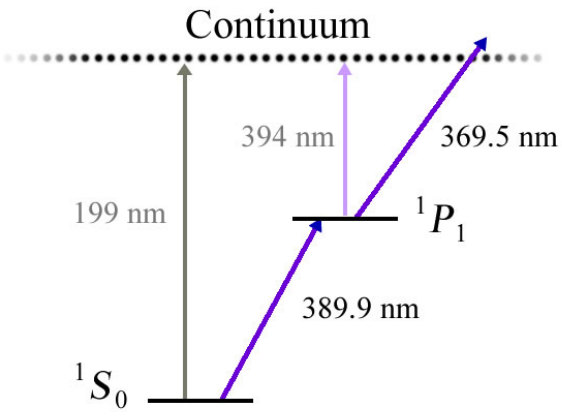

Figure 2.14: A partial energy diagram showing the two-stage photo-ionisation process used in the experiments. The grey arrow shows a single 199 nm photon ionisation process and the light purple arrow shows the ionisation process of a $^1P_1$ atom with a maximum wavelength of 394 nm.

which is enough to break the native oxide layer and evaporate Yb atoms. The neutral atom must be ionised so that it can be trapped by the electric field. Ionising ytterbium using photo-ionisation is possible with either a single 199 nm photon or a two-stage photo-ionisation process. The first photon, 399 nm, addresses the transition from $^1S_0$ to $^1P_1$ as shown in Fig. 2.14. The isotope shifts in this transition mean that the precise wavelength of the 399 nm laser can be altered to selectively ionised a specific isotope. From the $^1P_1$, any photon shorter than 394 nm can ionise the atom. The 369 nm photon which is used in $^2S_{1/2}$ to $^2P_{1/2}$ cooling cycle is used in the experiments.

This thesis tries to resolve the scalability challenge in building a practical quantum computer. Traditionally, to operate thousands of quantum gates simultaneously in a quantum computation task requires fine control and precise alignment of a massive amount of lasers. This is practically impossible. In 2001, an alternative gate operating scheme [36] was proposed using global, long-wavelength radiation in conjunction with locally applied magnetic fields. The long-wavelength radiation drives the internal states of the ions. The local magnetic field gradient provides the position-dependent individual addressing and strong coupling between the long-wavelength radiation and the ion. The principals of this scheme, known as the MAgnetic Gradient Induced Coupling (MAGIC) scheme, is discussed in section 3.1.1.

In this scheme, the qubit required for coherent manipulation experiments is the $^2S_{1/2}$ hyperfine manifold. The $F = 0$ state and $F = 1$ are "0" and "1" of the quantum binary. The microwave radiation at 12.64 GHz is used to trigger the flopping between the two

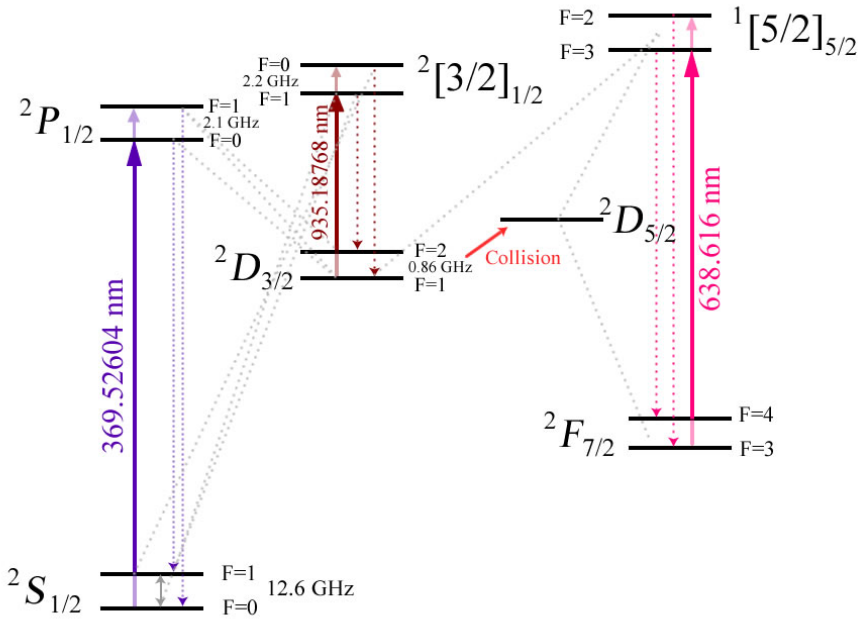

Figure 2.15: An energy level diagram for $^{171}Yb^+$ showing related transitions used in the MAGIC scheme. The solid lines denote the laser and microwave used to cool and manipulate the ions. The coloured faded lines represent power broadening, sidebands or scanning applied to the lasers for additional transitions. The dotted lines show the spontaneous emission of photons, coloured denoting primary paths and grey denoting secondaries.

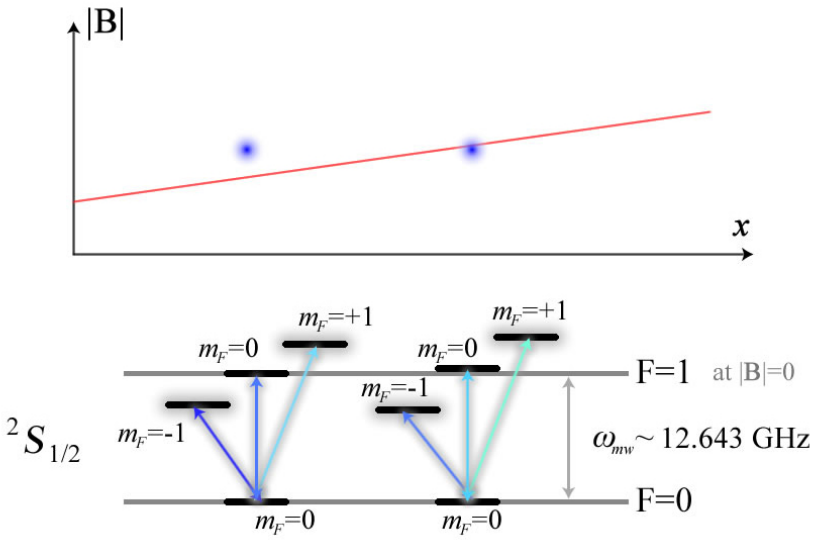

Figure 2.16: Individual addressing of two ions using the Zeeman splitting of $^2S_{1/2}, F = 1$ manifold for $^{171}Yb^+$. The two ions are sitting at a distance along the direction of magnetic gradient thus having different absolute magnetic field strength $|\mathbf{B}|$. The different $|\mathbf{B}|$ resulted in the difference of shifts of $F = 1$ states caused by the first order Zeeman effect. These states are strongly coupled to the secular motion due to the position-dependent gradient. The $F = 0, m_F = 0$ to $F = 1, m_F = 0$ transitions are widened due to the second-order Zeeman effect. Since the energy gaps between $F = 0$ and $F = 1$ states are different for all transitions, they can be individually addressed by applying corresponding microwave radiation.

states. The related energy level diagram for $^{171}Yb^+$ is shown in Fig. 2.15.

In the presence of a magnetic field, the $F = 1$ state is degenerate due to the Zeeman effect. Because of this, states with different m_F can be individually addressed with multiple microwave fields. Fig. 2.16 illustrates the energy shifts due to the Zeeman effect thus a state-dependent force can be used for coupling and individual addressing.

2.5 Ion trapping experiments

So far the theoretical description of trapped ion's motion is covered: analytical approach to electric field generated by surface traps, cooling trapped ions and coupling the internal states of ions using long-wavelength radiation. With these preliminary knowledge, the essential devices and equipments in ion trapping experiments are described in this section.

2.5.1 Lasers

Ionising and cooling Yb ions requires a number of lasers at different frequencies as described in section 2.3 and 2.4. As shown in Fig. 2.15, the lasers used are: a 369 nm laser used for optical pumping and ionisation (from $^1P_1$ state to continuum), a 399 nm laser for ionisation (from $^1S_0$ to $^1P_1$ state) and a 935 nm laser for repumping ions out of the D state.

The 369 nm beam is produced by a commercially available laser from M Squared. It is a diode-pumped titanium sapphire laser driven by a 12 W 532 nm diode laser[6]. The titanium-sapphire cavity[7] produces a 739 nm light which is frequency doubled to 369.5 nm by a doubler module[8] which outputs a 1 W blue light as shown in Fig. 2.17.

The 369 nm beam is split using a beam sampler[9] for two individual experiments. The beam then goes through a half-wave plate and an acousto-optical modulator (AOM)[10]. The light goes through the AOM twice in both directions to ensure the beam angle remains constants at different AOM frequencies. The AOM is driven by an AOM controller[11] to allow the laser to be tuned in frequency and amplitude. After the AOM, the beam passes through an electro-optical modulator (EOM) which adds sidebands to the light so that the hyperfine levels of Yb^+ could be addressed.

The 935 nm repump laser is a commercial diode laser by Toptica. The output of this beam is about 50 mW and passes through a beam sampler where a small fraction of the power is coupled into a wavemeter which monitors the wavelength as a feedback to the control PC. This then locks the wavelength by varying current and temperature of the diode. The remaining beam is coupled into a fibre. The 399 nm beam is supplied by a home-built diode laser. With 4 mW output power, this laser has a similar setup to the 935 nm laser.

At the output side of the fibres, as shown in Fig. 2.18, the 369 nm laser beam is overlapped with the 399 nm beam using a bandpass filter. The 369 nm beam passes through a telescope system and a pinhole which trim the spatial beam profile. A CMOS camera[12] is used to show the spatial beam profile, an example of which is shown in Fig. 2.19. The combined beam is again overlapped with the 935 nm beam. A precise overlapping

[6] Lighthouse Photonics Sprout-G.
[7] M Squared SolsTiS.
[8] M Squared ECD-X.
[9] Thorlabs BSF10-A.
[10] Isomet 1206C-833, A/R coated for 360-420 nm.
[11] Isomet 630C-110G.
[12] Thorlabs DCC1545M.

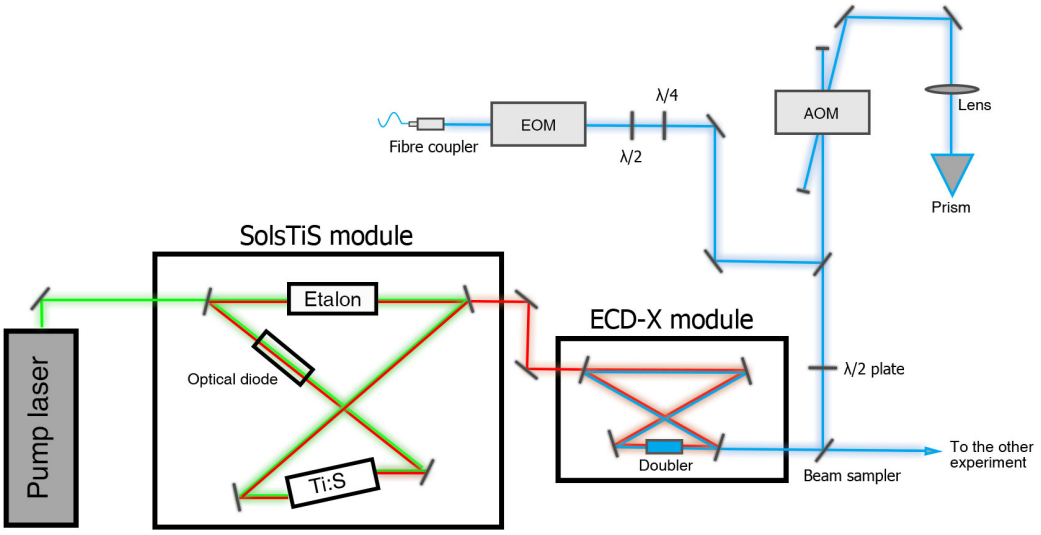

Figure 2.17: Schematic the optical paths of the M Squared 369 nm laser before coupling into the fibre.

is achieved by adjusting the two mirrors on each beam path before overlapping. The combined beam of all three lasers is steered to the optics sitting on an optical breadboard[13] for the ease of horizontal alignment of the two beams. The focusing lens is fitted on a gimbal mount[14] is used for precise control of the beam angle.

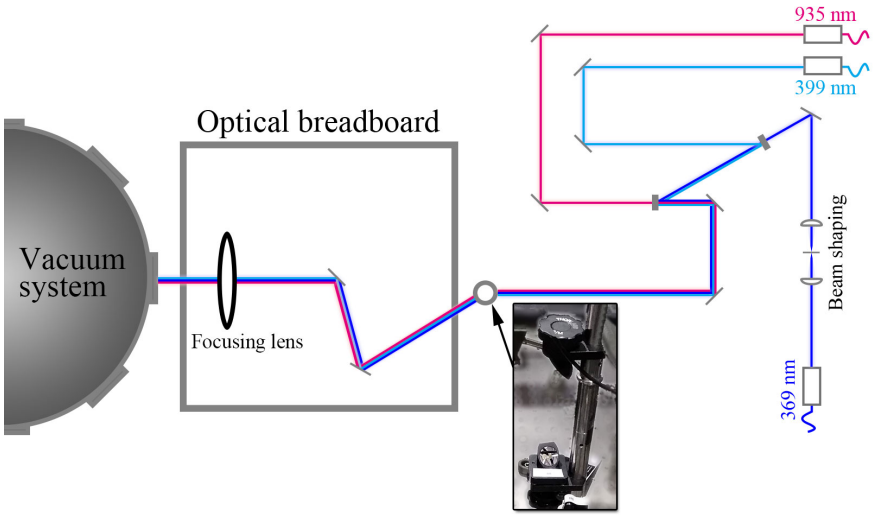

Figure 2.18: The optical paths of the lasers. The inset shows the set of mirrors to redirect the beam paths onto the optical breadboard.

The imaging optics used in this experiment are shown in Fig. 2.20 consisted of a triplet lens and a doublet lens. The triplet lens[15], with fixed magnification, is used to reduce the

[13] Solid aluminium optical breadboards, Thorlabs MB2020/M.
[14] Thorlabs GM200/M.
[15] 54-17-29-369, Special Optics.

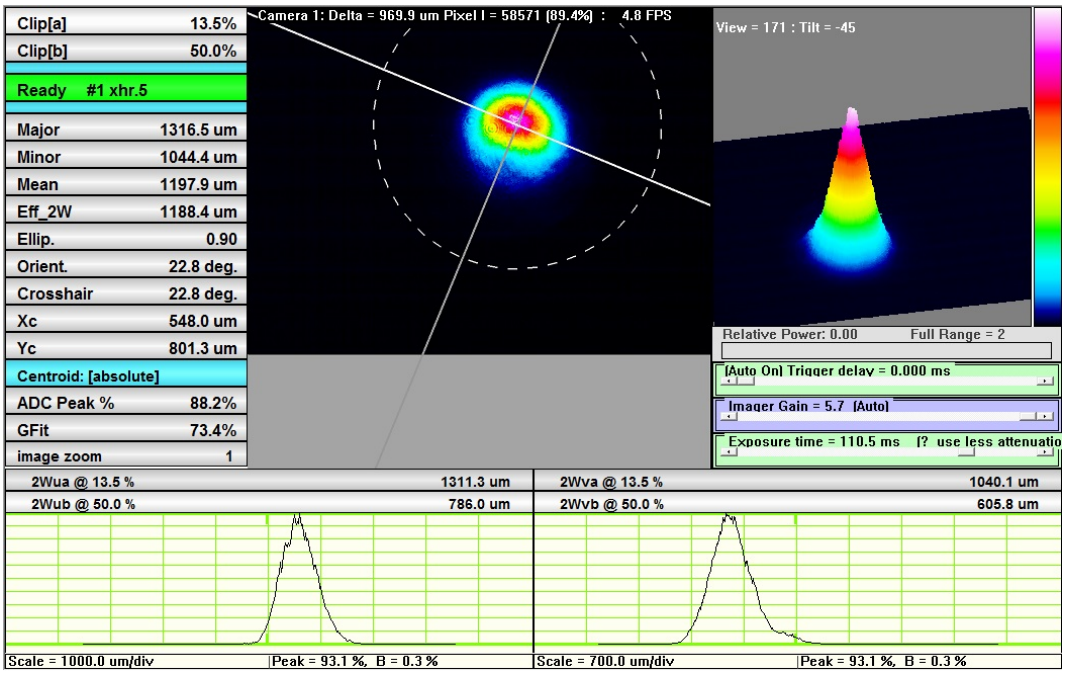

Figure 2.19: A screenshot of the beam profiler program showing a 369 nm laser beam after the telescope system with a near Gussian profile.

effect of spherical aberrations caused by the wide-angle of collection of photons from the ions. At the image distance, an iris[16] is placed to filter scattered light and background noise. The iris is followed by a doublet lens system so that the image size on the detector can be adjusted via the doublet magnification. Lenses and iris are enclosed in an adjustable tubing[17] mounted on a translation stage shown in Fig. 2.20. The 369 nm bandpass filter[18] removes ambient light and scattered lights from other lasers. The flipper mirror deflects the collected photons onto a photomultiplier tube[19] or electron multiplying CCD array[20].

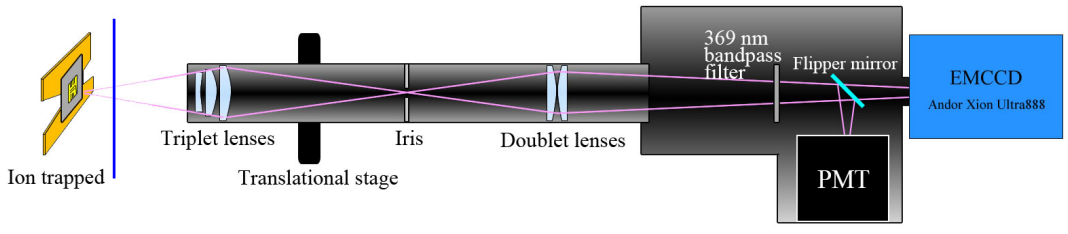

Figure 2.20: Schematic of the imaging setup for ion trapping experiments.

[16] SM1D12SZ, Thorlabs.
[17] SM1ZM, Thorlabs.
[18] FF01-370136, Semrock.
[19] H8259-01, Hamamatsu.
[20] iXon 885 EMCCD, Andor.

2.5.2 Vacuum system

All ion trapping experiments in the IQT group is carried out under Ultra-High Vacuum (UHV) of better than 10^{-11} Torr[21]. The UHV environment minimises the chance of collisions of ions with other atoms or molecules so that the ions remain trapped for long periods of time. The long trapping time and isolated environment meet the requirement for building a high-fidelity system.

There are two ways of achieving such a vacuum. A conventional system is baked at 200°C in a large home-built oven over weeks while being constantly pumped by a mechanical pump[22] so that the moisture and absorbed particles are removed from the chamber. Ultrasonic bath cleaning is often recommended before baking. The vacuum system is then transferred onto the experimental table where its pressure is maintained by a titanium sublimation pump[23] and an ion pump[24]. An ion gauge[25] is used to monitor the pressure.

The alternative way to obtain UHV is to go cryogenic. The system [72], shown Fig. 2.21, does not require baking. Once the chamber is closed, the cryogenic system is first mechanically pumped down to low pressure, then the compressor brings the temperature down to a few Kelvins where particles in the chamber are condensed onto the chamber walls as a result of random scattering. The cryogenic system used in this work has a minimum temperature of less than 4 K.

One complication that comes with UHV technology is that the materials used inside the system have to be UHV compatible. A non-compatible material will out-gas, releasing particles and preventing the system from achieving the required ultra-high vacuum. Extensive studies have been done on the UHV compatibility of various materials. When designing UHV parts, well-established databases and documents are helpful in picking the right material. In this thesis, two references are used, one published by Laser Interferometer Gravitational-Wave Observatory [73] and the other one is the database by National Aeronautics and Space Administration[26].

[21] 1 Torr= 1.33322 mbar.
[22] M S03525, Pfeiffer Vacuum.
[23] PN: 9160050, Varian.
[24] PN: 9191145, Varian.
[25] UHV-24p Bayard-Alpert, Variant.
[26] http://outgassing.nasa.gov/

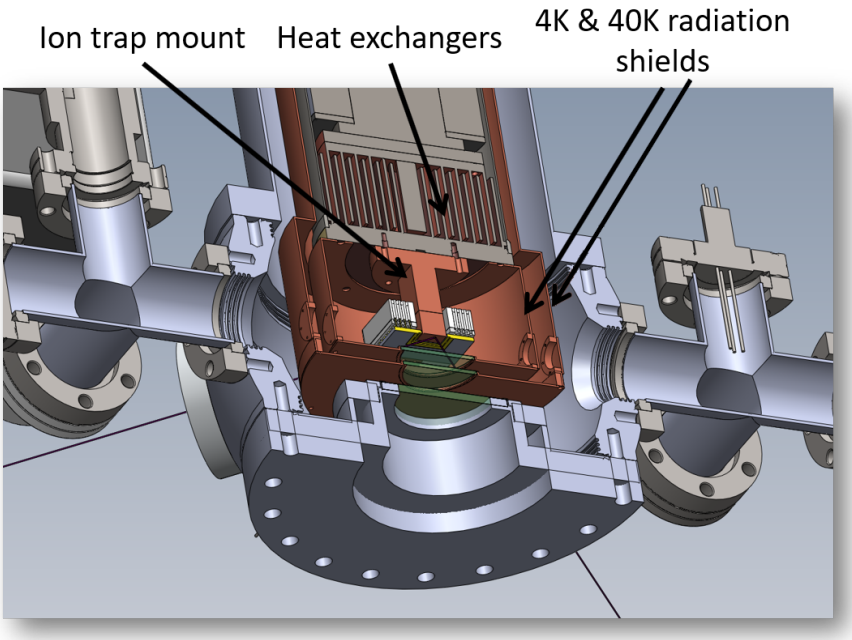

Figure 2.21: 3D illustration of the cryogenic system. The ion trap and its carrier are mounted on a copper block which is attached to a heat exchanger where cooled helium from the cryogenic pump cools the mount and 4 K radiation shields. There are two radiation shields (4 K and 40 K) to help reduce the heat exchange due to radiation. Each shield has multiple holes for optical access.

2.5.3 Oven and DC supply

The ion trap chips are placed on a ceramic chip carrier[27] and wirebonded. The chip carrier with its pin grid array is mounted on a customised carrier PCB with low-pass filters on it. The PCBs are fitted with spring-loaded pin receptacles which crimp Kapton insulated copper wires to D-sub vacuum feedthroughs. RF feedthroughs and high current feedthroughs are connected via their own vacuum interface.

The atomic oven that produces a neutral Yb flux consists of a $\sim$ 20 mm long stainless steel tube and a Yb wire wrapped in a constantan foil. The constantan foil heats up to 400°C at a constant current of 5-7 A. The heat is enough to break the naturally formed oxide layers and evaporate Yb atoms. The Yb wire can either be a 90.69% enriched ^{171}Yb wire[28] or a natural Yb wire[29]. The oven is illustrated in Fig. 2.22.

As explained in section 2.4, trapped ions gain additional motional quanta when experiencing electrical noise at frequencies close to its secular frequency. Fluctuations of both

[27] PGA10047002, Global Chip Materials.
[28] OA0036, Oak Ridge National Laboratory.
[29] GO0196, Goodfellow Cambridge Ltd.

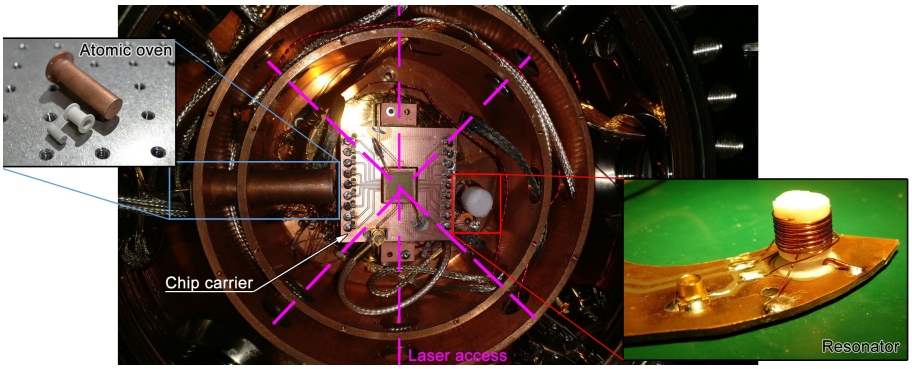

Figure 2.22: An image showing the inside of the cryogenic system. The pink dash lines are laser access. The details of the resonator is also shown in Fig. 2.24.

the RF and DC voltage amplitudes or RF frequency will cause a change in the secular frequency and position of the ion. Therefore, very low noise RF and DC voltages are required in ion trapping experiments.

To minimise the noise in DC signals, low-pass filters can be used to remove the AC components. There are two major sources of AC noises in DC signals, the first is from the power source. For example, a switch-mode power supply has very high energy efficiency, however, the switches between low-dissipation, full-on and full-off state produces a ripple voltage at the switching frequency and its harmonics. A low noise linear regulator is often used instead. An alternative to a conventional non-switching benchtop power supply is the battery based DC voltage supply. Battery-based voltage suppliers have little to no noise due to complete isolation from the mains. Since the batteries provide a high voltage, low current output, the battery does not drain much faster than its natural discharge. The collaborating researchers of the IQT group at the National University of Defence Technology used a 12 V car battery and it has not run flat for 3 years of continuous use.

The other source of noise in DC signals is what is called pickups. The DC electrodes and wires sometimes are weakly coupled to adjutant RF signal lines, picking up unwanted signals. To minimise such coupling in an ion trap chip, the DC and RF electrodes need to be perpendicular to each other. The DC lines are also filtered both on the PCB carrier and outside the vacuum using low pass filters.

2.5.4 RF systems

An RF source that can provide a thousand volts signal is required in an ion trap experiment. The natural choice for this task is an electronic resonator where a small input signal can drive high amplitude oscillations in the system. This can only happen if the power

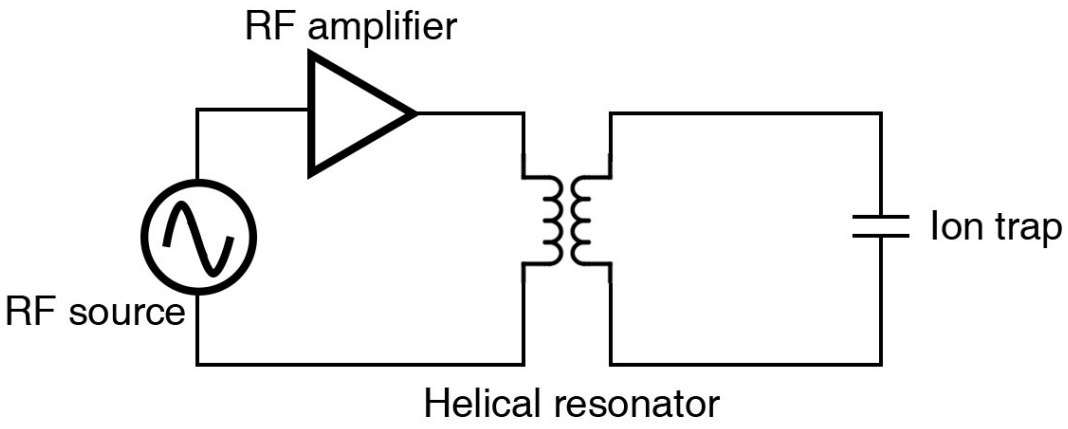

Figure 2.23: Circuit diagram of a basic RF delivery system.

dissipation in the system is smaller than the input power. The excess of the energy is stored in the system. The amplitude will grow until the dissipation equals the incoming power. Quality factor or Q factor is the ratio between the energy stored in the system per cycle and the energy dissipated per cycle. It is used to quantify how well the system is at maintaining the oscillation.

A typical RF delivery circuit diagram for ion traps is shown in Fig. 2.23. Due to the massive difference between the device size and the RF wavelength, at the trapping frequency, the ion trap behaves like a lumped capacitor. The relationship between the total inductance L, capacitance C, resistance R, the bandwidth Δf and the resonant frequency f_0 is described by

$$Q = \frac{1}{R}\sqrt{\frac{L}{C}} = \frac{f_0}{\Delta f} = \frac{1}{2\pi\sqrt{LC}}. \tag{2.39}$$

The amplitude of the generated RF voltage V is

$$V = \sqrt[4]{L/C}\sqrt{2PQ} \tag{2.40}$$

where P is the RF power.

The total capacitance C and total resistance R can be measured with a vector network analyser (VNA) or simulated using numerical packages such as EMPro. A typical ion trap chip has a capacitance of 10-30 pF and resistance of 0.1 Ω. The design and simulation of such a resonator are covered in section 4.5.3. The stability of the RF supply is critical to maintaining ions in coherence, K. Johnson *et al.* [74] reported a 10 ppm stabilised trapping in 1 MHz atomic oscillation.

Fig. 2.24(b) shows the compact resonator [75] inside the cryogenic system. The autotrans-

former is wound on a PTFE rod using superconducting niobium-tin wires whose critical temperature is 18.3 K. The PCB is coated with copper. Fig. 2.24(a) shows the change of Q factor vs different temperatures with a 60 pF capacitor fitted as a dummy trap. The temperature when a sudden increase of Q factor occurs is about 7 K, lower than the critical temperature. This is likely because of the presence of the offset magnetic field used to compensate the stray magnetic fields [76]. A portion of the signal (about 1/700) is taken to the measurement connector by a voltage divider. The half doughnut-shape of the board (shown in Fig. 2.24(b)) is to maximise the use of space in the chamber (inside the 4 K radiation shield on the ion trap mount shown in Fig. 2.21).

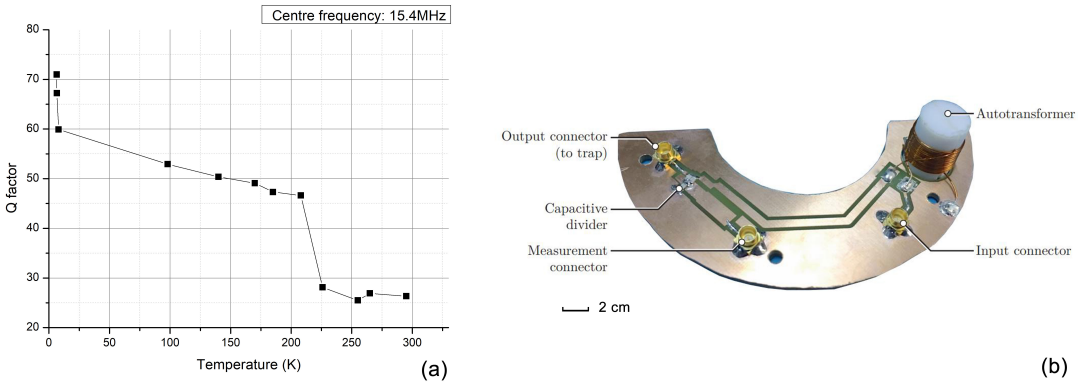

Figure 2.24: **(a)** The Q factor of the cryogenic resonator as a function of temperature. The resonant frequency of the circuit is 15.4 MHz. **(b)** The compact superconducting resonator, image reproduced from [72]. The resonator fitted in the vacuum system is shown in Fig. 2.22.

2.6 Conclusion

This chapter described the requirements for trapping Yb ions on a microfabriated surface ion trap and using them for quantum processing. The principals of a Paul trap and the analytical technique to model the electric potential were reviewed. A new technique was developed to allow the Mathieu stability parameters in a surface ion trap be correctly evaluated through a mathematical transformation. The experimental setups to trap, cool and manipulate an ion were described. With these requirements in mind, the following chapters develop novel ion trap structures for a faster, more reliable scalable quantum computer using microfabricated surface ion traps.

Chapter 3

Scalable quantum computers

In this chapter, the challenges of building a scalable quantum computer are discussed. A blueprint proposed by researchers to address the problems was reviewed. The design criteria and fabrication technologies for building the novel scalable quantum computer units are summarised and discussed.

3.1 The scalable quantum computer blueprint

In 2000, Dr David DiVincenzo proposed a list of conditions that are necessary for constructing a quantum computer, known as DiVincenzo's criteria [15]. The criteria require the system to be scalable and capable of initialising the states of qubits, implement a universal set of quantum gates, have a long enough coherence time and have qubit-specific measurement capability.

This thesis focuses on the development of a scalable quantum computer following the blueprint proposed by B. Lekitsch *et al.* [19]. In section 3.1.1, a quantum logic scheme used in the blueprint is introduced where, following DiVincenzo's criteria, the initialisation, universal quantum gate and individual addressing are explained. In section 3.1.2, the key features in implementing a scalable quantum computer following the blueprint, junction trap and microwave cavity integration, are presented.

In previously proposed trapped ion quantum computing architectures [35], modules are powered by laser-driven qubit gates which require precise position and control of a vast number of laser beams. It is both energy inefficient and very challenging in terms of engineering. In 2017, B. Lekitsch *et al.* published a blueprint paper [19] describing a new

architecture for a scalable trapped ion quantum computer. Rather than requiring multiple ultra-stable lasers to drive a qubit gate, this architecture is based on a concept involving global, long-wavelength radiation in RF or microwave regime in conjunction with locally applied magnetic fields. The principal of gate operations is based on a mechanism proposed by Mintert and Wunderlich in 2001 [36], known as the MAgnetic Gradient Induced Coupling (MAGIC) scheme.

3.1.1 MAGIC scheme for quantum gates

Internal electronic states are often used as qubits which can be coherently prepared using electro-magnetic radiation in optical or RF regime. Multiple qubits quantum operations are often realised by coupling the collective vibrational motion to the internal dynamics of individual ions which are trapped in the same trapping region. Ionic qubits using laser lights induced coupling has been the mainstream of the community since only with light the Lamb-Dicke parameter[1] is large enough in typical traps. Also, to individually address trapped ions typically spaced apart by a few microns, precisely tuned and focused laser beams are required.

The complexity of experimental set-ups can be reduced decisively when microwave radiation is used to drive the coupling. The coherence time of qubit is no longer affected by spontaneous emission due to the finite lifetime of qubit states, or the spontaneous scattering caused by non-resonant laser light driving Raman transitions [77].

The long-wavelength radiation was demonstrated in implementing single-qubit gates with errors of only 10^{-6} [68]. However, it alone can only couple the internal and motional states weakly.

The coupling strength between internal and motional states is described by Lamb-Dicke parameter

$$\eta = \frac{2\pi\Delta x}{\lambda} \tag{3.1}$$

where $\Delta x = \sqrt{\hbar/2m\omega_s}$ for an ion with mass m in a potential with secular frequency ω_s.

In the presence of laser radiation, η is on the order of 0.01. Lamb-Dicke parameter becomes extremely small ($\sim \times 10^{-5}$ times smaller) due to the long wavelength. The coupling is enhanced when an external magnetic field is present resulting in a sizable effective Lamb-Dicke parameter. This external magnetic field can either be static [36] or dynamic [67].

[1] Lamb-Dicke parameter describes the coupling strength between the internal and motional states.

The specific MAGIC scheme used in the blueprint utilises a static magnetic field with a high gradient. The fidelity of this gate scheme has recently been improved significantly, demonstrating the potential power of microwave based quantum computing logic. High fidelity results were published on single-qubit gates [78,79], two-qubit gates [37,67,70] and three-qubit gates [80].

The individual addressing of atoms is realised by driving the radiation field at a frequency specific for each individual ion due to the Zeeman effect. The Zeeman splitting of the hyperfine levels becomes position dependent thus adds a difference to the frequency between the hyperfine levels during oscillations. A magnetic field high gradient is required to resolve the closely spaced trapped ions.

The related energy levels and transitions are shown in Fig. 2.15. In the MAGIC scheme, the qubit required for coherent manipulation experiments is the $^2S_{1/2}$ hyperfine manifold. The $F = 0$ state and $F = 1$ are "0" and "1" of the quantum binary. The microwave radiation at 12.64 GHz is used to trigger the flopping between the two states. In the presence of a magnetic field, the $F = 1$ state is degenerate due to the Zeeman effect. Because of this, states with different m_F can be individually addressed with multiple microwave fields. Fig. 2.16 illustrates the energy shifts due to the Zeeman effect thus a state-dependent force can be used for coupling and individual addressing.

The large B field gradient can be delivered using permanent magnets or metal wires with a large current passing through them, known as Current-Carrying Wire (CCW) structures. Permanent magnets have been successfully used to demonstrate a microwave-based gate in [70] with 20-40 T/m. A maximum gradient of 157.4 T/m was predicted from simulations on permanent magnets [81]. The implementation of permanent magnets relies on the precise physical placement of the magnets, a small displacement will cause a strong Zeeman shift making Doppler cooling impossible.

The CCW structures (CCWs), however, are fabricated into the substrate prior to ion trap fabrication which is inherently scalable as it shares the same fabrication technologies used in ion trap fabrication. The CCW structures are driven by a large current, generating a strong static field gradient. The position of the magnetic field to the trapped ions is guaranteed by microfabrication techniques known as die bonding and lithography which are easier and more accurate than manual placement of permanent magnets. In addition, the CCWs can be easily tuned or completely switched off before and during the trapping, making no disturbance to the Doppler cooling process. The design and fabrication of

CCW structures are discussed in section 4.4.

The long-wavelength radiation can be excited using a global or near field. The global field is most commonly used for it is simple to set up. The radiation is broadcasted using an external horn [37, 70, 82]. D. Allcock *et al.* [79] was the first to demonstrate ion trap quantum gate with near field radiation by integrating microwave circuitry on a microfabricated ion trap. In section 4.3, the benefits and implementation of near field microwave circuitry is discussed, a novel integrated microwave cavity design featuring high Rabi frequency is reported.

3.1.2 The scalable quantum computer blueprint

The discussion so far covered the implementation of quantum gate logics suitable for a scalable quantum computer by DiVincenzo's criteria. In this section, the challenges and approaches towards a scalable quantum computer specifically in the design of the microfabricated systems and integration of functions are reviewed.

The problems and challenges of scalability can be summarised in three categories: a scalable scheme on implementing quantum logics fulfilling DiVincenzo's criteria, the design and engineering of individual units and the interconnection between units. With the first discussed in the last section, this section focuses on the remaining two. The quantum computer system is consists of many small identical elements or units. These units are capable of trapping and entangling ions and detecting the states of them. This requires the unit to consist of a versatile ion trap that can trap the ion stably, perform quantum gates and readouts. The processed quantum information then needs to be passed to its neighbour ions for either storage or further processing hence interconnections of high reliability and efficiency is required between units. There have been two major interconnection schemes proposed by the community so far. Photonic interconnects [35, 83] build fibre channels between units and implements ion-photon coupling devices at both sides. The communication qubit is driven to an excited state with fast laser pulses, through appropriate selection rules releasing an entangled photonic qubit. The entangled photons, through photonic channels, couple to targeted ions causing entanglement swapping. More complicated selection and manipulation of the photons can be realised by mode-matching the photons and interferometry. An alternative method was proposed by B. Lekitsch [19] where the QC units are aligned to great precision using fine piezo control so that ions can travel from one unit to the other through a set of specially designed open-end elec-

trode rails. The inter-unit chip shuttling enables multiple qubit gates on any neighbouring qubits.

Both interconnection schemes face challenges. The photonic interconnection is probabilistic due to the nature of the photon detection process. It is not ideal for deterministic quantum information applications. Moreover, the interaction rate between modules is fundamentally limited due to weak coupling strength between ions and photons. The inter-unit shuttling scheme does not suffer from these problems but requires micron-precise placement of the units, integration of complicated features in a single unit and sophisticated design of the interface.

In this thesis, the inter-unit shuttling scheme [19] is followed, demonstrating the integration of several key features required for a scalable quantum computer unit. Other researchers in the IQT group are working towards realising micron-precise alignment of the units and developing inter-unit shuttling.

The scalable quantum computer as described in the blueprint [19] is consisted of thousands of mass-produced identical units. Each unit is capable of initialising, trapping ions and performing quantum gate operations on them. Each operation is done in a different region in the unit. The regions are interconnected using a junction geometry allowing cold ions to travel across with a minimum gain of motional heating.

Quantum gate operation using long-wavelength radiation requires a high gradient static magnetic field and an efficient tuneable microwave source. So far, only macroscopic magnets and RF horns were demonstrated [79, 81]. They are not scalable as they are not capable of delivering cross-talk free radiation to ions at a chosen position and they are physically too big to fit in a quantum computer consisted of thousands of quantum computer units. Integrated structures to deliver high magnetic field gradient and tuneable microwave radiation have to be developed. In Chapter 4, a novel numerical method was developed, the designs of the three key elements are presented: the versatile junction ion trap, the scalable and efficient microwave delivery system and the CCW structures to deliver high gradient magnetic field.

3.2 10 criteria on designing ion traps

Before introducing the topics on designing and fabricating a scalable quantum computer, a general summary of principals to follow when designing a surface ion trap is given. It is

summarised as 'the 10 criteria'.

1. **Surface geometry** The surface geometry of electrodes should be designed to sustain an RF voltage high enough for ions of a certain species at the desired ion height. The geometry should also be able to provide principal axis rotation.
A higher RF voltage allows trapping of ions further away from the chip surface hence reducing the effects of electrical field noises and laser scattering from the surface. A higher RF voltage also allows for a higher trap depth and secular frequencies. Ions can be stably trapped with a higher voltage given that the RF frequency is properly tuned so that the Mathieu parameters are within the stable area.
Principal axis rotation is required to cool the ion effectively. To tilt the trapping field, a small DC potential can be applied by a rail of electrode parallel to the RF electrodes. Alternatively, asymmetric RF electrodes can be used.

2. **Ion height** The ion height is preferably between 20 and a few hundred µm.
The lower limit of the ion height is set by both the laser access and electrical noises. To avoid the liberation of electrode materials and the scattering of laser lights, the laser beams must be kept above the electrode surface. The heating of an ion due to electrical noises typically follows the d^{-n} law (detailed in point No.4) where d is the ion height. Excessively high heating can be expected with a low ion height trap.
The upper limit is decided by the fact that when the ion is placed far away from the surface, the RF voltage required to provide sufficient trapping is too high to sustain on the electrodes. An extremely high RF voltage may cause electrical breakdowns hence requires the traps to have high breakdown voltages. In Chapter 5, the design and fabrication of a high breakdown voltage ion trap is discussed.
A high RF voltage may cause the ion trap to produce an excessive amount of heat as well. The heat produced by RF signal and methods to manage the temperature on the chips are discussed in point No.4 and 10 respectively. Any vertical structures (such as wirebonds and on-chip sensors) must remain below the laser access.

3. **Electrical breakdown** Maximise the electrical breakdown voltage of the chip by proper design of surface geometry, layer structures and use of material.
Often a longer lifetime is expected when an ion trap is operating at a voltage far lower than its breakdown voltage.
A higher breakdown voltage allows a wider range of choice of trapping frequency and trap depth. Generally, when a deeper trap depth is desired, a higher RF trapping voltage

is used along with tuning of the resonant frequency for stable trapping as described by Mathieu stability parameters.

Several factors contribute to the breakdown voltage including the geometry of the electrodes, the dielectric properties of the insulating materials, vacuum pressure in the gap, interfaces between materials and microscopic surface asperity on electrodes. They are discussed in details in section 5.1.

4. **Heating of ions due to electric noises** The heating of cold ions due to electric noise should be minimised.

Cold trapped ions gain heating of their oscillatory motion through the coupling with electrical noise from vicinity electrodes. Typically, the rate of this heating is orders of magnitude larger than expected from electric field fluctuations due to thermal motion of electrons on electrode surfaces. This effect is known as anomalous heating and its nature and mechanism is an open question to the community. Generally speaking, the dependency of the heating rate and the ion-electrode separation follows d^{-n} law where n is a number dependent per experiment, typically about 2-4. Researches were reported on the mechanism of the heating suggesting that multiple mechanisms underlies behind [84]. The rules of thumb to follow in ion trap designs include minimise the exposed dielectric area [85], minimise the surface roughness of the electrodes[2] and use a high ion height. The exposed dielectrics is discussed in point No.5.

5. **Exposed dielectrics** The area of dielectric exposed to the trapped ion should be minimised.

UV lasers incident on dielectric surfaces can induce time-varying stray charges in the dielectric known as dielectric charging. This results in the unwanted coupling between the stray charges and trapped ions, causing the ion to heat up. Theses exposed dielectric may include a substrate or insulating layer not covered by the electrodes and viewports for imaging tubes or laser access. Exposed silicon is subject to an increased RF loss due to laser-induced charging effect as silicon has a small band-gap relative to the incoming photon's energy[3].

To minimise the exposed dielectric layers, two solutions are available. Researchers can either use a tall electrode as shown in Fig. 3.1(b) or in the case of a multiple metal layer ion trap, etch the insulating dielectric layer to expose the underlying metal (ground) layer as shown in Fig. 3.1(c).

[2] IssacHeating

[3] The band-gap of silicon is 1.17 eV at 10K, corresponding to a photon of 1061 nm wavelength. All of the lasers used for Yb trapping has a shorter wavelength than 1061 nm. Detailed in section 6.1.

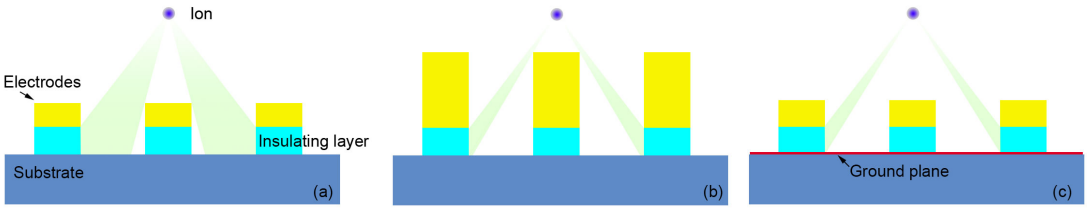

Figure 3.1: (Image not to scale) **(a)** A conventional layer structure. **(b)** Structure with tall electrodes to shield the ion's view on dielectrics. **(c)** Structure with ground plane to shield the ion's view on dielectrics.

To fabricate the structures required, smooth electroplating technique and deep oxide etch were developed and detailed in section 6.5 and 5.4.

The effect of exposed dielectric on viewports can be minimised by either coating the glass with conductive transparent material such as Indium Tin Oxide (ITO) or covered using a metal mesh of small fill factor. The design and simulation of the metal mesh are described in section 4.5.1. The exposed silicon surface should be minimised for similar reasons. The scattered laser light induces electron holes which increases RF loss of the trap[4].

6. **RF loss** The RF loss in both metal and dielectric materials should be minimised.

The RF signal dissipates due to several reasons in metal and dielectrics. The dissipated RF power causes excessive heat which increases electric noise due to thermal motion. The excessive heat can also further trigger thermal breakdown which is detailed in point No.10.

Mathematical estimation was made on different sources of RF loss in section 6.1. The RF loss in metal is best minimised by reducing the surface roughness of the electrodes. The majority of the RF loss in dielectric materials comes from the field-induced dipole oscillation. It can be minimised by using low loss materials or by minimising the couplings of the RF field in/through dielectrics. Chapter 6 focuses on the design and fabrication of a low loss ion trap.

7. **RF matching** All RF components including the RF surface electrodes and wirebonds should have a proper impedance matching.

Impedance is defined as the combined effect of capacitance, inductance and resistance that a circuit offers a signal at a specific frequency. Mathematically, impedance is in ohms the ratio of the voltage to the flow of current allowed by the circuit. Signal can propagate without reflection when the source impedance matches the target impedance. When the impedance is mismatched, a portion of the RF signal will be reflected travelling towards

[4]For details, see section 6.1.

the source. This reflected signal adds on the forwarding signal, causing wave interference. When this occurs in an ion trap, the target electrodes cannot produce a high voltage to trap ions and the reflected signal may cause excessive amount of heat on the chip or damage the RF power supply.

Up to 30 MHz where the trapping frequencies are often within, impedance matching is not critical because the wavelength is far larger than the size of the device. It is critical to the microwave used in the MAGIC scheme. For an on-chip microwave cavity, a proper impedance matching of the electrodes can be realised by implementing impedance transformer and adjusting the widths of the RF electrodes and its spacing as demonstrated in section 4.3.3. The impedance of the wirebonds is adjusted by changing its spacings and materials as detailed in section 6.2.1.

8. **Vacuum compatibility** All materials should be UHV compatible, the stress in the films must be managed.

The ion trap chip should withstand processes to achieve UHV including baking or ramping to cryogenic temperatures. The stress in microfabricated layers should be minimised to avoid delamination due to stress caused by the change of environments such as excessive heat and low pressure.

9. **Contaminant control** The chip should be fabricated, packed, transported in a contaminant-free environments. Minimise the contamination of the device as much as possible.

The contaminant can cause defects, asperity in surfaces and void volumes in interfaces. Cleans are desired between processes and transports. During the operation of an atomic oven, atomic flux can coat the chip surface resulting in unwanted sputtering. Section 4.5.2 reports a simulation result of a microwall structure to reduce the coating.

10. **Heat management** The heat produced by the chip must be minimised and properly mitigated.

The chip is operated with RF and DC supplies constantly, both will produce heat during trapping. Multiple issues were resultant from the excessive amount of heat accumulated. The electrical noise level rises due to an elevated temperature on electrodes and exposed dielectrics. Breakdown voltages decrease due to thermal activation of surface materials. Excessive stress between layers is expected due to thermal gradients which may cause delamination. A change of ion height was observed in the cryogenic system when trapping as a consequence of overheating the chip[5].

[5] An ion trap chip with high RF loss was used in the cryogenic system. The excessive heat generated

To minimise the heat produced, a low DC resistance and low RF loss design are desired. The substrate material should have a high thermal conductivity to provide a good thermal path for the trap. The fabrication of a low loss trap is described in Chapter 6
In the case where high thermal output structures such as CCWs are integrated, a special structure known as channel cooler should be used to provide enough cooling power [86].

From the items listed and discussed above, there are many key points to consider in designing an ion trap including ion height, electrode thickness, material properties of dielectrics, gap sizes, impedance matching and more. These principals also set guidelines for the fabrication. For example, low surface roughness is always preferable for lower RF loss, lower motional heating and less laser scattering. Throughout this thesis, these considerations are illustrated in the design, development and fabrication of novel ion traps for scalable quantum computing.

3.3 Review of fabrication technologies for miniature ion traps

The scalable quantum computer is made possible with the mass production of identical quantum computer units. Thanks to the development of modern electronics industry, state-of-art microfabrication techniques are available to make miniature structures in mass amount at low cost.

There are several fabrication technologies available. The fabrications of surface ion traps mainly fall into three categories: macroscopic traps, CMOS[6] and MEMS[7] traps.

Macroscopic ion traps refer to traps fabricated using conventional methods such as printed circuit board technology and micromachining. These technologies are well-established, cheap to use, reliable and easily accessible. But the fabrication resolution is limited to a few tens of microns. This limits the minimum ion height it can achieve and is physically large hence not ideal for a scalable quantum computer.

CMOS is a technology for constructing ICs such as microprocessors, digital logic circuits and image sensors. A few ion traps [87, 88] were fabricated using CMOS technology. Standardisation of the foundry process permits mass production of the ion traps with high yield rate. Moreover, the ion traps can be processed along with other CMOS electronics

in the chip caused thermal expansion of the substrate resulting in the misalignment of the laser beams. The change in height was 40-60 μm.

[6] Complementary MetalOxideSemiconductor.

[7] MicroElectromeChanical Systems.

and Though-Silicon-Vias (TSVs). It is possible to integrate filtering, Digital-Analogue Converter (DAC) in the same chip. However, the choices of materials are limited in CMOS processes. The substrate is limited to silicon of different purity. Electrode surface material is limited to Al, Cu and thin gold. Changes and optimisations to processes are required, K. K. Mehta *et al.* [87] reported an increased surface laser light scattering due to significantly high electrode surface roughness.

MEMS is a technology to fabricate microscopic devices with complicated structures where the electronic structures may have coupling to another (typically mechanical) system or carry high voltage or high current. MEMS technology is widely used today in applications such as accelerometers, miniature optical waveguides, thermal sensors, bio-sensors and optical switches. The boom in the smartphone and internet-of-things markets contributed to the rapid development of MEMS technologies. The wide choices of materials in MEMS foundry permits the fabrication of versatile ion trap structures. MEMS technology has fast become the most popular choice in the ion trap community. Recently, Sandia National Laboratories [89] reported 'High Optical Access (HOA) trap' allowing the tightly focused laser beam to be accommodated across the surface or through the central slot of the trap to achieve high laser intensities at the ion's positions and to individually address them. The integration of optics and filtering electronics [89–91] were also reported. Hong *et al.* [92] reported an advanced ion trap with no exposed dielectric surface.

In this thesis, MEMS technology is chosen to build the complicated structures and versatile geometries required for the scalable quantum computer. Surface traps, compared to quadrupole traps, have a lower trap depth due to the surface electrode field presented in section 2.1.1 hence often requires a higher trapping voltage. The high RF voltage applied through the microgaps induces electrical breakdowns in vacuum. The performance of the device is significantly limited by the breakdowns. The breakdown voltage can be improved by modifying the fabrication process. In Chapter 5, improved breakdown voltages were reported by improving the dielectric film quality. The novel fabrication techniques developed can be adapted to improve the performance of other MEMS ion traps and devices.

The high RF voltage applied to the chip induces RF loss which can cause effects including excessive motional heating of the cold ions, lowered breakdown voltage and damage to the trap structures. Chapter 6 investigates the RF loss in ion traps and reports the methods to reduce the loss.

3.4 Conclusion

This chapter described the key research problems for developing a scalable quantum computers. The scalable quantum computer will require a versatile ion trap with junction for ion shuttling between units. The cold ion qubit states are addressed using long wavelength radiation which requires a large magnetic field gradient in order to obtain a sizeable Lamb-Dicke parameter for a strong spin-motion coupling. A scalable microwave field generation is required to deliver a strong coupling to drive the quantum gates.

Three key elements are need: a versatile junction ion trap, an efficient microwave delivery system, a structure to produce a high gradient static magnetic field. In the following chapter, a novel numerical method was developed and the novel designs of the three elements were presented.

The discussion on the current status of the fabrication technologies shows that the advanced MEMS fabrication technique is the option to mass produce the scalable quantum computer units. The breakdown voltage and the RF loss limits the performance of the MEMS ion traps. They are investigated in details in Chapter 5 and 6.

Chapter 4

Design and simulation of novel ion traps

The scalable quantum computer blueprint requires three key elements: a X junction trap to shuttle ions efficiently, a compact and efficient microwave delivery system and structures to generate high gradient static magnetic field for the quantum gates. In this chapter, a new simulation tool was introduced for the precise simulation of the electromagnetic field generated by microscopic structures.

4.1 Dynamic simulation tool

4.1.1 Pseudopotential and the dynamic methods

Prior to designing an ion trap or starting an ion trapping experiment, studying the trapping potential is critical. From the trapping potential, trapping parameters including the RF driving frequency, RF voltage, trap depth, ion height and secular frequencies of the ion's motion are calculated. In section 2.1.1 and 2.2, the basis for describing the RF trapping potential was reviewed using pseudopotential approximation and an analytical description based on gapless approximation. The analytical approximation method provides a result of limited accuracy and cannot be used in complicated geometries. Numerical tools, such as CPO[1], ENT [93]and COMSOL[2], were developed and used to efficiently solve the potential to a high accuracy. The basic steps include: meshing the geometry for numerical methods,

[1] https://simion.com/cpo/
[2] https://www.comsol.com/

calculation of electrostatic fields, solving for the pseudopotential and solving for trapping parameters.

These methods were used in the community for years in various traps and systems. However, the development of a scalable quantum computer unit posts new challenge and requirements. Due to the complicated geometries used, the conventional method is no longer valid.

An example to show the limitation of the conventional method is 'vertical shuttling trap' [72]. This chip consists of three regions, high ion height trapping region, vertical shuttling region and low ion height region. It was designed to trap ions at high ion height and brings them down to a lower height for a stronger coupling to the integrated microwave cavity. From section 2.2, it is known that ion height is determined by the electrode widths and spacings. The chip design (Fig. 4.1) uses wider electrodes in high ion height region and narrower in the low region. The RF was fed using a 45° bend for correct resonator length. The chip was designed using a conventional numerical method.

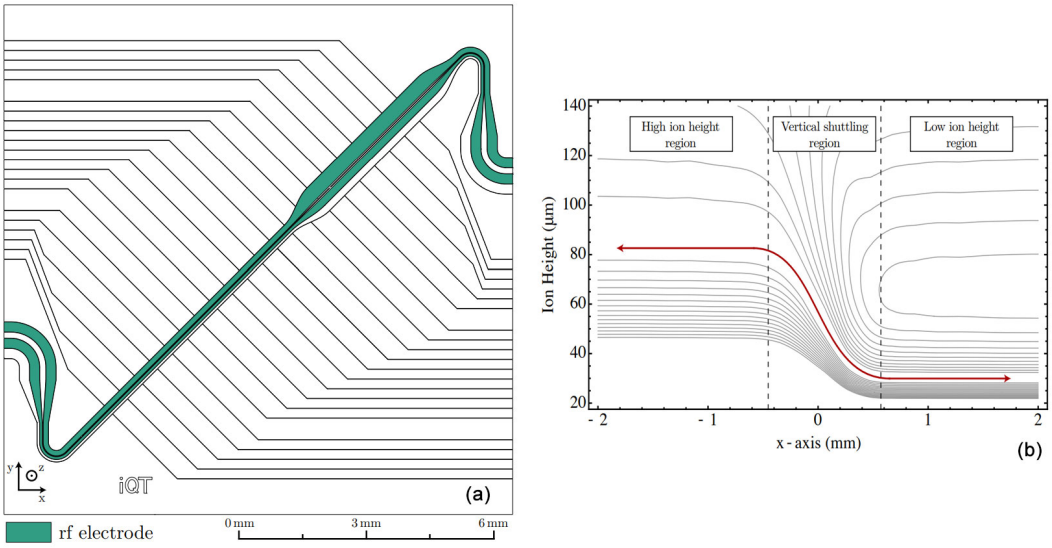

Figure 4.1: Vertical shuttling trap. **(a)** Complete design of the trap. **(a)** Pseudopotential of the vertical shuttling region along the axial direction when driving at 10 MHz, 150 V. The plot shows the variation in potential minimum from the high ion height region to the low ion height region.

The chip was mounted and tested but failed to trap. It was later confirmed that this chip had weak trapping potential [72][3]. This suggests that the conventional method does not apply to scenarios where electrostatic approximation does not hold. The electrostatic approximation assumes that the RF voltage is the same on all electrode surfaces. This

[3]See section 6.2.1 for detailed investigation on the failure of this trap.

is only true in quadrupole traps and infinitely long linear ion traps. When considering the fringe fields in a finitely long linear trap, or traps with non-constant impedance, this approximation does not hold. A new simulation method considering the wave nature of the RF signal is needed.

A new simulation tool based on a commercially available numerical package was developed and named 'Dynamic Simulation Tool' (DST). To explain the issue with the vertical shuttling trap, DST was used to simulate it. A unit power RF source at 20 MHz was used in a conventional simulation tool (ENT) and DST. The surface electric field strength distribution on the chip surface using the two methods are plotted in Fig. 4.2. ENT, the static solver, does not calculate the impedance-induced non-uniform distribution of the field. DST can produce the result of the RF propagation where the RF input does not reach the trapping rails due to the 135° bend. The RF wave resembles the water wave. The 'water' poured in by the source travels in the tapering waveguide(Fig. 4.2(b1)) until it hits the bend (Fig. 4.2(b2)). Due to the sharp corner, most of the wave is reflected back to the source. The amount of wave reflected is quantified using what is known as 'input return loss' defined as the ratio between the incident wave voltage and reflected wave voltage. In this case, the absolute value of the input return loss from the simulation result is 0.9998 indicating that almost all incident wave is reflected. RF reflection is discussed in details in section 6.2.

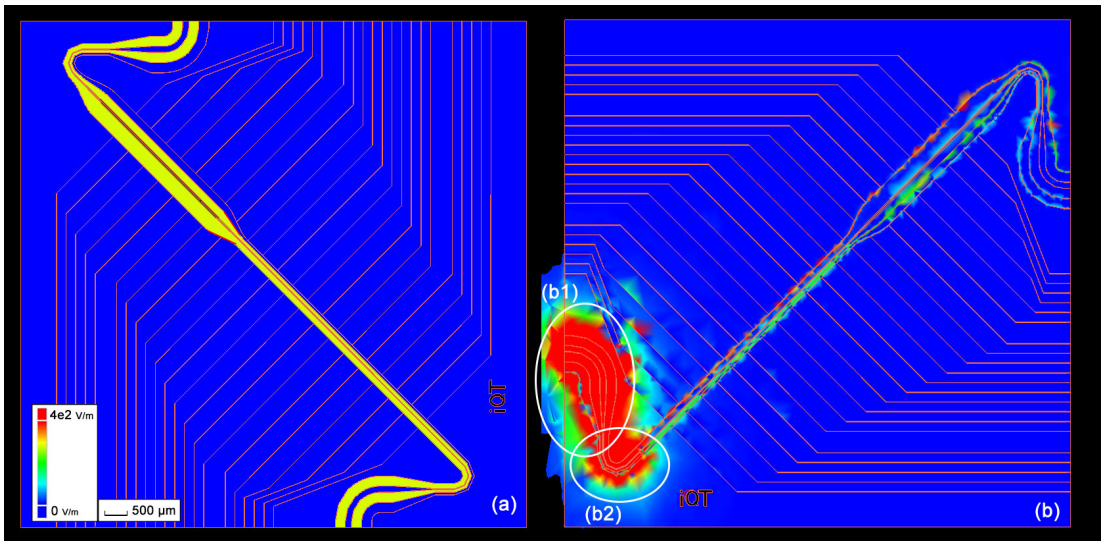

Figure 4.2: Simulated electric field strength distribution on electrode surfaces of the vertical shuttling chip using different simulation tools. (**a**) ENT. The static solver produces an electric field that distributes uniformly. (**b**) DST. The dynamic solver calculates the propagation of the electromagnetic wave.

4.1.2 The benchmark test

It has been established that DST is superior in designing ion traps as it calculates the RF propagation. To prove that DST is an efficient and accurate solution to meet the demand of designing complicated geometries, a benchmark test is necessary. The electric field simulation is the core of studying ion traps numerically. It is essential to produce a highly accurate result. A device known as idealised spherical deflector analyser (ISDA) is used as the benchmark model. An ISDA has the electric field of a spherical capacitor, consisting of two concentric spherical electrodes held at different potentials. The electric field is uniform between the electrodes:

$$E(R) = \frac{(V_2 - V_1)R_2R_1}{(R_1 - R_2)R^2} \tag{4.1}$$

where V_i and R_i are the voltage and radius of the ith electrode and R is the distance from the centre.

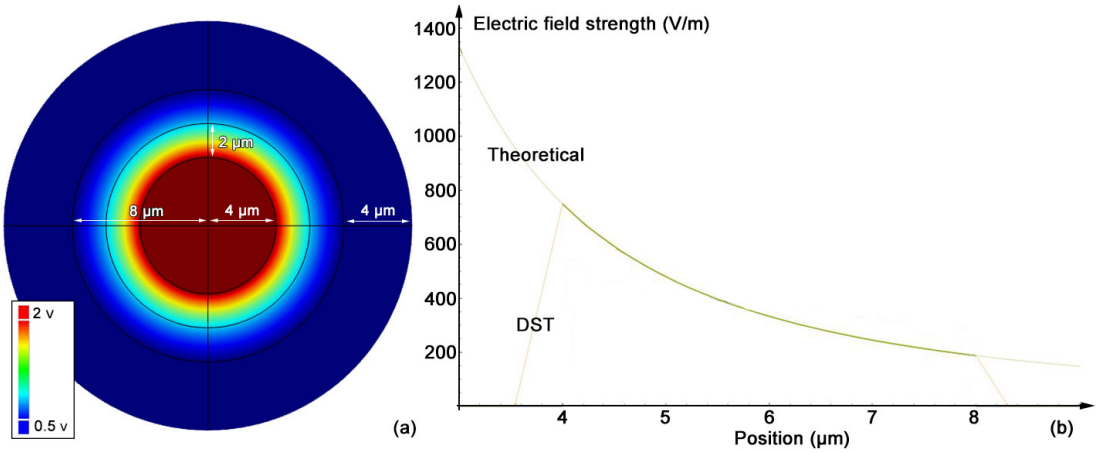

Figure 4.3: (**a**) The crossview of the potential plot in the ISDA using DST. (**b**) The electric field strength plot. Comparison between the theoretical and simulated results.

In this benchmark, the radius of the electrodes are 4 and 8 mm, the voltages are 2 and 0.5 V respectively. The outer electrode is modelled with a 4 mm thick metal shell. The cross-view of the geometry is shown in Fig. 4.3(a). The electrodes are made of perfect electric conductors and gaped by air. No electric breakdown or dielectric charging effects were considered. The models was evenly meshed with 461 triangles using an open-source software Gmsh [94]. The resultant E field plots are shown in Fig. 4.3(b). The departure from the theoretical result near the electrodes is because the change of electric field value has to be finite in numerical evaluations. To quantify the departure, the Root-Mean-Square (RMS) difference between simulated and theoretical results are calculated over the

air gap. The departures is only 3.33 μV_{RMS}. In ion traps with similar gap sizes, this departure is much smaller than the noise generated in a typical RF power supply [63].

In the following sections and chapters, this well-established simulation tool is used to aid the design of the elements required to build a scalable quantum computer unit.

4.2 Junction design for scalable quantum computer units

The basic unit to build a scalable quantum computer is a versatile ion trap unit capable of initialising, trapping, entangling and shuttling ions with a defined control sequence. In the blueprint [19], the core of the quantum unit is the monolithic microfabricated X junction ion trap.

The challenge in making such a trap is that the ion has to be shuttled through the centre of a junction where two linear pairs of the RF rails merge. To allow adiabatic shuttling, optimisation has to be made towards the design of the geometry of the junction in pursuit of a minimal RF barrier. When adiabatic shuttling is desired, the RF barrier has to be very small to avoid adding motional excitations to the shuttled ions [95].

4.2.1 RF barrier

RF barrier occurs when several linear sections merge. Due to the impact of nearby electrodes near the junction, the ion sees a huge RF potential wall. As a result of that, the ion height, trap depth and escape point change making the ion unstable. The RF barrier at position x is defined as

$$\lambda(x) = \frac{\Psi(x)}{\Xi} \tag{4.2}$$

where $\Psi(x)$ is the electrical potential at position x and Ξ is the trap depth of the linear trapping region, a constant according to equation 2.24. The RF barrier Λ of a junction trap is therefore defined as the ratio of the maximum electrical potential along the ion's path to Ξ. For example, Fig. 4.4(c) shows a part of the geometry of a junction trap. Fig. 4.4(a) shows the electric potential along z at the position where the electrical potential of the ion, β, is at maximum along the ion's path. Fig. 4.4(b) shows the electric potential at a linear trapping region where Ξ is a constant. The ion experiences the maximum electric potential at (a)'s position, therefore the RF barrier of the trap is defined as $\Lambda = \beta/\Xi$. Techniques and results on reducing RF barrier will be discussed and presented in section

4.2.3.

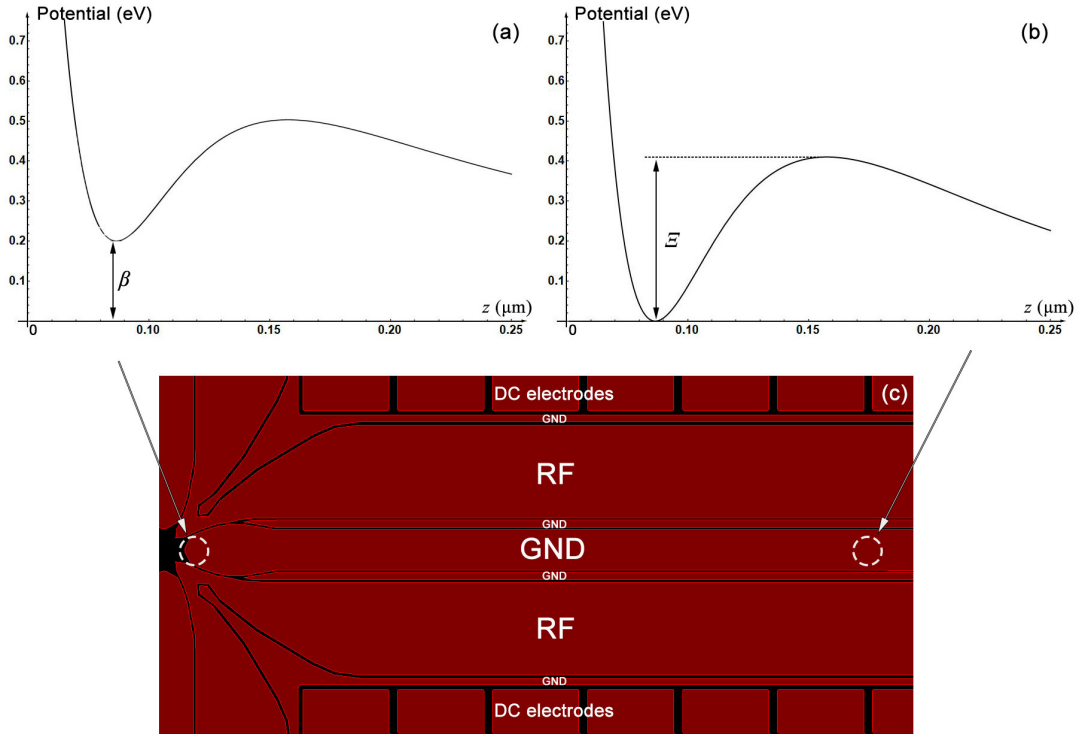

Figure 4.4: The definition of RF barrier. **(a)** the electric potential along z at a position near the junction centre where β is a maximum, **(b)** the electric potential along z at a position in a linear trapping region where the trap depth Ξ is a constant and **(c)** part of the electrode geometry of a junction ion trap.

4.2.2 Optimisation using pseudostatic methods

A static simulation tool (ENT) was used to find the pseudopotential of the ion traps. For a better comparison between different designs, the trap depths of the linear regions are normalised.

Fig. 4.5 (b) shows the unoptimised geometry where the two pairs of linear electrodes simply join together. In this unoptimised geometry, the junction is at the centre of the chip where two pairs of RF electrodes joins. The RF electrodes on the four arms are identical and the linear trapping region where RF electrodes remain the same width starts at 1.5 mm away from the centre. The linear trapping region produces a trapping field with 150 μm ion height.

From the simulation result, the ion height and pseudopotential remain relatively constant from $x = -0.5$ mm (furthest away from the junction) until $x = -0.13$ mm where the pseudopotential becomes firstly lower then sharply higher. Near the junction centre, the ion height sharply increases as the ion is impacted by both of the linear sections. The

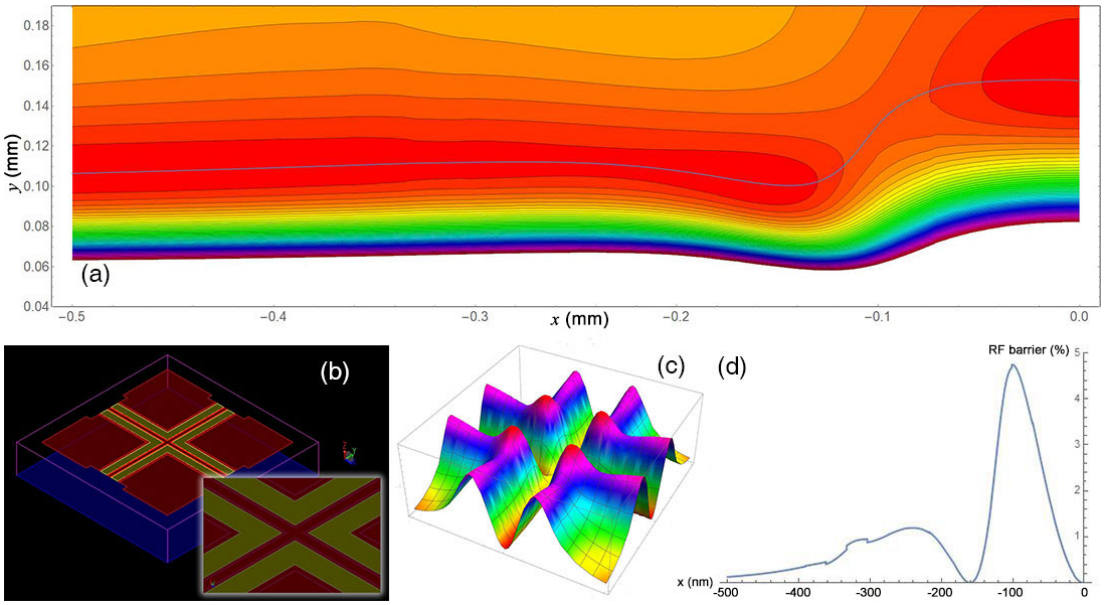

Figure 4.5: **(a)** The potential along x axis from the linear section to the centre of the junction. **(b)** Unoptimised X junction geometry with ground electrodes marked red and RF electrodes marked yellow. **(c)** The pseudopotential of the junction. **(d)** The RF barrier along x axis.

maximum RF barrier of this geometry is about 5%.

To reduce the barrier, in an optimised design shown in (b) in Fig. 4.6, the widths of the RF rails are shrunk in the junction, producing a much lower maximum RF barrier of 3%.

Several attempts were made before a further optimised geometry is found. Such geometry features pointy RF rails and grounds towards the centre and the four small patches of ground electrode surrounded by RF electrodes. The optimised geometry and corresponding field plot are shown as (b) and (c) in Fig. 4.7. The maximum RF barrier near the junction centre is only 0.2% and the maximum RF barrier of the whole chip is only 1.7% which is contributed by the linear-to-junction transition area. The transition from a linear to junction needs to be smoothed out by using a Bézier curve on the electrode profile.

4.2.3 Optimisation using dynamic methods

So far only the static tool was used to evaluate the electric field for its short computation time and low computational resources consumption. To fully optimise the geometry, the revised optimised trap was simulated in the DST where the E field distribution is solved using a full-wave method rather than electrostatically. The simulation of the optimised junction geometry gives Fig. 4.8 where it is obvious that the E field is stronger near the centre of the junction due to a higher current density. This yields a slightly higher RF

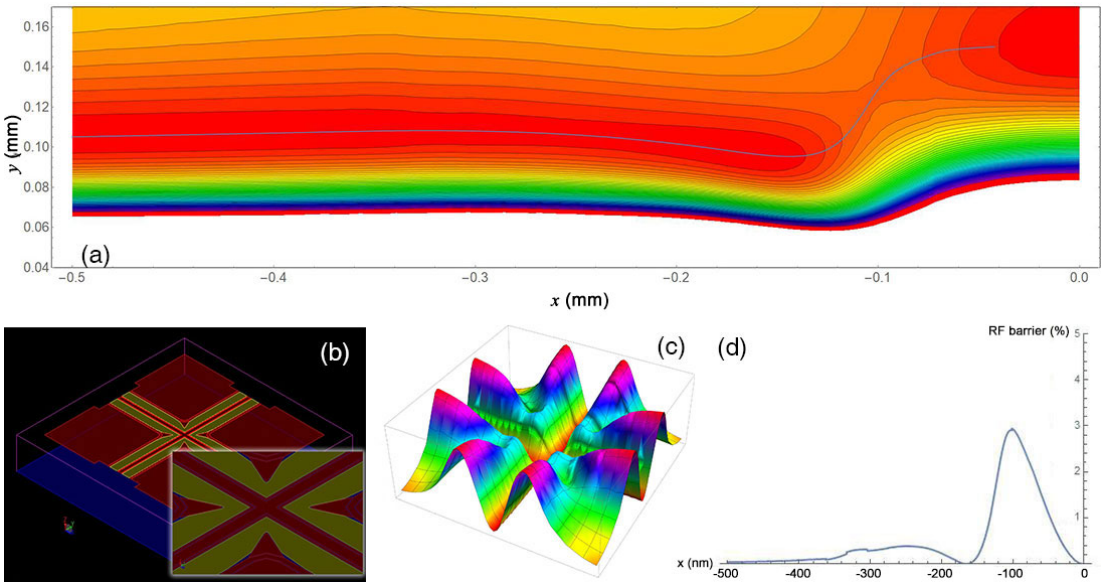

Figure 4.6: **(a)** The potential along x axis from the linear section to the centre of the junction. **(b)** The X junction geometry with smaller RF electrodes near the junction. **(c)** The pseudopotential of the junction. **(d)** The RF barrier along x axis.

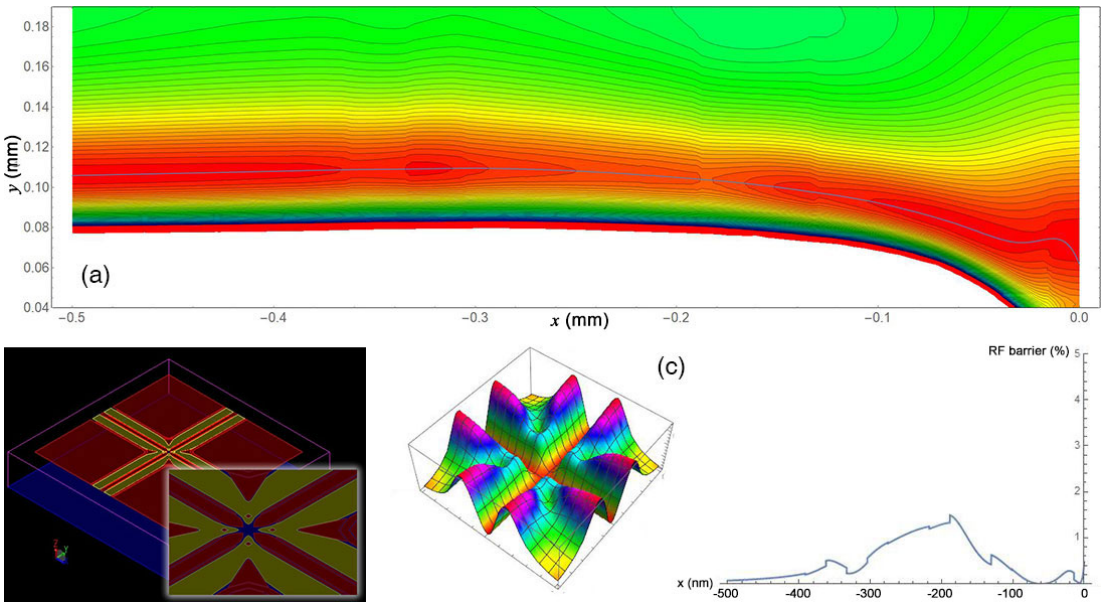

Figure 4.7: **(a)** The potential along x axis from the linear section to the centre of the junction. **(b)** Further optimised X junction geometry with ground electrodes marked red and RF electrodes marked yellow. **(c)** The pseudopotential of the junction. **(d)** The RF barrier along x axis.

barrier compared to the barrier obtained with the static method. This requires that the widths of the RF rails be adjusted. The final optimised geometry produces a maximum RF barrier of only 0.3%, see Fig. 4.9.

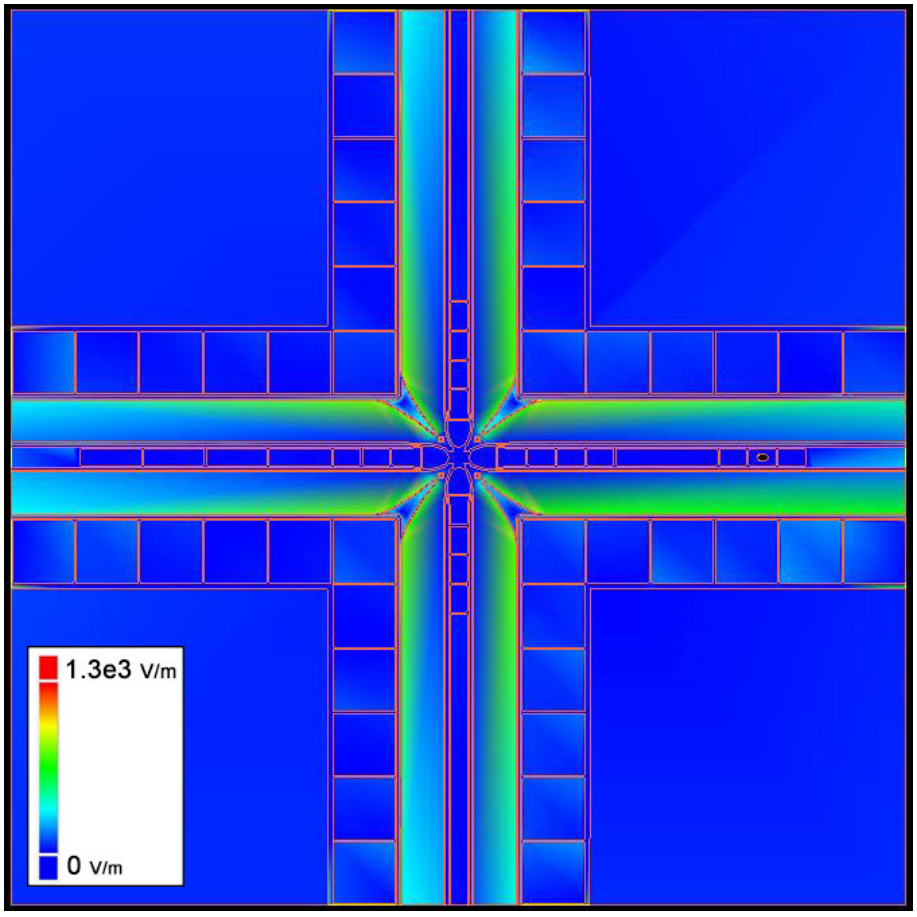

Figure 4.8: The E-field strength distribution of the junction geometry on the chip surface at a single unit input power. The power input is at the right arm. The RF is connected using VIAs so that RF signals can travel to another arm with little loss.

To show that the ion can shuttle stably through the final optimised junctions, a simulation based on [51] was performed. The travelling paths of the ions calculated is shown in Fig. 4.10. The similar optimisation process was used in designing the geometry of an optical detection slot where the central ground electrode was modified to allow photons emitted by the ion to be collected by the photon detectors underneath the chip. This increases the collection efficiency of the photons thus the gate fidelity. The electrode is fabricated with indium tin oxide (ITO), an electrically conductive and optical transplant material. An optimised detection slot (see the layout in appendix B) was obtained with only 0.2% RF barrier.

The optimisation was done manually and was consisted of more than 80 different interval designs. Such optimisation can be done much faster using a machine learning algorithm.

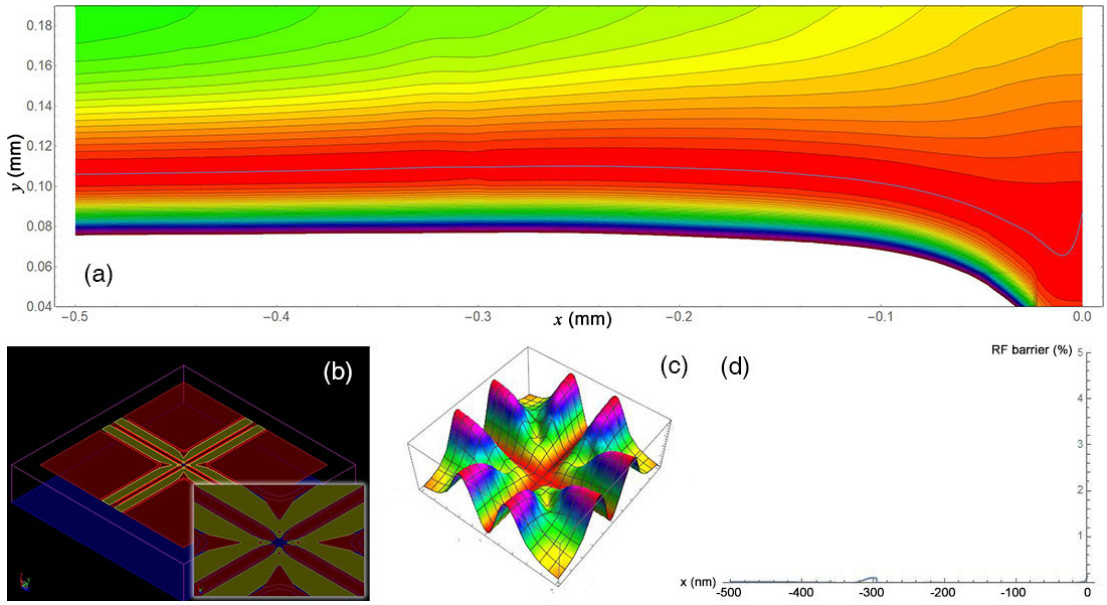

Figure 4.9: **(a)** The potential along x axis from the linear section to the centre of the junction. **(b)** Fully optimised X junction geometry with ground electrodes marked red and RF electrodes marked yellow. **(c)** The pseudopotential of the junction. **(d)** The RF barrier along x axis, the maximum RF barrier is only 0.2%.

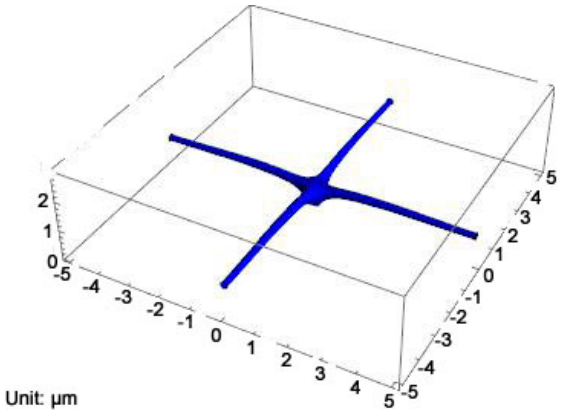

Figure 4.10: The travelling paths of multiple ions during a shuttling process on an ion trap with the fully optimised junction geometry shown in 4.9.

4.3 High Rabi frequency using integrated microwave cavity

As explained in section 3.1, it is practically impossible to operate laser gate based quantum computers in large scale due to the massive number, real-time control and precise alignment of the lasers required. Section 3.1.1 points out that the community is focusing on and have demonstrated gate schemes using long-wavelength radiations in RF and microwave regime. High fidelity single and two-qubit gates were demonstrated at as fast as 1.6 μs, but gates with superconducting qubits have easily achieved tens of nanosecond gate time. This means that when several operations are required in computing, a trapped-ion based quantum computer may take considerably longer time despite its high fidelity. Long gate time also impedes the implementation of the trapped ion being used as a practical quantum simulator. The key to achieving 'quantum supremacy' is to develop and demonstrate a fast quantum gate with high fidelity. In this section, the delivery of long-wavelength radiations in microfabricated ion traps was discussed. Several methods to improve the field-ion coupling and an ion trap design with a high clock rate suitable for scalable quantum computers were demonstrated.

4.3.1 Rabi frequency

In atomic quantum computing, quantum information is often encoded with either hyperfine ground or meta-stable excited atomic states. These states provide well-defined quantum bits (qubits) with long coherence times. Quantum computing is performed by manipulating the qubit states allowing for precisely switchable interactions using a laser or RF radiation. The manipulation needs to be done with high fidelity and speed. High fidelity is essential to the realisation of complicated quantum algorithms. High computing speed is ever required by the growing demand for computing power. As explained previously in section 3.1.1, quantum gates with cold ions are relatively slow compared to superconducting qubit gates. There are two ways to improve. D. De Motte [72] outlined a hybrid system where cold ions are used as storage qubits and superconducting qubits as computing qubits. The hybrid system is challenging to engineer. It requires an ultrastable cryogenic environment, stress-free superconducting films and a strong coupling between the superconducting qubit and the ion. Alternatively, high-speed gates can be developed by increasing the coupling between the inducing fields and the ion. In this section, designs and methods to improve the atomic clock rate using strong field coupling are presented.

A microwave or RF pulse applied to the ion whose photon energy matches the energy gap between a pair of states will cause the state of the ion to oscillate between these two states. The frequency of this atomic transition in the presence of such an oscillatory driving field is known as 'Rabi frequency':

$$\Omega = \frac{\vec{\mu}\dot{\vec{B}}_{\mathrm{mw}}}{\hbar} \tag{4.3}$$

where

$$\vec{\mu} = \frac{2\mu_B}{\hbar}\vec{J} \tag{4.4}$$

and

$$\vec{B}_{\mathrm{mw}} = (B_x e^{-i\phi_x}, B_y e^{-i\phi_y}, B_z e^{-i\phi_z}). \tag{4.5}$$

$\vec{B}_{\mathrm{mw}}$ is the B field vector of the microwave or laser radiation. The magnetic dipole momentum for the hyperfine splitting transition of the ion between $\langle\downarrow|$ and $|\uparrow\rangle$ can in general be written in form of $\vec{\mu}_{\downarrow\uparrow} = \langle\downarrow|\,\vec{\mu}\,|\uparrow\rangle$.

For $^{171}\mathrm{Yb}^+$, the nuclear spin is $I = 1/2$ and for the hyperfine splitting of the ground state $^2S^1_{1/2} J = 1/2$, $S = 1/2$ and $L = 0$. Magnetic dipole momentum μ_{B} for ytterbium is 9.274×10^{-24} A/m^2. In MAGIC scheme, the microwave magnetic field couples to the magnetic momentum of the electron spin of the ion. The Rabi frequency of the $^{171}\mathrm{Yb}^+$ hyperfine transition $|F = 0, m_F = 0\rangle \rightharpoonup |F' = 1, m'_F\rangle$ is

$$\Omega_{0,0}^{1,m'_F} = 2\vec{\mu}_B/\hbar \left\langle 1, m'_F\right| \vec{J}\dot{\vec{B}}_{mw} \left|0, 0\right\rangle . \tag{4.6}$$

where $m'_F = -1, 0, 1$. The scalar product $J\dot{B}_{\mathrm{mw}}$ is

$$\begin{aligned} J\dot{B}_{\mathrm{mw}} = & \quad B_x e^{-i\phi_x} J_x + B_y e^{-i\phi_y} J_y + B_z e^{-i\phi_z} J_z \\ = & \frac{1}{2}(B_x e^{-i\phi_x} - iB_y e^{-i\phi_y})J_+ + \frac{1}{2}(B_x e^{-i\phi_x} + iB_y e^{-i\phi_y})J_- + B_z e^{-i\phi_z} J_z \end{aligned} \tag{4.7}$$

where B_x, B_y, B_z are the components of B_{mw} along the corresponding axes. According to Böhi [96], the Rabi frequencies are

$$\begin{aligned} \Omega_- = & \Omega_{0,0}^{1,-1} = \frac{2\mu_B}{\hbar} \langle 1, -1| \frac{1}{2}(B_x e^{-i\phi_x} + iB_y e^{-i\phi_y})J_- \left|0, 0\right\rangle \\ \Omega_\pi = & \ \Omega_{0,0}^{1,0} = \frac{2\mu_B}{\hbar} \langle 1, -1| B_z e^{-i\phi_z} J_z \left|0, 0\right\rangle \\ \Omega_+ = & \ \Omega_{0,0}^{1,1} = \frac{2\mu_B}{\hbar} \langle 1, -1| \frac{1}{2}(B_x e^{-i\phi_x} - iB_y e^{-i\phi_y})J_- \left|0, 0\right\rangle . \end{aligned} \tag{4.8}$$

Solving the equations above produces

$$\begin{aligned} \langle 1,-1|\, J_- \,|0,0\rangle &= \sqrt{\frac{1}{2}}\hbar \\ \langle 1,-1|\, J_z \,|0,0\rangle &= \frac{\hbar}{2} \\ \langle 1,-1|\, J_+ \,|0,0\rangle &= -\sqrt{\frac{1}{2}}\hbar. \end{aligned} \tag{4.9}$$

So the Rabi frequencies are

$$\begin{aligned} \Omega_- &= -\sqrt{2}\frac{\mu_B}{\hbar}B_- e^{-i\phi_-} \\ \Omega_\pi &= \frac{\mu_B}{\hbar}B_\pi e^{-i\phi_\pi} \\ \Omega_+ &= \sqrt{2}\frac{\mu_B}{\hbar}B_+ e^{-i\phi_+} \end{aligned} \tag{4.10}$$

where

$$\begin{aligned} B_- e^{-i\phi_-} &= \frac{1}{2}(B_x e^{-i\phi_x} + iB_y e^{-i\phi_y}) \\ B_\pi e^{-i\phi_\pi} &= B_z e^{-i\phi_z} \\ B_+ e^{-i\phi_+} &= \frac{1}{2}(B_x e^{-i\phi_x} - iB_y e^{-i\phi_y}). \end{aligned} \tag{4.11}$$

B_+, B_- and B_π are the real-valued amplitudes of the magnetic field components parallel to the static magnetic field which defines the quantisation axis. ϕ_+, ϕ_- and ϕ_π are the corresponding phase components of them. The physical interpretation is that on a Bloch sphere [4], the phase decides which meridian will the Bloch vector go along.

To calculate the Rabi frequency in a given microwave field, the B components and their phase information are needed. By physically realigning the magnets, B_x and B_y can be nulled giving the Rabi frequency Ω

$$\Omega = \Omega_\pi = \frac{\mu_B}{\hbar}B_z e^{-i\phi_z}. \tag{4.12}$$

Choosing $\phi_z = 0$, it is then obvious that Ω is proportional to the z component of the B field strength at ion's position.

[4] Bloch sphere is a geometrical representation of the pure state space of a two-level quantum mechanical system (qubit).

4.3.2 Microwave delivery systems

Horn

Most commonly, ion trappers use horns to broadcast microwave at cold ions [37,80,82,97–99]. High fidelity was reported and they are easy to make and maintain. However, horns suffer from a key problem making them not efficient or scalable.

Horns are hardly efficient. The radiation from a horn produces interference fringes due to the reflection from chamber walls and the chip surface. Since it is practically impossible to predict the maximum positions of the field, a high-power horn is required to guarantee the coupling strength. However, a high-power horn is not efficient and its excessive radiation can cause potential health and safety hazard to the operators. Even at high-power output, a single horn still has a limited power to cover arrays of ions required. Radiation from multiple horns causes interference. The coupling between the field and the ions varies in space due to interference and attenuation. The produces varying gate frequencies and Zeeman splits across the chip making it hard to perform gate operations or individually address ions. Horns are therefore not suitable for arrays of traps in a scalable quantum computer.

Patch antenna

Instead of using a horn at a distance, a small, compact patch antenna that can fit in the vacuum system at proximity to the cold ions. A patch antenna is a planar structure that can be made on a piece of vacuum-compatible PCB. The patch antenna was designed for the cryogenic system described in section 2.5.2 and optimised to operate at 12 GHz, this is because it is estimated that the PCB material will shrink in size at cryogenic temperatures, shifting to a higher centre frequency. The impedance of the antenna is designed at 377 Ω for the maximum radiation into freespace [5]. It is matched to a 50 Ω SMA connector using the combination of an open-stub and two notches. The design and predicted results are shown in Fig. 4.11. The fabrication and testing of the resonator are detailed in [75].

[5] The impedance of freespace is a physical constant $Z_0 = \mu_0\varepsilon_0 \approx 376.73\ \Omega$ where μ_0, ε_0 are magnetic constant and electric constant respectively. For discussion on impedance mismatch, see section 6.2.

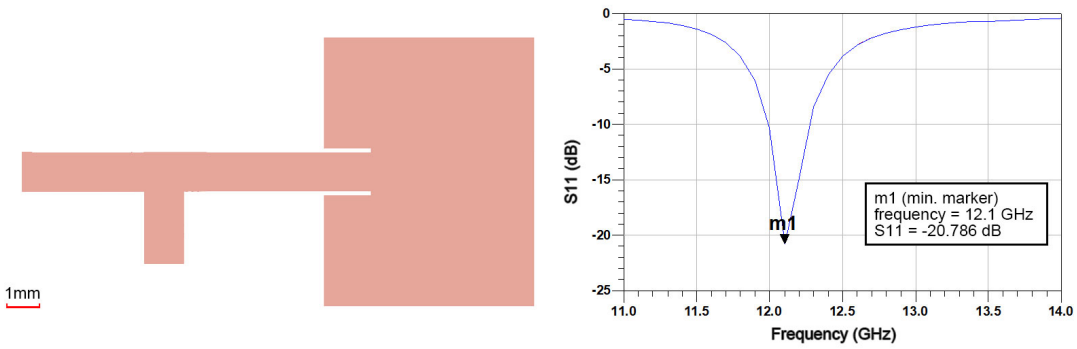

Figure 4.11: **(left)** The design of the patch antenna. SMA connector sits on the left end of the stub. The open-stub and two notches transform the input impedance to 377 Ω. **(right)** Simulation result of S_{11} plot at room temperature. The centre frequency is 12.1 GHz

Imaging tube waveguide

This method is a far-field method using the imaging tube as a waveguide. Instead of placing a horn or patch antenna aside the trap, the imaging tube, made of conductive metal and directing at the chip surface, is a waveguide structured directed at the chip. A simulation was performed where a copper imaging tube of 64.4 mm tall, 18.05 mm radius and 1 mm in thickness is fed with a 12.64 GHz source. A viewport is placed at the end of the imaging tube which is 5 mm thick, 55 mm in radius with a 30 mm radius hole. This stainless steel viewport is electrically grounded with the tube. The chip is placed 16 mm away from the tube end. The waveguide carries 2 TE_{11} modes with vertical and horizontal field orientations. The simulation shows that at 1 W power input, an average 2.47 A/m H field can be expected for trapped ions. Careful positioning of the trap will be required for the high field strength at the ion position due to the RF boundary conditions of the setup. In section 4.5.1, an updated design with metal mesh on viewport is presented. The metal mesh can reduce the exposed dielectric window surface at the sacrifice of the H field strength.

Similar to this method, simulations were reported on using a coil fitted at the viewport window [81].

Near-field and far-field designs

The methods discussed above use far-field radiation. The far-field radiation covers a wide area including multiple trapping sites. It is impossible to tune the coupling of the field to the trapped ions individually. The interference between microwave emitters makes the

coupling strength unpredictable. These methods are also oversized for a scalable quantum computer.

An alternative to the far-field methods are the near-field emitters. Depending on the nature of the waveguide structure, near field designs can be categorised into the travelling wave designs and the standing wave designs depending on the nature of the wave in the structure. A travelling wave design example is [100] where a 3D microwave circuitry was integrated to couple with a Be ion 35 µm above resulting in a Rabi frequency of 200 kHz. Standing wave designs were reported [79] where a half-wavelength cavity is used to form a null at a cold Ca ion 75 µm above the surface. So far, there is no near-field microwave delivery method reported for Yb ions using the MAGIC scheme. To develop a fully scalable quantum computer, it is essential to have a highly integrated microwave delivery method achieving a high clock rate.

Anti-Parallel Wires

A novel near-field design was proposed by the IQT group. It is called 'Anti-Parallel Wires' (APW), a travelling wave method design. Previously, Dr Navickas reported the design and implementation using stripped coax cables [101]. But it suffers from problems including reduced laser access, requiring fine alignment of the wires and inefficient microwave delivery.

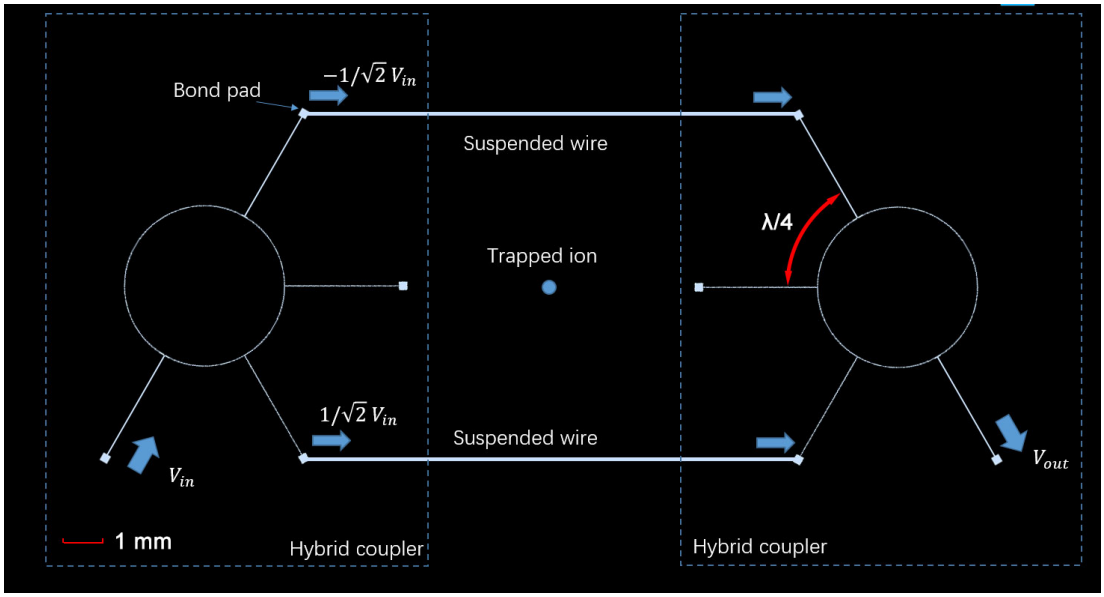

Figure 4.12: Schematic of the Anti-Parallel Wires. The suspended wires are not to scale. The hybrid couplers (inside the dashed boxes) are scaled as noted. The left hybrid coupler splits the input signal into two with equal amplitude but 180° difference in phase. The output signal is the recombined signal from the two wires.

The improved design is shown in Fig. 4.12 where a pair of wires is suspended above the ion trap carrying microwave currents going in opposite directions. The wires are of equal impedance forming a balanced line or balanced signal pair. The balanced line is resistant to external noises, the principle behind is explained in textbooks [102]. Using Ampère's right hand rule, it is found that an additive magnetic field exists between the wires. The polarisation of the field is dependent on the phase between the two wires. A simulation was performed where a pair of wires sitting 422 µm apart carries 1 W power in total. The diameters of the wires are 30 µm. The impedance of the wires are therefore 400 Ω. The impedance of the microwave source is matched to the wires. The wires are 10 mm long, sit in free-space. By setting the wires to have opposite phase, the magnetic field oscillates along the quantisation axis. Fig. 4.13 shows the simulated H field distribution of the setup. The ion sits 200 µm above the plane of the wires. The expected H field strength is about 16 A/m. Compared to the horn used in [37], the Rabi frequency in this setup is expected to be 3 times higher.

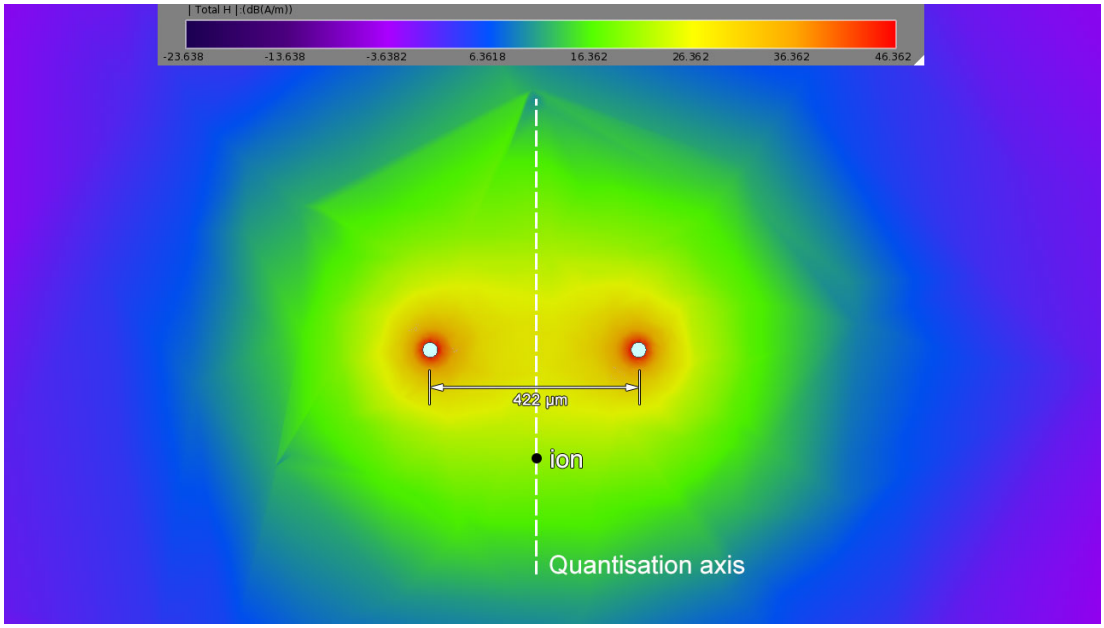

Figure 4.13: The simulated H field distribution of the Anti-Parallel Wires. The quantisation axis is normal to the trap surface.

To guarantee an equally divided current and an equal impedance in each wire and to provide mechanical attachment of the wires, a hybrid ring coupler was designed (shown inside the dash line boxes in Fig. 4.12). The hybrid ring coupler equally splits an input signal with 180 degrees difference in phase. This is because the electrical length is a quarter wavelength between the two ports sitting at 60 degrees apart. To maximise the radiation, the impedance of the wires and the coupler were designed to be 350 Ω, close

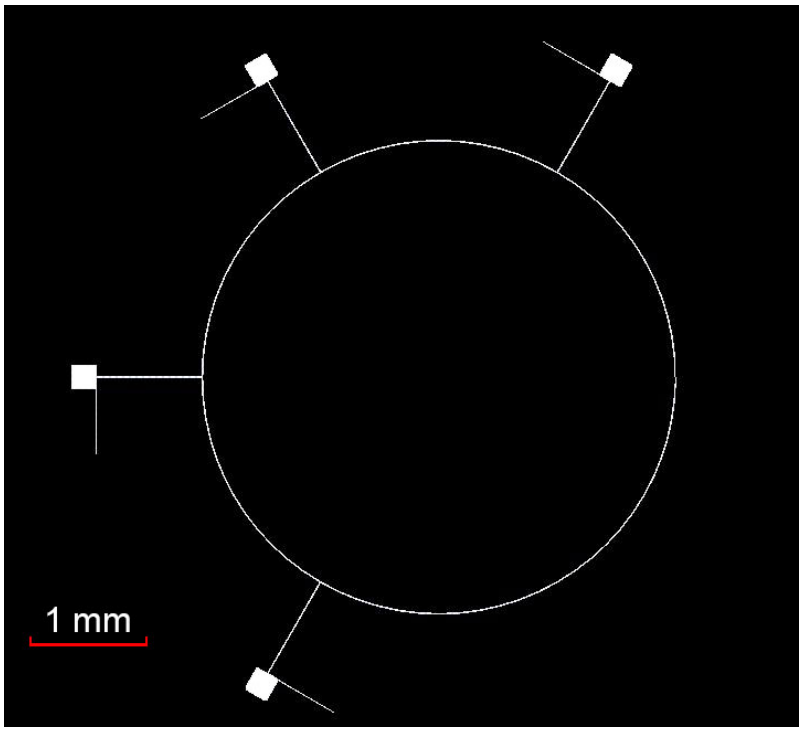

Figure 4.14: An alternative design of the hybrid ring with open-stub impedance transformer.

to 377 Ω, the impedance of freespace. This results in a very small electrode width of 5.7 μm. The rings were fabricated along with other ion trap chips sharing the same mask (B.7) and fabrication processes. The connection between the bond pads and the ring is a tapered microstrip impedance transformer. An alternative hybrid ring design is shown in Fig. 4.14 where open-stub impedance transformers are used.

Integrated microwave cavity

The APW requires precise alignment of micron-scale devices which is less ideal for scalable quantum computers. Yet a novel design, known as the 'integrated microwave cavity', was developed. It uses a standing wave on a three-quarter-wavelength ($3\lambda/4$) cavity fabricated in place of the central ground electrode in a linear trap.

The $3\lambda/4$ cavity holds a standing electromagnetic wave of 12.64 GHz as shown in Fig. 4.18. It transforms an open circuit on end A to a short circuit on end B. A current antinode (marked 'C') is a quarter wavelength away from end A. From Ampère's circuital law, it is known that at C position, a maximum B field strength can be expected. This resonator cavity is noise-rejecting also. At resonant, end B behaves like a short-circuit ($Z = 0$). When the frequency of the noise is other than 12.64 GHz, the cavity has higher

impedance.

The design of such a cavity starts with the calculation of the wavelength in the particular waveguide structure. In this work, an asymmetric 120 µm ion height trap is used. The central ground electrode of this trap is 70 µm wide. The RF electrodes are grounded to the microwave ground. The structure makes a coplanar waveguide as shown in Fig. 4.15. By using 'linecalc'[6], the effective dielectric constant of this structure is estimated $\varepsilon_{\text{eff}} = 5.3$. The microwave wavelength in such a structure is then $\lambda = c/(f\sqrt{\varepsilon_{\text{eff}}})$ where c is the speed of light and $f = 12.64$ GHz. The three-quarter-wavelength is $3\lambda/4 = 7.71$ mm. In the next section, the simulation of the cavity is described in details based on the design in this section.

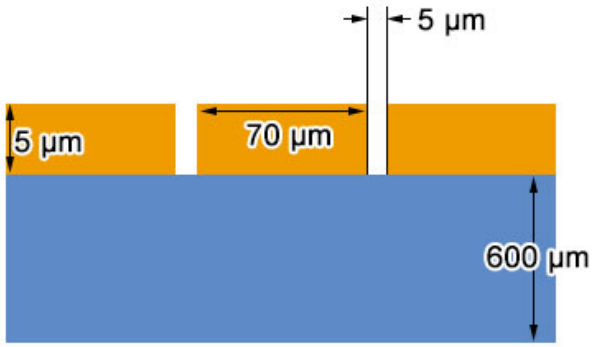

Figure 4.15: (Image not to scale) CPW structure used for the microwave cavity. The ■ substrate is 600 µm thick sapphire. The ■ electrodes are 5 µm thick gold. The gaps between electrodes are 5 µm. The central electrode is 70 µm wide. The side grounds are significantly larger than the central.

4.3.3 Integrated standing wave microwave cavity

In the sections above, it is demonstrated that a high Rabi frequency can be achieved by a strong microwave B field coupled to the trapped ions. Several different methods to deliver such a field were discussed including both near-field and far-field methods. In this section, the design and simulation of the integrated microwave cavity described in the last section is detailed.

Optimising the cavity and the feed

It was estimated that in the 120 µm ion trap structure, $3\lambda/4 = 7.71$ mm. A geometry consisted of a $3\lambda/4$ long CPW with ion trap electrodes (as shown in Fig. 4.16(a)) was

[6] A tool by Keysight.

imported into DST, the dynamic simulation tool mentioned in section 4.1. The CPW is directly excited by a 50 Ω microwave feed. The S-parameter of the feed port was calculated, noted as S_{11}. The phase of S_{11} is defined by the difference between the forwarding and reflected voltage signals. As explained in the last section, the $3\lambda/4$ cavity transforms the open circuit at the far end to a short circuit at the near end. To optimise the length of the cavity, the target is to let the phase of S_{11} equal to 180°. The simulated result is shown in Fig. 4.16(c). The optimised cavity length was found $l = 7.05$ mm. This result is confirmed by the fact that at 12.64 GHz, the S_{11} magnitude is a minimum (Fig. 4.16(b)).

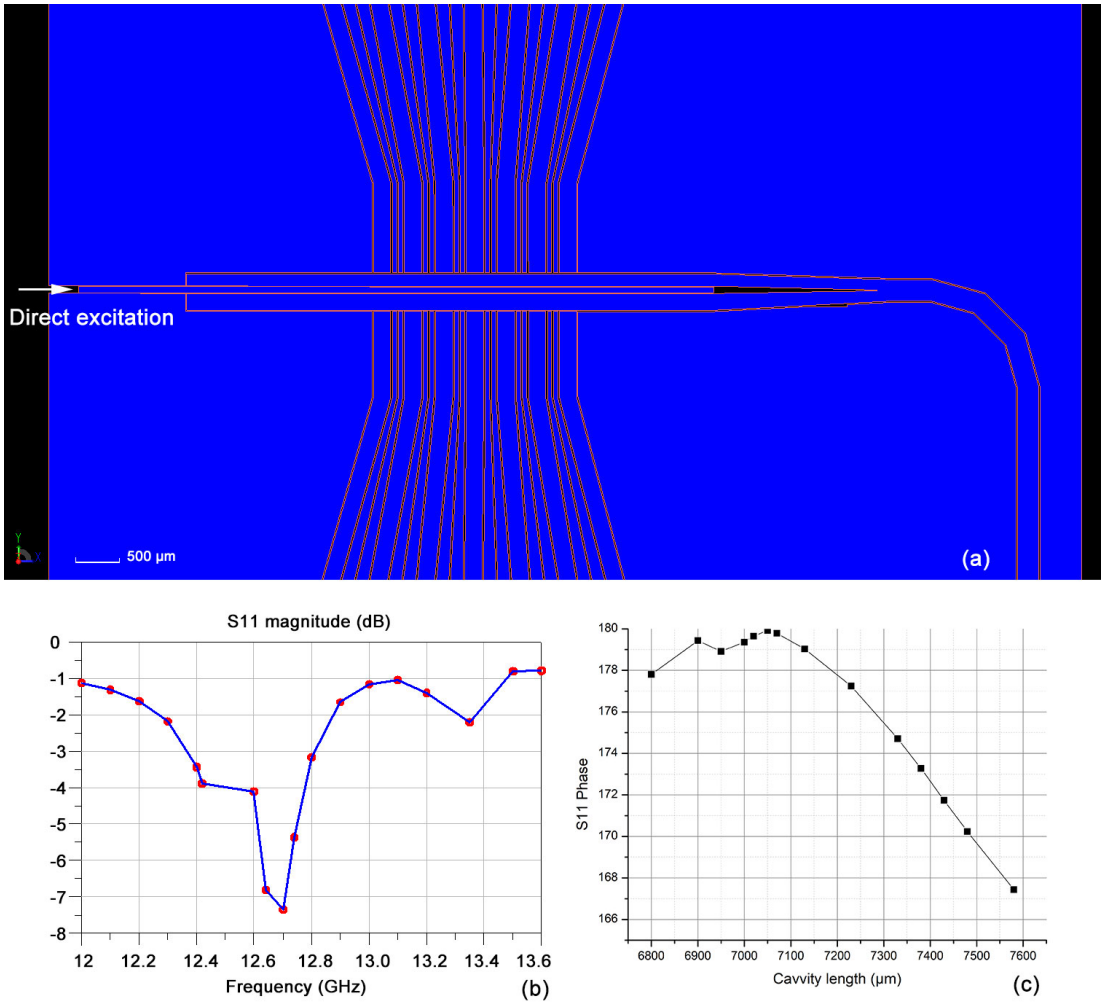

Figure 4.16: (**a**) Geometry of the microwave cavity with a virtual direct feed. (**b**) Magnitude of S_{11} at different frequencies at optimal length. (**c**) Change of S_{11} phase with the cavity length.

The cavity cannot be directly fed at the centre of the chip edge due to blocking the laser access. A feedline waveguide was designed to accommodate the microwave feed. The feedline is a CPW waveguide laying vertical to the cavity, running through the whole

chip. To reduce impedance mismatch and provide enough space for wirebonding, a tapered impedance transformer is designed, see Fig. 4.17. It transforms the 50 Ω wirebond feed to the 31 Ω waveguide. Fig. 4.17 shows the simulated magnetic field strength distribution on the chip surface. The cavity acts like a short circuit making the current go to the cavity rather than to the right hand side.

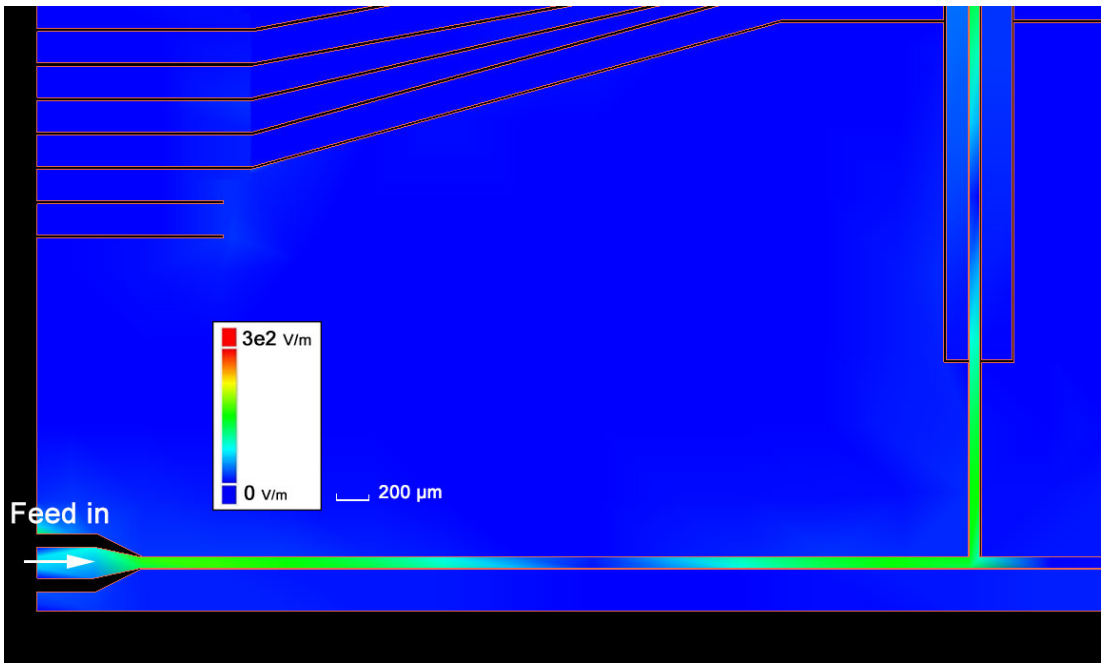

Figure 4.17: The left half of the feedline of the cavity and the simulated magnetic field strength distribution on the chip surface. The right hand side is the exact mirror. The cavity acts as a short circuit making the current prefer to go into the cavity rather than to the right.

Magnetic field generated

So far the cavity and its feed have been designed and optimised, in this section the field emitted from the structures is studied. A commercial numerical software EMPro was used to simulate the B field. To validate the simulation method and model setup, two published results [67, 79] were reproduced. The calculated results were similar to the reported experimental data (see table 4.1). The deviation is expected due to systemic error and the RF loss which is not measurable[7].

Having established a valid simulation method, the cavity design was designed, optimised and simulated. The electrodes are 4 µm, higher than the skin depth at the microwave frequency (0.67 µm). A 50 Ω CPW feed line was designed to impedance match the input

[7]The RF loss is modelled as a constant 1 dB loss in the simulation model.

Table 4.1: Comparison between the simulated and reported Rabi frequency and B field strength.

Item	Simulated	Reported
Ω_π [79] (MHz)	50-52	53
B field strength at port 2 [67] (μT)	20	24.4

wirebond pairs. The simulated microwave B field strength is plotted in Fig. 4.18. The microwave forms a standing wave along the trapping rail. At the maximum position, the simulation predicted a resultant $\Omega_\pi = 3.6$ MHz given 1 W input power. Compared to the current setup where a 1 W horn was used to produce free-space radiation resulting in $\Omega_\pi = 80$ kHz [37], the $3\lambda/4$ cavity is 45 times better.

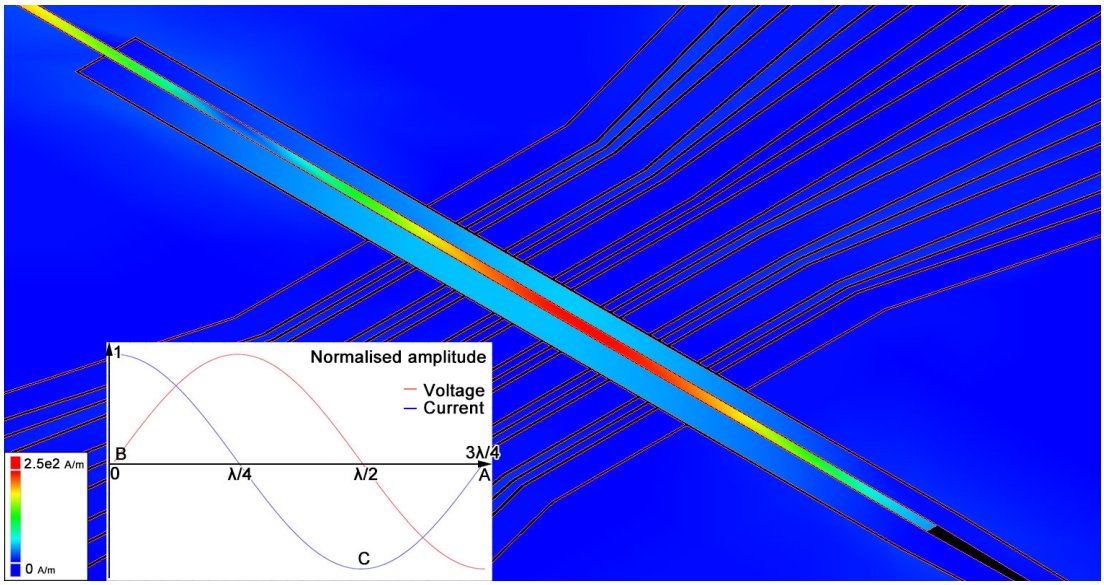

Figure 4.18: Simulated magnetic field strength distribution on the chip surface. The scale of the chip is found in Fig. 4.16. The inset shows the relative amplitudes of the voltage and current on the cavity (along the centre of the cavity, the input side is noted as $x = 0$). At the cavity end A ($x = 3\lambda/4$), the circuit is open. At the input end B ($x = 0$), it is transformed into a short circuit. At C position, a maximum B field strength can be expected.

The cavity is compact, easy to fabricate and capable of delivering high B field strength at ion's position. Compared to other methods reviewed earlier, this design does not require precision mechanical alignment or extra space in vacuum. This design is fully scalable because the coupling of the field to each ion can be individually controlled and there is no crosstalk or interference between trapping areas. The strong coupling produces a predicted 45 times increase in Rabi frequency which can potentially increase the computing speed of the scalable quantum computer.

4.4 Current Carrying Wires for high gradient static magnetic field generation

As outlined in section 3.1, the quantum gates implemented using MAGIC scheme requires a high static magnetic field gradient. This large B field gradient can be delivered using permanent magnets or metal wires with a large current passing through them, known as Current-Carrying Wire (CCW) structures. Permanent magnets have been successfully used to demonstrate a microwave-based gate in [70] with 20-40 T/m. A maximum gradient of 157.4 T/m was predicted from simulations on permanent magnets [81]. The implementation of permanent magnets relies on the precise physical placement of the magnets, a small displacement will cause a strong Zeeman shift making Doppler cooling impossible.

The CCW structures are fabricated into the substrate prior to ion trap fabrication which is inherently scalable as it shares the same fabrication technologies used in ion trap fabrication. The CCW structures are driven by a large current, generating a strong static field gradient. The position of the magnetic field to the trapped ions is guaranteed by a microfabrication technique which is easier to implement and more accurate than manual placement of permanent magnets. Moreover, the CCWs can be easily tuned or completely switched off before and during the trapping, making no disturbance to the trapping or cooling process.

There are several challenges that have to be addressed. The geometry of the CCW has to be optimised for a maximum field gradient and zero field strength at the RF nil position. The thermal dissipation of the structure due to a large driving current passing through has to be considered. Effective cooling methods have to be provided.

4.4.1 Magnetic gradient generated from an integrated structure

To achieve high magnetic field gradient at the RF nil, an anti-parallel configuration was designed by Dr Eamon Standing [81] where a pair of wires are placed in parallel and the currents in the flow in opposite directions. Based on Dr Standing's work, Raphaël Lebrun investigated in the optimisation of the geometry to yield a maximum gradient with a zero field strength for various ion heights. The optimised geometries for 250 μm ion height are presented in Fig. 4.19. Due to the large current passing through, the wires have to be made thick. In the optimised geometries above, the wires are 30 μm thick.

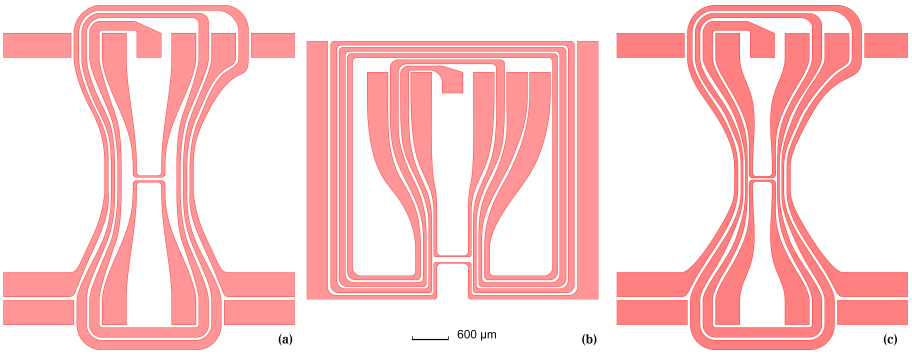

Figure 4.19: The optimised geometries of CCW structures with different ion heights designed by Raphaël Lebrun. **(a)** 160 µm ion height, maximum gradient along the trapping axis 103.2 T/m with 12 A current, **(b)** 235 µm ion height, maximum gradient along the trapping axis 235 T/m with 12 A current, **(c)** 110 µm ion height, maximum gradient along the trapping axis 204 T/m with 12 A current.

When choosing the correct material to create the structures, several factors have to be considered. First, the material used has to have a high electrical and thermal conductivity to avoid excessive heating such as gold, silver, copper and aluminium. However, due to the electromigration effect, the large current passing through the wires will cause voids in the metal crystals and consequentially fails. J. Black *et al.* [103] investigated such effect and proposed the Black's equation to evaluate the Mean Time To Failure (MTTF),

$$\text{MTTF} = \frac{A}{j^n} e^{\frac{E_a}{kT}} \tag{4.13}$$

where A is a constant, j is the current density, n is a model parameter, E_a is the activation energy of the material, k is Boltzmann's constant and K is the temperature of the device. A and n are experiment-specific parameter not universal. To improve the MTTF, a high activation energy E_a material is desired, see table 4.2. Although silver has the highest electrical and thermal conductivity, it has a very low electromigration activation energy thus not reliable. Aluminium is not suitable due to having the lowest activation energy. Copper is the second-best in term of thermal and electrical conductivity and the highest electromigration activation energy thus an ideal candidate. Gold is second to copper in the term of conductivities yet still have relatively high activation energy. It can be an alternative to copper in the case that the foundry or cleanroom used does not allow copper[8].

Second, the material has to be deposited in bulk with ease. Depositing a 30 µm tall structure is challenging in microfabrication due to the intrinsic stress and the cost being high to

[8]Copper is a diffusive material thus often unwanted by clean rooms, especially by the CMOS foundries. Southampton Nanofabrication Centre does not allow copper.

Table 4.2: Electrical properties of the materials used in CCW fabrication.

Material	Bulk electrical conductivity ($\times 10^7$ S/m)	Electromigration activation energy (eV)	Thermal conductivity (W/mK)
Gold	4.1	0.92	315
Aluminum	3.8	0.6	204
Silver	6.1	0.67	407
Copper	5.8	1.2	386

be deposited with common microfabrication techniques. Copper and gold electroplating techniques can effectively reduce the cost of material and time. The cost of electroplating a 30 μm tall CCW wafer with gold is about 370 GBP[9] while thermal evaporation costs at least 8 times more [10]. When copper electroplating is used rather than gold, the cost is estimated to be merely 16 GBP per wafer [11]. In the University of Sussex, both gold and copper electroplating techniques were developed and outlined in section 6.5. Silicon substrates are used for the CCW fabrication due to its high thermal conductivity.

4.4.2 Simulation and maximum current density

The maximum gradient obtainable is limited by the maximum current allowed that passes through the structure. To find out the maximum current, both theoretical estimation and numerical simulation were done.

The power dissipated P is purely ohmic so the simple equation applies here is $P = I^2\rho l/wt$ where I is the current passing through, ρ is the resistivity of the metal used, l, w, t are the length, width and thickness of the wire respectively. In the CCW geometry shown in Fig. 4.19, the thinnest wire is only 68 μm while the widest over 200 μm, the geometry has to be subdivided into smaller sections of similar width and then integrate the whole volume for the total dissipation,

$$P = \int_l I^2 \frac{\rho \mathrm{d}l}{w(l)t(l)}. \tag{4.14}$$

Using this equation, it is estimated that a 12 A current produces about 6.2 W of heat.

A numerical simulation was performed to determine the exact heat output, the resulting thermal distribution of the structure is shown in Fig. 4.20. The total heat output given

[9] Calculation based on using Metalor ECF 64 electroplating solution and the assumption that all gold contents in the solution can be fully consumed. Price is based on the quote provided to the author by the local distributors in British pound sterling (GBP).

[10] Estimation was made based on the price offered by Southampton Nanofabrication Centre.

[11] Calculation based on using NB SEMIPLATE CU 100 copper plating solution by Microchemicals GmbH and the assumption that all copper contents in the solution can be fully consumed.

12 A passing through is 6.35 W which agrees with the theoretical estimation.

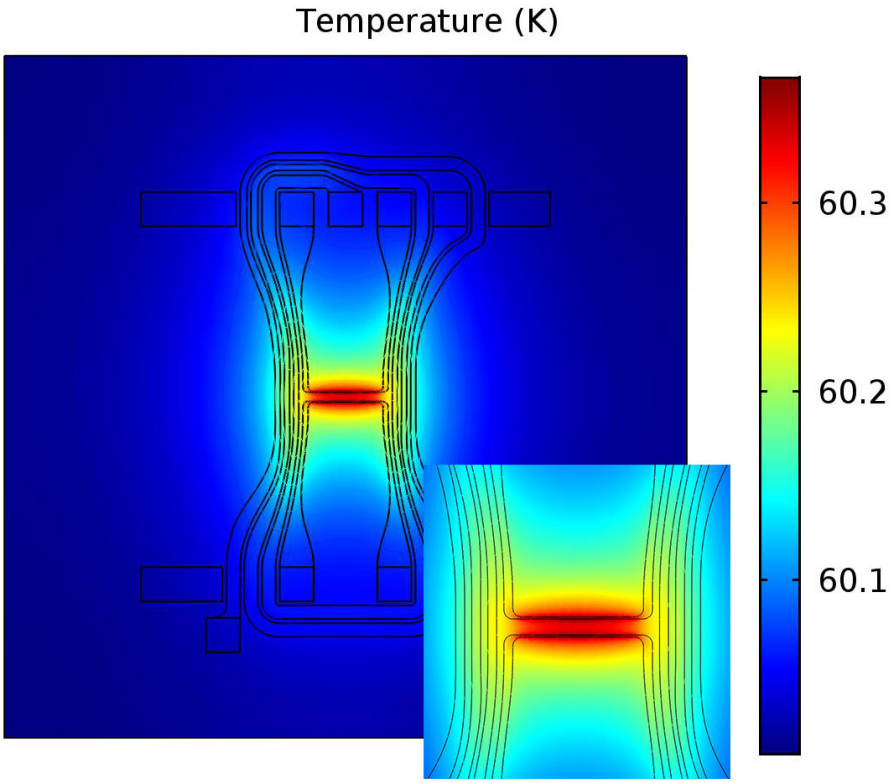

Figure 4.20: Temperature distribution of the structure shown in Fig. 4.19 (a) driven by 12 A DC current. The inset shows the detailed temperature distribution near the centre.

4.4.3 The fabrication of CCW structures

The fabrication of a CCW integrated chip consists of two parts: the fabrication of CCW structures and the fabrication of the traps. Once the CCW structures are fabricated, any planar ion traps can be made on top of it using the readily available fabrication workflow. This allows any established ion trap fabrication workflow to treat the CCW-embedded substrate as a typical silicon substrate.

The CCW structure fabrication starts with a blank silicon wafer. A 30 µm thick lamination film photoresist[12] was used for the UV lithography. Subsequentially, a Bosch process is used to create a deep trench of 30 µm deep. The silicon wafer is then loaded into a furnace for wet oxidation. A 2.5-hour process produced 555 nm of oxide as an insulation layer. The trenches are filled with a thin layer of Cr (10 nm), Pt (10 nm) and Au (200 nm). The wafer is electroplated with copper until all the trenches are filled. The excess amount of copper is Chemical-Mechanical-Planarised to flat[13]. With a 3 µm PECVD oxide insulation

[12] Ordyl AM 130.
[13] The process is known as a Chemical-Mechanical-Planarisation (CMP) process.

layer, the CCW structure is completed.

There are a number of challenges in developing the process. First, the roughness of the trench sidewalls needs to be minimised. Bosch process is a switched process of depositing polymer and removing silicon with SF_6 plasma. The process leaves scallops as the cycle goes. Due to the presence of the scallops, voids are created in the electroplating process due to the uneven growth of the metal. The voids increase the resistivity of the electrodes and reduce its lifetime. The Bosch process needs to be optimised to achieve a minimised scallop size in the trenches. Second, the surface roughness of the CMP process needs to be optimised. The surface roughness is critical to the subsequent ion trap fabrication process. However, due to the difference in the rate of etching silicon and metal at the same time and the nature of the etch, the post-CMP surface RMS roughness is more than 100 nm. In this thesis, the focus is placed on the Bosch process. The CMP process was outsourced to DISCO Corporation.

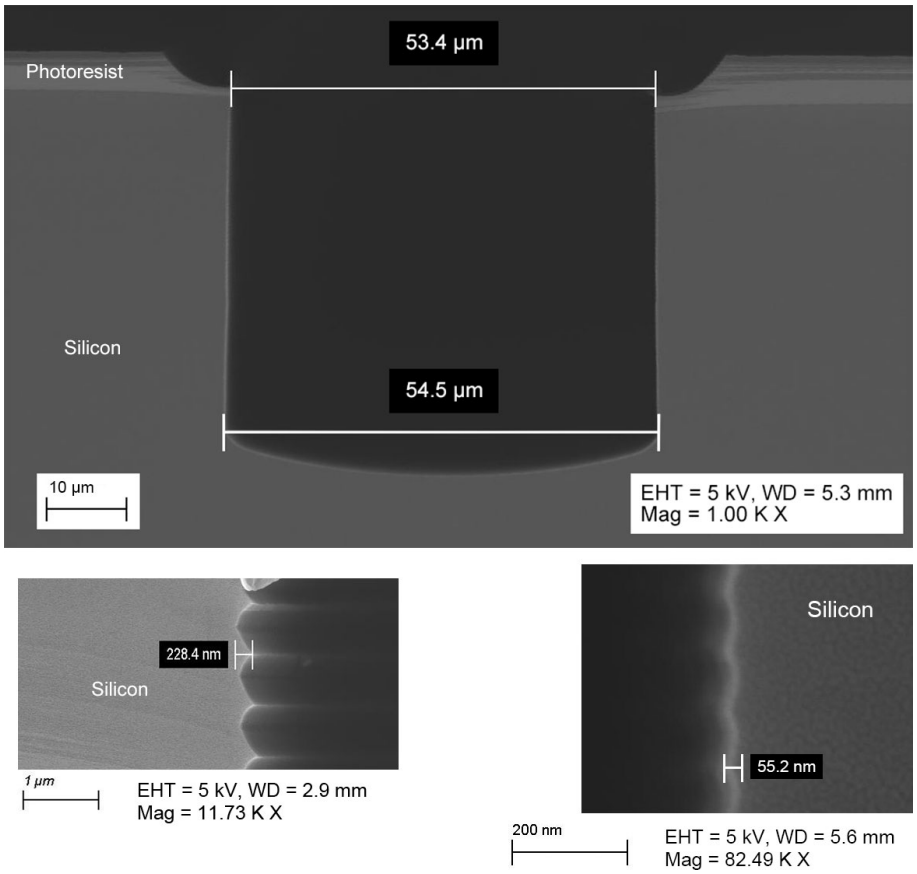

Figure 4.21: SEM images of the trenches made using Bosch processes. (**top**) the optimised Bosch process fabricated a 50 µm trench for CCW structures. The trench was slightly bigger than design due to fabrication process. (**bottom left**) big scallop size with the unoptimised Bosch process. (**bottom right**) small scallop size with the optimised Bosch process. EHT, WD and Mag are SEM working parameters standing for Extra High Tension, Working Distance and Magnification.

Bosch process is a well-known deep reactive silicon etching method. This switching process consists of two alternating steps:

- SF_6 plasma etch. An isotropic etch that attacks polymer and silicon.
- C_4F_8 plasma polymer deposition. This step produces a chemically inert passivation layer similar to Teflon.

Due to the high etch rate, the Bosch process is massively popular in the industry. Each etch cycle leaves the sidewall with a small scallop due to the isotropic silicon etch. To minimise the scallop size, a short switch time process was developed[14]. The scallop size was reduced from 228 nm to 55 nm. The SEM images of the fabricated trench and the scallops are shown in Fig. 4.21.

4.5 Other designs

4.5.1 Metal mesh on viewports

In Fig. 2.20, the scattered photons from a trapped ion is collected through the imaging viewport coated with an anti-reflective coating for 369 nm light. The fused silica dielectric window has the risk of building up a static charge. As discussed in 3.2, exposed dielectric surface must be minimised for the least motional heating of the ions. To shield the ion from the windows, a stainless steel mesh cover was investigated. The mesh together with the metal viewport, acting as a Faraday cage, reduces exposed dielectric surface area at a cost of diminished collection efficiency. In this section, the optimisation of the mesh is presented for the best compromise between collection efficiency, dielectric shielding and microwave delivery efficiency when using the imaging tube as a waveguide (4.3.2).

Fig. 4.22 shows the simulation setup and the results. The simulation is based on the viewport used in the cryogenic system [72]. The window is fused silica, 40 mm diameter and 2 mm thick. It sits about 35 mm away from the trapped ions. A mesh can be mounted on the inner radiation shield which is 25 mm away from the window. To simulate the effect of the stray charge on the window, a 500 V static potential presents on the window surface. The shielding is evaluated by the average of the voltage induced by the charges on the chip surface. The simulated result is summarised in table 4.3.

[14] Developed on SPTS Rapier DRIE tool.

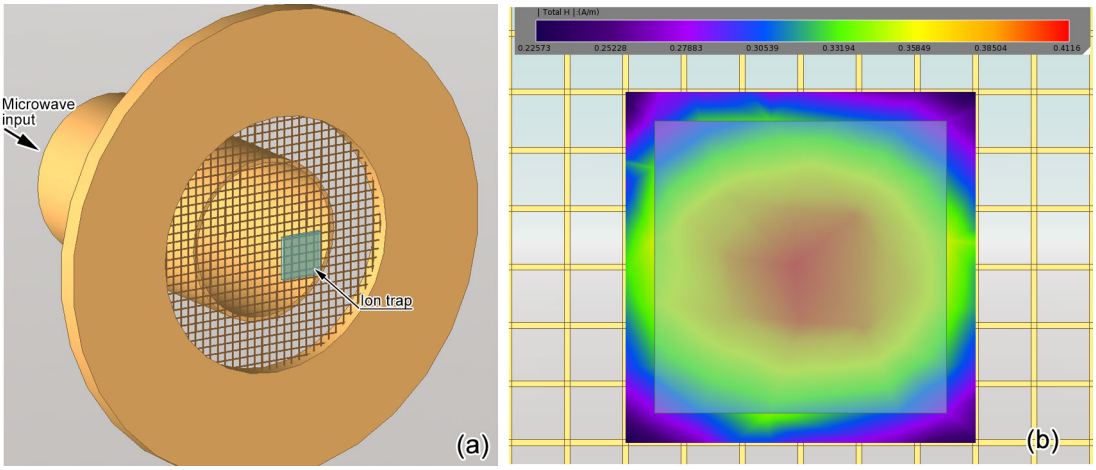

Figure 4.22: (a) The simulation setup. (b) The H field strength on the trapped ion's plane. The semi-transparent box indicates the size of the chip.

Table 4.3: Simulated average electric potential on the chip surface with different mesh wire radius and spacing.

Radius (mm)	Spacing (mm)	Electric potential (V)
0.2	2	-1.24E-06
0.2	4	-9.58E-08
0.2	6	5.33E-06
0.2	8	4.25E-07
0.2	10	9.16E-07
0.2	12	-8.83E-06
0.4	2	-1.65E-05
0.4	4	-4.31E-06
0.4	6	-6.88E-06
0.4	8	-4.03E-06
0.4	10	-1.74E-05
0.4	12	5.41E-05
0.6	2	4.11E-06
0.6	4	-2.03E-05
0.6	6	-1.65E-05

Radius (mm)	Spacing (mm)	Electric potential (V)
0.6	8	5.93E-05
0.6	10	2.59E-05
0.6	12	5.73E-05
0.8	2	-3.71E-06
0.8	4	-1.51E-05
0.8	6	-5.46E-05
0.8	8	-5.23E-05
0.8	10	-6.00E-05
0.8	12	8.91E-05
1	2	-5.30E-06
1	4	-1.92E-05
1	6	-7.54E-05
1	8	7.61E-07
1	10	1.22E-04
1	12	-9.38E-06

The minimum electric potential is achieved when the mesh is made of 0.2 mm radius wires spaced 8 mm apart.

To improve the optical collection, a central hole is opened in the mesh. With a diameter of 18 mm, the average electric potential on the chip surface is expected to be $8.4 \times 10^{-0.6}$ V according to the simulation.

In section 4.3.2, a method that uses imaging tube as a waveguide to deliver microwave was discussed. The complete optimal mesh was simulated using the same setup. The microwave H field strength is heavily attenuated to only 0.29 A/m. With the 18 mm central hole cut, it produces a moderate H field strength of 2.14 A/m.

For installation into the cryogenic system, the mesh was cut according to the simulation estimates, After a standard acetone and isopropanol clean process, this mesh was secured in place using 12 screws on the inner radiation shield. This mesh was used in the cryogenic system where successful trapping was demonstrated [75].

4.5.2 Microwall to reduce oven coating

When operating an ion trap, an atomic oven is ohmically heated realising an atomic beam towards the ion trap. The atomic beam is often cone-shape to cover a wide region above the chip surface where the emitted neutral atoms are ionised by laser-induced photoionisation. A common problem comes with it is the coating of electrode surfaces with evaporated atoms.

The coating on the electrode surface reduces breakdown voltage or short electrode, builds charges up and increase surface roughness. For surface traps, a design known as 'back-side loading' was used [66, 104–106] where a through-substrate-hole within the electrode structure allows the atomic flux to pass through the trap structure, emitting a vertical atomic beam. This method requires the electrode geometry to be adjusted and optimised for minimum RF barrier. The optimisation process of such electrode is the same as the method described in optimising a junction (4.2). Backside loading chips have problem with barium and similar atoms where the atom clusters or their oxide can block the small apertures of the chip rendering the trap useless [107]. This requires a universal solution to oven coating.

A novel method to reduce oven coating is to build a microscopic wall on the chip surface. The wall shadows the atomic beam, prevent coating on the electrodes. To make sure that

the wall does not act as a ground plane that alters the trapping potential, a simulation was performed. A linear ion trap with 100 µm ion height was used for this simulation. The RF electrodes sit in the centre of the chip. The wall is placed on the left-hand side of the chip away from the centre. The trap is simulated at 20 MHz in the simulation tool described in section 4.1. The wall is 6 mm long, 0.5 mm wide. By varying the distance between the wall and the trap centre, the impact of the wall on the trapping field potential is studied. It is found that the wall will only change the potential when being placed very close by as shown in Fig. 4.24 where the distance is only 500 µm. 4.23 shows a normal trapping field with the wall being placed 3.5 mm away.

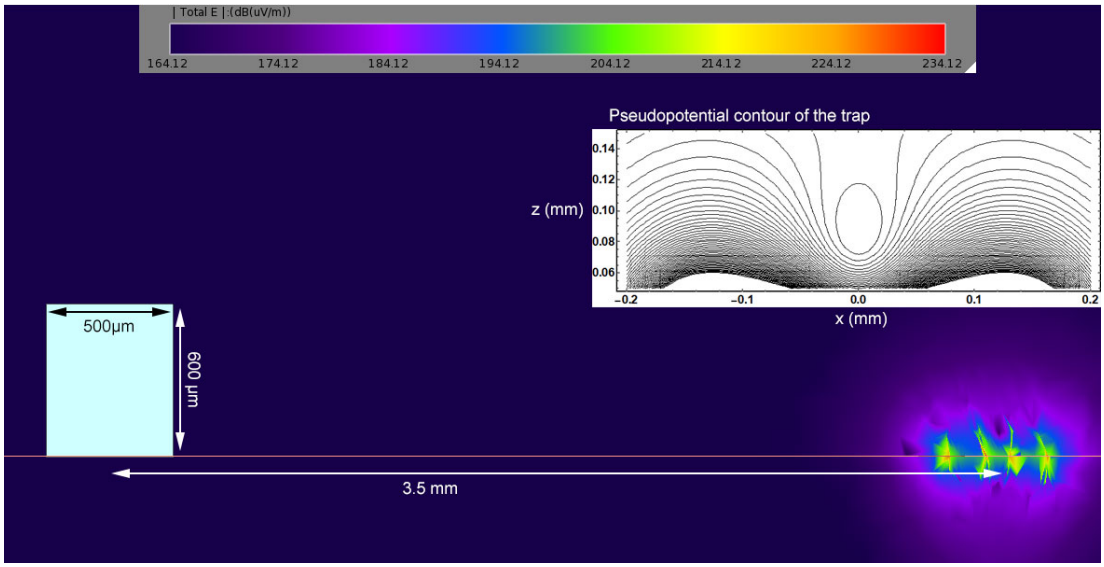

Figure 4.23: Field distribution and pseudopotential of a trap with the wall placed 3.5 mm away from the centre. The pseudopotential contour is shown in the inset.

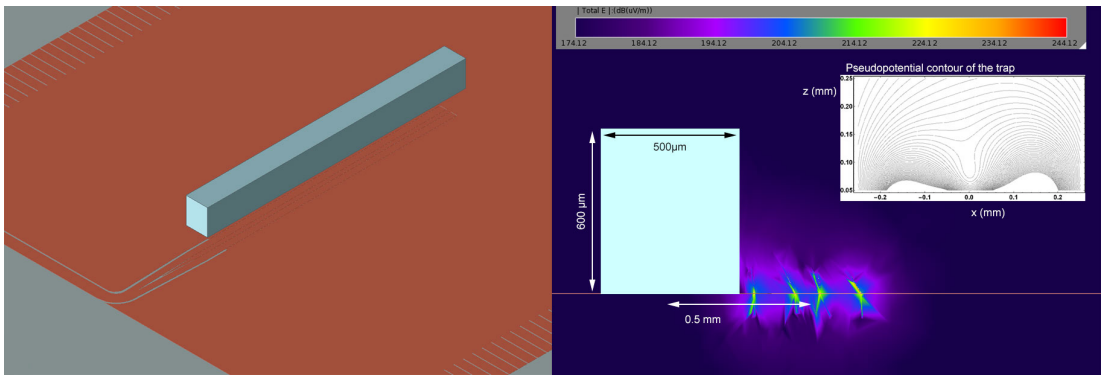

Figure 4.24: (left) 3D representation of the wall sitting close to the chip centre. (right) Field distribution and pseudopotential of a trap with the wall placed near the centre. The pseudopotential contour is shown in the inset. The field is asymmetric because the close-by wall acts as a ground.

Having predicted that the wall, when placed 3.5 mm away, does not impede trapping, it

was constructed using Aluminum 6061, an easy-to-machine, corrosion-resistant soft metal, on a linear trap chip. The metal wall was milled on a CNC machine and was glued on the chip surface using epoxy. It was used in a system operated by Dr David Murgia reporting a reduced coating of Yb atoms [76].

4.5.3 Helical resonator

As discussed in section 2.5.4, to deliver a high voltage gain RF signal, a resonant circuit shown in Fig. 2.23 is needed. A helical resonator is used as the inductive component for a high Q factor and impedance matching. A helical resonator can be described as a transmission line tank where the transmission line is wound in a helix to be minimised in size and encased in a conductive can. A typical helical resonator consists of three parts, the antenna coil, the pickup coil and the grounded shield. The antenna coil couples to the pickup coil inductively acting like a transformer. The pickup coil is floating at the bottom and grounded at the top where it's closest to the antenna. The bottom is loaded with the capacitive ion trap. The equivalent LCR circuit has a resonant frequency of f_0

$$f_0 = \frac{1}{2\pi\sqrt{LC}} = Q \times \Delta f \tag{4.15}$$

where Δf is the bandwidth of the passband and Q the quality ('Q') factor. The physical meaning of the Q factor is obvious: for a given amount of power, the higher the Q the higher the power at the central frequency is. Presume a constant resistance R and power P in the system, the RMS voltage applied onto the chip is $V_{\mathrm{RMS}} = \sqrt{LP/CR} = Q\sqrt{PR}$. To maximise the trapping voltage, it is essential to improve the Q factor of the resonator circuit.

The inductance of the helical resonator can be altered by adjusting the geometry of the coils. However, due to the complicated couplings that exist between wires and coils, the analytical calculation of the inductance is hardly possible. Nor is there a qualitative relationship between a geometric parameter and the inductance. To determine the exact dimensions of the rods and wires for fabricating the coils, numerical electrical simulation packages can be utilised to assist in designing.

A model with the components described above was established in EMPro with its native CAD editor shown in Fig. 4.25(a). There are two coils in a helical resonator, the antenna coil and the pickup coil shown in Fig. 4.25(b) and (c). To simplify the study, the geometric

Table 4.4: The inductance of the helical resonator using different wire diameters. The number of turns and the radius of the pickup coil are fixed at 35 and 62 mm respectively.

Wire diameter/mm	Inductance/nH
1.5	173.568
2	3287.69
2.5	1506.75
3	1443.30
3.5	1817.37

parameters of the antenna coil are fixed and the operating frequency is set to a constant 20 MHz.

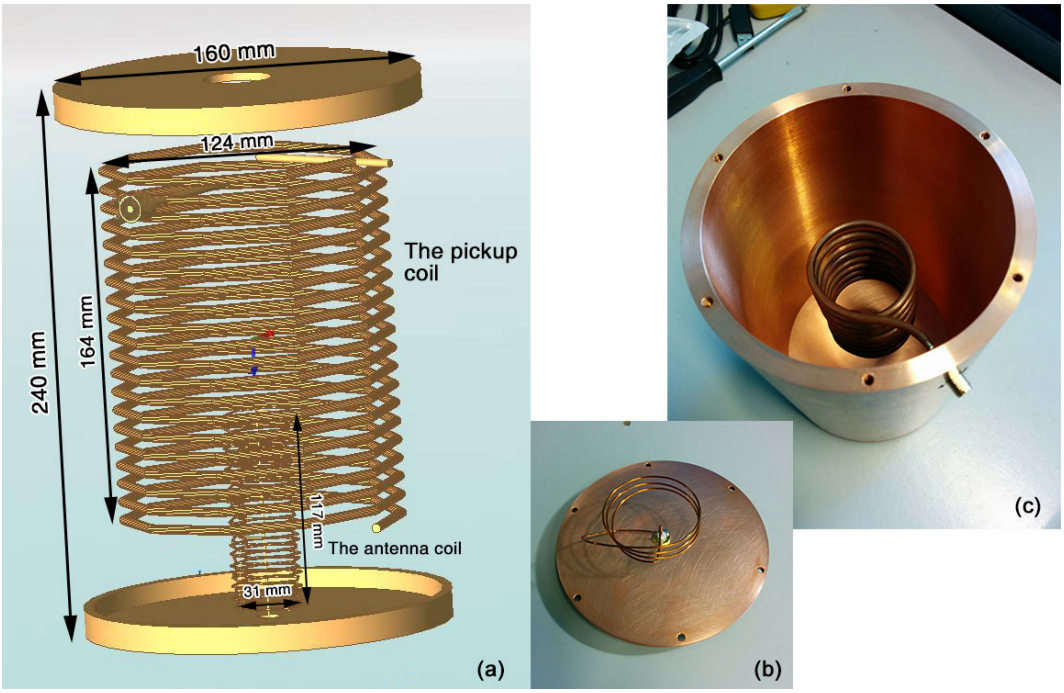

Figure 4.25: (**a**) 3D geometry of the helical resonator in EMPro, the shield is hidden from view. (**b**) the antenna coil and the base. (**c**) the pickup coil and the can.

A series of simulations were performed using a python script[15], sweeping variables including the diameter, the number of turns and the wire diameter of the pickup coil. As shown in table 4.4, the change of inductance with wire diameter is not proportional. Considering that many other parameters do not have a proportional relationship, it is sensible to optimise the resonator by enumerating all possible geometries. The result of the simulation indicated that for a maximum inductance at 20 MHz, the pickup coil is made of 35 turns with a radius of 40 mm and uses a 3.9 mm diameter copper wire. The maximum inductance achieved is ~ 160.05 μH.

[15] Available on https://github.com/ww9980

4.6 Conclusion

In this chapter, a novel numerical method was developed and the novel designs of the three key elements in a scalable quantum computer were presented: a junction ion trap to allow ions be shuttled with minimised motional heating, a scalable efficient microwave delivery system that can deliver 45 times faster quantum gates, a CCW structure to produce a tunable high gradient static magnetic field. This numerical tool models the electromagnetic field dynamically. This gives the researcher a new way of studying the microscopic phenomenon in an ion trap device as described in the following chapter.

In addition, three minor improvements were designed: the metal mesh on the viewport to reduce electrical noise, the microwall to reduce oven coating and the numerical simulation of a helical resonator. These improvements will contribute to reduce motional heating of the trapped ions and reduce the risk of the chips breaking down.

Chapter 5

Fabrication and testing of high breakdown ion traps

5.1 Breakdowns in ion traps

A practical quantum computer requires thousands of identical quantum computer units to work simultaneously. It is essential that these units can operate reliably at high voltages. Microfabricated devices may experience electrical breakdowns resulting in the device being temporarily or permanently malfunctioning. The breakdown mechanism in the air was described by Paschen's Law[1]. It does not apply to microscopic gaps in ultra-high vacuum (UHV) environment. Hong *et al.* [85] suggested that the safe maximum breakdown voltage in ion traps is 300 V. This limits the maximum trap depth achievable and range of choice of the driving RF frequency[2].

In a gas environment, the breakdown is typically an avalanche process where an initial free electron gets accelerated, hitting gas atoms, releasing more free electrons and eventually forms a conductive plasma path between electrodes. This process is concluded by J. Townsend in circa 1897, hence known as Townsend avalanche. The avalanche process is one of many breakdown mechanisms in a vacuum.

Experimentally, vacuum breakdown is more often found between two electrodes and in a dielectric layer rather than in the gaps. In a vacuum, the breakdown between electrodes is

[1] Paschen's law describes the relationship between the breakdown voltage and the product of the pressure and the gap length in a gas. It was first discovered it empirically by F. Paschen and described in details by J. S. Townsend.

[2] A suitable Mathieu q factor is needed for stable trapping. Mathieu q factor is proportional to the ratio between the driving voltage and frequency.

primarily along the surface of insulators, known as surface flashover. The flashover is often initiated by the emission of electrons from the triple junction where vacuum, conductor and insulator join or by the surface contamination where the microscopic irregularities enhance local field causing field emission. These electrons usually then multiply as they traverse the insulator surface as surface secondary electron emission avalanche or as an electron cascade causing desorption of gas [108]. The desorbed gas is then ionised leading to a surface flashover. Fig. 5.1 shows the post-breakdown images of some typical modes.

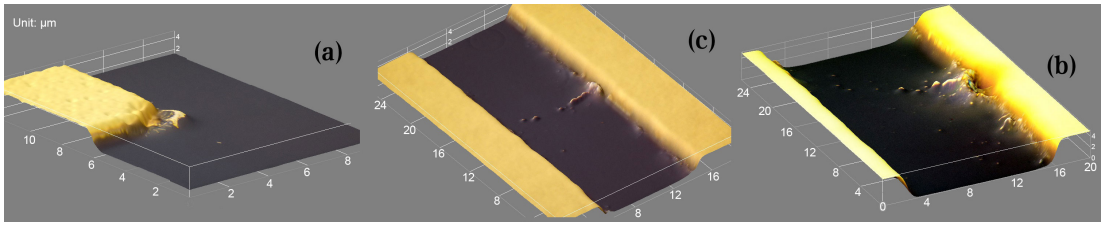

Figure 5.1: 3D reconstructed images of post-breakdown electrodes showing different breakdown modes. The colour difference is due to the optical setup. (**a**) Corner. The potential gradient of a corner is often higher than its nearby areas causing a breakdown. (**b**) Slingshot. A small amount of material is carried away from the electrodes forming a line or curve similar to the trajectory of a slingshot. (**c**) Eruption. Material scatters near the electrode. Erosion can be seen on the electrode.

When breakdown is purely within the insulator itself, it is known as (bulk) dielectric breakdown. Dielectric strength describes the maximum electric field strength a material can withstand under certain test conditions[3]. Due to the impurities and distribution of internal pressure, dielectric breakdown often starts with a localised degradation of the material. This process is best visualised with plexiglass treeing artworks[4].

To improve the breakdown voltage of ion trap devices for the optimal stability and performance in constructing a scalable quantum computer, the design guidelines are summarised and discussed:

- **Surface**. A smooth surface is favourable in vacuum and air alike. A stronger electric field strength presents due to surface asperities making them more likely to trigger the avalanche process.
- **Electrode geometry**. Avoid sharp electrode shapes for the same reason.
- **Outgassing**. Conductor surfaces should have low outgassing, no adsorbed gases, surface contaminations, not prone to oxide. Outgassing, adsorbed gases and contaminations can release atoms into vacuum triggering the avalanche process. Oxidation

[3]Standard test method: ASTM D149-09.
[4]Also known as Lichtenberg figure.

layers develop fast in a vacuum. The metal-oxide interface has a longer settling time hence more likely to accumulate charges causing stress and releasing atoms.

- **Thick electrode layer**. A thicker electrode layer is preferred as it makes the triple junction stand further away from the strong field.

- **Thick dielectric layer**. A thicker dielectric layer is preferred in a vacuum. A thicker dielectric layer has a longer path between electrodes making surface flashover harder to trigger. In MEMS fabrication, silicon dioxide is the most common thick dielectric material.

- **Dielectric strength**. Dielectric breakdown happens when the field strength exceeds the dielectric strength. A thicker dielectric layer also means a lower electric field strength. In MEMS fabrication, silicon nitride, alumina has high dielectric strength values.

- **Dielectric defects**. Avoid dielectric defects as they enhance the field locally. The enhanced field causes field emission, local heating and ionic erosion. Once the discharge process happens, treeing and burn-through occur rapidly. PECVD deposited SiO_2 are often porous, trapping many residual gases. In this chapter, the optimisation of SiO_2 process is reported maximising the film density.

- **Thermal effects**. Typically breakdown voltage degrades with temperature rise.

  - Thermal expansion induces stress. This worsens electrical and structural properties of the device.

  - High temperature lowers the threshold of field emission and outgassing.

  - Pressure of trapped gas in defects increases.

- Strong electrical field and sudden change of temperature, pressure and electrostatic field induce mechanical stress in microfabricated films which can cause delamination.

Despite the requirement for high breakdown voltage, another advantage of having high-quality dielectric films is its long lifetime. Empirical relationship $LV^n = C$ describes the relationship between typical device lifetime L and typical operating voltage of V. C is a system-specific constant, n is an empirical slope factor. The breakdown voltage of a trap can be experimentally determined or predicted using numerical simulations.

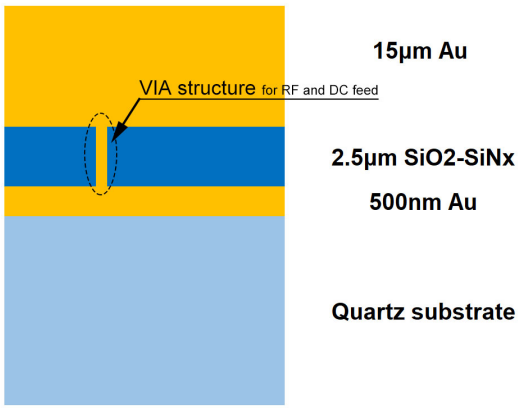

Figure 5.2: (Image not to scale) Layer structure of the ring ion trap.

5.2 Investigation of the ring trap

In this section, a breakdown in a trap is investigated using numerical methods. The trap in question has a ring-shaped electrode layout and hence is known as a ring trap. This chip was designed and fabricated by Dr Marcus Hughes [109]. The chip was built on quartz wafer with 15 thick µm gold electrodes sitting on top of a 2.5 µm SiO_2-SiN_x layer insulating a buried gold layer of 500nm as shown in Fig. 5.2. VIAs are used to connect the two metal layers for feeding RF and DC signals, see Fig. 5.2. The trap has a capacitance of 39 pF and resonates at 13.60 MHz. Initially, ions were trapped at 200 V_{PP} . To increase the trapping time, the applied voltage was ramped up to 400 V_{PP} . With a Q value of 135, the input RF power is 0.44 W. A strong flash was observed with a sudden drop in Q value at this power level. The capacitance of the chip dropped to 4.2 nF and Q value to 40 with a minor shift of resonance frequency to 13.40 MHz. Because the chip was changed electrically, this is classified as a breakdown event. No successful trapping was made after the breakdown. The chip was removed from the system and microscope images (Fig. 5.3) show the damage on the electrode surfaces after the breakdown. Burns and scorches marks were observed at several different sites.

To investigate the origin of this breakdown, the dynamic numerical simulation toolkit introduced in section 4.1 was used. The model calculates the electric field strengths both in freespace and the space inside dielectric materials based on the geometry and RF source specified.

Fig. 5.4 shows the electric field strength distribution on the chip surface given 0.44 W of RF input power at 13.40 MHz. The very high field strength at the input electrode indicates an impedance mismatch resulting in a high reflection which is supported by the

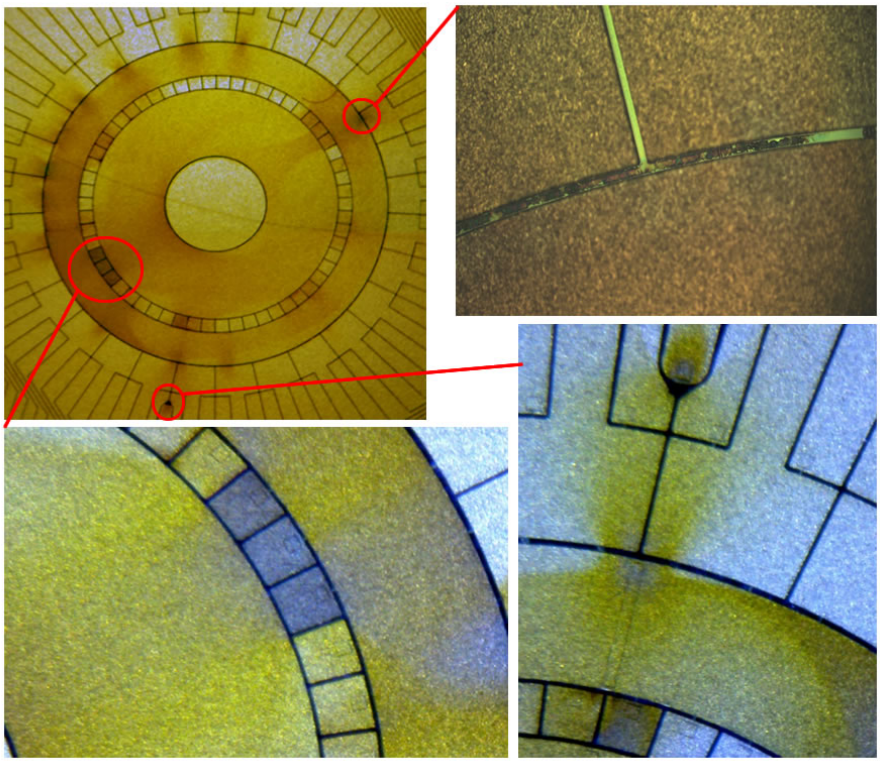

Figure 5.3: Microscope images of the damages on the ring trap after the breakdown.

measured reflection coefficient [5]. The simulated reflection coefficient (0.508) agrees very well with the measured reflection coefficient (0.524).

Fig. 5.5**(a)** shows a zoomed-in comparison between the simulated result and microscope images at the ring electrodes and the RF feed VIA. The burns and heavily decolourised scorches marks match the strong field strength places. The field strength near the RF feeds VIA ranges from 4×10^6 to 8×10^6 V/m. Between room temperature and 200°C[6] where the breakdown happened, the dielectric strength[7] of SiO_2 is 4×10^7 [110]. The dielectric strength is dependent on a number of factors including the dielectric interface, the morphology, the efficiency of heat dissipation, etc. Considering that it was a PECVD film, the dielectric strength is expected to be lower. The simulated field strength is higher than the estimated dielectric strength suggesting that a dielectric breakdown was likely. After the breakdown, oxide tunnelling currents run via the electrical treeing in the dielectric layers which cause the material to burn due to resistive heating.

[5] The reflection coefficient is S_{11} for a one-port network which also equals to the square root of the reflected power over the total input power.

[6] Reported by Dr Marcus Hughes, Dr Tomas Navickas and Dr David Murgia.

[7] Dielectric strength is a property of dielectric material describing the maximum voltage the material can withstand before breaking down in a certain environment.

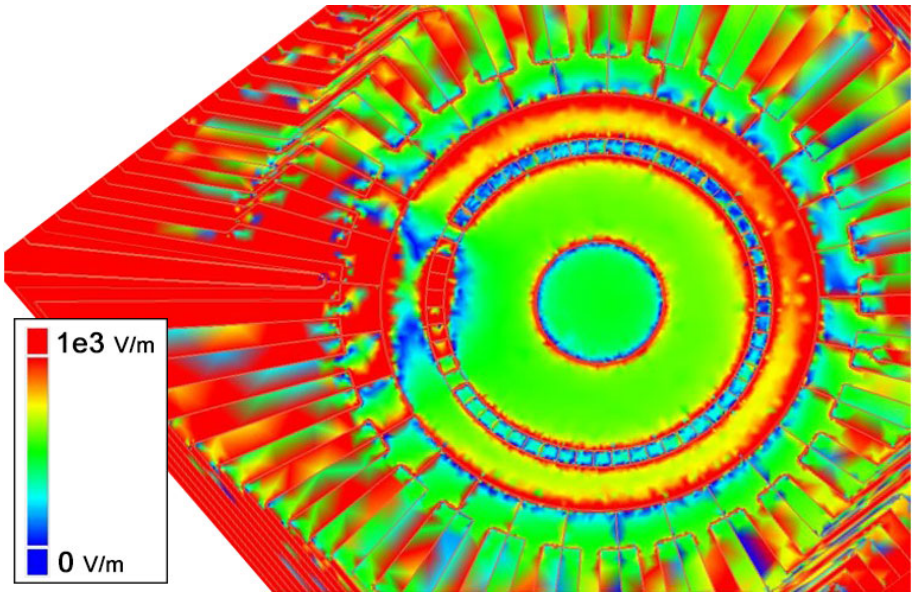

Figure 5.4: The simulation result showing the electric field strength distribution on the chip surface.

To verify the speculation, the chip was scanned with SEM[8]. The SEM result reports that the dielectric near the RF feed is heavily deteriorated and the metal VIA was melted. The deteriorated dielectric is made of SiO_xH_y and SiC_z where x, y, z are arbitrary numbers. The deteriorated dielectric has a higher loss compared to a functional, undamaged dielectric. The melted metal has poor conduction. They result in the high impedance of the VIA. In a conclusion, the measured S_{11} parameter, microscopic imaging and SEM result agree well with the simulation results and provided us with the full picture of the breakdown failure process that the electric field near the RF VIA feed exceeded the dielectric strength causing damage to both the dielectric and the metal resulting in a high impedance mismatch, the reflected RF power further damages other parts of the chip causing breakdowns.

5.3 High-quality thick dielectric layers

5.3.1 Residual stress in deposited films

MEMS ion traps are fabricated using multiple layers of dielectrics and metals. The mechanical performance of the layers under UHV and high voltage environments is critical to the reliability of the device. Stress in thin films and multilayers have three primary origins: intrinsic, thermal and mechanical. Intrinsic stress arises during the deposition processes due to grain growth, crystal defect, lattice misfit, phase transition and the evaporation of

[8]Scanning Electron Microscope. Performed by collaborators at the University of Nottingham.

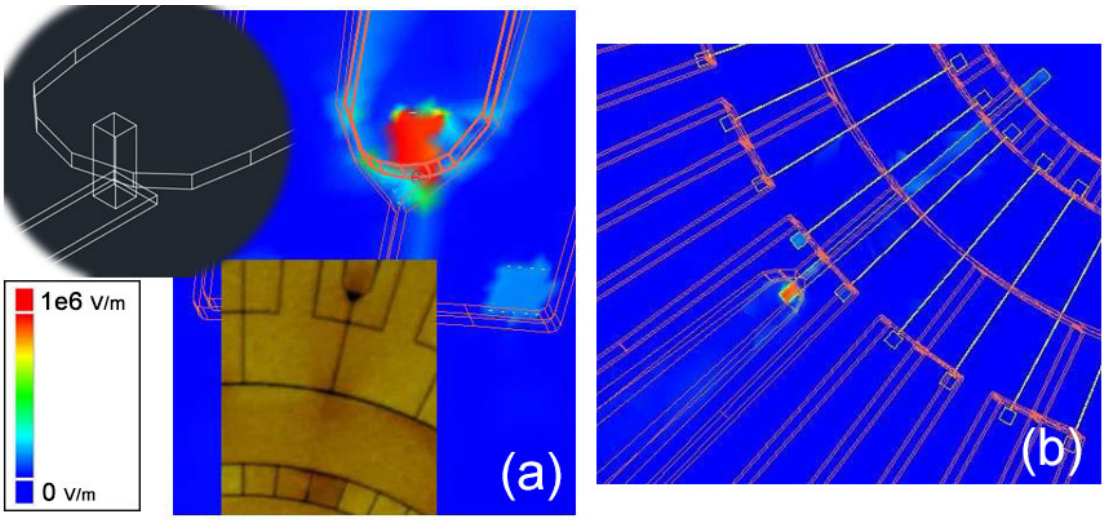

Figure 5.5: **(a)** Zoom-in comparison between the simulated electric field and microscope image of the RF VIA. The top-left inset image shows the 3D structure of the VIA. **(b)** The electric field strength distribution of the ring trap showing that the maximum electric field is at the RF VIA.

a solvent. Thermal stress arises due to the change of temperature where the layers expand at different rates. Mechanical stress is attributed to the electrostatic force due to space charges, the presence of alternating field and externally applied forces such as a change of pressure.

The intrinsic stress of a deposited thin film can often be measured experimentally by finding the radius curvature before (R_0) and after (R) the deposition of the thin film. Given that the thickness of the substrate is h_s and a thin film of h_f thickness is deposited, the Stoney formula [111] is generally used to calculate the intrinsic stress of the deposited thin film assuming that the substrate and films are isotropic, homogenous and linearly elastic. The intrinsic stress σ is:

$$\sigma = \frac{E_s}{6(1-\nu_s)} \frac{h_s^2}{h_f} \left(\frac{1}{R} - \frac{1}{R_0}\right) \tag{5.1}$$

where E_s is the Young's modulus of deposited material, ν_s the Poisson's ratio of that. σ can be either positive (tensile) or negative (compressive). When the intrinsic stress of a thin film is very high ($\sim$ GPa), failures during fabrication and operation are expected including delamination, debonding, surface cracking and channelling. A laser thin film stress measurement tool by KLA-Tencor[9] was used in this work. The processes were then optimised to reduce the stress of deposited dielectric films.

[9]KLA-Tencor FLX-2320 Film Stress Measurement System.

5.3.2 Oxide and nitride films

A practical ion trap quantum computer requires the dielectric used to have high reliability and high dielectric strength as the chips will operate at high RF voltages contineously to output maximised computing power. As discussed in section 3.2, the keys to a high breakdown voltage dielectric material are thick layers and high dielectric strength. Thick layers give a longer breakdown path, high dielectric strength prevents bulk breakdown.

In MEMS devices, silicon nitride[10] stands out as an insulating dielectric for its excellent dielectric strength[11] and resistivity[12]. However, high-quality silicon nitride is hardly achievable above a few hundred nm due to the intrinsic stress.

SiO_2 is the most popular candidate for thick ($\sim$ µm) dielectric layers but has ordinary dielectric strength and resistivity. Most commonly, high-quality oxide and nitride layers in MEMS devices are deposited with PECVD processes[13]. The mechanical and dielectric properties of the deposited films are strongly dependent on their layer composition. The ratio of the Si−O, Si−N, N−H and Si−H bond components are controlled by process parameters including the flow rate of the gases, the chamber pressure, the RF frequency and power and the temperature of the substrate. It has been known that the existence of N−H and Si−H bonds in the film significantly deteriorates the film quality and was investigated by the community [112–114]. The change in film components is often characterised by wet etch rate and film density which was reported to be linearly related [115]. A slower etch rate often indicates a better film quality. In this work, the quality of the film is characterised by the wet etch rate using 7 : 1 HF solution.

Silicon nitride is deposited using SiH_4 and NH_3 mixture: $SiH_4 + NH_3 \longrightarrow SiN_x + H_2$[14]. Silicon dioxide can be deposited using two different chemistries, SiH_4 based and TEtraethyl OrthoSilicate(TEOS)[15] based. In SiH_4 chemistry, the reaction is similar to the nitride deposition $SiH_4 + N_2O \longrightarrow SiO_y + N_2 + H_2$[16]. When using TEOS as precursor at elevated

[10] The silicon to nitride ratio varies in PECVD nitride films hence denoted as SiN_x. Some authors prefer to use Si_3N_4 which is the most thermodynamically stable composition.
[11] Typically 10 MV/cm.
[12] Typically 10^{16} Ωcm.
[13] A PVD nitride recipe was developed in Southampton Nanofabrication Centre using AJA ORION magnetron sputter. However, it was not used due to the relative slow deposition rate (< 1.4 nm/min).
[14] Equation not balanced as x stands for an arbitrary positive number.
[15] Tetraethyl orthosilicate, also known as tetraethoxysilane, is the chemical compound with the formula $Si(OC_2H_5)_4$. It's a colourless liquid in room temperature. In PECVD tools, TEOS liquid is carried into the chamber by an inert gas such as Ar.
[16] Equation not balanced.

temperatures[17], $Si(OC_2H_5)_4 \longrightarrow SiO_2 + 2\,(C_2H_5)_2O$[18].

High-quality films often suffer from high intrinsic stress which increases the undesired surface roughness and sometimes results in film delamination. In this thesis, the conflict between quality and thickness is resolved in a novel structure known as 'sandwich' dielectric, detailed in 5.3.4. To gain high-quality films, processes were developed using alternating frequency source, detailed in 5.3.3.

5.3.3 Optimisation of PECVD films

The quality of the film can be improved by optimising the PECVD processes by changing the flow rates of the gases, the power and frequency of the plasma source and the bias, and changing the chamber pressure.

Hussein *et al.* [116] reported the correlation between the N_2O/SiH_4 gas flow ratio and the film quality. The Si−H bond strength is around 384 kJ/mol which is lower than that of Si−O (452 kJ/mol). To help reduce the formation of Si−H bonds, an elevated temperature is desired. It has been known that meta-stable states of hydrogenated amorphous silicon environment experiences Staebler-Wronski effect [117] where light exposure causes an increase in the defect density. In short, by adjusting the N_2O/SiH_4 ratio, a low Si−H film is obtainable.

Following the previous studies [116, 118], the gas flow ratio was optimised for the silicon dioxide recipe. The SiH_4:N_2O:N_2 ratio was changed from 41 : 8 : 100 (recipe A.1.2) to an optimised ratio of 4.2 : 350 : 80 (recipe A.1.3). The excessive amount of N_2O removes possible H atoms and the carrier gas N_2 is reduced to increase the efficiency of H atom removal. The etch rate was reduced from $\sim$ 1200 nm/min to $\sim$ 800 nm/min.

A conventional PECVD silicon dioxide recipe uses the SiH_4 chemistry and is driven by an RF plasma source at 13.56 MHz. In the dual-frequency process, the RF provides a stable discharge, generating reactive species and a strong coupling to the substrate. With the additional low-frequency excitations, ion bombardments are enhanced leading to a denser film at a cost of minor ion implantation effects which produce intrinsic compressive stress. High intrinsic stress makes the film more fragile during a breakdown. A novel multilayer deposition technique was developed to eliminate the problem and detailed in section 5.3.4.

[17] Typically $> 600°C$.
[18] Ideal case. The composition of SiO_2 may vary.

Table 5.1: Etch rates of PECVD films before and after optimisations.

Recipe name	Recipe	Etch rate (nm/min)	Stress (MPa)
SiO_2	A.1.2	1200	-
SiO_2 optimised	A.1.3	800	-
TEOS LF only	A.1.5	500	212
TEOS optmised	A.1.6	340	23
SiN_x	A.1.7	800	-
SiN_x optimised	A.1.8	180	-

To optimise the film quality produced by a TEOS process (recipe A.1.4), an additional LF source was used. Before developing the dual-frequency recipe, an LF only recipe was developed (recipe A.1.6) which uses 50 W of 50 kHz low-frequency source. The produced SiO_2 film has a very high compressive residual stress of 212 MPa. The wet etch rate is $\sim$ 500 nm/min. The optimised (recipe A.1.5) LF and RF time were found to be 12s and 8s. The resultant film has lower residual stress of 23 MPa and a lower rate of 340 nm/min. A similar procedure was used to optimise silicon nitride recipes. By adding a 10s LF excitation and tuning the gas flow rates, the wet etch rate was decreased from $\sim$ 800 nm/min to $\sim$ 180 nm/min. The optimisation results are summarised in table 5.1. Before running any deposition process, a pre-deposition *in situ* clean process (recipe A.1.1) was used to produce a constant initial chamber condition. The chamber is cleaned using long N_2O plasma process after every 30 µm of SiO_2 or 3 µm of SiN_x deposition accumulated. The chamber is also cleaned throughout using a wet chemistry[19] after every 9 plasma cleans or 3 weeks.

In a conclusion, PECVD is a highly versatile technique for depositing high-quality Si-based dielectrics for ion trap fabrication. Optimisation methods and results were reported on high-quality PECVD films with low etch rates and low residual stresses.

5.3.4 The sandwich layers

The dielectric layer in an ion trap is designed to maximise the breakdown voltages of the ion traps. Previous investigation [119] reported an improved breakdown voltage by using a thin layer of silicon nitride as insulating layer. High breakdown voltages were reported [88, 120] in ion traps fabricated with thick SiO_2 layers. However, the thin silicon nitride and thick silicon dioxide layers both have high residual stresses making them less reliable. By developing the deposition technique of a nitride-oxide-nitride 'sandwich' layer structure, the breakdown voltage was expected to be improved and the stress minimised.

[19] Performed by the technicians of Southampton Nanofabrication Centre.

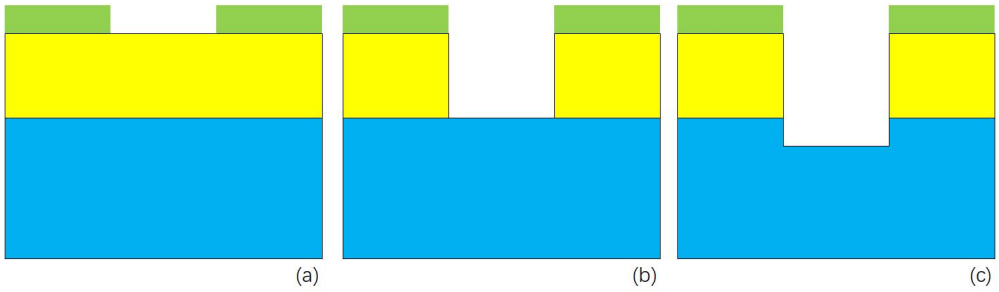

Figure 5.6: (Image not to scale) Fabrication workflow of a thin electrode ion trap on oxide substrate. Colour keys: ■ oxide substrate, ■ photoresist, ■ 300 nm thin gold electrodes. The 10 nm Cr and 20 nm Pt barrier layers are hidden.

The stress of a silicon nitride film produced using the optimised recipe described in section 5.3.3 is $\sim$ 200 MPa tensile. To compensate for the stress, the optimised TEOS based SiO_2 PECVD recipe was used which provides residual stress of a compressive nature. The residual stress of a 4.5 µm SiO_2 layer is $\sim$ 600 MPa. The sandwich structure consisted of 200 nm nitride, 4.5 µm oxide and 200 nm nitride has residual stress of 225 MPa. To minimise the stress, the thickness of the three layers were optimised. The optimised layer thickness are 200 nm, 4 µm and 200 nm respectively which gives an optimised stress of 45 MPa.

In a short conclusion, a new structure of thick dielectric layer for ion traps was proposed and optimisation of such films was performed achieving minimum residual stress of only 45 MPa. The high-quality dielectric films and the new structure are used in the development of reliable, high breakdown voltage ion traps.

5.4 Oxide etch and undercuts

Oxide dry etch

In some fabrication, tall electrodes are not used due to lack of electroplating availability. Such fabrication workflow is summarised in Fig. 5.6(a) and (b) where the thin gold electrode on the oxide substrate is etched using a photoresist mask. To increase the breakdown voltage in devices fabricated using thin electrodes, oxide etch is required to create a trench into the substrate (Fig. 5.6(c)) hence a longer surface flashover path.

The oxide etch is no new process for the MEMS industry. The challenges in developing this specific oxide etch are high photoresist selectivity, high etch rate and minimising etch

Table 5.2: The oxide etch recipes. 'sccm' is 'standard cubic centimeters per minute'.

Recipe	Gas (sccm)				RF power (W)	Pressure (mT)	Platen temperature ($°C$)
	Ar	C4F8	O2	H2			
1	150	30	30	0	500	150	10
2	150	30	20	0	700	150	10
3	150	60	20	0	700	200	10
4	150	30	30	0	500	150	0
5	150	80	30	0	700	150	0
6	150	30	30	0	700	150	0
7	150	30	10	20	700	150	0

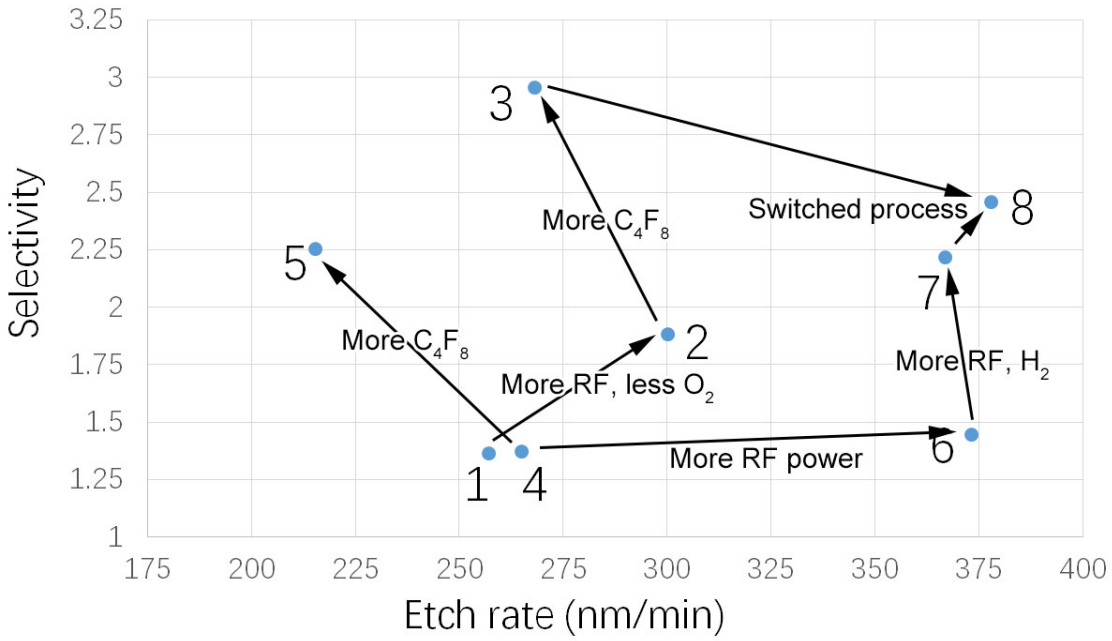

Figure 5.7: Process development walkmap showing the relative relations and the results of different recipes. An arrow indicates that the target recipe is derived from the source recipe. This walkmap aids the development of processes by visualising the results.

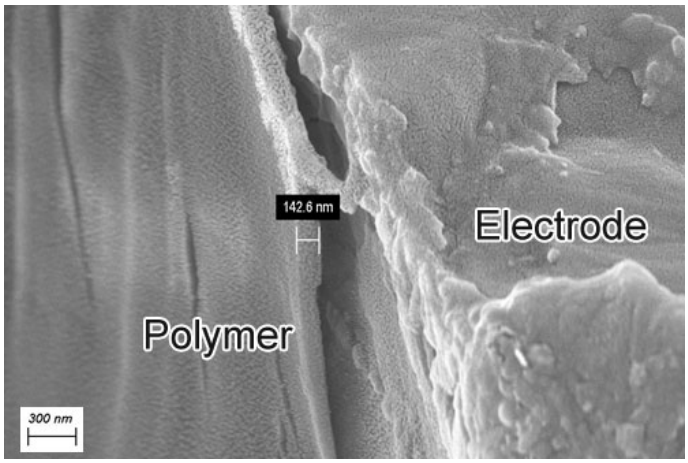

Figure 5.8: SEM image of the polymer on electrode sidewall after SF_6 and O_2 post-etch clean. SEM working at: EHT = 5 kV, WD = 3.6 mm, Mag = 26.62 K X.

residues. After the metal etches, only about 1.5 µm out of the initial 2.7 µm photoresist is left. To etch a decent depth, high oxide to photoresist selectivity is required. To avoid the glow discharge of the high-fluorine or high-chlorine etch residue described in Chapter 7, a minimal etch residue process is required.

An OIPT SYS 380 ICP RIE Tool was used. To maximise the selectivity, a C_4F_8 based recipe (A.3.4.1) was used as the start position. The ICP power is fixed at 100 W. Several changes were made to the gas flow ratios, pressure, RF power and platen temperature as shown in table 5.2. To aid the development, a 'process walkmap' (Fig. 5.7) was created showing the relative relations and results. The selectivity and etch rate of a tried process is plotted. Recipe 4 (A.3.4.4) is a duplicate of recipe 1 but at 10°C chiller temperature. Recipe 8 (A.3.4.8, not included in table 5.2) is an alternating process between high C_4F_8 gas flow step and high H_2 flow step. The high etch rate and high selectivity is attributed to the switching process of aggressive etching and polymerisation.

The high selectivity of the process due to C_4F_8 and H_2 leaves the resultant trench with a thick layer of polymer. Results of recipe 8 shown in Fig. 5.8 have a polymer thickness between 200-400 nm. Two further polymer and residue removal recipes (A.3.4.S and A.3.4.O) were developed. Recipe A.3.4.S is an alternating process using SF_6. Recipe A.3.4.O is a high-temperature oxygen ashing process. Two recipe 8 processed wafers were first etched using recipe A.3.4.S for 2 mins then oxygen ashed (using A.3.4.O) for 10 mins. Fig. 5.8 shows that the polymer thickness on the two samples ranges from 40-150 nm. The remaining polymer was easily removed using a post-etch N-Methyl-2-Pyrrolidone (NMP) wet clean process (recipe A.4.2).

HF undercut

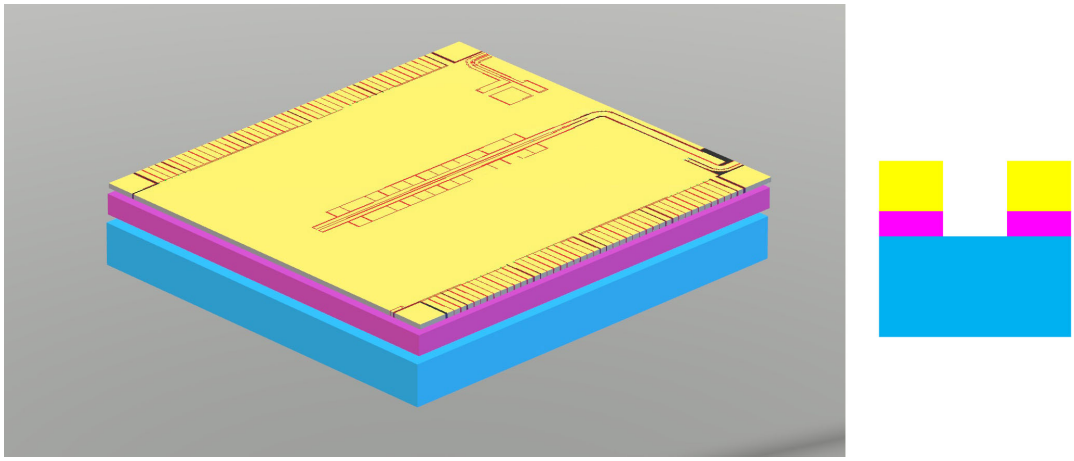

Figure 5.9: (Image not to scale) Layer structure of the high breakdown voltage chip. (left) 3D rendering. (right) cross-view. Colour keys: gold electrode, dielectric layer, substrate.

The breakdown voltage can be increased by creating an 'undercut' in the oxide layer in ion traps with the simple electrode-dielectric-substrate layer structure (Fig. 5.9). When using SiO_2 as the dielectric layer, the isotropic etching ability of an HF solution can be used to create undercuts which help to increase the breakdown voltage significantly [119]. In the Southampton Nanofabrication Centre, HF vapour etches recipe (A.4.3) was developed. Fig. 5.10 shows the SEM image of an undercut produced on an ion trap chip in the Southampton Nanofabrication Centre with a high aspect ratio of $\sim 5:1$.

HF acid also attacks silicon nitride but the mechanism differs in the active etching species. Where SiO_2 is etched as a result of the catalytic effect of coordinating the difluoride to the OH surface groups, the nitride is etched due to its lower bond strength [121]. By diluting HF with HCl or some organic solvents, a lower degree of ionisation results in H passivation hence a selective etching of Si_3N_4. In this work, only high concentration HF solution is used as described in A.4.3 and the etch rate of SiO_2 is significantly higher than that of Si_3N_4.

5.5 Breakdown experiments

5.5.1 Electrical and vacuum setup

To test the chips for breakdown, a high vacuum environment is needed. A specially designed bell jar vacuum apparatus (shown in Fig. 5.11) were used. The bell jar is not

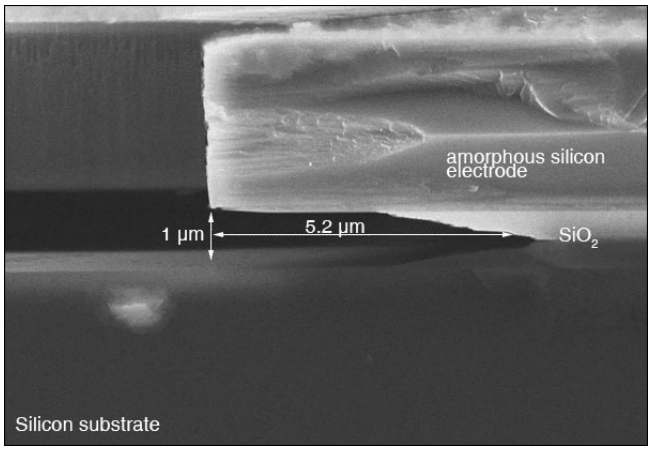

Figure 5.10: SEM image of an undercut created using hydrofluoric acid. The dielectric layer is a 1 µm SiO_2 layer sandwiched by two 200 nm SiN_x layer. The undercut is 5.2 µm deep. SEM working at: EHT = 5 kV, WD = 3.2 mm, Mag = 32.48 K X.

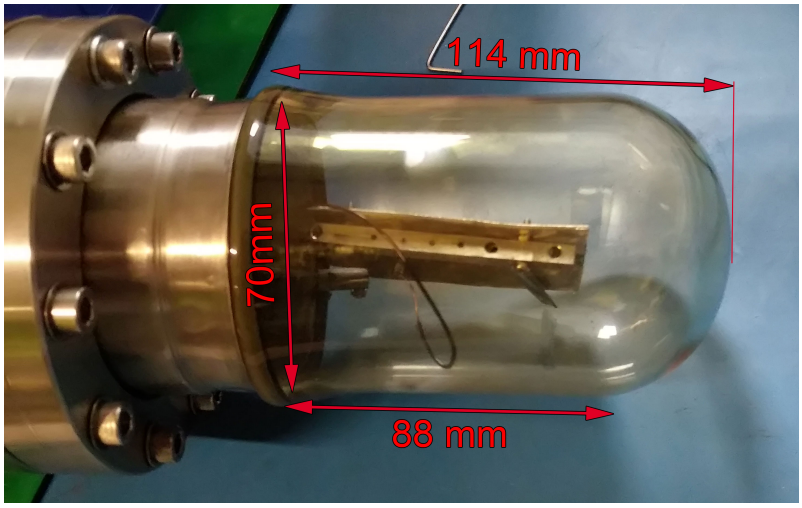

Figure 5.11: The bell jar and its dimensions.

coated so that an external CCD can collect photons of different wavelengths.

The vacuum systems were evacuated using a turbo-molecular pump station[20] which maintains a high vacuum between 1-6 $\times 10^{-6}$ Torr. The optical path of the CCD is presented in Fig. 5.12. The imaging tube is about 1 cm away from the chip. In addition to the CCD, a webcam was used to capture the live development of the glow.

The high RF voltages required for breakdown experiments are supplied with a system shown in Fig. 5.13. A sinusoidal signal of a certain frequency is produced by a variable frequency generator[21]. It is amplified by an RF amplifier[22] followed by a directional coupler[23] and a power metre. The amplified signal is fed into a resonator circuit where

[20] Leybold Turbolab 350 Cart Turbo Pumping Station
[21] R&S SML Signal Generator.
[22] Mini-Circuits LZY-22+.
[23] Mini-Circuits ZMDC-20-3+.

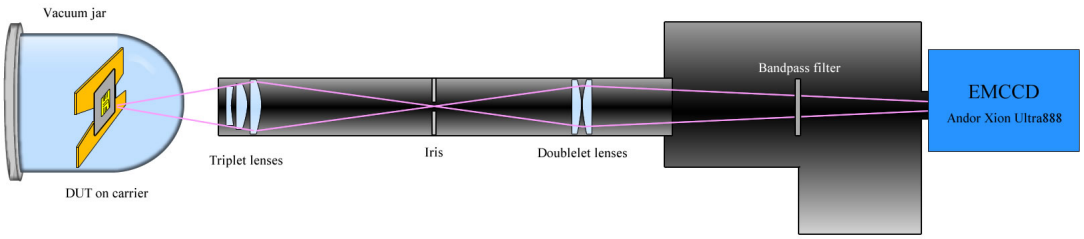

Figure 5.12: The optical path from the bell jar to the CCD. 'DUT' stands for 'device under test'.

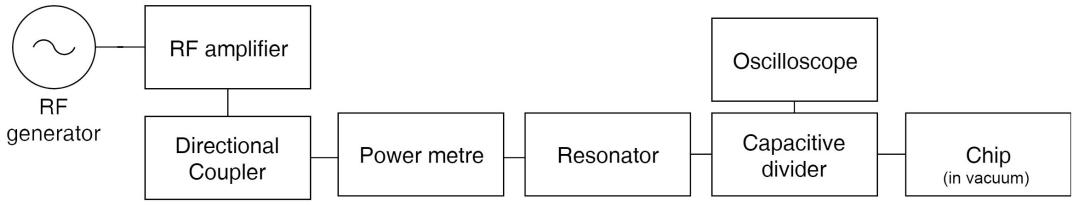

Figure 5.13: System diagram of the RF supply.

the chip (seen as a capacitor), along with a capacitive voltage divider is resonating with a helical coil. The maximum input voltage of the oscilloscope is 600 VPP , to measure a wider range of voltage on the chip, a capacitive divider is used consisting of C_1 (20 pF) and C_2 (0.3 pF). The capacitor C_2 is connected into an oscilloscope[24]. Very high voltages on the chip are measured by using the pre-calibrated ratio between the voltage on C_2 and the chip. Table 5.3 shows the calibration data at 25.5075 MHz. A nearly constant ratio of 716 between the two voltages was found. Once the scope on the chip is disconnected, a voltage higher than 600 VPP was applied.

5.5.2 Probes

Electrical breakdown often damages the electrodes leading to unwanted short-circuits. To test the electrical connectivity between two points on a microfabricated device requires precise contact with little to no damage to the surface. In this work, this was done using

[24]Gwinstek GDS-2000E.

Table 5.3: The capacitive divider calibration data at 25.5075 MHz.

V_{C_2}(mVPP)	$V_{C_{\text{trap}}}$(VPP)	Ratio
28.2	20.2	716
56	40.4	721
84	60	714
112	80	714

a home-built probe station. This probe station consists of two fine adjustable probe arms sitting on a base which holds the chip in place. The station used two gold-coated tungsten probe tips[25] with 10 µm diameter mounted at 45° angles on two micropositioners[26]. The two micropositioners are sitting at 90° angle and hold extension arms that can be fine position controlled on both X, Y and Z axes. Chips are mounted to this stage with conductive tabs[27] and the whole probe station sits on an optical breadboard[28] which can be placed under a microscope for precise operation.

To test the DC connectivity of a chip before and after a breakdown, a multimeter is connected to both probes. The resistance of the probe is recorded first by simply contacting the tips. This typically is less than 0.5 Ω and is subtracted from the subsequent measurements. Then the tips are placed on the electrodes of interest and the corresponding bond pads. A typical malfunctioning ion trap chip has very large resistance in the DC electrodes or a short-circuited path from RF to ground electrodes.

RF active probe

Probing RF signals on an electrode is different from DC. When measuring an RF signal, one can not directly hook up test leads or a stripped coax because the cable and measurement device will act as a load thus change the behaviour of the signal. A typical passive probe act as an impedance transformer to convert the lower impedance from a measurement instrument port to a high one. This prevents power from being pulled from the signal line while still able to pick up a weak but unaltered signal. Take the probe tip and the parasitics of the cable as a system, the transfer function is

$$G(j\omega) = \frac{U_a(j\omega)}{U_e(j\omega)} = \frac{Z_a(j\omega)}{R_t + Z_a(j\omega)} \tag{5.2}$$

where

$$Z_a(j\omega) = R_s || \frac{1}{j\omega(C_s + C_{\text{tip}} + C_{\text{cable}})}. \tag{5.3}$$

In the equations above, C_s and R_s are the internal capacitance and resistance of the measuring port, C_{cable} and C_{tip} are the parasitic capacitance of the cable and probe tip.

[25] Signatone SE-TG.
[26] Signatone S-725CRM
[27] PELCO Tabs carbon conductive tabs.
[28] Thorlabs MB3030/M

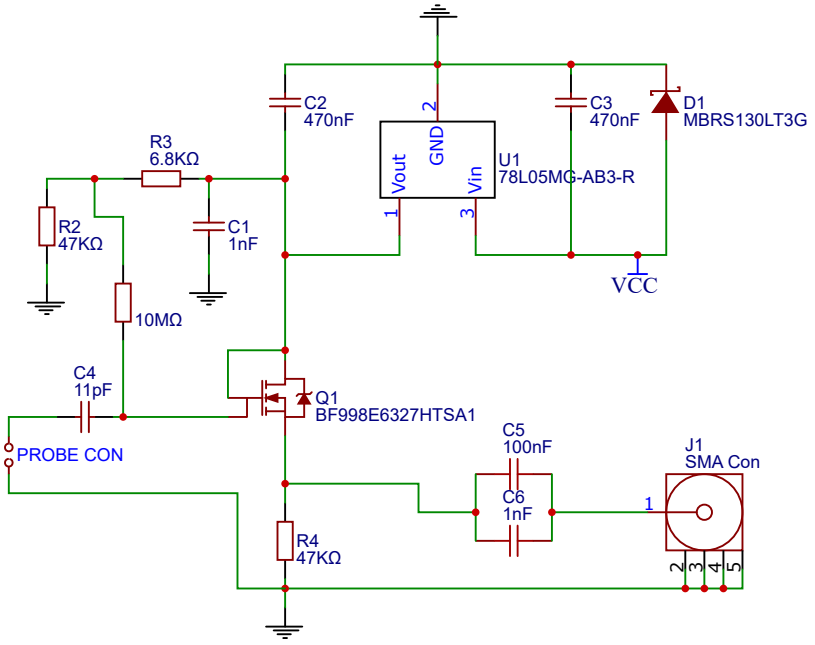

Figure 5.14: Circuit diagram of the active probe. The dual-gate MOSFET is used to amplify the small signal picked up from the 10 MΩ load.

R_t is the resistance of an attenuation resistor placed between the probe and the measuring device. The transfer function is frequency-dependent unless R_t is carefully chosen and replaced by a value of multiplier of $Z_a(j\omega)$. This approach is valid only if the elements act as lumped elements, which tends to break down around 200-800 MHz. By matching the attenuation resistance to make it frequency independent, the R_t value usually is very large making the signal picked up very weak.

An active probe is needed to solve this problem. As shown in Fig. 5.14, it features high input impedance, frequency-independent transfer function and a relatively higher output signal level. The typical input impedance of a commercial probe is > 1 MΩ. In this design, the input impedance is 10 MΩ.

The key part in an active probe is the small-signal amplifier. A BF998 MOSFET[29] was used which operates in source-follower configuration providing a low output impedance to drive the test equipment while maintains the input impedance high. The 10 MΩ is a bias resistor to ensures that the MOSFET operates in its ideal DC working point. A 150 nF capacitor is placed on the output path to block off the DC working point. Fig. 5.15 shows the assembled probe. The circuit is based on a double-sided RO4350 PCB. The spring-loaded probe tips were soldered on a separate carrier PCB of the same material.

[29] BF998, a silicon N-channel dual-gate MOSFET by NXP semiconductors.

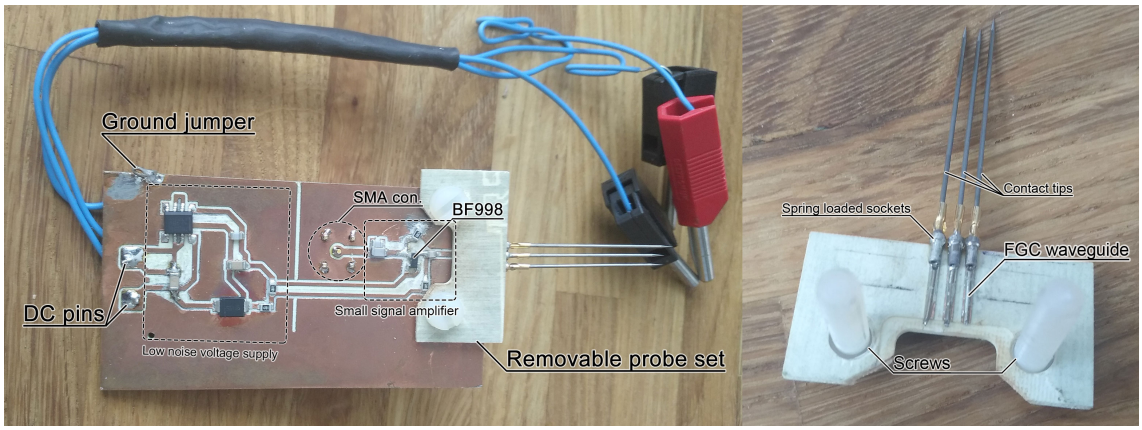

Figure 5.15: (**left**) The active probe. The probe is driven by a low noise voltage supply (in the annotated dash line box). 5 V DC voltage is required to drive it. The target small signal is picked up from the removable probe set, fed into the small signal amplifier whose core component is the BF998 MOSFET amplifier. The amplified signal outputs to a vector network analyser via the SMA connector. The ground jumper connects the grounds on both sides of the PCB. (**right**) The probe set is removable from the probe allowing the probe to be replaced at a low cost or reconfigured to a different impedance or softer contact. When requiring a higher impedance, simply change the spacing of the tips and the Finite Ground Coplanar (FGC) waveguide. To minimise the damage to the contact surface, the tips are fitted on spring-loaded sockets. When a softer contact is required, the sockets can be swapped.

The two PCBs are aligned and mechanically held together with two PEEK mounting screws. The carrier PCB can be dismounted and replaced when a new set of probe tips are needed. The RF probe sits on a spring-loaded socket [30] which provides a small degree of elasticity. The probe tips are from Signatone, part number SE-20T. Tips of other sizes can be used with modified carrier PCB. To isolate noise, part of copper on the main PCB was removed to make the DC supply part and amplifier part isolated from each other. To test the impedance, a 50 Ω straight trace was made with 2 SMA ports on both ends. The S_{11} of the trace is −50 dB. The measured input impedance of this active probe is 10 MΩ with 0.7 pF capacitance. The bandwidth is from 100 kHz to 1.5 GHz (±2.5 dB). The noise figure is 1.1 dB. The nominal gain calculated is approximate −20 dB.

5.5.3 Fabrication of the test traps

Metals for ion trap fabrication

Metals such as gold and aluminium were used as the material for electrodes for their high electrical conductivity and resistance to erosions and sputtering. Typically, the electrode

[30] Part number: P70-1030045R

consists of a thin layer of adhesion metal, a thin layer of the diffusion barrier and a bulk layer of the electrode material. Metallisation system describes how the metal layers are constructed to produce the best performance and reliability.

Due to the porous nature of polycrystalline gold, a bilayer metallisation such as Cr/Au or Ti/Au system is only functional at low temperatures. D. Miller *et al.* [122] studied Cr-Au system reporting that annealing Cr-Au system above 225° results in grain growth and change in the composition of the film. The mechanism of diffusion is constituted by the thermally activated jump motions of atoms in both the bulk metal and the interface. The diffusion is temperature and crystal structure-dependent. The diffusive nature of metals such as gold, silver and copper requires the metallisation system to provide a 'diffusion barrier'. S. Dayluk *et al.* [123] reported that Pt is an effective diffusion barrier for Cr and Au below 400°. In addition, Al_2O_3 adhere well to Pt without no interdiffusion [124] hence all fabrications using a sapphire substrate does not require an additional Cr adhesion layer. For a detailed theory on metal diffusion phenomena, please refer to [125] by Prof. Günter Gottstein and [126] by R. Cahn.

Ti/Pt/Au is a well-studied metallisation system widely used in MEMS fabrication and ohmic contact of diodes. The sandwiched Pt layer is added to stop the interdiffusion between Au and Ti [127]. Investigation [128] showed a maximum operation temperature of $\sim 450°C$. However, Ti/Pt/Au system suffers from a major confliction with the undercut process. HF is used to create SiO_2 undercut and it attacks Ti at an impressive rate. The rate of HF attacking Ti was measured where a sample sputtered with a 20 nm Ti layer was submerged in an HF 20 : 1 etchant. The Ti layer visually vanished in less than 3s. Prior to this work, several samples fabricated in IQT group [129] failed due to underestimating the etch rate of Ti in HF. Even though the Ti layer was covered by the Au layer, HF etchant still managed to remove it entirely. As a result, the gold electrodes peeled off from the substrate almost completely. To salvage the chips, the RCA-1 solution was used to strip the remaining metals and clean the surface. For details, refer to appendix A.4.4.

To overcome this problem, the Cr/Pt/Au metallisation system is used. Cr, unlike Ti, is chemically resistant towards HF. Moreover, the coefficient of thermal expansion at room temperature of Cr ($4.9 \times 10^{-6}/°C$) is closer to Si_3N_4 ($\sim 2 \times 10^{-6}/°C$) and sapphire ($\sim 4 \times 10^{-6}/°C$) than that of Ti ($8.6 \times 10^{-6}/°C$). Cr is adhesive to most oxides, metals and polymers. Cr forms a Cr_2O_3 layer of about 1 nm thick at an elevated temperature or when exposed to an oxygen plasma. Research [130] showed that this oxide layer degrades

its adhesion and ability to bond. To produce a reliable metallisation, Cr_2O_3 must be prevented during deposition. This is achieved by ensuring a high vacuum in the PVD/CVD chamber and by controlling the temperature of the substrate.

Attention should be paid to nickel, a metal that is widely used as a diffusion barrier and surface finishing of electroplated gold. Owing to its high permeability, the skin depth of RF is very low resulting in a very low Q factor device due to high resistance. The same conclusion applies to cobalt and other ferromagnetic metals.

For CCW structures, electrodes are typical ~ 30 µm high. Using Cr/Pt/Au system is no longer economic. As discussed in section 4.4.1, copper is the ideal material for fabricating such a bulky electrode. Copper naturally has good adhesion to SiO_2, however, a diffusion barrier layer has to be introduced between copper and SiO_2. Study [131] showed that a thin layer of Ti between 5 and 7.5 nm can block the motion of copper into oxide.

Fabrication of high breakdown voltage ion trap

Several specially designed structures were fabricated. The design of the breakdown test structures is shown in Fig. 5.16. The gaps of the structures are 3 µm and 5 µm. The corners of the electrodes are rounded (5 µm radius) as discussed in section 5.1. Two batches of samples were prepared. They were both using 6 inch HR silicon substrates from Topsil. The experiment batch has 12 µm of high-quality, stress-free 'sandwich' structure thick dielectric described in section 5.3. The control batch has 555 nm[31] of thermally grown[32] native oxide. Electrodes in both batches were photoresist-masked electroplated 4 µm gold[33]. The seed layer was 200 nm sputtered Au, 20 nm Pt and 20 nm Cr as discussed in section 5.5.3. The recipes for seed layers are in appendix A.2, the thickness of the films were endpointed by an in situ quartz crystal sensor[34]. The electroplating process is detailed in section 6.5. The seed layer was removed using ion milling technique (recipe A.3.3) after electroplating. The fabrication workflow of the experiment batch and its results can be easily transferred to a scalable quantum computer unit design with the same minimum gap size and electrode corner shape.

The processed wafers were diced using Mitsuboshi Diamond MS300A-CE scriber[35]. The

[31] Measured using JA Woollam M-2000 spectroscopic ellipsometer. Mean-squared-error= 3.5.
[32] Wet oxidation at 800°C using the Tempress Furnaces.
[33] The 'grown in pattern' method, see section 6.3.
[34] Inficon SQM-160 thin film deposition monitor.
[35] Recipe: 10 MPa blade pressure, diamond coated resin blade.

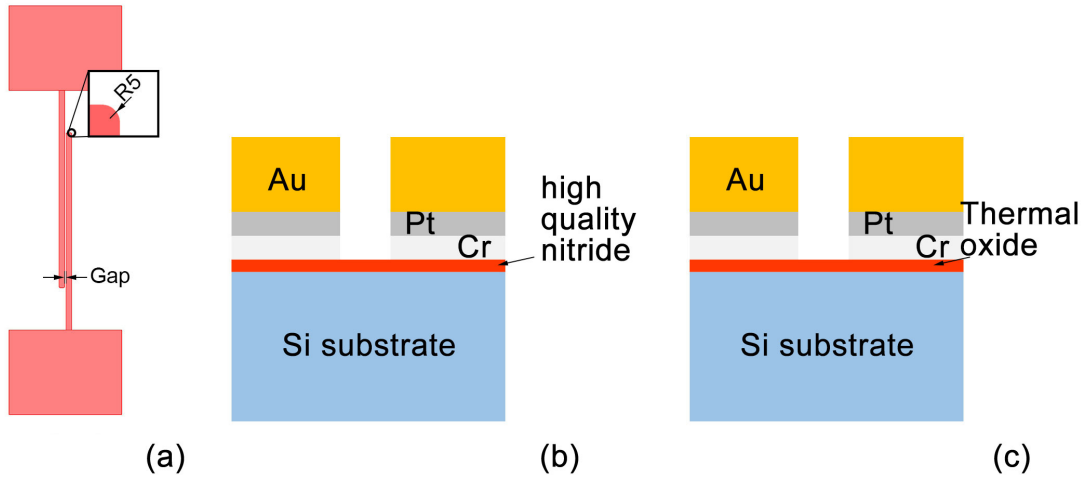

Figure 5.16: Breakdown structures. **(a)** Geometry of the breakdown patterns. Devices with gaps of 3 µm and 5 µm were measured. The fingers are 700 µm long and 20 µm wide. The corners at the ends are rounded with 5 µm radius. The bond pads are 300×410 µm. **(b)** (image not to scale) layer structure of the experiment batch. The high-quality nitride layer is 0.5 µm thick. **(c)** (image not to scale) layer structure of the control batch. The thermal oxide is 555 nm. In all batches, the metal layers are 4 µm Au, 20 nm Pt and 20 nm Cr.

chips were glued onto a PCB chip carrier[36] using indium[37]. The chips were wirebonded with gold bondwire[38] using a wirebonder[39].

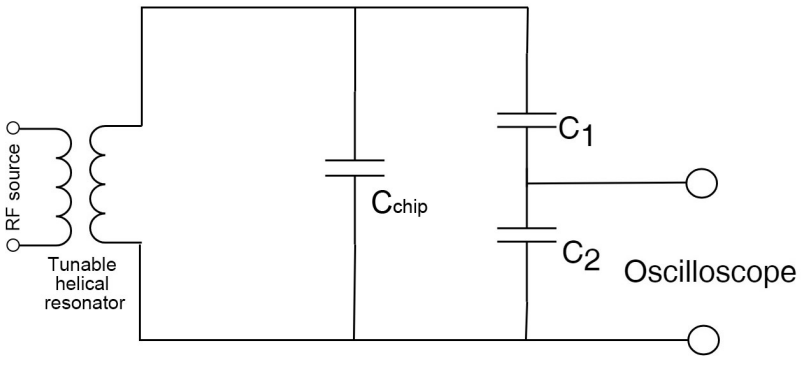

Figure 5.17: Circuit diagram of the resonant circuit.

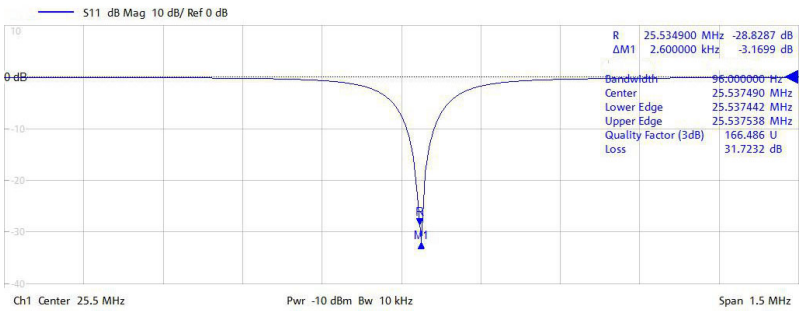

Figure 5.18: S_{11} plot of a dummy chip with resonant frequency at 25.53749 MHz and Q factor of 166.486.

5.5.4 Experimental methods

The resonant frequency of the circuit (shown in Fig. 5.17) is chip-specific. It is found by replacing the RF generator, the amplifier with a VNA and performing a scan of the S_{11} parameter[40]. The resonance of the circuit changes as the inductance of the helical resonator is tuned. Fig. 5.18 shows the S_{11} plot of a chip where the resonant frequency of the circuit is 25.53749 MHz. The resonance gives us the Q factor of the circuit, a Q value of 50 or more is required to produce a high voltage on the trap. In Fig. 5.18, the Q factor is 166.486.

For a breakdown test, a chip is supplied with an RF signal at the resonant frequency. The voltage on the trap is calculated from the known ratio of the measured voltage on C_2 to that on the trap. Every 5 min, the chip voltage is stepped up by 25 Vpp . Every 100 Vpp increase, the voltage is kept for 30 min rather than 5 min to allow the system to reach an equilibrium.

A sudden loss of resonance or arcing on cameras indicates a breakdown. This often changes the capacitance of the chip. 2 hours after the breakdown, the RF was switched on and the resonance on the same chip was found again. If a resonance is found, the breakdown is considered a partial breakdown, otherwise a total breakdown if there is no resonance between 1-30 MHz. Some devices can operate at the new resonant frequency for a short while.

Optical microscopes and Scanning Electron Microscope (SEM) were used to inspect the

[36] Desgined by Dr David Murgia.
[37] Indium, 1.6mm diameter, 99.99% pure from CMR direct.
[38] 99.99% pure Au, 8 grams of minimum tensile strength from Coining.
[39] Model: Kulicke & Soffa 4523A.
[40] S_{11} is a measure of how much power is reflected from the circuit. At its resonance, the reflection is at the minimum.

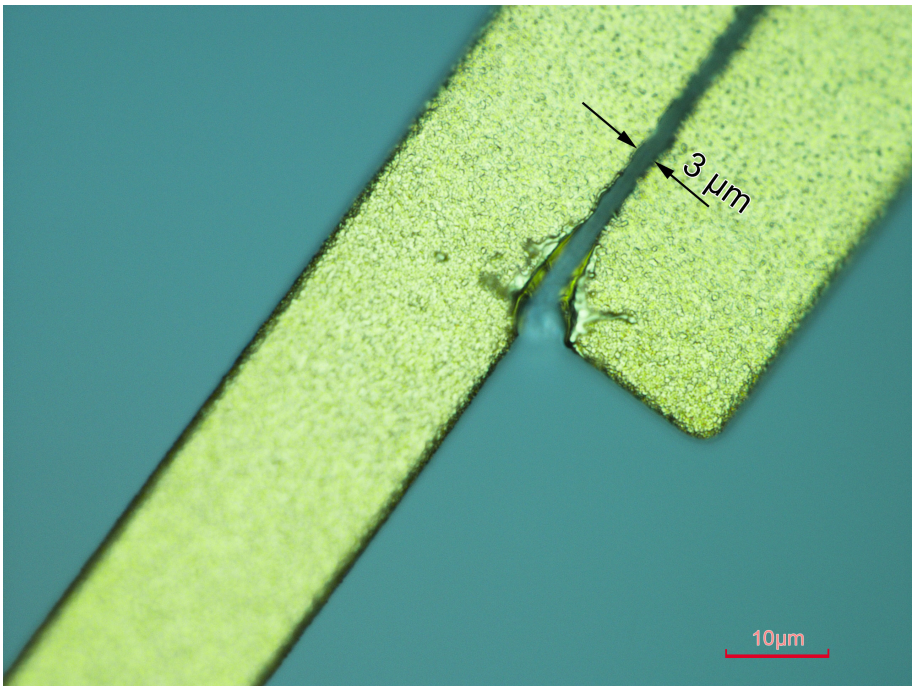

Figure 5.19: Microscope image of electrodes after surface flashover on a sample of 3 µm gap with an optimised PECVD dielectric film. The surface flashover voltage is 570 Vpp .

electrodes both before and after the experiment. Probes described in section 5.5.2 are used to measure both DC and RF resistivity between two points on the electrodes.

5.5.5 Improved breakdown voltage with high-quality dielectric films

Previously in section 5.3, methods were reported on depositing PECVD films with low etch rates and low residual stresses. To characterise the improvement of surface flashover with the high-quality film, samples fabricated with conventional PECVD films and high-quality films were tested.

Using the experimental methods described in the last section. Those surface flashovers occur at the sharp end of the electrodes and the electrode materials are carried away from the gap. Fig. 5.19 shows a microscope image of the electrodes after surface flashover. Fig. 5.20 shows the surface flashover voltages of chips fabricated with conventional and optimised PECVD nitride films. The optimised PECVD nitride film reveals a higher surface flashover voltage in both 3 µm gap and 5 µm gap.

In section 5.3, a thick, stress-free dielectric structure known as the 'sandwich' layers was reported. A linear ion trap fabricated with 6 µm thick dielectric layer was used in the cryogenic system and successfully trapped ions[41]. The trap uses silicon as substrate and

[41] Trapping experiment and heating rate measurement done by Anton Grounds.

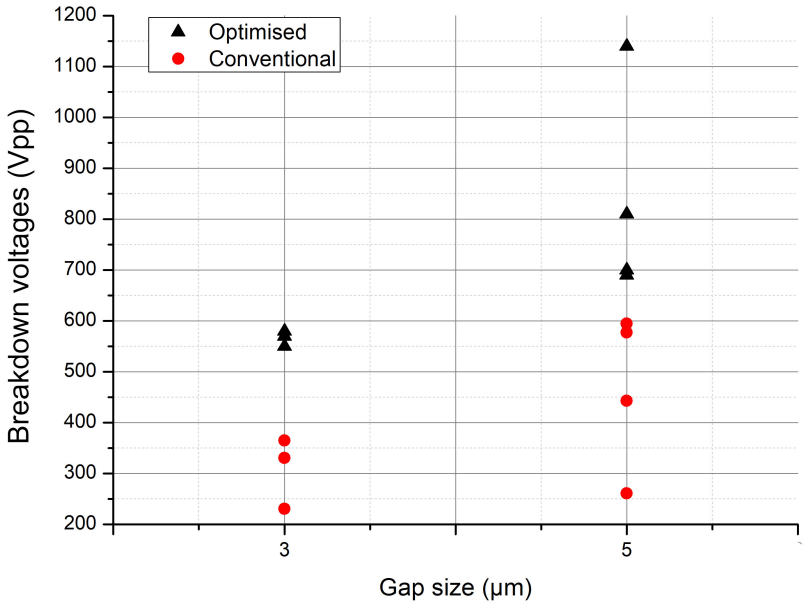

Figure 5.20: Plot of surface flashover voltages of chips with (▲) optimised PECVD dielectric films and (●) conventional PECVD dielectric films.

has 3 µm thick gold as electrodes. The geometry of the trap is shown in Fig. 5.21. The trap was designed and simulated with the DST, the targeted ion height was 100 µm. The actual ion height measured was 96 µm, this is due to the error in fabrication lithography and thermal expansion in cryogenic temperature. Ions were trapped at 400 Vpp , 14.929 MHz for over 7 hours. The radial secular frequencies are 1.052 MHz and 1.131 MHz. The trap exhibits an average heating rate of 423(3) phonons/s at 138.8 kHz, corresponding to $S_E(1\text{ MHz}) = 2.45(10) \times 10^{-13}\ (\text{V/m})^2$.

5.6 Conclusion

This chapter described the experimental works on improving the breakdown voltage through optimising the film quality using a different microfabrication process. The optimised dielectric films had low stress and an improved breakdown voltages. The experiment entailed the construction of a vacuum jar, the optical path and the active RF probe. The numerical tool developed in the last chapter served to investigate the breakdown observed experimentally. Reliable trapping was demonstrated. The ion trappers will benefit from this work by improving the breakdown voltages in ion traps fabricated using dielectric layers. It will also benefit the spacing engineering community in the development of ion thrusters with higher operating voltages. Further tests can be done using the oxide etched samples to qualify the improvement of breakdown voltage due to the oxide etch.

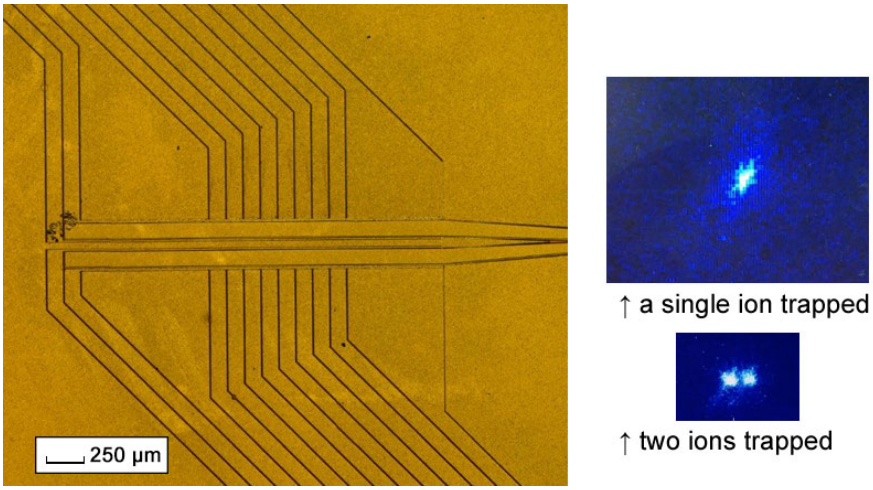

Figure 5.21: (left) The layout of the linear trap and (right) CCD images of trapped ions. The trap has a total of 16 control DC electrodes, 4 rotation DC electrodes. The colour difference in the gold surface and the black stains are due to the plating defects.

Chapter 6

Design and fabrication of low loss ion traps

6.1 RF loss in ion traps

RF loss happens when an RF signal is applied to a chip that has a lossy dielectric substrate, resistive electrodes or geometries with certainty properties, resulting in a dissipation of RF power in form of heat and radiation The consequences of poor thermal management of a chip are stated in point 10 of section 3.2. In ion trap fabrication, materials are carefully chosen in pursuit of a minimum thermal dissipation from RF loss. An efficient way of cooling the chips is to use micromachined channel cooler which is detailed in [86]. In this section, the RF loss in the trap was studied using what is known as the transmission line model.

RF signals are conveyed through structures known as waveguides. The electrical characteristics of a waveguide are described with the transmission line model where the signal and ground electrodes are represented as an infinite series of two-port elementary components. Each represents an infinitesimally short segment with a distributed resistance R in series, a distributed inductance L in series, a shunt capacitance C between two conductors and a shunt resistor with a conductance of G.

The line voltage $V(x)$ and current $I(x)$ can be expressed in the frequency domain as

$$\frac{\partial V(x)}{\partial x} = -(R + j\omega L)I(x), \tag{6.1}$$

$$\frac{\partial I(x)}{\partial x} = -(G + j\omega C)V(x). \tag{6.2}$$

By differentiating both equations with respect to x, a pair of hyperbolic partial differential equations was obtained:

$$\frac{\partial^2 V(x)}{\partial x^2} = \gamma^2 V(x), \tag{6.3}$$

$$\frac{\partial^2 I(x)}{\partial x^2} = \gamma^2 I(x) \tag{6.4}$$

where γ is the propagation constant

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)}. \tag{6.5}$$

These are called Telegrapher's equations. The characteristic impedance (Z_0) is defined as the ratio between the amplitudes of the voltage and the current of a single wave propagating along the line in a uniform transmission line,

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}. \tag{6.6}$$

Z_0 is determined by the geometry and the materials of the waveguide. The impedance describes the opposition that a part of the waveguide gives to a travelling wave.

Rewrite γ into

$$\gamma = \alpha + j\beta, \tag{6.7}$$

where α is the attenuation constant in Nepers/meter. Break it down into four components representing metal loss α_{C}, dielectric loss α_{D}, dielectric conduction loss α_{G} and radiation loss α_{G}:

$$\alpha = \alpha_{\mathrm{C}} + \alpha_{\mathrm{D}} + \alpha_{\mathrm{G}} + \alpha_{\mathrm{G}}. \tag{6.8}$$

In the discussion below, each term is studied in detail.

Metal loss: skin depth

The metal loss in RF is greater than that of equal DC voltage due to the skin effect. The skin effect describes the phenomenon where the current density of an alternating current is largest near the surface of the conductor and decreases as the depth is greater in the conductor. For conductors made of a single kind of metal, the skin depth δ_s describes the

depth below the surface of the conductor at which the current density falls to $1/e$ of that at the surface:

$$\delta_s = \sqrt{\frac{2\rho}{2\pi f \mu_0 \mu_r}} \tag{6.9}$$

where f is the frequency and ρ, μ_0, μ_r are the resistivity, permeability constant and relative permeability of the metal.

A gradient in the current density from the surface to the skin depth exists. At the surface, the conductivity that the RF signal sees is 100% of that of the material, at one skin depth, it decreased to $1/e$ (36.8%), at two skin depths, it is $1/e^2$ (13.5%) and so on. Approximate the attenuation due to the skin effect with the minimum RF sheet resistance

$$R_{\mathrm{M}} = \frac{\rho}{\delta_s} = \sqrt{\pi f \mu_0 \mu_R \rho}. \tag{6.10}$$

The attenuation is thus

$$\alpha_{\mathrm{CS}} = \frac{R_{\mathrm{M}}}{2Z_0}, \tag{6.11}$$

Note that the unit of α_C is Nepers per meter. To convert it into dB per meter, it must be multiplied by 8.686 (dB per meter/Nepers per meter).

Metal loss: surface roughness

Another source of loss comes from the metal-air interface. The incident wave is reflected, scattered and absorbed by the rough surface. The induced loss is empirically described by [132]

$$\alpha_{\mathrm{CR}} = \alpha_{\mathrm{CS}}\left(\frac{2}{\pi}\tan^{-1}\left(1.4\frac{\delta}{\delta_s}\right)\right) \tag{6.12}$$

where α_{CR} is the loss due to roughness, δ is the RMS roughness. So the total conductor's loss is $\alpha_{\mathrm{C}} = \alpha_{\mathrm{CS}} + \alpha_{\mathrm{CR}}$.

Attenuation due to dielectric damping and substrate conductivity

For a dielectric material, an applied electric field $\vec{E}$ causes the polarization of atoms/molecules of the materials to create electric dipole moments that augment the total displacement flux, $\vec{D}$. This induced polarization vector is called electric polarization $\vec{P}_e$:

$$\vec{D} = \epsilon_0 \vec{E} + \vec{P}_e, \tag{6.13}$$

where ϵ_0 is the vacuum permittivity. In a linear medium, the electric polarisation is linearly proportional to the applied electric field:

$$\vec{P_e} = \epsilon_0 \chi_e \vec{E} \tag{6.14}$$

where χ_e is the complex electric susceptibility. Then,

$$\vec{D} = \epsilon_0 \vec{E} + \vec{P_e} = \epsilon_0 \vec{E} + \epsilon_0 \chi_e \vec{E} = \epsilon_0 (1 + \chi_e) \vec{E} = \epsilon \vec{E}, \tag{6.15}$$

where ϵ is the complex permittivity of the medium. It can be rewritten in form of

$$\epsilon = \epsilon_r - j\epsilon_i \tag{6.16}$$

where the imaginary part, $-j\epsilon_i$, accounts for the loss in the medium due to the damping of the vibrating dipole moments (i.e. dielectric damping [133]). It must be negative to satisfy energy conservation. The conduction current density is related to the applied field in the following way,

$$\vec{J_c} = \sigma \vec{E}, \tag{6.17}$$

where σ is the conductivity of the material. For a material with both conductor loss and dielectric damping loss,

$$\bigtriangledown \times \vec{H} = j\omega \vec{D} + \vec{J_c} = j\omega [\epsilon_r - j(\epsilon_i + \frac{\sigma}{\omega})] \vec{E}. \tag{6.18}$$

The imaginary part represents for the loss in the material. It includes dielectric damping loss (ϵ_i) and the conductivity loss (σ/ω). Rearrange the terms in ϵ

$$\epsilon = \epsilon_r - j(\epsilon_i + \frac{\sigma}{\omega}) = \epsilon_r (1 - j(\frac{\omega \epsilon_i + \sigma}{\omega \epsilon_r})) = \epsilon_r (1 - j \tan\delta) \tag{6.19}$$

where $\tan\delta$ is called loss tangent. As shown above, the loss tangent describes the dielectric damping loss and the conductivity loss of a material. It is frequency dependent. The loss tangent of a material is often experimentally measured.

At 1-50 MHz range, the ion trap can often be seen as a lumped capacitor because the device dimension is far smaller than the wavelength. To model the lumped capacitor, the loss due to the dielectric conduction and the dielectric damping effect is represented by an equivalent series resistance (ESR). The equivalent circuit of the lumped capacitor is an ESR in series with an ideal capacitor with impedance X_c. Since the loss tangent is equal

to the tangent of the angle between the capacitor's impedance vector and the negative reactive axis,

$$\tan\delta = \frac{\mathrm{ESR}}{|X_\mathrm{c}|} = \omega C_\mathrm{c}\mathrm{ESR}, \tag{6.20}$$

where C_c is the capacitance of the device modelled.

Since the loss tangent is also the ratio of the resistive power loss over the reactive power oscillating in the capacitor, the reciprocal of the loss tangent is the quality factor Q (or Q factor)

$$Q = 1/\tan\delta. \tag{6.21}$$

When $\sigma = 0$, the loss is purely due to the dielectric loss due to damping effect,

$$\alpha_\mathrm{D} = \tan\delta\frac{\omega C_c Z_0}{2}. \tag{6.22}$$

The loss due to substrate conduction is very often ignored in some applications such as coax cables and LEDs. The attenuation due to this type of loss mechanism is

$$\alpha_\mathrm{G} = GZ_0/2 \tag{6.23}$$

where the conductance $G = \sigma A/l$. A is the cross-sectional area of the conductor, l is the length of the conductor. The loss α_G is dependent on the substrate resistivity.

Radiation

The last type of attenuation is the attenuation due to radiation, α_R, which is hard to calculate due to its dependency on the coupling of the field to the environment. Often people rely upon numerical simulation tools to calculate it.

Light-induced charging

In the model and discussion above, the RF loss due to light-induced charging was not covered. In surface ion traps, laser beams are placed close to the trap surface. Scattered laser light can cause photoelectric effect on electrode surfaces. The light-induced damage on electrodes can cause the surface roughness to increase. As discussed in section 5.5.3, gold is chosen as the electrode material for its higher activation energy required. The scattered lights, when shining on the exposed silicon substrate, can create light-induced

electron holes. The band-gap of silicon is 1.17 eV at 10 K which corresponds to light with a wavelength 1061 nm. All wavelengths of the lasers used for Yb trapping were shorter than that. The electron holes induced locally increase the electrical conductivity of the silicon and consequently the RF loss [134]. It is recommended that the exposed silicon be coated with silicon nitride.

RF loss budget

Using the equations derived above, the loss caused by different mechanisms can be evaluated including metal resistivity, loss due to a rough metal surface, dielectric damping and electromagnetic radiation. Assume that the chip is made of an HR silicon substrate with resistivity $R_s = 10$ kΩcm, dielectric constant $\epsilon_R = 11.7$, loss tangent $\tan\delta = 0.005$ [1] and the device is operating at 10 MHz. The electrodes are made of gold with perfect surface smoothness and they are 4 μm thick. Use equation 6.11, 6.22 and 6.23,

$$\alpha_{\mathrm{C}} = 8.25 \times 10^{-5} \quad (\mathrm{dB/m}) \tag{6.24}$$

$$\alpha_{\mathrm{D}} = 0.311 \times 10^{-3} \quad (\mathrm{dB/m}) \tag{6.25}$$

and

$$\alpha_{\mathrm{G}} = 0.030401 \quad (\mathrm{dB/m}). \tag{6.26}$$

The total attenuation of an HR silicon ion trap α_1 is 3.36×10^{-2} dB/m.

Many chips in this work are made of R-plane sapphire substrates supplied by Precision Micro-Optics which have a resistivity of 10^{11} kΩcm, dielectric constant $\epsilon_R = 10$ and dielectric loss of 0.0001, therefore, at the frequency of interest,

$$\alpha_{\mathrm{C}} = 8.25 \times 10^{-5} \quad (\mathrm{dB/m}) \tag{6.27}$$

$$\alpha_{\mathrm{D}} = 0.576 \times 10^{-5} \quad (\mathrm{dB/m}) \tag{6.28}$$

and

$$\alpha_{\mathrm{G}} = 3.04 \times 10^{-9} \quad (\mathrm{dB/m}). \tag{6.29}$$

The total attenuation of sapphire ion trap $\alpha_2 = 1.4 \times 10^{-4}$ dB/m.

[1] HiRes series wafers were supplied by Topsil. In this thesis, unless stated otherwise, 10k silicon or HR silicon wafer refers to the HiRes series 10 kΩcm silicon wafer by Topsil.

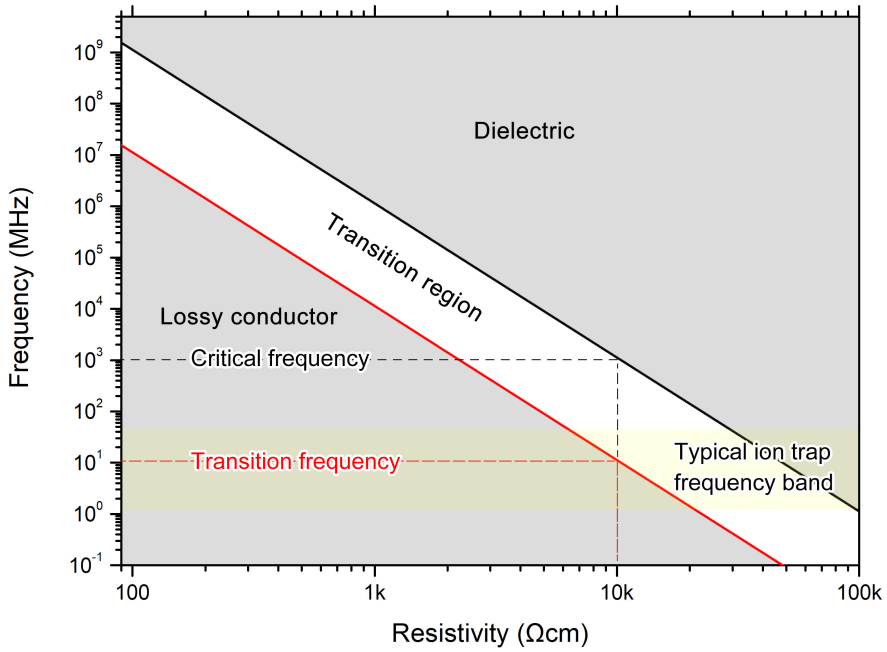

Figure 6.1: Frequency as a function of silicon substrate resistivity. Silicon is mainly a dielectric in the top-right region, a conductor in the bottom-left region and a mix of the two in the transition region between the two. The shaded yellow area is the frequency band where typical ion traps operate at. The dashed lines show the critical frequency and transition frequency of a 10 kΩcm silicon substrate.

The ratio between the two attenuations are

$$\alpha_2/\alpha_1 = 240. \tag{6.30}$$

The loss in HR silicon chips is 240 times worse than the loss in sapphire chips. The 10 K HR silicon substrate ion trap and sapphire substrate ion trap were made and tested. The details and results of the tests are in section 6.6.

The substrate resistivity of silicon

This section discusses the dependency between the substrate loss and the resistivity of the silicon substrates. From equation 6.23, it is obvious that if the resistivity of the dielectric is greater than 1 MΩcm, α_G is less than 1% of α_{CS} at 10 MHz. α_G can therefore be ignored for most substrates but silicon since the resistivity of silicon substrates can range from as low as 1 Ωcm (heavily doped lossy silicon) to 100 kΩcm (expensive high purity float-zone silicon for GHz applications). Assuming that the electrodes are made of 4 μm thick perfectly smooth gold, when the conduction loss α_G is greater than the metal sheet resistance loss α_{CS}, no doubt the substrate behaves more like a conductor than a dielectric.

Fig. 6.1 shows the frequency as a function of silicon substrate resistivity. The red line is where $\alpha_{CS} = \alpha_G$, the area below the line is the lossy conductor region. The black line is where $\alpha_{CS}/\alpha_G = 10$ dB, i.e. the region where the sheet resistance loss is significantly higher than α_G. The loss mechanism in the region above the black line is dominated by α_{CS}. In this discussion, α_{CR} and α_D are ignored as they are dependent on the surface roughness of the electrode surface and the nature of the dielectric material. From Fig. 6.1, 10k silicon substrate is very lossy below 10 MHz as indicated by the red dash line. For 10k silicon, the critical frequency is, as the black dash line indicated, about 100 MHz. The shaded yellow area is the frequency band where typical ion traps operate at. In a short conclusion, for ion trap applications, silicon substrates need to have a minimal resistivity of 100 kΩcm to be considered not lossy.

So far the attenuations due to the metal and dielectric properties are discussed based on the microscopic mechanisms including dielectric damping, skin effect and substrate conduction. It is demonstrated that a sapphire substrate is 240 times better than an HR silicon in term of RF loss using the model developed. This method can aid the design of GHz/THz devices, RF MEMS switches and millimeter-wave attenuators by selecting the correct substrate. However, in this model, surface roughness was not considered. For a long time, it has been known that the RF resistance also deviates from the metal resistivity [135]. Such discrepancy is attributed to the surface roughness of the conductor. Recent works [136, 137] reported the quantitative model using different methods. Further work can be done to include the effect of surface roughness to give a more precise value of the attenuation.

6.2 Minimisation of impedance mismatch

6.2.1 Reflection due to impedance mismatch

In the model above, the transmission line was assumed to be infinitely long and uniform thus the wave travels forward perfectly. However, in reality, waveguides often have bends and changes in their geometries which cause changes in transmission line characteristics (known as impedance mismatch). As a result of mismatching, a portion of the electromagnetic wave is impeded and reflected. Reflection coefficient Γ is defined by

$$\Gamma = \frac{E_-}{E_+} = \frac{Z_L - Z_S}{Z_L + Z_S} \tag{6.31}$$

where E_- is the electric field strength that is reflected and E_+ is that of the incident wave. By definition, the percentage of the reflected power is Γ^2.

The fraction of incident power delivered to the load is

$$P_\mathrm{d}/P_\mathrm{i} = 1 - \Gamma^2 \tag{6.32}$$

where P_d is the delivered power and P_i is the incident power where the reflected power $P_\mathrm{r} = P_\mathrm{i} - P_\mathrm{d}$. Mismatch loss L_m then is

$$L_\mathrm{m} = 10\log_{10}(\frac{P_\mathrm{i}}{P_\mathrm{i} - P_\mathrm{r}}) = -10\log_{10}(1 - \Gamma^2). \tag{6.33}$$

Mismatch loss represents the amount of power that is reflected hence not delivered to the output due to the impedance discontinuity of the transmission medium. To further explain the concept of mismatch loss, the mismatch loss is calculated where 3 different components are connected to the same standard 50 Ω impedance coax input with an arbitrary RF signal excitation. The first component is a 50 Ω dummy load, $\Gamma = 0$ thus, $L_\mathrm{m} = 0$. There is no mismatch loss, in this case, it is a perfect match. The second component is an actual sapphire chip with measured impedance of $(200 + j300)$ Ω. With some simple calculation, we have $\Gamma = 0.756$, thus $L_\mathrm{m} = 3.687$ dB. Finally, an HR silicon chip, with a measured impedance of $(340 + j480)\Omega$, results in $\Gamma = 0.8433$ and $L_\mathrm{m} = 5.39$ dB.

The impedance is dependent on the material of the chip, the vertical structure of the chip and the geometry of the surface structure. For example, a chip with a ground plane is likely to have a higher capacitance.

Fig. 6.2(a) shows the electrical field strength distribution, simulated using the toolkit introduced in section 4.1, of the 'vertical shuttling trap' who has sharply bending RF rails (Fig. 4.1). It was reported by researchers [72] that the chip was not able to trap ions due to insufficient trapping potential despite a high RF input applied. From the simulations, it is clear that the sharp bend causes an impedance mismatch and prevents sufficient transmission of RF signal along the rail. This is an example of poorly designed geometry causing power loss. The RF signal is fed from the lower edge of the chip passing through a near 135° bend, then the linear trapping area. In a perfectly matched case with no reflection, the electric field strength should be uniform all along the electrodes as shown in Fig. 6.2(b) however, due to the presence of the bend, the RF signal is heavily impeded thus little electric field reaches the trapping region. This was confirmed by successful

trapping after replacing the chip with a chip with only straight RF electrodes.

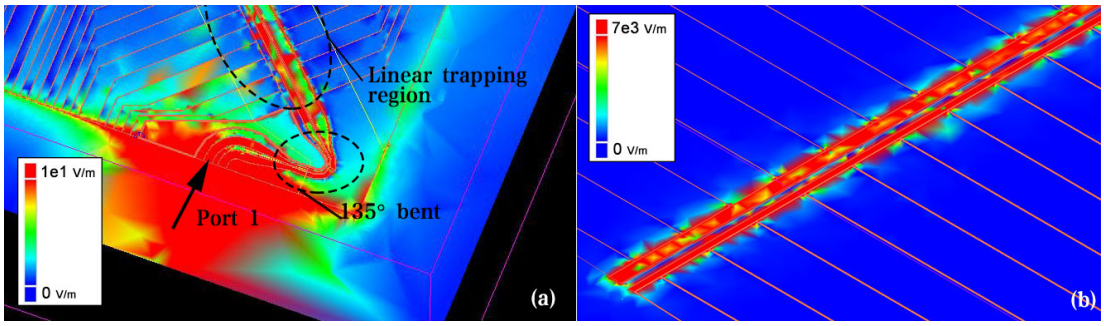

Figure 6.2: Simulated electric field strength distribution on the chip surface plane with and without a 135° bend structure. **(a)** A strong electric field near the input port (port 1) presents. The electric field strength on electrode surfaces in the linear trapping region is weaker compared to that in (b). **(b)** Without the 135° bend structure, the RF signals are no longer reflected thus remains uniform. The electric field strength on electrode surfaces in the linear trapping region is stronger than 3×10^3 V/m.

To quantify the mismatch, the S-parameters are compared between the current geometry and the geometry without bends. S_{11} is the input voltage reflection coefficient on the input port (port 1 as shown in Fig. 6.2) representing the ratio of the reflected voltage over the forward travelling voltage on this port. A much smaller reflection is observed without the bend as the S_{11} dropped from -17.4 to -27.0 dB.

RF phase mismatch

RF phase mismatch refers to the phenomenon where a difference exists between the phases on the pair of RF electrodes that form a quadrupole. It may be caused by asymmetries in the electrical impedance of the electrodes or a difference between RF path lengths. Following the work in [129, 138, 139], the effect of the phase mismatch on the trapped ion is investigated.

Assume that the amplitude of the RF field at the RF nil is E_0 and is driven at frequency Ω. The phase mismatch between the two electrodes is δ. The electric field at ion's trapping position is

$$E_{\mathrm{RFnil}} = E_0 \cos \Omega t - E_0 \cos(\Omega t + \delta). \tag{6.34}$$

When the mismatch is small enough, $\delta \ll 1$, the equation above simplifies to

$$E_{\mathrm{RFnil}} = E_0 \delta \cos \Omega t. \tag{6.35}$$

The non-vanishing oscillating field E_{RFnil} will act on the ion a net force $F = eE_{\mathrm{RFnil}} = m\ddot{x}$. Solving the equation of motion (equation 2.5) gives the micromotion amplitude

$$x_{\mathrm{m}} = -\frac{qE_0\delta}{m\Omega^2}. \tag{6.36}$$

When a typical ion trap operates at 200 V, the amplitude of electric field at the RF nil E_0 is approximately $750,000$ V/m. The corresponding micromotion amplitude is $x_{\mathrm{m}} \simeq 2\times10^{-7}$ m. Assuming a cooling beam with wavevector $k_{\mathrm{m}} = 0.5 \times 2\pi/\lambda$ cools the ion and the driving frequency is $\Omega = 20$ MHz, the Doppler shift caused by the micromotion is

$$k_{\mathrm{m}}x_{\mathrm{m}}\Omega = 340 \times 10^5 \quad \text{(Hz)} \tag{6.37}$$

which is on the same order as the shift induced by $163,000$ motional quanta for $\omega_z = 2\pi \times 180$ kHz thus significant for any coherent operations on this trap.

6.2.2 Modes of RF signals in an ion trap

To study the trapping field produced by a specific electrode geometry, the modes in RF waveguide structures are reviewed. First, let it be reminded that AC signals are non-existent in the absence of ground. The electromagnetic wave propagates as the electrons oscillate in both the signal and ground conductors. The ground, when considered ideal, is defined as an infinitely large conductor where the fluctuations of the potential are negligible. The ground defines where and how the electric field distributes in the space between itself and the signal electrode. In addition, from the current's point of view, the ground offers a return path to the source thus a closed-loop forms. A poor ground will increase the resistance of the whole system.

When an electromagnetic wave is propagating down in a well-defined form, the structure that confines it could be considered a waveguide. By far the most commonly used planar waveguides include parallel-plate, stripline, microstrip and coplanar waveguide (CPW). They can be precisely machined using widely available low-cost printed circuit board technologies. They can also be easily fabricated with microfabrication techniques.

Waves in the parallel-plate waveguide and the stripline in Fig. 6.3(a) and (c) propagates with TEM mode. In the microstrip and CPW in Fig. 6.3(b) and (d), the electric field was distributed in two dielectric domains: the air and the substrate dielectric, thus the dominant mode is quasi-TEM as shown in Fig. 6.4. This mode has a 0-Hz cutoff frequency

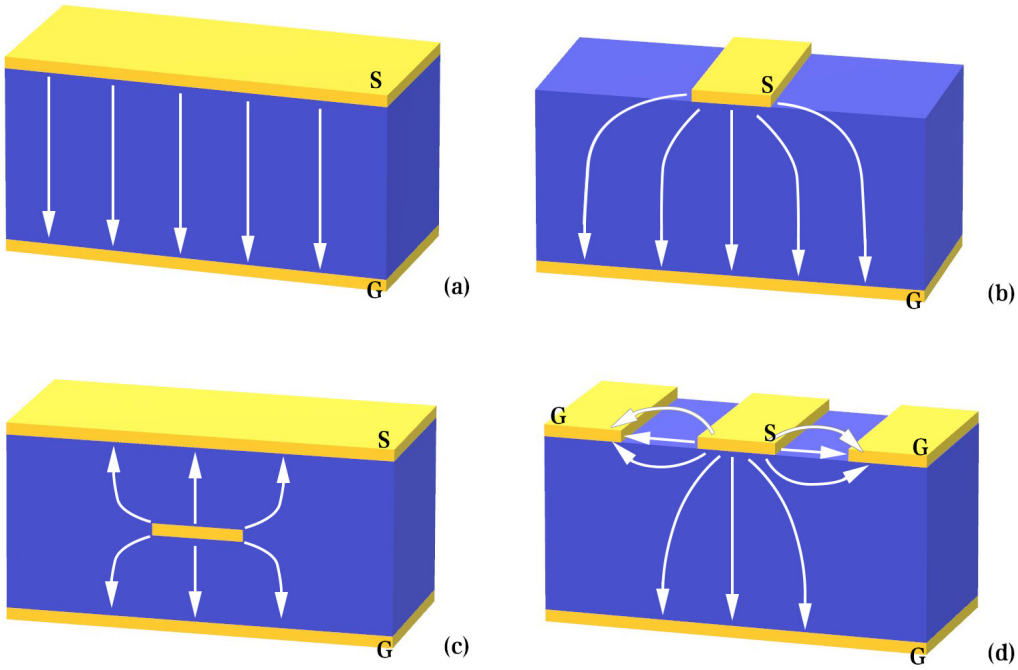

Figure 6.3: Common multiconductor planar transmission lines and their TEM mode E-field lines. Electric field lines are marked with white arrowed lines. Conductors (Yellow) are spaced with dielectrics (blue). '**G**' marks a ground electrode and '**S**' marks a signal electrode. The modes are **(a)** parallel-plate, **(b)** microstrip, **(c)** stripline and **(d)** CPW.

and a slow change of characteristic impedance and propagation constant with increasing frequency. Apart from these, the quasi-TEM mode is very similar to TEM mode.

When a ground plane presents is present in a CPW structure, it is known as a grounded coplanar waveguide (GCPW) which is used as an alternative to microstrip. Typically the spacing between the signal strip and the top grounds is larger than the thickness of the substrate, so the GCPW field is concentrated between the signal electrode and the substrate ground plane. This makes GCPW more isolated than microstrip and less prone to radiate.

In most surface ion trap designs, the structures are either CPW or GCPW. Due to the E-field distribution described above, the electric field strength produced by the planar waveguide structures in a surface ion trap is weaker at RF nil when the same voltage is applied compared to that of a conventional 3D quadrupole trap. Therefore surface ion traps have a much smaller trap depth, typically only ~ 0.1 eV while a conventional quadrupole trap can easily have 1 eV. As reviewed in section 6.1, stronger E-field in the dielectric material layers causes more heating due to dielectric dipole damping. In the presence of an excessively strong field, the electrical breakdown happens and destroys

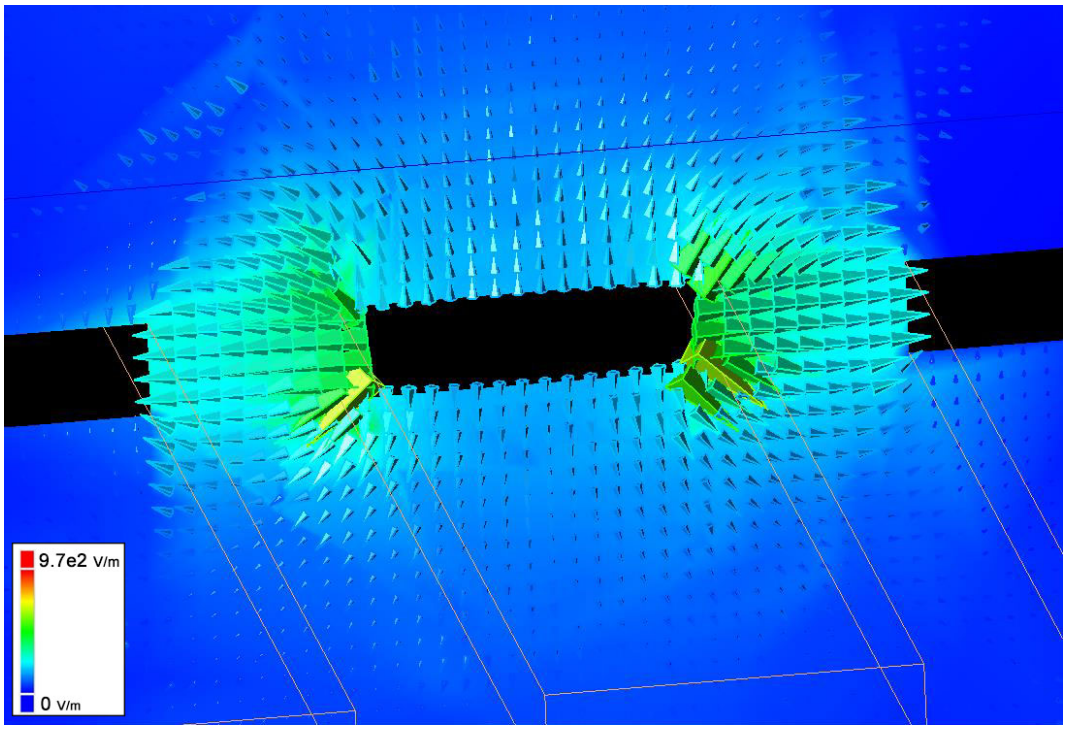

Figure 6.4: E-field distribution of a CPW. The central electrode carries the signal and the outer two electrodes are grounds.

the device. The breakdowns of ion traps are discussed in Chapter 5. The planar waveguides are compatible with both low-cost state-of-art printed circuit board technology and microfabrication technology used for ion trap minimization.

In this work, the monolithic ion trap chip is placed on a PCB and wirebonded to the planar waveguide on the carrier PCB, see Fig. 6.5. The bond wire connection forms an arch shape providing mechanical strain relief. In the IQT group, 3 major types of bondwires were used, gold and aluminium wires of 25 µm diameter, and gold ribbon with 100 µm by 25 µm cross-section[2].

The maximum current that the bond wire can withstand is limited by the resistive heating. For a given current I, electrical resistivity ρ, a wire with length l and cross-sectional area A, the heat $q = I^2R = I^2\rho l/A$. The temperature gradient over the wire $\Delta T = ql/(4A\lambda)$ where λ is the thermal conductivity of the wire material. The maximum current that the wire can take $I_{\max}$ presents when the wire reaches its melting point T_{M}. Substituting the equations above, the maximum current $I_{\max}$ yields

$$I_{\max} = \sqrt{\frac{\lambda}{\rho}\frac{A}{l}}\sqrt{T_{\mathrm{M}} - T_0} \tag{6.38}$$

[2]All coining products were from AMETEK Inc.

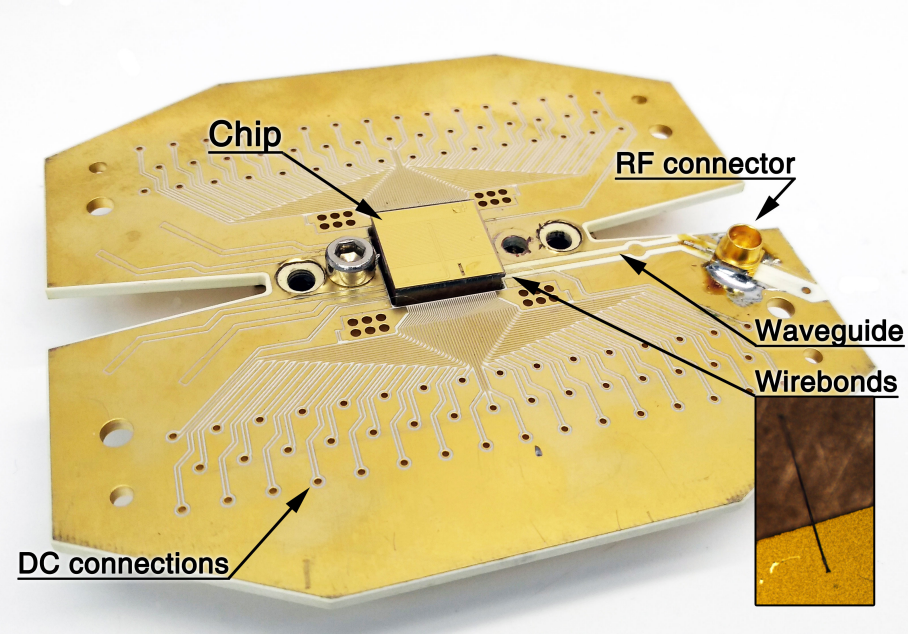

Figure 6.5: Image of an ion trap chip sitting on a carrier PCB. Bond wires are used to connect RF signals from the waveguide on the PCB to the RF electrodes on the chip.

where T_0 is the ambient temperature of the PCB and ion trap chip.

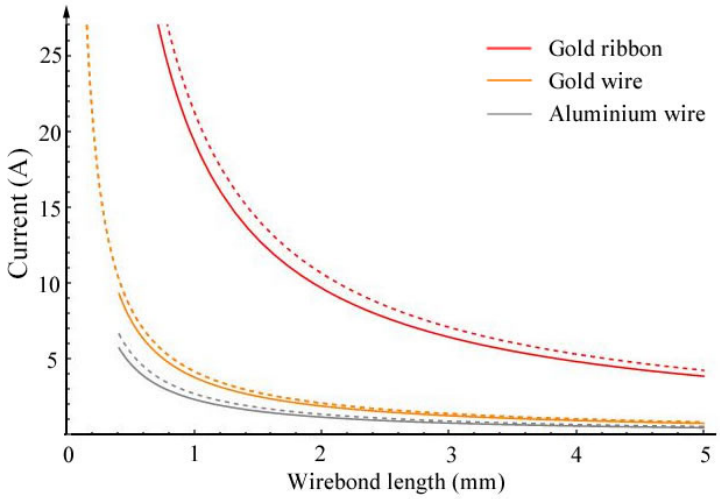

Figure 6.6: Plot of maximum current each single wirebond can take at various lengths. The dashed lines indicates scenarios for liquid nitrogen cooled system ($\sim$ 80 K). The solid lines are for room temperature systems ($\sim$ 300 K).

Fig. 6.6 shows the maximum current of different bond wires in a conventional 300 K environment and a liquid nitrogen system (80 K). Aluminium wires have a lower maximum current due to lower electrical and thermal conductivity. Gold ribbons are used when a high current is desired such as connecting CCW structures.

When the signal travels from the carrier to the chip, there is a change of impedance due

to the presence of the wirebonds. The theoretical model of bond wires was well studied by K. Mouthaan and others [140–142], known as 'Philips/TU Delft bond wires model' which is based on calculating the self and mutual inductance matrixes of the coupled bond wires as a function of geometrical shapes of the wires. With this model, the RF loss is calculated given a defined wire shape. Fig. 6.7 shows the RF loss of the same bond wire with different frequency. The loss is negligible at 10-20 MHz however, significant at 12 GHz.

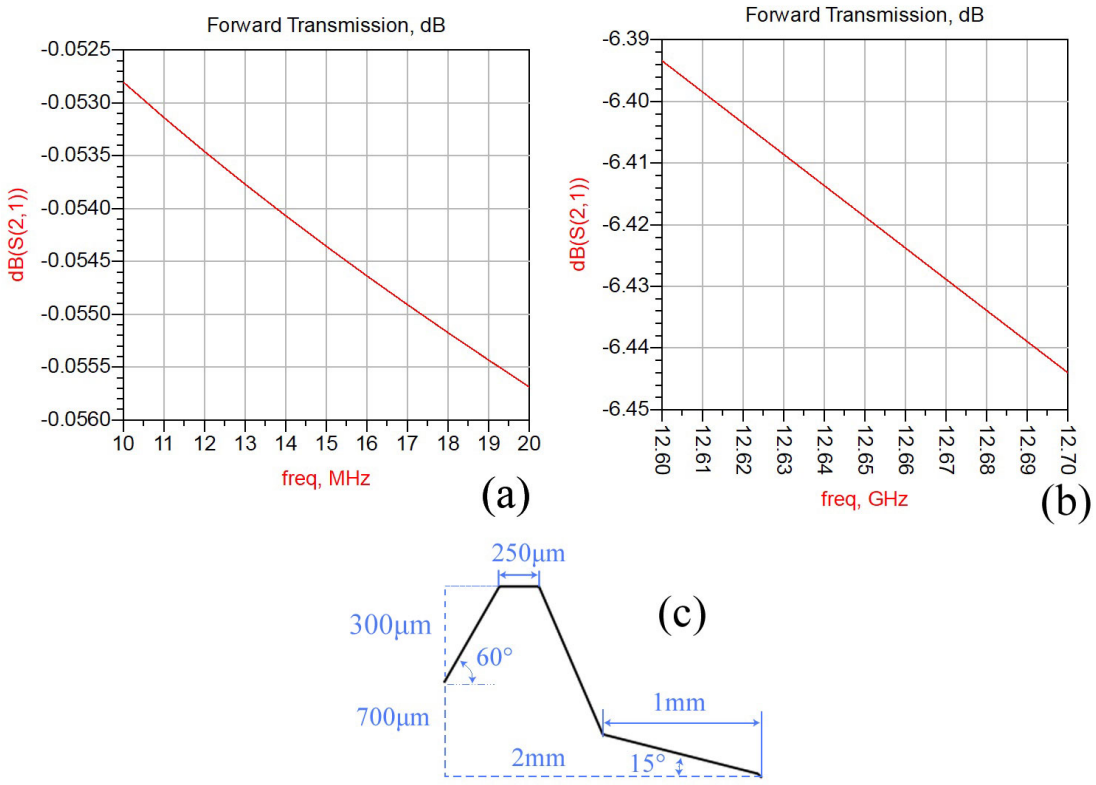

Figure 6.7: Plot of the forward transmission (S_{21}) in dB changes with frequency. **(a)** 10-20 MHz and **(b)** 12 GHz. The shape of the wirebond used in the model is specified in **(c)**.

To reduce the RF loss at microwave frequency, a structure of wirebonds that is similar to CPW has to be used. The central wire carrier the signal and the sides grounds. By doing this, the loss is significantly reduced from −6.41 dB to −1.5 dB or less. Fig. 6.8 shows the RF loss against the spacing between the wires, suggesting that the spacings should be kept as small as the practice allows.

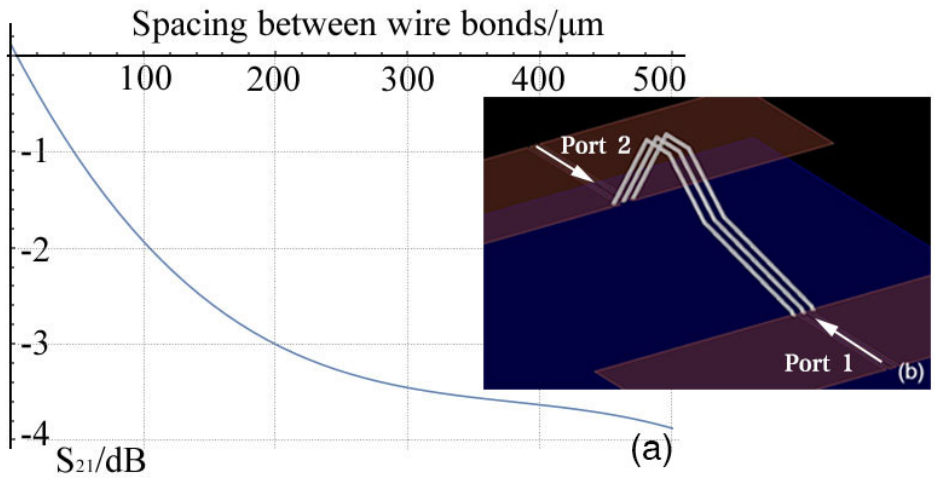

Figure 6.8: **(a)** S_{21} parameter decreases as the spacing between wires increases. **(b)** 3D representation of the three wire model. The shape of the bond wire is defined in Fig. 6.7 (c).

6.3 Deposition of tall, smooth electrodes

6.3.1 Deposition of ion trap electrodes

As discussed in section 3.2, scalable quantum computer units fabricated using modern MEMS technology need tall electrodes with low surface roughness for reduced motional heating and thermal generation. Fig. 3.1 shows that a tall electrode can effectively shield cold ions from seeing stray charges on dielectric surfaces thus reduces motional heating. In 6.1, the theoretical model suggests that a smooth surface is the key to reduce RF loss.

A conventional way of depositing patterned electrodes is 'lift-off' process (shown in Fig. 6.9(a)). However, it does not work with a thick metal layer as it does not debond well enough. There are two typical ways to fabricate patterned thick electrode layer. Etch-down process (Fig. 6.9(b)): the thick metal layer can be deposited first then etched using a mask. This method is not often used for three main reasons. First, the removal of the metal is limited by the etch selectivity against the mask. Second, metal etch often suffers from what is known as 'loading effect' where the etch rate is dependent on the size of the features. This causes uneven etch across different gaps. Third, the etch rate slows down as the aspect ratio increases in deep metal etch. This limits the height of the electrode achievable with this method. Ultimately, this method is not practical or economical in the mass production of quantum computing units. The other process is shown in Fig. 6.9(c) called 'Grow in pattern'. In this process, the photoresist is patterned on a seed layer. The electroplated metal grows in between the resist. Patterned electrodes are made after

removing the resist and exposed seed layer metal. This process is chosen in this work as it does not require deep metal etch. The challenges in developing this process are the adhesion of the photoresist to the seed layer and the chemical stability of the photoresist during plating. They were solved and detailed in section 6.5.2.

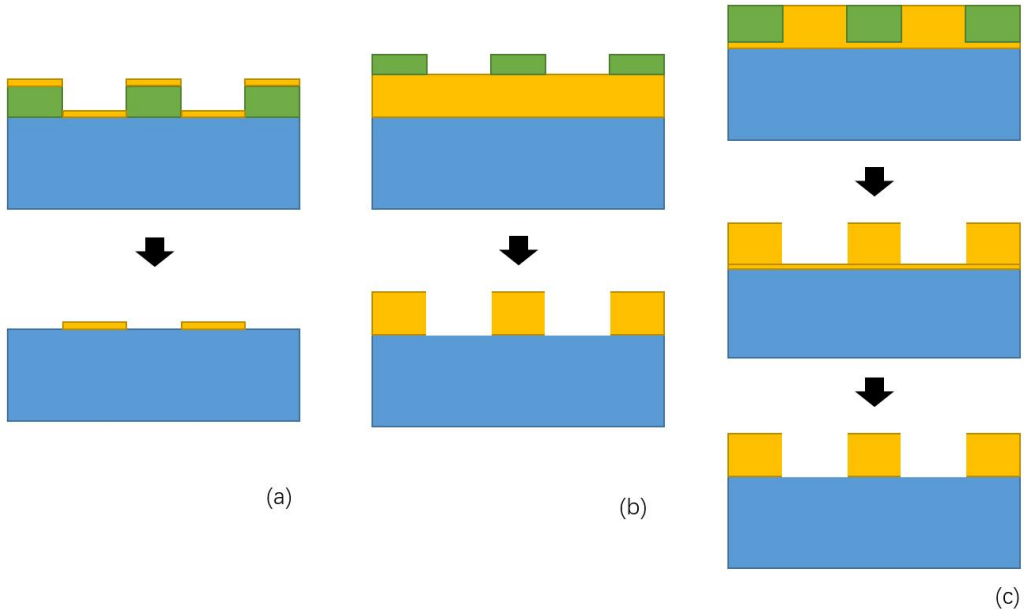

Figure 6.9: (Image not to scale) Colour keys: substrate, photoresist, thick plated electrodes. (**a**) Lift-off process. A layer of photoresist is laid prior to the coating of the metal layer. Then the photoresist is removed along with its coatings, leaving only the wanted metal patterns. (**b**) Etch-down process. The metal layer is etched using either photoresist or other materials such as SiO_2 as the mask. (**c**) 'Grow in pattern' process. The metal electrode is grown in between the resists.

6.3.2 Electroplating chemistries

Gold electroplating is extensively used in decorations, electronics industry and dental applications. In all applications, it is desirable to electrodeposit gold structures which are ductile, with low stress and hardness and good surface roughness [143]. The extent to which these properties can be obtained depends largely on the characteristics of the plating process. There are three major baths used by researchers today in gold electroplating of MEMS devices: cyanide, sulfite and thiosulfate bath.

Before reviewing specific plating processes, it is useful to review some fundamental aspects of the aqueous solution chemistry of gold. Gold exists primarily in Au(I) and Au(III) states. Electroplating baths formulated from Au(I) complexes are more popular than that from Au(III) because Au(I) ions in aqueous solution are prone to disproportionation to

form metallic gold or undergo hydrolysis to form AuOH [144]. The Au(I) ion reacts with ligands such as cyanide and sulfite forming complexes. The formation process involving a ligand, L, is written as $Au^+ + L^- \longleftrightarrow AuL$. The overall stability constant β[3] is defined as:

$$\beta = [AuL]/[Au^+][L^-]. \tag{6.39}$$

It describes the equilibrium of the chemical reaction in the electroplating baths. A high stability constant is desirable as the complex is more concentrated thus the potential difference plays the most important role in the reduction reaction. When a smooth deposition is required, electroplating baths like $Ag(NH_3)_2^+$, $Ag(S_2O_3)_2^{3-}$, $Ag(CN)_2^-$ are needed. The stability constants of the complexes listed above are 1.1×10^7, 2.9×10^{13} and 1.3×10^{21} respectively while the effective stability constant of $AgNO_3$ is 1 since it is not a complex compound.

Cyanide bath is the most commonly used gold plating solution. Gold is deposited from cyanide baths under alkaline, neutral or acid solutions at a higher rate than most non-cyanide gold plating processes [143]. $Au(CN)_2^-$ is resistant to disproportionation, hydrolysis, oxidation and ligand substitution reactions that may cause instability or decomposition. It means a long lifetime and easy-to-control plating process. Moreover, a better surface finish is often obtained through a cyanide-based process because of a slower deposition rate from a high stability constant as shown in table 6.1. However, due to the high toxicity of cyanide baths, cyanide is not often used in university clean rooms.

Sulfite baths are often used because of their ability to produce thick gold electrodes with smooth, bright, ductile and low-stress features [143]. However, the stability constant of $Au(SO_3)_2^{3-}$ is 10^{11} times lower than $Au(CN)_2^-$.

A number of works [145, 146] demonstrated micro-patterned gold structures with sulfite based plating structures. Sulfite baths are usually formulated from sodium or potassium salts. Ammonium sulphite is also available mainly for dental and industrial applications. The chemistry behind a sulfite-based process is that the excess sulfite in solution tends to decompose spontaneously to form gold and sulfite ions:

$$Au(SO_3)_2^{3-} \longleftrightarrow Au^+ + 2\,SO_2^{3-}. \tag{6.40}$$

Metallic gold is formed in the disproportionation reaction of Au(I):

[3] Also known as 'formation constant K_f'.

Table 6.1: Stability constants of various Au(I) complexes [143].

Au(I)	log β
$Au(CN)_2^-$	38.7
$Au(SO_3)_2^{3-}$	26.8
$Au(NH_3)_2^+$	19.2
$AuCl_2^-$	9.2

$$3\,Au^+ \longleftrightarrow 2\,Au + Au^{3+}. \tag{6.41}$$

An equilibrium is related to the bath temperature which is described by the electrode kinetics. Arrhenius theory gives the relation between the rate constant k and the temperature T

$$k = Ae^{-E_a/RT} \tag{6.42}$$

where A is frequency factor, a constant describing the number of attempts made at surmounting the barrier, E_a is the activation energy, an energy barrier that has to be surmounted by the reactants before they can be converted to product, and R is the molar gas constant.

A is dependent on the properties of the electrodes including potentials, surfaces, materials, etc. By raising the temperature, a higher deposition rate can be achieved.

The sulfite ion also decomposes which is a pH dependent equilibrium:

$$SO_2^{3-} + H_2O \longleftrightarrow SO_2 + 2\,OH^-. \tag{6.43}$$

So most sulfite solution has a pH of ~ 9. When the pH approaches 7, the equilibrium shifts to the right thereby releasing SO_2. In addition, there is a reaction that produces $S_2O_4^{2-}$ which is suppressed by stabilising additives in commercial solutions. In this work, a sulfite-based solution, Metalor ECF 64D, was used in the electroplating process.

6.4 Modelling the electroplating process

The electroplating process is well understood by the research community. Both mathematical models [147] and fabrication techniques [145,148] were developed investigating various phenomena in both cyanide and non-cyanide solutions. However, only a few works [149]

were published on numerically studying the electroplating deposition process for MEMS devices. The use of numerical tools helps researchers to fine-tune their plating parameters before actual plating and through numerical models, new plating techniques could be better understood and explored. Due to limited resources, pulse plating was not considered due to the cost of a high-precision pulse plating power supply.

6.4.1 Theoretical description of electroplating processes

During electroplating, an external electrode potential drives electrons to flow from cathode to anode through the electrolyte and reduction happens as the energy of the electrode increases above the lowest vacant molecular orbital of the compound in the solution. The electrons are transferred from the cathode electrode to the metal ions in the electrolyte. The metal particles adhere to the working surface depositing a thin film. Similarly, on the anode, oxidation happens where electrons are transferred from the electrolyte to the electrode. The dominating law here is Faraday's law which describes the relationship between the quantity of current passing through a system and the quantity of electrochemical change that occurs subsequently. All processes that obey such laws are termed faradaic processes. The processes that involve changes in the electrode-electrolyte interface without charge transfer taking place. Such processes are known as nonfaradaic processes [150], the majority of which is due to adsorption and desorption.

In a system without nonfaradaic processes, there is no change in charge transfer characteristic overall potential range. In this case, the pair of electrodes can be viewed as a perfect capacitor described by

$$Q = C_{\mathrm{d}} E \tag{6.44}$$

where Q is the charge stored, C_{d} the equivalent capacitance, E the potential across the electrodes.

By representing the resistance of electrolyte with R_d, the electroplating system can be viewed as an RC circuit. When a potential E is applied at $t = 0$, the charging process results in

$$Q = EC_{\mathrm{d}}(1 - e^{-t/R_d C_{\mathrm{d}}}). \tag{6.45}$$

Rewriting it gives the time dependency of the charging current in response to a potential step

$$I = E/R_{\mathrm{s}} e^{-t/R_{\mathrm{d}} C_{\mathrm{d}}}. \tag{6.46}$$

The time constant $\tau = R_{\mathrm{d}} C_{\mathrm{d}}$ of this RC circuit is significant as any faradaic current can only be measured after $t = \tau$ to avoid the influence of the charging current. Consequentially, the simulation of the charging process needs to be time-dependent.

After the charging process, the main aspects of interest are the electrolyte charge transport and electrochemical kinetics.

The potential distribution in the electrolyte ϕ is solved for with

$$\vec{i} = -\sigma \nabla \phi \tag{6.47}$$

$$\nabla \cdot \vec{i} = 0 \tag{6.48}$$

where $\vec{i}$ is the current density vector in the electrolyte and σ is the electrolyte conductivity assumed to be a constant. The current density obtained in the absence of nonfaradaic effects is known as the exchange current density. Faraday's law state the quantitative relationship between the electrons transferred and the quantity of material deposited on the working surface

$$M = \frac{mIt}{\eta \mathcal{F}} \tag{6.49}$$

where M, m, η, are the total mass, atomic weight and valency of the deposited material respectively, I is the depositing current, t is the deposition time, and $\mathcal{F}$ is Faraday's constant.

The process described above covers the electrochemistry before and after establishing the equilibrium in the absence of nonfaradaic effects. However, on passing a faradaic current, the potentials on the working electrodes E_{a} shift from the equilibrium potential E_{eq}. The extent of such shift is characterised by the overpotential

$$\bar{\eta} = E_{\mathrm{a}} - E_{\mathrm{eq}}. \tag{6.50}$$

The shift is mainly due to losses in the form of adsorption, desorption and internal resistance loss which can be characterised from the polarization curve (V-I curve).

The Butler-Volmer theory [151] models the electrode kinetics giving the charge transfer current in region n

$$i_n = i_0 (\exp\left(\frac{1.5\mathcal{F}\bar{\eta}}{RT}\right) - C \exp\left(-\frac{0.5\mathcal{F}\bar{\eta}}{RT}\right)) \tag{6.51}$$

Table 6.2: List of reproduced electroplating processes.

Wafer ID	Current	Potential	Time	Final thickness at substrate centre	Simulated thickness at the centre
GT	138 mA	3 V	3600s	1.40 µm	1.50 µm
S2a	170 mA	1.53 V	1836s	1.75 µm	1.82 µm
S7	150 mA	1.25 V	2064s	1.44 µm	1.485 µm
HR22	170 mA	1.3 V	1800s	1.80 µm	1.82 µm

where i_0 is the exchange current density on cathode, R the molar gas constant, T the temperature and C a constant relating to the ion concentration in the electrolyte.

The resultant growth of the film is time-dependent

$$\frac{\mathrm{d}f_n}{\mathrm{d}t} = -\frac{i_n C_{\mathrm{col}}}{\rho} \tag{6.52}$$

where f_n is the thickness of the film at region n, C_{col} is the coulombic efficiency of the growth, and ρ is the resistivity of the material. By integrating f_n over the entire working space and over time, the final thickness of the film is obtained.

6.4.2 Optimising the plating parameters

Before investigating the effect of several parameters on the plating, a preliminary validation was performed to guarantee the accuracy of the results.

The electroplating processes with both low current and high current obtaining results were reproduced in good agreement with the experiments, see table 6.2. Moreover, the plating results in an uneven thickness distribution over the wafer and this was reproduced to a good precision as well.

With the model established, the impacts of a few parameters in the electroplating process including how the seed layer thickness helps to mitigate plating unevenness, how the intrinsic stress changes depending on the plating time were investigated. A technique to improve the surface uniformity, called the current thief, was developed.

The geometry of the model is shown in Fig. 6.10. The anode electrode is placed 20 mm away from the cathode. A sulphite based solution is used. Fig. 6.11 and 6.12 show the electrolyte potential, current density vectors and electric potential distribution on the working surface at $t = 6000$ s respectively with plating parameters assumed in table 6.3.

Using the high-precision model established, several parameters were investigated in opti-

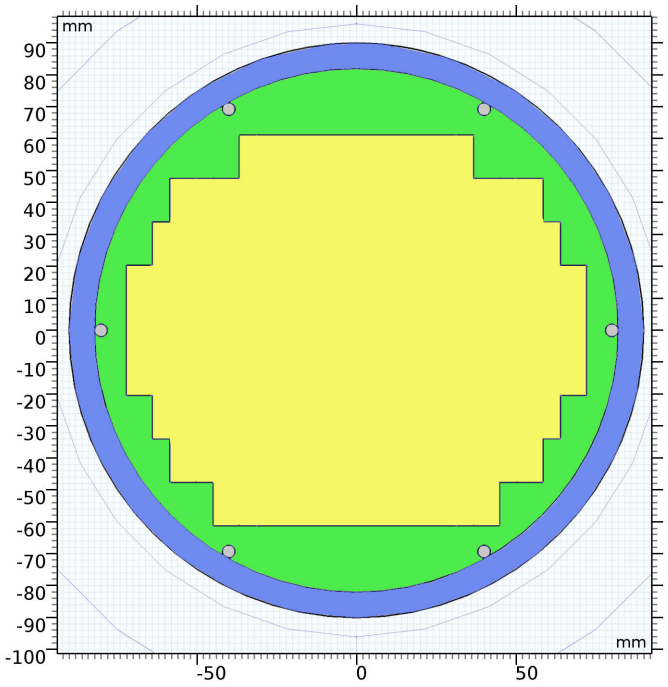

Figure 6.10: The dimensions of the substrate on a wafer mount. Yellow region represents the electrode surface to be electroplated, the details of the photoresist covered pattern is removed to simplify computation. Green area is covered with photoresist. Blue ring is an auxiliary electrode known as the current thief. Finally, the grey circles are ground pads which are mounted with copper pins and electrically contacting the seed layer to the source ground.

Table 6.3: List of parameters used in the simulation.

Name	Value	Description
Electrolyte conductivity	20 S/m	Sulphite based gold plating solution
Equilibrium potential	1.5 V	
Temperature	55 °C	
Electrode transfer coefficient	0.5	
Seed layer thickness	200 nm	Gold seed layer
Cell current	0.1 A	

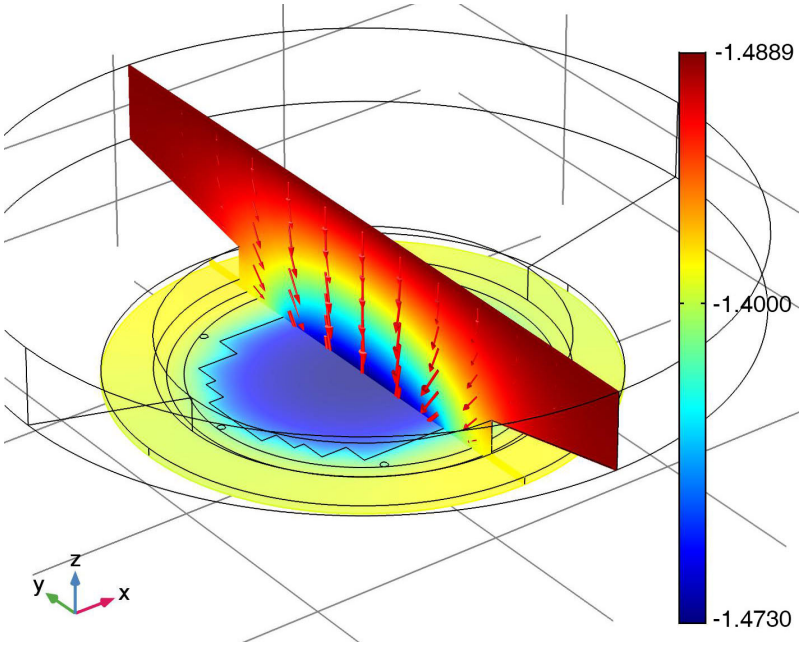

Figure 6.11: Electrolyte potential (V) near the working surface at $t = 6000$ s. The arrow volume represents relative magnitude and direction of current density vector. The potential is minus because it is relative to the ground pads.

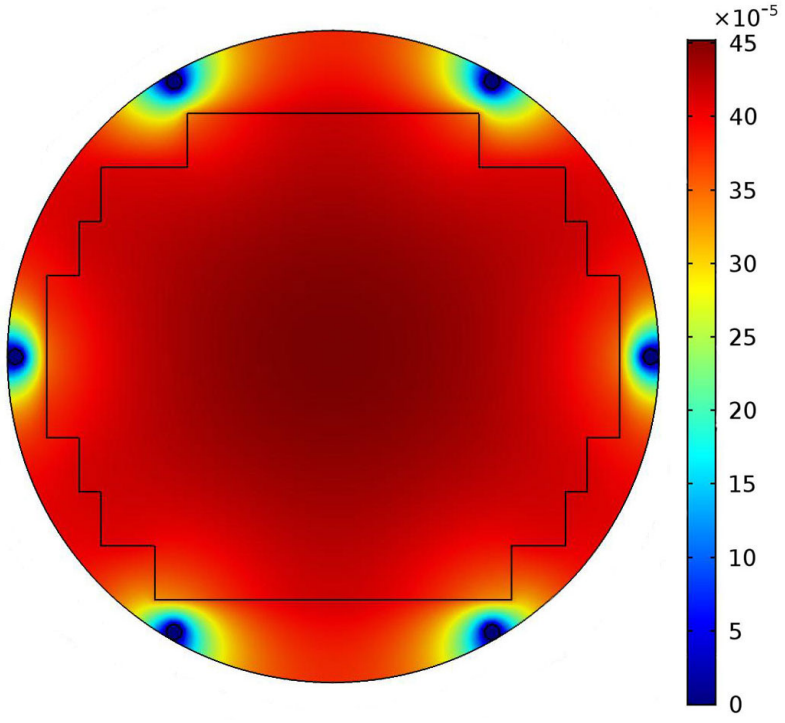

Figure 6.12: Electric potential distribution (V) on the working surface at $t = 6000$ s. The seed layer is well conducting producing only a small potential difference in the plating area.

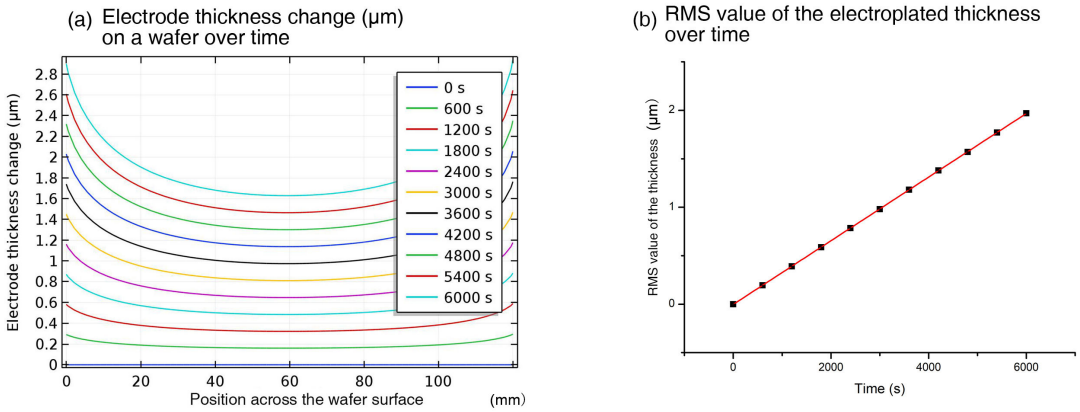

Figure 6.13: **(a)**The electrode thickness change (μm) on a wafer over time, **(b)** RMS value of the plated thickness over plating time. Position across the wafer refers to the distance from the leftmost point along the diameter parallel to the wafer edge which ranges from 0 to 150 mm in a 6 inch wafer.

mising plating quality. Unless stated, all other parameters are kept as in table 6.3. The first set of results is shown in Fig. 6.13(b) and are for the Root-Mean-Square (RMS) value of electroplated thickness (R_q) over plating time. The RMS value characterises the unevenness of the plated surface. R_q is linearly proportional to the plating time leading to an extreme surface profile (Fig. 6.13(a)) which suggests that such plating technique is restricted to a maximum plating thickness.

Poor surface roughness causes several impacts on the performance of the trap. For example, the RF field is attenuated due to a rough surface. Hammerstad's surface roughness model [132][4] describes the relationship between the attenuation due to metal conductivity α_m and R_q,

$$\alpha_m = \alpha_c(1 + \frac{2}{\pi}\tan^{-1}(1.4\frac{R_q^2}{\delta^2})) \tag{6.53}$$

where α_c is the attenuation constant due to conductor loss, and δ is the skin depth.

The change in attenuation against R_q/δ is plotted in Fig. 6.14. From this equation, when $R_q/\delta = 1.5$, the attenuation is 1.72 times of that in a perfectly flat surface. This is not a problem for the trapping RF which has a skin depth of 15-24 μm at a typical frequency range of 10-25 MHz. However, the 12.64 GHz microwave signal has a skin depth of ~ 2 μm which is vulnerable to a rough surface. To quantify the surface roughness of a single chip, the entire wafer is divided into chips of 12 mm × 12 mm. Along the diameter, there are 9 chips. Assuming that the plating time is 6000s, the RMS values of the 9 chips are plotted in Fig. 6.15(a). Using the results in Fig. 6.14, the attenuation ratio of each chip is

[4]Classic Hammerstad model breaks down in case of very rough surface when $R_q \gg 2$ μm.

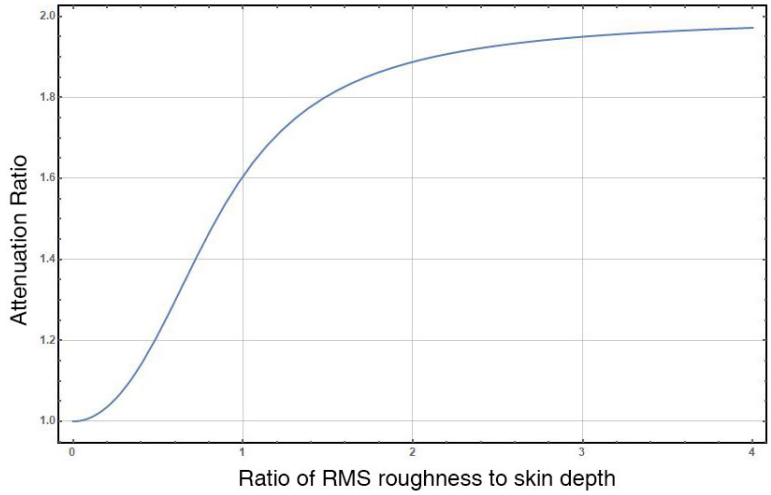

Figure 6.14: The ratio of α_m to α_c over the ratio of RMS surface roughness R_q to the skin depth δ of the plated metal. Produced from eq. 6.53.

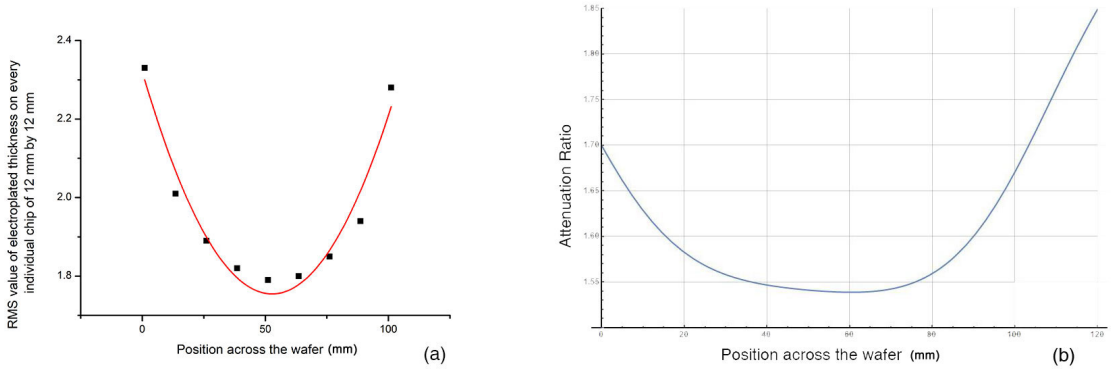

Figure 6.15: When the wafer is plated for 6000s, **(a)** shows the RMS values of the plated surface on single chips (12 mm $\times$ 12 mm) along the diameter parallel to the wafer edge, **(b)** shows the attenuation ratio of the chips versus their positions on the diameter.

plotted in Fig. 6.15(b). Chips at different positions on the wafer have different degrees of attenuation. This suggests that the central-most 5 chips have the best RF performance.

The last simulation experiment is an investigation into the impact of seed layer thickness on plating quality. Seed layer gold is often deposited with DC sputtering or thermal evaporation, however, both techniques are very expensive and time-consuming. It is desirable to have a thinner seed layer to save fabrication cost. Fig. 6.16 shows the electroplated thickness measured at both the centre and the edge of substrates with different seed layer thicknesses. The plating process is little affected by the seed layer thickness above 100 nm. The ratio of the plated thickness at the edge to the centre remains almost unchanged suggesting that there isn't a threshold that limits the current density near the substrate centre.

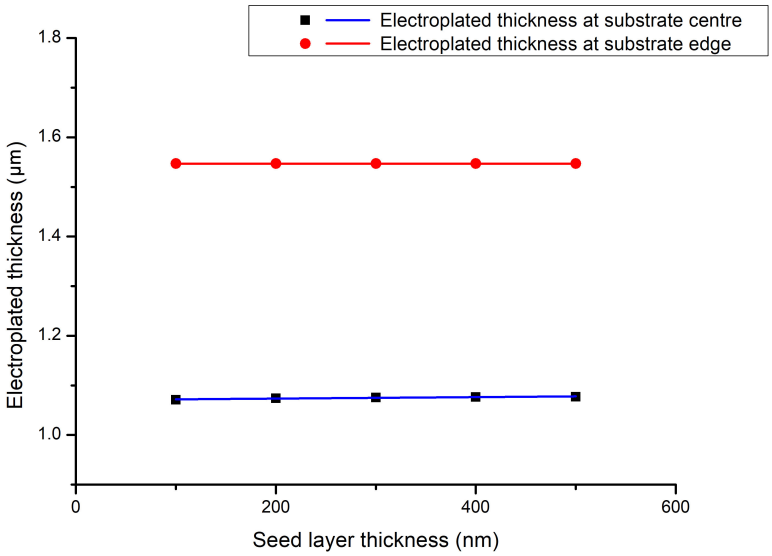

Figure 6.16: Electroplated thickness measured at both the centre and the edge of the substrate versus seed layer thickness.

Further to the studies above, a current thief plating technique was investigated. The current thief comprises a conductive ring surrounding the wafer placed very near the high current density area of the substrate so that a portion of the current is bypassed via the ring preventing from overplating hence improve the uniformity. The thief electrodes deliberate waste the deposited material hence must be carefully designed to balance the cost and the gain of uniformity. The effect of the current thief of different electrode widths is shown in Fig. 6.17 where the RMS value is compared in three different scenarios from no current thief, to with current thief of different sizes. The plated thicknesses at $t = 6000$ s in the three cases are 1.8, 1.35, 1.2 µm respectively. The current thief does help to improve the uniformity of the plated surface, however at a cost of a slower plating rate and a waste of plating material. The 8 mm current thief is a good compromise hence was used in the electroplating system.

Summary of the electroplating model

With this high-precision numerical model of electroplating, the electrochemical process of gold plating is studied with special focus on the electroplated thickness and surface uniformity over time. Surface roughness resulting from the plating process is unfavourable in microwave devices, in this study, the safe area that microwave devices can be placed on a mask is reported. The effect of seed layer thickness is studied and no significant change in the plated surfaces was observed when the thickness of the seed layer was increased from 100 nm to 500 nm. By employing a 100 nm seed layer rather than any thicker, the

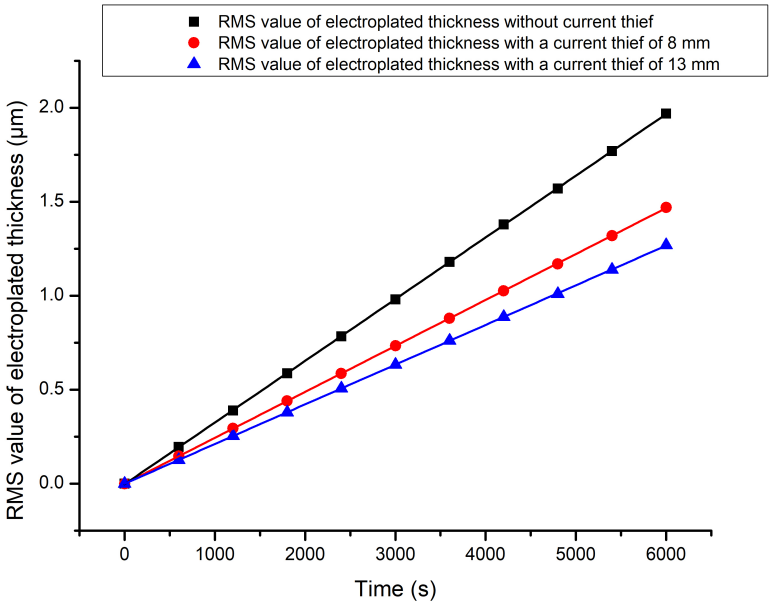

Figure 6.17: RMS value of electroplated thickness over time of three different scenarios: without current thief technique, with a current thief of 8 mm wide and with that of 13 mm.

fabrication expense and time are minimised.

A current thief technique was developed which improved the surface uniformity at a relatively mild cost of electroplating rate. The design was modelled and simulated with the FEM tool and several designs were compared.

Several interesting properties can be investigated further with this developed model such as the formation of intrinsic film stress and techniques to reduce excessive stress, optimising the components of the electroplating baths and designing optimised photomasks for minimum waste of deposited material, etc. So far, this model can only simulate the single component electrochemical environment, further work can be done to adapt this model to simulate a bi-component electrodeposition process such as Ni/Cu electroplating.

6.5 The electroplating experiments

6.5.1 Electroplating set-up

The electroplating set-up is consisted of serval parts as noted in Fig. 6.18. The tank[5] holds approximately 16 L plating solution[6] heated by a 700W PTFE rod heater[7]. The

[5] Yamamoto-MS A-52-ST6-P01A.
[6] ECF 64D.
[7] GALMAFORM U-FK 14070.

liquid is circulated and filtered by a pump[8]. A liquid level sensor[9] is installed to avoid overflowing. A paddle agitator[10] improves plating uniformity by agitating the solution near the wafer which is mounted on a home-built mount[11]. The design of the wafer mount with 'current thief' is detailed in section 6.4. A fine platinum mesh placed near the mount can potentially refine the grain size and accelerate plating but due to limited resources, no Pt mesh was used. The anode is a platinum-coated titanium plate[12]. To supply a high precision constant current, a PID laser diode control[13] was used which has an accuracy as low as 100 μA and a noise floor smaller than 1.5 μA. The required current resolution depends on the resistivity of the wafer. In this work, the substrate is prepared with a seed layer of 20 nm Cr, 50 nm Pt and 200 nm Au. The ECF 64D solution is prepared at mildly alkaline pH = 9.

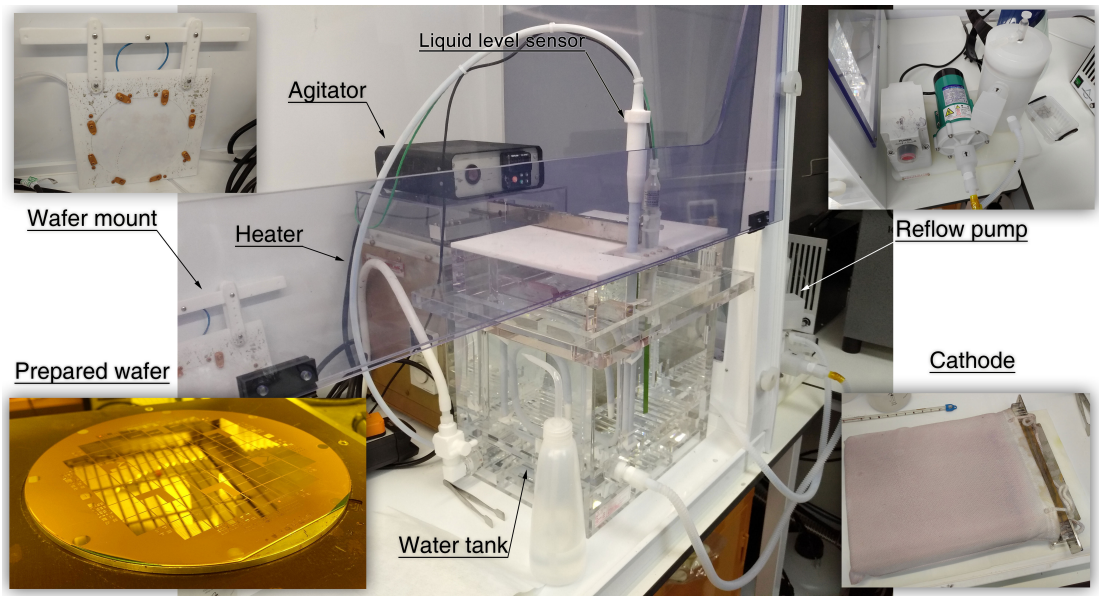

Figure 6.18: The electroplating kit and its components.

6.5.2 Development of a stable photoresist film for electroplating

Most Novolak-based positive photoresists are highly resistant to acids except in oxidising acids or concentrated hydrofluoric acid. However, a non-cross-linked positive photoresist gets dissolved in seconds in a developer which is alkaline. In this thesis, photoresist masks were coated on substrates and submerged in electroplating baths with pH value from 9

[8] Iwaki magnet pump MD-20RZM-220N .
[9] Yamamoto-MS A-60-L170.
[10] Yamamoto-MS A-52-ST6-P04W.
[11] Constructed by Dr Reuben Puddy.
[12] Yamamoto-MS A-52-ST6-P08-18.
[13] ITC502, Thorlabs.

Table 6.4: Chemical processes and chemical stability changes of AZ 9260 thin film photoresist with baking temperature.

Temperature/°C	Chemical process	Chemical stability
90-130	Remaining solvent evaporates	Increased
130-150	Inhibitor cracks thermally	Decreased
150-180	Resist thermally cross link	Increased

to 11. To improve the chemical stability of the resist mask, a hard baking recipe (A.5.3) was developed where, at an elevated temperature, the remaining solvents in the resist film vaporise and the polymer thermally cross-links. For the specific resist used, AZ 9260, the chemical processes in different temperature ranges are shown in table 6.4.

A good substrate adhesion of photoresist is required in both liftoff processes and electroplating processes using a photoresist mask. The adhesion of the resist to the substrate can be improved by processing of the resist and by using substrate preconditioning.

Adhesion promoters such as HMDS[14] or TI Prime are often used. HMDS is a Si-based adhesion promoter. When it comes in to contact with oxidised surfaces, the Si atom bonds to them. The methyl groups in HMDS form a hydrophobic surface thus improve resist adhesion. TI Prime is a Ti-based adhesion promoter, it bonds to oxidised surfaces likewise. They perform excellently on silicon, metal and glass surfaces. However, since gold does not oxide at room temperature, neither of them will work.

Resist adhesion can also be improved via hard baking. During hardbaking, the resist mechanically relaxes which suppresses peeling. However, a temperature beyond the softening point will deteriorate the resist profile.

The adhesion is best improved by adding an extra thin Ti or Cr layer. Ti, for example, bonds easily with oxygen in polymers and at the same time forms a strong metallic bond with Au atoms. This extra thin layer is ideal for low-temperature applications ($< 300°C$). However, titanium must be avoided if the subsequent process is electroplating. Titanium is highly reactive and often forms a passivation layer (titanium oxide) stopping metallic gold in the bath to form sufficient bonding on the electroplating seed layer[15]. Table 6.5 summaries the results of resist adhesion tests. On wafer ID 1-4, due to a poor adhesion or the presence of titanium oxide layers, resist peeled off from the surface shortly after being submerged in the electroplating bath. A further test involving wafer ID 5-8 confirmed that the minimum thickness of the Cr layer required is 1 nm.

[14] Hexamethyldisilazane.
[15] Seed layer refers to the thin metal layer used as the cathode on which plated metal grows.

Table 6.5: Results of the resist adhesion experiments with different seed layers. All wafers are using the 4.7 µm AZ 9260 photoresist (recipe A.5.1). TI Prime were applied using the recipe in appendix A.5.2.

Wafer ID	Seed layer	Result
1	Au 200nm only	Resist peeled off
2	Au 200nm, TI Prime	Resist peeled off
3	Au 200nm, Ti 5nm	Resist peeled off
4	Au 200nm, Ti 1nm	Resist peeled off
5	Au 200nm, Cr 5nm	Resist persisted
6	Au 200nm, Cr 7nm	Resist persisted
7	Au 200nm, Cr 5nm and TI Prime	Resist persisted
8	Au 200nm, Cr 1nm	Resist persisted

In a conclusion, the adhesion of photoresists to gold surfaces can be significantly improved by coating a 5 nm Cr or Ti layer. When electroplating is required in the subsequent steps, the Cr layer is preferred.

6.5.3 Electroplated surfaces

3 HR silicon and 3 sapphire wafers were prepared using the photoresist described previously. The seed layer was 200 nm Au, 20 nm Pt and 20 nm Cr as discussed in section 5.5.3. The seed layer has a surface roughness of 2.31 nm[16]. Several experiments were made at different plating current and time. The plating experiments were summarised in table 6.6 and compared with a wafer electroplated by Dr Wei Wu from the National University of Defence Technology (NUDT) in Changsha, China. A smaller current is helping the surface to be smoother because of a smaller grain size formed. The NUDT wafer is a 4 inch, 0.46 mm thick BF33 glass substrate[17]. NUDT was unable to disclose further information on their process parameters including the current, start voltage and seed layer structures. The optical images of three different surfaces were compared in Fig. 6.19.

6.6 Low loss trap experiment

Wafer S4 is a bare sapphire wafer[18] with 4 µm plated gold electrode layer using a modified 'grow in pattern' process. In the modified 'grow in pattern' process, an additional inversed mask was used to pattern the photoresist prior to the dry etch. This photoresist, only

[16] All surface roughness measurements in this section were made by Dr Wei Wu in Changsha using Atomic Force Microscope (AFM). Calculated using open-source software Gwyddion. If not specified, 'surface roughness' refers to the RMS roughness S_q.

[17] BOROFLOAT 33 glass, a type of borosilicate float glass.

[18] R-plane sapphire wafer supplied by Precision Micro-Optics.

Table 6.6: Results of the electroplating experiments. Wafer with ID 'NUDT' is a wafer fabricated and electroplated by Dr Wei Wu from NUDT, Changsha. The roughness is the average of the RMS roughness S_q at 9 points on a single wafer. Wafer ID S1, S2 and S3 are HR silicon substrates with 200 nm silicon nitride. S4, S5, S6 are bare sapphire substrates. 'N/M' stands for 'not measured'.

ID	Current (mA)	Start voltage (V)	Time	Current thief equipped?	Thickness (μm)	Roughness (nm)
NUDT	-	-	-	No	3	101.227
S1	200	3.24	12 mins	No	1.2	>200
S2	170	1.53	30.6 mins	Yes	3.5	187.778
S3	36.2	0.864	2 hrs	Yes	3.2	40.853
S4	21	1.60	4 hrs	No	4	40.141
S5	32.6	0.88	2 hrs	Yes	3.5	N/M
S6	150	1.42	34.7 mins	Yes	3.2	N/M

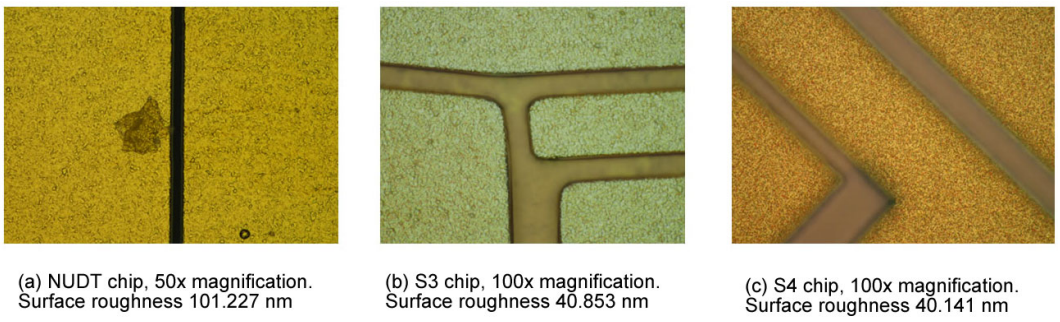

Figure 6.19: The optical images of gold surfaces using different plating recipes. The surface roughness was measured using AFM by Dr Wei Wu at National Defence University of Technology in Changsha, China. The difference in the colour of the gold layers is due to the setup of the optical microscopes.

sitting on the top of the electrodes, protects the electrode surface from being etched. A chip from the NUDT wafer and a chip from wafer S4 were bonded up and tested in the cryogenic system [75]. The geometry and trapping parameters were previously reported in [152]. The chip picked from wafer S4 is a 100 μm linear trap chip with its sapphire substrate. Both traps were bonded on the same copper mount, resonator and chip carrier set. The compact resonator features a superconducting-wire-winded autotransformer which was characterised using a dummy load in section 2.5.4. The critical temperature of the resonating circuit with a dummy load was 7 K. The traps were loaded into the vacuum chamber and cooled down to cryogenic temperatures. The Q factor was recorded as the system temperature goes down to 30 K where the RF generator is switched on to find the resonance. The resonance of the traps were found at 24.35 MHz and 28.46 MHz. The power output on the RF generator was set to −20 dBm as the temperature continues to drop to 14 K. After the RF amplifier[19], the input power into the system is about 0.2 W. The Q factor vs temperature plot is shown in Fig. 6.20. The Q factor of the (S4) sapphire chip with smooth gold surface is almost twice as much as that of the NUDT chip. Moreover, at 14 K, the Q factor of S4 suddenly increased as the resonator went superconducting. However, the NUDT chip did not behave alike which indicates that the circuit was yet not below its critical temperature. This might be attributed to the extra heat dissipated by the NUDT chip.

A lower Q factor allows the S4 chip to operate at a higher voltage at the same input power level. Due to dissipating less heat, the S4 chip can operate at a lower temperature. This reduces the risk of a breakdown due to thermally activated electron release. A colder surface produces a smaller Johnson noise. This may mean that the motional heating of the ion is less but recent study [47] suggests that the surface roughness is the dominant factor.

The scalable quantum computer requires numerous amount of auxiliary electronics to be placed inside the vacuum systems for the minimised noise due to vacuum feed couplings. The integration of these electronics and the CCW structures posts a challenge in developing a low loss ion trap on a silicon substrate rather than a sapphire substrate. This allows the electronics be fabricated on the monolithic ion trap unit chip using the state-of-art commercially available fabrication workflows. As highlighted in Fig. 6.1, this requires the silicon substrate be extremely resistive. Combined with the other techniques developed in this chapter, the silicon low loss chip will be yet another step forward to the practical

[19] Mini Circuits LZY-22+. Gain at 20-30 MHz is typically 44.5 dB.

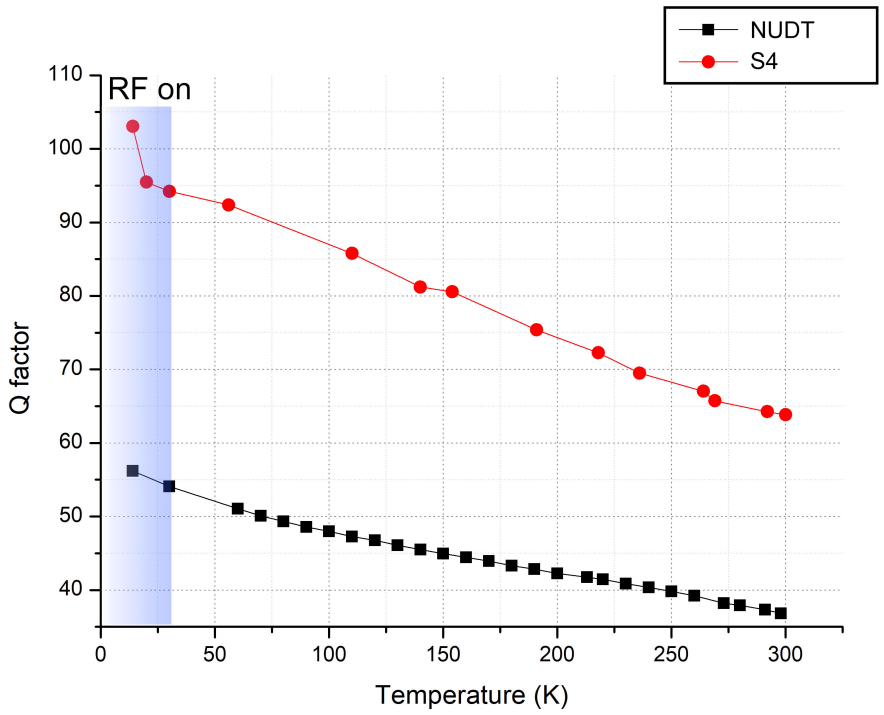

Figure 6.20: Q factor of two ion traps at different temperatures. ■ stands for the NUDT trap. The centre frequency at 14 K is 24.35 MHz. ● stands for the S4 trap. The centre frequency at 14 K is 28.46 MHz. The blue shaded area indicates that the RF generator is switched on.

scalable quantum computer.

6.7 Conclusion

This chapter described the experimental works on reducing the RF loss in traps by developing the smooth electroplating technique and the use of a sapphire substrate. The discussion in this chapter showed that the RF loss limits the performance of the MEMS ion traps and can be minimised by improving the fabrication processes and matching the impedance. This work pointed out that for ion trap applications, the resistivity of the silicon substrates need to be > 100 kΩcm. The smooth electroplating technique was developed to achieve a minimal RMS surface roughness of only 40.1 nm. The low-loss ion trap produced has a Q factor twice as much as the conventional trap has using the optimised trap and the superconducting resonator. Recommendations for future research include the development of a low loss silicon based ion trap for a fully integrate scalable quantum computer unit.

Chapter 7

Investigation on the anomalous glow discharge

Electrical breakdown is the most common failure mode in MEMS devices. In Chapter 5, the electrical breakdown in microfabricated ion trap devices is reviewed and an improved breakdown voltage with optimised PECVD silicon nitride film is reported. In this chapter, an anomalous phenomenon known as 'glow discharge' is reported. During experiments, glow discharges were observed. The glow discharge prevented trapping and caused damage to the chip. Several experiments were conducted to investigate its nature.

7.1 Anomalous glow discharge phenomenon

An experimental observation of a glow discharge failure mode in ion trap operation is reported. This was not reported by the ion trap community before. The chips, under normal operating conditions, emit photons of various wavelengths and are unable to trap ions. It is found that the intensity of the photon emission is dependent on the applied RF trapping voltage. A series of experiments were designed and conducted to investigate the nature of this phenomenon.

The glowing chips were made on 6 inch HR silicon substrate with 3.7 µm gold electrode as shown in Fig. 7.1. The gold was plated using 'Grow in pattern' method shown in Fig. 6.9(c), the exposed seed layer was removed by ICP Cl_2 etch (A.3.2). Before the Cl_2 metal etch, a chamber conditioning process (A.3.1) cleans the chamber and passivates the ceramic chamber wall.

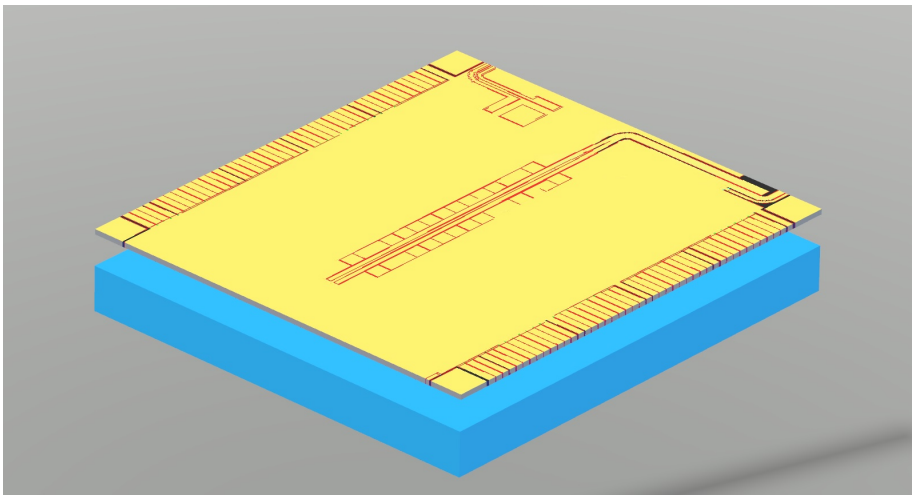

Figure 7.1: (Image not to scale) Layer structure of the test chips.

Table 7.1: The initial glow voltages and significant glow voltages.

Chip ID	Initial glow voltage (Vpp)	Significant glow voltage (Vpp)
1A	90	250
1B	106	300
1C	125	225
1D	125	320
1E	250	300
1F	250	320

7.2 Voltage dependency

All chips that were reported to have glow discharge issues were fabricated in the Southampton Nanofabrication Centre using the fabrication flow described in section 5.5.3 with a chloride-based dry etch process. Before trapping, a portion of the chips from the batch was tested for breakdowns. The breakdown voltages were above 550 Vpp . The chips were loaded into various vacuum systems for trapping, however, high intensity of photon emission was observed on the CCD cameras when RF trapping voltages were raised above a threshold voltage.

It was observed that the intensity of the glow was typically proportional to the voltage of the RF signal applied, as shown in Fig. 7.2. To quantify the glow intensity, the minimum voltage at which the photon counts on CCD at a fixed exposure time of 400 ms is above 1000 is 'initial glow voltage'. The minimum voltage at which the photon counts is above 5000 is called 'significant glow voltage'. Table 7.1 shows the initial glow voltages and significant glow voltages of 6 chips. It was observed that when the chip was new, the initial glow voltage was higher than that measured later, as summarised in table 7.2.

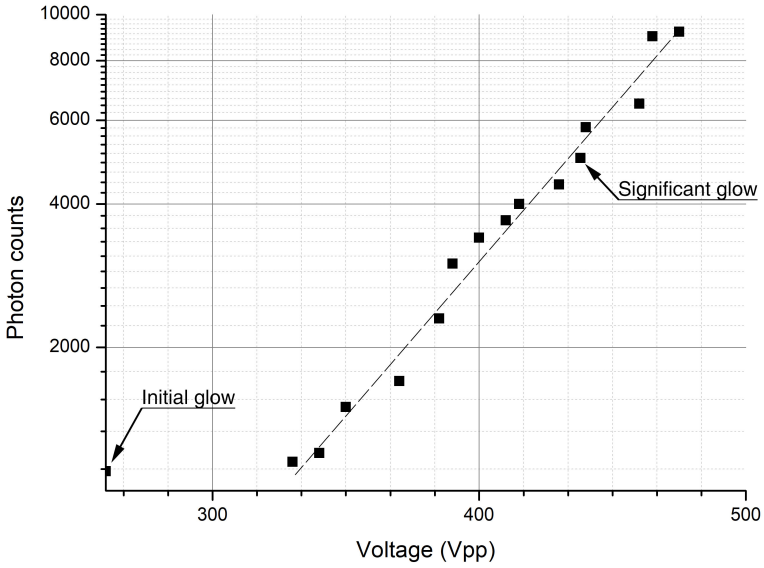

Figure 7.2: Plot of voltages versus photon counts. The initial glow voltage is 106.8 Vpp . The significant glow voltage is 438 Vpp .

Table 7.2: Initial glow voltages when the chip was new and when it was used.

Chip ID	When new (Vpp)	When used (Vpp)
2A	450	300
2B	238	182
2C	350	140

It was also found that the pressure in the vacuum chamber is almost linearly proportional to the voltage applied to the chip as shown in Fig. 7.3. The voltage was raised by about 2 Vpp at a step size of 3 min. To maintain a pressure $< 3 \times 10^{-9}$ mBar, a 30 min pumping down process was added before going to 106 Vpp . The gradient of the pressure rise with voltage is larger after the 30 min pumping. The evidence suggest that this is because the chip is hotter with a long period of operation, hence releasing more particles giving rise to the gradient. A reference experiment was performed where the chip was left at 100 Vpp overnight. The pressure recorded remains at $2.5 \pm 0.3 \times 10^{-9}$ mBar. However, it is unsure if the pressure is related to the applied voltage or the time of applying RF voltages.

7.3 Three-band spectrum analysis

To find out the nature of the glow, the optical spectrum of the photon emission was studied using the trap imaging CCD with sets of optical filters. The filters used were the

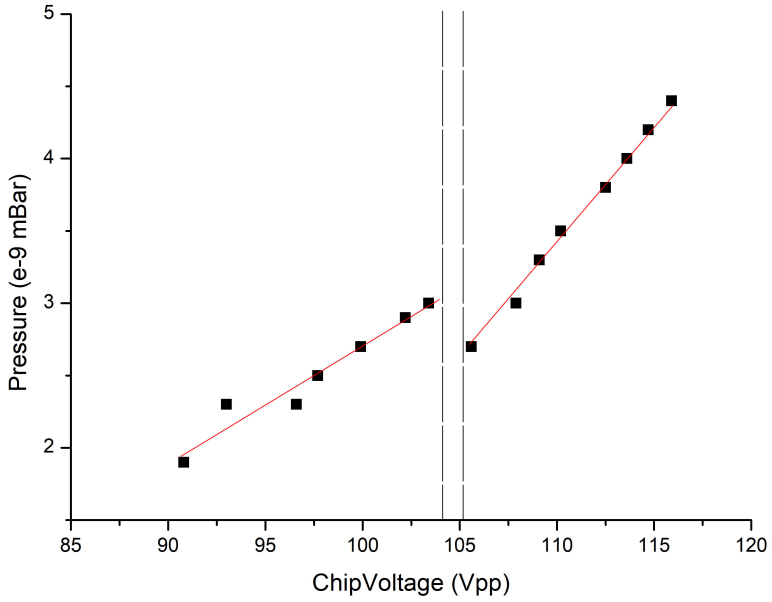

Figure 7.3: Plot of voltages versus chamber pressure. The break near 105 Vpp stands for a 30 min pumping down process to maintain low pressure in the chamber before applying higher voltages.

UV filter[1] and the dichroic mirror[2]. With no filter in the path, a full band where the CCD shows photons of all wavelengths is acquired. With the UV filter alone, we have the UV band where only 365-375 nm photons can pass. When using the dichroic mirror alone, only photons with wavelengths longer than 550 nm can pass. By subtracting the image obtained with the UV filter and the dichroic mirror from the full spectrum image, a third band is obtained. This method is known as 'three-band spectroscopy'.

Fig. 7.4 shows CCD images of glows at various RF voltages applied and its wavelengths measured using three-band spectroscopy techniques. A strong correlation between high voltages and strong UV glow was found. The UV glow does not share the same position with the glow at other wavelengths indicating that there is more than one source of the glow.

Different atoms contribute to photons of different wavelengths. It is necessary to list the possible contaminants from the process of fabrication, cleaning, wirebonding and operating. This include the electrode and dielectric material Si, Au and Cr, the process gas elements F (from CF_4), O (from O_2), Cl (from Cl_2), S (from sulphite based electroplating bath), H (from Si−H bonds in the PECVD films) and N (from SiN_x).

[1] 370/10 nm single-band bandpass filter, part number: FF01-370/10-25 by Semrock.
[2] Longpass dichroic mirror/beamsplitter with 550 nm cutoff wavelength. Part number: DMLP550 by Thorlabs.

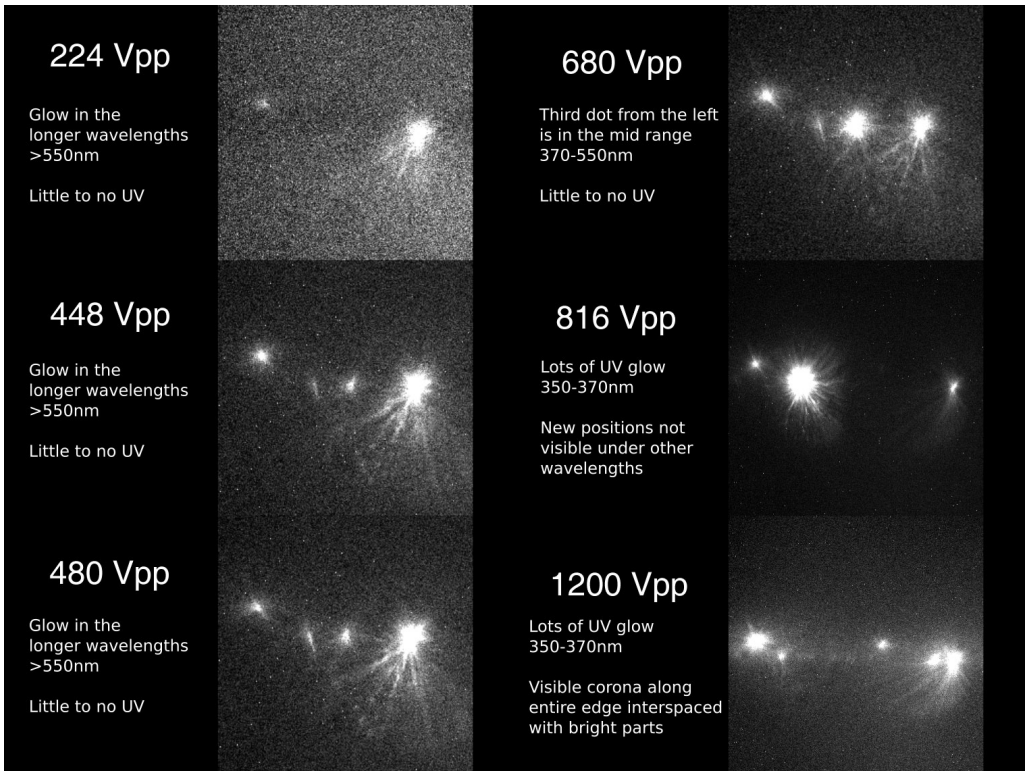

Figure 7.4: CCD images of glows with respect to applied RF voltages and its wavelengths using three band spectroscopy technique. The images were taken by Anton Grounds.

Base on the data from NIST Atomic Spectra Database [153], Fig. 7.5 shows the relative intensities of the elements in the UV band. Chlorine, ytterbium, argon and hydrogen have a significantly higher intensity. Chlorine as a reaction gas was introduced during dry etch processes. Chlorine and fluorine are well-known as sources of the contaminant in nanofabrication industry [154]. The main reaction products, $AuCl_3$ and AuCl, have low vapour pressures below 200°C. Due to the non-volatility, the reaction products attach to the surfaces of the electrodes forming a veil which is hard to remove. In the presence of plasma or high temperature, the products diffuses [155] into the electrodes forming firmer bonds. The residuals of the gold etch process is resistant to the subsequent wet chemical cleaning process.

Ytterbium is deposited on the chip surface from the atomic oven during trapping. The collisions of thermally ionised ytterbium atoms with the background gas are inelastic, either populating the $^{171}Yb^+$ ion in the metastable $F_{7/2}$ state or forming a YbH^+ molecule and get absorbed on the chip surface [11]. The 355 nm Raman laser quickly returns the ions to their atomic ground-state manifold.

Argon was used in essentially every single plasma process and due to its heavy atomic weight, under the acceleration of a strong field, it can be implanted into substrates and

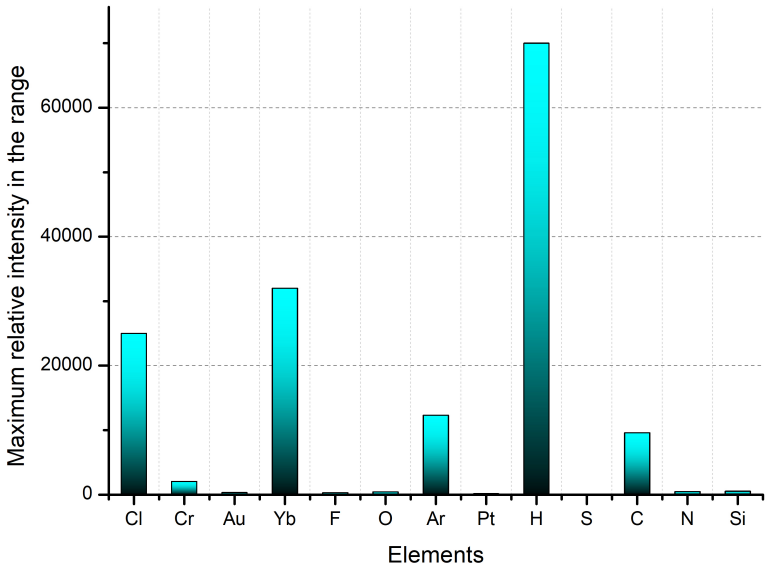

Figure 7.5: Relative intensities of selected elements in the UV glow band. Data from NIST Atomic Spectra Database [153].

dielectric films. Hydrogen atoms exist in the form of Si−H as explained in section 5.3. In the presence of a high external electric field, H atoms can be released from the film [156].

From the discussion above, the evidence suggest that argon and hydrogen are not the sources of the glow, leaving only chloride and ytterbium in question.

7.4 Dry etched and wet etched samples

To verify the hypothesis that chlorine atoms, induced from the dry etch process, is the source of the glow, two batches of samples were prepared. The layer structure of the samples is shown in Fig. 7.6(c). The first batch of samples was wet etched using recipe A.4.1. The second batch of samples was dry etched using recipe A.3.2. All of the chips were tested using the cryogenic system for a higher maximum voltage.

The experimental results were summarised in table 7.3. At 270 Vpp , the glow started with a non-sustaining flash in the dry etched chip and several flashes followed between 270 and 330 Vpp . Nothing was observed in the wet etched chip in this range. The glow flashing continued on the dry etched chip up to 330 Vpp where the resonance suddenly changed. At 476 Vpp , the dry etched chip glows consistently while the wet etched chip does not glow. The wet etched chip was left for 72 hours at this voltage and no glow was observed. Microscope images (Fig. 7.6(a) and (b)) showed that the electrodes were damaged in both samples but no redeposition in the gaps was observed.

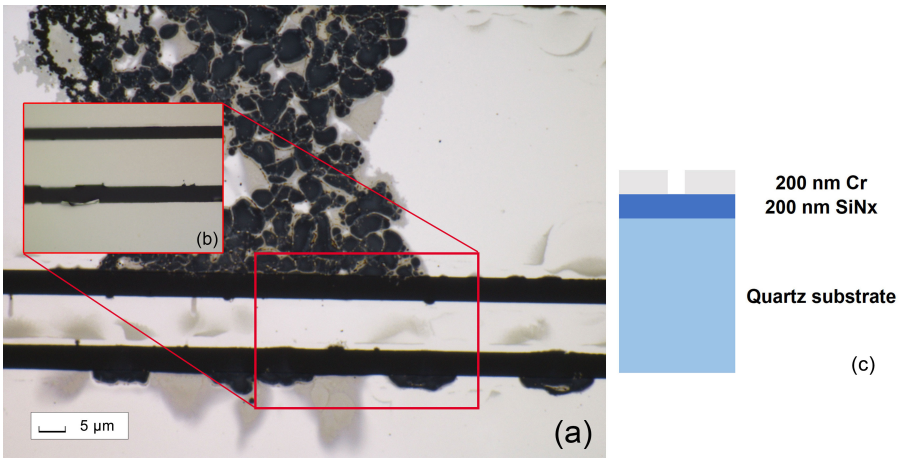

Figure 7.6: Microscope images of the dry etched chip before and after the glow test. **(a)** after the test, the electrode edges were damaged. The black area indicates a poor adhesion of the metal layer to the substrate. **(b)** before the test. **(c)** (Image not to scale) Layer structure of the dry etched and wet etched samples.

Table 7.3: Glow test results of the dry etched and wet etched chips.

Voltage (Vpp)	Wet etched sample	Dry etched sample
270	-	First weak glow observed
330	-	Resonance was altered, glow
476	-	Glow consistently

The differences between Cr and Au as electrode material explains the results. Cr has a native thin oxide layer which improves the breakdown voltage [157]. Cr is very tough compared to Au which is very ductile and malleable. When the glow happens a hot plasma is formed for a very brief period in time, this plasma is close to the metal surface and within the trenches. With Au being so soft the plasma eruption throws the Au outward from the plasma focal point, this then narrows the gaps and allows a constant flow of electrons which forms the glow discharge observed. With Cr, the metal surface is much tougher so the relative damage caused is lower. This evidence suggests that the initial plasma flash was started but the glow did not sustain. When enough power is supplied to damage the Cr then the same effect is seen as with the Au.

The results of the wet etched and dry etched samples is the direct support of the hypothesis that the the UV photon emission observed was due to chloride contaminant in the dry etch process due to the high-energy chlorine plasma. An alternative method to identify elements is Energy Dispersive X-ray (EDX) analysis. Due to limited resources, no EDX analysis was conducted.

Table 7.4: Initial glow voltage and significant glow voltage of chips with and without chemical cleaning. 'N/A' stands for no data because the chip breakdown before reaching a significant glow voltage.

Initial glow voltage (Vpp)		Significant glow voltage (Vpp)	
Without cleaning	With cleaning	Without cleaning	With cleaning
90	250	250	320
125	225	250	300
106	300	N/A	250
125	320	N/A	300

7.5 Cleaning the samples

Dry etch residue removal is a common problem for semiconductor manufacturing, MEMS device fabrication and IC packaging industry. Efforts were made to remove the dry etch residue by using industry-standard wet clean chemicals, thermal annealing processes and specialised dry etch process.

7.5.1 Wet chemical clean

Gold and other metals were used as bondpads in the production of memory, MEMS sensors and other electronics. Removing the dry etch residue is critical in improving the yield rate and elongating the device lifetime. Samsung, Micron and other manufacturers have been using wet chemistry for decades. A recent thesis [158] reported the industry-standard cleaning methods using specialised chemicals including REZI-38 and EKC 6800. The thesis [158] described the challenges in the fabrication of dynamic random-access memory where fluorine contamination were found after a dry etch process reducing the reliability of the memory. The author describes the halogen contamination as an unsolved challenge in the nanofabrication industry.

In Southampton Nanofabrication Centre, recipes were developed using REZI-38 and EKC 6800 to remove the residue after etch. A batch of 8 chips was prepared where 4 of them were chemically cleaned with REZI-38 and the other 4 cleaned with DI water. They were tested for the glow. The results are summarised in table 7.4. The chemical cleaning improved both the initial glow voltage and significant glow voltage but did not remove the glow completely.

The same test was performed using EKC 6800 and REZI-38 mixed with H_2O_2. No significant improvement was found in the EKC 6800 cleaned chips. Some electrodes delaminated

Table 7.5: Results of the thermal anneal processes. '+' and '++' in gold bubble column indicates possibly thermally-induced bubble due to film stress. '++' suggests a worse surface compared to '+'. The REZI-38 chips were heated to 50°C. Chips that were not rinsed in REZI-38 were submerged in DI water at room temperature for 10 mins.

Batch	Chip ID	Gold bubbles	REZI-38	H_2O_2	time	Glow?
400°, 15s	1	++	60mL	No	10min	Yes
	2	++	60mL	No	10min	Yes
	3	+	50mL	10mL	10min	Yes
	4	++	50mL	10mL	10min	Yes
	5	+	30mL	1.5mL	5min	Yes
	6	+	30mL	1.5mL	5min	Yes
	7	No	No	No	10min	Yes
300°, 30s	8	+	No	No	10min	Yes
	9	++	No	No	10min	Yes
	10	+	60mL	No	10min	Yes
	11	++	50mL	10mL	10min	Yes
	12	++	30mL	1.5mL	5min	Yes
	13	++	60mL	No	10min	Yes
	14	No	60mL	No	10min	Yes
	15	No	60mL	No	10min	Yes
	16	+	No	No	10min	Yes
300°, 15s	17	No	60mL	No	10min	Yes
	18	No	50mL	10mL	10min	Yes
	19	No	30mL	1.5mL	5min	Yes
	20	No	60mL	No	10min	Yes

from the REZI-38, H_2O_2 mixture cleaned chips due to its aggressive etch.

7.5.2 Thermal anneal

Rapid thermal anneal processes are used in semiconductor device fabrication to alter the electrical properties. Specialised treatments are designed for densifying thin films, repairing damage from ion implantation and reflowing the electrode surfaces. 29 chips were prepared and thermally annealed using three different recipes. The recipes were 15s at 300°C, 30s at 300°C and 15s at 400°C. All processes were performed in N_2 environment at 1 atm pressure. Bubbles were found on the gold electrode surface of some of the chips. This is likely due to the thermally induced stress during the process. Part of the thermally annealed chips was treated using REZI-38 wet clean. Some REZI-38 liquid were enhanced with H_2O_2 for an improved etch ability. The chips were tested for glow, the results are summarised in table 7.5.

The table suggests that the anneal processes were unable to remove the residue that caused

glow. The 300°C, 30s and 400°C, 15s processes damaged the electrode surfaces.

7.6 Recommended process in deep metal etching

As demonstrated, it is extremely difficult to remove etch residue after the dry etch process. To avoid chlorine contamination, some alternative processes were proposed.

Number one is Ion Beam Etching (IBE) process. This process uses purely the bombardment of inert atoms like argon to remove atomic layers. The process was developed in Oxford Instruments Ionfab 300 Plus system. Due to the high aspect ratio, a gentle wet gold etch (recipe A.4.1) is necessary to remove the sputtered gold particles after the IBE etch. IBE-etched chips were tested and they showed no glow.

The IBE process is only useful to remove a thin layer of seed metal, not suitable for removing thick metal layers. In addition, because the gold electrode surfaces were etched, the electrode surfaces become rougher. This is not ideal according to the discussion in section 3.2. Hoping that thermal reflow will improve the surface roughness after IBE etch, 3 IBE etched gold chips were thermally annealed using the 300°C, 15s recipe. The surface roughness increased from 91 nm and 105 nm to 243 nm and 241 nm respectively.

Another novel method to remove the chlorine contamination was inspired from a patent [159] where high-temperature ammonia gas was used in halogen removal. It may be possible to use hot ammonia plasma to remove the chlorine contamination. However, due to limited time and resources, no conclusive result was produced.

7.7 Conclusion

This chapter described the experimental works on investigating the anomalous glow discharge effect observed. The results and analysis reported in this experiment supported the hypothesis that the glow discharge was partially caused by the chlorine contamination induced in the dry etch process. The effort in removing the contamination was reported with no effective methods found. The recommended alternative process was described. These efforts were valuable to the MEMS community in analysing the contamination source, targeting process fault and optimising the processes. Recommendations for future research include the continued investigation of the glow discharge at different wavelengths to ultimately model the glow discharge and in-vacuum breakdowns in microscopic gaps.

Chapter 8

Conclusion and outlook

This thesis contributes towards the microfabrication of a scalable ion trap quantum computer using microwave radiation driven quantum gates by developing the key elements required for the scalable quantum computer units and improving the performance of the ion traps through optimised fabrication processes.

A novel dynamic simulation tool was introduced addressing the problem currently faced by the ion trap designers. This numerical model was used to design three key elements in a microwave-driven scalable quantum computer: the junction trap to shuttle ions, the CCW structures to generate the high gradient magnetic field and the microwave delivery system. A very low RF barrier X junction trap was obtained allowing ions to be shuttled across a junction without gaining excessive motional quanta. The physical size of the CCW structures are discussed and the maximum current is predicted. The fabrication of the CCW structure was developed, featuring the optimised Bosch process for silicon etch. A general review of microwave delivery system was given including horn, patch antenna, imaging tube, anti-parallel wires and integrated cavity. Discussions were given on the pros and cons of each scheme. An innovative integrated microwave cavity was reported where the Rabi frequency of a single qubit gate is 45 times faster compared to a conventional permanent magnet setup. Other features designed simulated including the viewport mesh and the microwall to minimise oven coating and prolong the service life of a trap

The breakdown is an important topic in achieving reliable trapping. Using the tool developed, a simulation investigation was reported suggesting that the failure of a ring trap is likely due to the breakdown of a VIA structure. This inspires a novel high strength 'sandwich' dielectric structure. The PECVD processes were optimised for maximised density.

The 'sandwich' structure has a minimised residual stress and in theory, can be deposited to high thickness. In addition, for ion traps with bare oxide substrates, silicon deep etch was developed. The experiments showed that the films using the improved processes were able to withstand nearly twice as higher voltage. The 'sandwich' dielectric layer ion trap reported that it successfully trapped ions at cryogenic temperatures without breakdown.

The RF loss in ion traps is discussed. Calculation shows that for ion trap applications, the resistivity of silicon substrates have to be more than 100 kΩcm. To aid reducing RF loss, smooth electroplating techniques were developed reporting a surface smoothness $S_q = 40.1$ nm. The Q factor of this trap, compared to a trap built by the collaborator's, is 2 times as high at 14 K.

Lastly, this thesis reports an anomalous glow discharge phenomenon. The voltage dependency and the spectrum of the glow were studied. Experiments were designed and conducted to investigate the nature of the glow using different fabrication techniques. The evidence suggests the glow at UV range was partially caused by the residual chlorine from the dry etch process. Efforts were made to chemically remove the residue but no effective method was found.

Future Work

Future work is to be done on implementing the genetic algorithm to allow a fully automated optimisation using the numerical tools presented in this thesis. The development of a low loss silicon trap with integrated electronics is recommended basing on the progress reported in this work. Further investigation of the nature and sources of non-UV glow discharge will help understanding plasma physics in micro-gaps under high vacuum environment. The IQT group will trap on the fabricated chips and demonstrate shuttling through the X junction and quantum gates using the structure proposed in this work.

Bibliography

[1] G. E. Moore. Cramming more components onto integrated circuits. *IEEE Solid-State Circuits Society Newsletter*, volume 86(1):82–85, 1998. 1

[2] P. W. Shor. Algorithms for quantum computation: Discrete logarithms and factoring. In *Proceedings of the 35th Annual Symposium on Foundations of Computer Science*, pp. 124–134. IEEE Computer Society, 1994. ISBN 0-8186-6580-7. 1

[3] L. K. Grover. A fast quantum mechanical algorithm for database search. In *STOC Proceedings of the 28th Annual ACM Symposium on Theory of Computing*, pp. 212–219. ACM, 1996. 1

[4] R. J. Clark, T. Lin, K. R. Brown, and I. Chuang. A two-dimensional lattice ion trap for quantum simulation. *Journal of Applied Physics*, volume 105(1):013114–013114–8, 2009. doi:10.1063/1.3056227. 1

[5] K. Kim, M.-S. Chang, S. Korenblit, R. Islam, E. E. Edwards, J. K. Freericks, G.-D. Lin, L.-M. Duan, and C. Monroe. Quantum simulation of frustrated Ising spins with trapped ions. *Nature*, volume 465:590–593, 2010. 1

[6] A. Friedenauer, H. Schmitz, J. T. Glueckert, D. Porras, and T. Schaetz. Simulating a quantum magnet with trapped ions. *Nature Physics*, volume 4:757 to 761, 2008. doi:10.1038/nphys1032. 1

[7] A. M. Turing. On computable numbers, with an application to the Entscheidungs problem. In *Proceedings of the London Mathematical Society*, volume 42 of *2*, pp. 230–265. 1937. doi:10.1112/plms/s2-42.1.230. 1

[8] D. Deutsch. Quantum theory, the Church-Turing principle and the universal quantum computer. In *Proceedings of the Royal Society of London A*, volume 400, pp. 97–117. 1985. doi:10.1098/rspa.1985.0070. 1

[9] M. Johanning, A. F. Varón, and C. Wunderlich. Quantum simulations with cold trapped ions. *Journal of Physics B*, volume 42(15):154009, 2009. 1

[10] J. W. Britton, B. C. Sawyer, A. C. Keith, C. J. Wang, J. K. Freericks, H. Uys, M. J. Biercuk, and J. J. Bollinger. Engineered two-dimensional Ising interactions in a trapped-ion quantum simulator with hundreds of spins. *Nature*, volume 484:489–492, 2012. doi:10.1038/nature10981. 1

[11] J. Zhang, G. Pagano, P. W. Hess, A. Kyprianidis, P. Becker, H. Kaplan, A. V. Gorshkov,

Z. Gong, and C. Monroe. Observation of a many-body dynamical phase transition with a 53-qubit quantum simulator. *Nature*, volume 551(7682):601, 2017. 1, 146

[12] R. Schützhold, M. Uhlmann, L. Petersen, H. Schmitz, A. Friedenauer, and T. Schätz. Analogue of cosmological particle creation in an ion trap. *Physical Review Letters*, volume 99:201301, 2007. doi:10.1103/PhysRevLett.99.201301. 1

[13] L. Lamata, J. León, T. Schätz, and E. Solano. Dirac equation and quantum relativistic effects in a single trapped ion. *Physical Review Letters*, volume 98:253005, 2007. doi:10.1103/PhysRevLett.98.253005. 1

[14] B. Horstmann, B. Reznik, S. Fagnocchi, and J. I. Cirac. Hawking radiation from an acoustic black hole on an ion ring. *Physical Review Letters*, volume 104:250403, 2010. doi:10.1103/PhysRevLett.104.250403. 1

[15] D. P. Divincenzo. The physical implementation of quantum computation. *Fortschritte der Physik*, volume 48:2000, 2000. 2, 36

[16] M. Suchara, A. Faruque, C.-Y. Lai, G. Paz, F. Chong, and J. D. Kubiatowicz. Estimating the resources for quantum computation with the QuRE toolbox. Technical Report UCB/EECS-2013-119, UC Berkeley, 2013. 2

[17] F. Arute, K. Arya, R. Babbush, D. Bacon, J. C. Bardin, R. Barends, R. Biswas, S. Boixo, F. G. Brandao, D. A. Buell, et al. Quantum supremacy using a programmable superconducting processor. *Nature*, volume 574(7779):505–510, 2019. 2

[18] Y. Wang, Y. Li, Z.-q. Yin, and B. Zeng. 16-qubit IBM universal quantum computer can be fully entangled. *npj Quantum Information*, volume 4(1):46, 2018. 2

[19] B. Lekitsch, S. Weidt, A. G. Fowler, K. Mølmer, S. J. Devitt, C. Wunderlich, and W. K. Hensinger. Blueprint for a microwave trapped ion quantum computer. *Science Advances*, volume 3(2):e1601540, 2017. 2, 3, 36, 39, 40, 52

[20] C. Monroe and J. Kim. Scaling the ion trap quantum processor. *Science*, volume 339(6124):1164–1169, 2013. doi:10.1126/science.1231298. 2

[21] C. Wunderlich, T. Hannemann, T. Körber, H. Häffner, C. Roos, W. Hänsel, R. Blatt, and F. Schmidt-Kaler. Robust state preparation of a single trapped ion by adiabatic passage. *Journal of Modern Optics*, volume 54(11):1541–1549, 2007. doi:10.1080/09500340600741082. 2

[22] M. Acton, K.-A. Brickman, P. C. Haljan, P. J. Lee, L. Deslauriers, and C. Monroe. Near-perfect simultaneous measurement of a qubit register. *Quantum Information and Computation*, volume 6(6):465–482, 2006. ISSN 1533-7146. 2

[23] A. H. Myerson, D. J. Szwer, S. C. Webster, D. T. C. Allcock, M. J. Curtis, G. Imreh, J. A. Sherman, D. N. Stacey, A. M. Steane, and D. M. Lucas. High-fidelity readout of trapped-ion qubits. *Physical Review Letters*, volume 100:200502, 2008. doi:10.1103/PhysRevLett.100.200502. 2

[24] P. Fisk, M. Sellars, M. Lawn, and C. Coles. Accurate measurement of the 12.6 GHz "clock" transition in trapped $^{171}Yb^{+}$ ions. *IEEE Transactions on Ultrasonics Ferroelectrics and*

Frequency Control, volume 44(2):344–354, 1997. ISSN 0885-3010. doi:10.1109/58.585119. 2

[25] J. Chiaverini, D. Leibfried, T. Schaetz, M. D. Barrett, R. B. Blakestad, J. Britton, W. M. Itano, J. D. Jost, E. Knill, C. Langer, R. Ozeri, and D. J. Wineland. Realization of quantum error correction. *Nature*, volume 432, 2004. doi:10.1038/nature03074. 2

[26] A. G. Fowler, A. M. Stephens, and P. Groszkowski. High-threshold universal quantum computation on the surface code. *Physical Review A*, volume 80:052312, 2009. doi:10.1103/PhysRevA.80.052312. 2

[27] D. Leibfried, B. DeMarco, V. Meyer, D. Lucas, M. Barrett, J. Britton, W. M. Itano, B. Jelenkovic, C. Langer, T. Rosenband, and D. J. Wineland. Experimental demonstration of a robust, high-fidelity geometric two ion-qubit phase gate. *Nature*, volume 422, 2003. doi:10.1038/nature01492. 2, 24

[28] W. Paul. Electromagnetic traps for charged and neutral particles. *Reviews of Modern Physics*, volume 62(3):531–540, 1990. doi:10.1103/RevModPhys.62.531. 2

[29] W. Paul, O. Osberghaus, and E. Fischer. Ein Ionenkäfig. *Forschungsberichte des Wirtschafts und Verkehrsministeriums Nordrhein-Westfalen*, volume 415, 1958. doi:10.1007/978-3-663-04689-9. 2

[30] E. Fischer. Die dreidimensionale Stabilisierung von Ladungsträgern in einem Vierpolfeld. *Zeitschrift für Physik*, volume 156(1):1–26, 1959. doi:10.1007/BF01332512. 2

[31] W. Neuhauser, M. Hohenstatt, P. Toschek, and H. Dehmelt. Optical-sideband cooling of visible atom cloud confined in parabolic well. *Physical Review Letters*, volume 41:233–236, 1978. doi:10.1103/PhysRevLett.41.233. 2

[32] D. J. Wineland, R. E. Drullinger, and F. L. Walls. Radiation-pressure cooling of bound resonant absorbers. *Physical Review Letters*, volume 40:1639–1642, 1978. doi:10.1103/PhysRevLett.40.1639. 2

[33] C. Monroe, D. M. Meekhof, B. E. King, W. M. Itano, and D. J. Wineland. Demonstration of a fundamental quantum logic gate. *Physical Review Letters*, volume 75:4714–4717, 1995. doi:10.1103/PhysRevLett.75.4714. 2, 24

[34] J. I. Cirac and P. Zoller. Quantum computations with cold trapped ions. *Physical Review Letters*, volume 74(20):4091–4094, 1995. doi:10.1103/PhysRevLett.74.4091. 3, 24

[35] C. Monroe, R. Raussendorf, A. Ruthven, K. R. Brown, P. Maunz, L.-M. Duan, and J. Kim. Large-scale modular quantum computer architecture with atomic memory and photonic interconnects. *Physical Review A*, volume 89:022317, 2014. doi:10.1103/PhysRevA.89.022317. 3, 36, 39

[36] F. Mintert and C. Wunderlich. Ion-trap quantum logic using long-wavelength radiation. *Physical Review Letters*, volume 87:257904, 2001. doi:10.1103/PhysRevLett.87.257904. 3, 25, 37

[37] S. Weidt, J. Randall, S. C. Webster, K. Lake, A. E. Webb, I. Cohen, T. Navickas, B. Lekitsch, A. Retzker, and W. K. Hensinger. Trapped-ion quantum logic with global radiation fields. *Physical Review Letters*, volume 117:220501, 2016. doi:10.1103/PhysRevLett.117.220501. 3,

38, 39, 61, 64, 69

[38] W. Paul and H. Steinwedel. Ein neues Massenspektrometer ohne Magnetfeld. *Zeitschrift für Naturforschung A*, volume 8:448, 1953. 5, 11

[39] W. Paul, H. Reinhard, and U. Von Zahn. Das elektrische massenfilter als massenspektrometer und isotopentrenner. *Zeitschrift für Physik A Hadrons and Nuclei*, volume 152(2):143–182, 1958. 5

[40] E. Fischer. Die dreidimensionale stabilisierung von ladungsträgern in einem vierpolfeld. *Zeitschrift für Physik A Hadrons and Nuclei*, volume 156(1):1–26, 1959. 5

[41] S. Earnshaw. On the nature of the molecular forces which regulate the constitution of the luminiferous ether. *Transactions of the Cambridge Philosophical Society*, volume 7:97–112, 1842. 5

[42] H. G. Dehmelt. Radiofrequency spectroscopy of stored ions I: Storage. *Advances in Atomic and Molecular Physics*, volume 3:53, 1967. 7

[43] R. C. Sterling. *Ytterbium Ion Trapping and Microfabrication of Ion Trap Arrays*. Ph.D. thesis, University of Sussex, 2011. 10

[44] D. Church. Storage-ring ion trap derived from the linear quadrupole radio-frequency mass filter. *Journal of Applied Physics*, volume 40(8):3127–3134, 1969. 11

[45] M. G. House. Analytic model for electrostatic fields in surface-electrode ion traps. *Physical Review A*, volume 78(3):033402, 2008. 12

[46] R. Schmied. Electrostatics of gapped and finite surface electrodes. *New Journal of Physics*, volume 12(2):023038, 2010. 12

[47] K.-Y. Lin, G. H. Low, and I. L. Chuang. Effects of electrode surface roughness on motional heating of trapped ions. *Physical Review A*, volume 94:013418, 2016. doi:10.1103/PhysRevA.94.013418. 13, 23, 140

[48] Q. A. Turchette, D. Kielpinski, B. E. King, D. Leibfried, D. M. Meekhof, C. J. Myatt, M. A. Rowe, C. A. Sackett, C. S. Wood, W. M. Itano, C. Monroe, and D. J. Wineland. Heating of trapped ions from the quantum ground state. *Physical Review A*, volume 61:063418, 2000. doi:10.1103/PhysRevA.61.063418. 13, 23

[49] J. Labaziewicz, Y. Ge, P. Antohi, D. Leibrandt, K. R. Brown, and I. L. Chuang. Suppression of heating rates in cryogenic surface-electrode ion traps. *Physical Review Letters*, volume 100:013001, 2008. doi:10.1103/PhysRevLett.100.013001. 13, 23

[50] L. Deslauriers, S. Olmschenk, D. Stick, W. K. Hensinger, J. Sterk, and C. Monroe. Scaling and suppression of anomalous heating in ion traps. *Physical Review Letters*, volume 97:103007, 2006. doi:10.1103/PhysRevLett.97.103007. 13, 23

[51] A. Nizamani and W. Hensinger. Optimum electrode configurations for fast ion separation in microfabricated surface ion traps. *Applied Physics B*, volume 106(2):327–338, 2012. doi:10.1007/s00340-011-4803-x. 14, 18, 56

[52] R. B. Blakestad, C. Ospelkaus, A. P. VanDevender, J. H. Wesenberg, M. J. Biercuk, D. Leibfried, and D. J. Wineland. Near-ground-state transport of trapped-ion qubits

through a multidimensional array. *Physical Review A*, volume 84:032314, 2011. doi: 10.1103/PhysRevA.84.032314. 15

[53] D. Gerlich. *Inhomogeneous RF Fields: A Versatile Tool for the Study of Processes with Slow Ions*. John Wiley and Sons, Inc., 2007. ISBN 9780470141397. doi:10.1002/9780470141397.ch1. 18

[54] J. Mikosch, U. Frühling, S. Trippel, D. Schwalm, M. Weidemüller, and R. Wester. Evaporation of buffer-gas-thermalized anions out of a multipole RF ion trap. *Physical Review Letters*, volume 98:223001, 2007. doi:10.1103/PhysRevLett.98.223001. 18

[55] D. Wineland and H. Dehmelt. Proposed 10^{14} delta upsilon less than upsilon laser fluorescence spectroscopy on Tl^+ mono-ion oscillator III. In *Bulletin of the American Physical Society*, volume 20, pp. 637–637. 1975. 22

[56] S. A. Schulz, U. Poschinger, F. Ziesel, and F. Schmidt-Kaler. Sideband cooling and coherent dynamics in a microchip multi-segmented ion trap. *New Journal of Physics*, volume 10(045007):15, 2008. 23

[57] S. Ejtemaee and P. Haljan. 3D Sisyphus cooling of trapped ions. *Physical Review Letters*, volume 119(4):043001, 2017. 23, 24

[58] D. Wineland, C. Monroe, W. Itano, B. King, D. Leibfried, D. Meekhof, C. Myatt, and C. Wood. Experimental primer on the trapped ion quantum computer. *Fortschritte der Physik*, volume 46(4-5):363–390, 1998. doi:10.1002/(SICI)1521-3978(199806)46:4/5⟨363::AID-PROP363⟩3.0.CO;2-4. 23

[59] D. A. Hite, Y. Colombe, A. C. Wilson, K. R. Brown, U. Warring, R. Jördens, J. D. Jost, K. S. McKay, D. P. Pappas, D. Leibfried, and D. J. Wineland. 100-fold reduction of electric-field noise in an ion trap cleaned with *in situ* argon-ion-beam bombardment. *Physical Review Letters*, volume 109:103001, 2012. doi:10.1103/PhysRevLett.109.103001. 23

[60] N. Daniilidis, S. Gerber, G. Bolloten, A. R. M. Ramm, E. Ulin-Avila, I. Talukdar, and H. Häffner. Probing surface electric field noise with a single ion. *arXiv:1307.7194*, 2013. 23

[61] J. Labaziewicz, Y. Ge, D. R. Leibrandt, S. X. Wang, R. Shewmon, and I. L. Chuang. Temperature dependence of electric field noise above gold surfaces. *Physical Review Letters*, volume 101:180602, 2008. doi:10.1103/PhysRevLett.101.180602. 23

[62] D. T. C. Allcock, L. Guidoni, T. P. Harty, C. J. Ballance, M. G. Blain, A. M. Steane, and D. M. Lucas. Reduction of heating rate in a microfabricated ion trap by pulsed-laser cleaning. *New Journal of Physics*, volume 13(12):123023, 2011. 23

[63] M. Brownnutt, M. Kumph, P. Rabl, and R. Blatt. Ion-trap measurements of electric-field noise near surfaces. *Reviews of Modern Physics*, volume 87(4):1419, 2015. 24, 52

[64] A. Safavi-Naini, P. Rabl, P. F. Weck, and H. R. Sadeghpour. Microscopic model of electric-field-noise heating in ion traps. *Physical Review A*, volume 84:023412, 2011. doi:10.1103/PhysRevA.84.023412. 24

[65] S. X. Wang, J. Labaziewicz, Y. Ge, R. Shewmon, and I. L. Chuang. Individual addressing of ions using magnetic field gradients in a surface-electrode ion trap. *Applied Physics Letters*,

volume 94:094103, 2009. 24

[66] D. Stick, K. M. Fortier, R. Haltli, C. Highstrete, D. L. Moehring, C. Tigges, and M. G. Blain. Demonstration of a microfabricated surface electrode ion trap. *arXiv:1008.0990v2*, 2010. 24, 77

[67] C. Ospelkaus, U. Warring, Y. Colombe, K. R. Brown, J. M. Amini, D. Leibfried, and D. J. Wineland. Microwave quantum logic gates for trapped ions. *Nature*, volume 476, 2011. doi:10.1038/nature10290. 24, 37, 38, 68, 69

[68] T. P. Harty, D. T. C. Allcock, C. J. Ballance, L. Guidoni, H. A. Janacek, N. M. Linke, D. N. Stacey, and D. M. Lucas. High-fidelity preparation, gates, memory, and readout of a trapped-ion quantum bit. *Physical Review Letters*, volume 113:220501, 2014. doi: 10.1103/PhysRevLett.113.220501. 24, 37

[69] D. Hayes, D. Matsukevich, P. Maunz, D. Hucul, Q. Quraishi, S. Olmschenk, W. Campbell, J. Mizrahi, C. Senko, and C. Monroe. Entanglement of atomic qubits using an optical frequency comb. *Physical Review Letters*, volume 104(14):140501, 2010. 24

[70] A. Khromova, C. Piltz, B. Scharfenberger, T. F. Gloger, M. Johanning, A. F. Varón, and C. Wunderlich. Designer spin pseudomolecule implemented with trapped ions in a magnetic gradient. *Physical Review Letters*, volume 108:220502, 2012. doi:10.1103/PhysRevLett.108.220502. 24, 38, 39, 70

[71] J. E. Sansonetti and W. C. Martin. Handbook of basic atomic spectroscopic data. *Journal of Physical and Chemical Reference Data*, volume 34(4):1559–2259, 2005. 24

[72] D. De Motte. *Cryogenic Ion Trapping for Next Generation Quantum Technologies*. Ph.D. thesis, University of Sussex, 2016. 31, 35, 49, 58, 75, 116

[73] D. Coyne et al. LIGO vacuum compatible materials list. *LIGO-E960050-v12*, 2013. 31

[74] K. G. Johnson, J. D. Wong-Campos, A. Restelli, K. A. Landsman, B. Neyenhuis, J. Mizrahi, and C. Monroe. Active stabilization of ion trap radiofrequency potentials. *Review of Scientific Instruments*, volume 87(5):053110, 2016. doi:10.1063/1.4948734. 34

[75] A. Grounds. *A Cryogenic System for Scalable Ion Trap Quantum Computing*. Ph.D. thesis, University of Sussex, 2020. 34, 61, 77, 140

[76] D. Murgia. *Microchip Ion Traps with High Magnetic Field Gradients for Microwave Quantum Logic*. Ph.D. thesis, Imperial College London, 2017. 35, 79

[77] S. Wölk and C. Wunderlich. Quantum dynamics of trapped ions in a dynamic field gradient using dressed states. *New Journal of Physics*, volume 19(8):083021, 2017. 37

[78] K. R. Brown, A. C. Wilson, Y. Colombe, C. Ospelkaus, A. M. Meier, E. Knill, D. Leibfried, and D. J. Wineland. Single-qubit-gate error below 10^{-4} in a trapped ion. *Physical Review A*, volume 84:030303, 2011. doi:10.1103/PhysRevA.84.030303. 38

[79] D. T. C. Allcock, T. P. Harty, C. J. Ballance, B. C. Keitch, N. M. Linke, D. N. Stacey, and D. M. Lucas. A microfabricated ion trap with integrated microwave circuitry. *Applied Physics Letters*, volume 102(4):044103, 2013. doi:10.1063/1.4774299. 38, 39, 40, 63, 68, 69

[80] C. Piltz, T. Sriarunothai, S. S. Ivanov, S. Wölk, and C. Wunderlich. Versatile microwave-

driven trapped ion spin system for quantum information processing. *Science Advances*, volume 2(7), 2016. doi:10.1126/sciadv.1600093. 38, 61

[81] E. Standing. *Design and Fabrication of High Magnetic Field Gradients Towards Fault Tolerant Two-Qubit Gates with Trapped Ions Using Long-Wavelength Radiation*. Ph.D. thesis, University of Sussex, Brighton, 2016. 38, 40, 62, 70

[82] E. Mount, S.-Y. Baek, M. Blain, D. Stick, D. Gaultney, S. Crain, R. Noek, T. Kim, P. Maunz, and J. Kim. Single qubit manipulation in a microfabricated surface electrode ion trap. *New Journal of Physics*, volume 15(9):093018, 2013. 39, 61

[83] K. R. Brown, J. Kim, and C. Monroe. Co-designing a scalable quantum computer with trapped atomic ions. *npj Quantum Information*, volume 2:16034, 2016. 39

[84] J. A. Sedlacek, A. Greene, J. Stuart, R. McConnell, C. D. Bruzewicz, J. M. Sage, and J. Chiaverini. Distance scaling of electric-field noise in a surface-electrode ion trap. *Physical Review A*, volume 97:020302, 2018. doi:10.1103/PhysRevA.97.020302. 42

[85] S. Hong, M. Lee, H. Cheon, T. Kim, and D. Cho. Guidelines for designing surface ion traps using the boundary element method. *Sensors*, volume 16(5):616, 2016. 42, 82

[86] E. Colgan, B. Furman, M. Gaynes, W. Graham, N. LaBianca, J. Magerlein, R. Polastre, M.-B. Rothwell, R. J. Bezama, R. Choudhary, K. Marston, H. Toy, J. Wakil, J. Zitz, and R. Schmidt. A practical implementation of silicon microchannel coolers for high power chips. *IEEE Transactions on Components Packaging and Manufacturing Technology*, volume 30(2):218–225, 2007. doi:10.1109/TCAPT.2007.897977. 45, 108

[87] K. K. Mehta, A. Eltony, C. Bruzewicz, I. Chuang, R. Ram, J. Sage, and J. Chiaverini. Ion traps fabricated in a CMOS foundry. *Applied Physics Letters*, volume 105(4):044103, 2014. 45, 46

[88] M. Niedermayr, K. Lakhmanskiy, M. Kumph, S. Partel, J. Edlinger, M. Brownnutt, and R. Blatt. Cryogenic surface ion trap based on intrinsic silicon. *New Journal of Physics*, volume 16(11):113068, 2014. 45, 91

[89] P. L. W. Maunz, C. R. Clark, R. A. Haltli, A. E. Hollowell, J. F. Rembetski, P. J. Resnick, J. D. Sterk, D. L. Stick, B. Tabakov, and M. G. Blain. Characterization of a High-Optical-Access surface trap optimized for quantum information processing. Technical report, Sandia National Laboratories, Albuquerque, NM, USA, 2015. 46

[90] A. Van Rynbach, P. Maunz, and J. Kim. An integrated mirror and surface ion trap with a tunable trap location. *Applied Physics Letters*, volume 109(22):221108, 2016. doi:10.1063/1.4970542. 46

[91] B. Brandstatter, A. McClung, K. Schuppert, B. Casabone, K. Friebe, A. Stute, P. O. Schmidt, C. Deutsch, J. Reichel, R. Blatt, and T. E. Northup. Integrated fiber-mirror ion trap for strong ion-cavity coupling. *Review of Scientific Instruments*, volume 84(12):123104, 2013. doi:10.1063/1.4838696. 46

[92] S. Hong, Y. Kwon, C. Jung, M. Lee, T. Kim, and D. D. Cho. A new microfabrication method for ion-trap chips that reduces exposure of dielectric surfaces to trapped ions. *Journal of*

Microelectromechanical Systems, volume 27(1):28–30, 2018. ISSN 1057-7157. doi:10.1109/JMEMS.2017.2772310. 46

[93] K. Singer, U. Poschinger, M. Murphy, P. Ivanov, F. Ziesel, T. Calarco, and F. Schmidt-Kaler. *Colloquium*: Trapped ions as quantum bit: Essential numerical tools. *Review Modern Physics*, volume 82:2609–2632, 2010. doi:10.1103/RevModPhys.82.2609. 48

[94] C. Geuzaine and J.-F. Remacle. Gmsh: A 3D finite element mesh generator with built-in pre- and post-processing facilities. *International Journal for Numerical Methods in Engineering*, volume 79(11):1309–1331, 2009. 51

[95] R. B. Blakestad, C. Ospelkaus, A. P. VanDevender, J. M. Amini, J. Britton, D. Leibfried, and D. J. Wineland. High-fidelity transport of trapped-ion qubits through an X-junction trap array. *Physical Review Letters*, volume 102:153002, 2009. doi:10.1103/PhysRevLett.102.153002. 52

[96] P. Böhi, M. F. Riedel, T. W. Hänsch, and P. Treutlein. Imaging of microwave fields using ultracold atoms. *Applied Physics Letters*, volume 97(5):051101, 2010. 59

[97] S. C. Webster, S. Weidt, K. Lake, J. J. McLoughlin, and W. K. Hensinger. Simple manipulation of a microwave dressed-state ion qubit. *Physical Review Letters*, volume 111:140501, 2013. doi:10.1103/PhysRevLett.111.140501. 61

[98] S. Hong, M. Lee, H. Cheon, J. Ahn, M. Kim, T. Kim, and D. Cho. New scalable microfabrication method for surface ion traps and experimental results with trapped ions. In *Proceedings of the 28th IEEE International Conference on Micro Electro Mechanical Systems*, pp. 292–295. IEEE, 2015. 61

[99] H. O. Everitt. *Experimental Aspects of Quantum Computing*. Springer, 2005. 61

[100] A. Bautista-Salvador, G. Zarantonello, H. Hahn, A. Preciado-Grijalva, J. Morgner, M. Wahnschaffe, and C. Ospelkaus. Multilayer ion trap technology for scalable quantum computing and quantum simulation. *New Journal of Physics*, volume 21(4):043011, 2019. doi:10.1088/1367-2630/ab0e46. 63

[101] T. Navickas. *Towards High-Fidelity Microwave Driven Multi-Qubit Gates on Microfabricated Surface Ion Traps*. Ph.D. thesis, University of Sussex, 2018. 63

[102] E. Holzman. *Essentials of RF and Microwave Grounding*. Artech House, 2006. 64

[103] J. R. Black. Electromigration - A brief survey and some recent results. *IEEE Transactions on Electron Devices*, volume 16(4):338–347, 1969. 71

[104] B. Tabakov, F. Benito, M. Blain, C. R. Clark, S. Clark, R. A. Haltli, P. Maunz, J. D. Sterk, C. Tigges, and D. Stick. Assembling a ring-shaped crystal in a microfabricated surface ion trap. *Physics Reviews Applied*, volume 4:031001, 2015. doi:10.1103/PhysRevApplied.4.031001. 77

[105] J. Britton, D. Leibfried, J. A. Beall, R. B. Blakestad, J. H. Wesenberg, and D. J. Wineland. Scalable arrays of RF paul traps in degenerate Si. *Applied Physics Letters*, volume 95:173102, 2009. 77

[106] J. T. Merrill, C. Volin, D. Landgren, J. M. Amini, K. Wright, S. C. Doret, C.-S. Pai, H. Hay-

den, T. Killian, D. Faircloth, K. R. Brown, A. W. Harter, and R. E. Slusher. Demonstration of integrated microscale optics in surface-electrode ion traps. *New Journal of Physics*, volume 13(10):103005, 2011. doi:10.1088/1367-2630/13/10/103005. 77

[107] R. D. Graham, S.-P. Chen, T. Sakrejda, J. Wright, Z. Zhou, and B. B. Blinov. A system for trapping barium ions in a microfabricated surface trap. *AIP Advances*, volume 4(5):057124, 2014. doi:10.1063/1.4879817. 77

[108] H. C. Miller. Surface flashover of insulators. *IEEE Transactions on Electrical Insulation*, volume 24(5):765–786, 1989. ISSN 0018-9367. doi:10.1109/14.42158. 83

[109] M. D. Hughes. *The Development of Microfabricated Ion Traps Towards Quantum Information and Simulation*. Ph.D. thesis, University of Sussex, 2012. 85

[110] B. El-Kareh. *Fundamentals of Semiconductor Processing Technology*. Springer Science & Business Media, 2012. 86

[111] L. Freund, J. Floro, and E. Chason. Extensions of the Stoney formula for substrate curvature to configurations with thin substrates or large deformations. volume 74, pp. 1987–1989. AIP, 1999. 88

[112] K. Wörhoff, A. Driessen, P. Lambeck, L. Hilderink, P. W. Linders, and T. J. Popma. Plasma enhanced chemical vapor deposition silicon oxynitride optimized for application in integrated optics. *Sensors and Actuators A: Physical*, volume 74(1-3):9–12, 1999. 89

[113] M. Alayo, I. Pereyra, and M. Carreno. Thick SiO_xN_y and SiO_2 films obtained by PECVD technique at low temperatures. *Thin Solid Films*, volume 332(1-2):40–45, 1998. 89

[114] Y. Kim, D. Kim, and D. Yoon. PECVD SiO_2 and SiON films dependant on the RF bias power for low-loss silica waveguide. *Thin Solid Films*, volume 475(1-2):271–274, 2005. 89

[115] E. P. Van de Ven, I.-W. Connick, and A. S. Harrus. Advantages of dual frequency PECVD for deposition of ILD and passivation films. In *Proceedings of the 7th International VLSI Multilevel Interconnection Conference*, pp. 194–201. IEEE, 1990. 89

[116] M. Hussein, K. Wörhoff, G. Sengo, and A. Driessen. Optimization of plasma-enhanced chemical vapor deposition silicon oxynitride layers for integrated optics applications. *Thin Solid Films*, volume 515(7-8):3779–3786, 2007. 90

[117] A. Kołodziej. Staebler-Wronski effect in amorphous silicon and its alloys. *Opto-electronics Review*, volume 12(1):21–32, 2004. 90

[118] K. Mackenzie, D. Johnson, M. DeVre, R. Westerman, and B. Reelfs. Stress control of Si-based PECVD dielectrics. In *Proceedings of the 207th Electrochemical Society Meeting*, pp. 148–159. 2005. 90

[119] R. C. Sterling, M. D. Hughes, C. J. Mellor, and W. K. Hensinger. Increased surface flashover voltage in microfabricated devices. *Applied Physics Letters*, volume 103(14):143504, 2013. doi:10.1063/1.4824012. 91, 95

[120] R. C. Sterling, H. Rattanasonti, S. Weidt, K. Lake, P. Srinivasan, S. Webster, M. Kraft, and W. K. Hensinger. Fabrication and operation of a two-dimensional ion-trap lattice on a high-voltage microchip. *Nature Communications*, volume 5, 2014. 91

[121] D. M. Knotter and T. D. Denteneer. Etching mechanism of silicon nitride in HF-based solutions. *Journal of The Electrochemical Society*, volume 148(3):F43–F46, 2001. 95

[122] D. C. Miller, C. F. Herrmann, H. J. Maier, S. M. George, C. R. Stoldt, and K. Gall. Intrinsic stress development and microstructure evolution of Au/Cr/Si multilayer thin films subject to annealing. *Scripta Materialia*, volume 52(9):873–879, 2005. 101

[123] S. Danyluk, G. McGuire, K. Koliwad, and M. Yang. Diffusion studies in Cr-Pt thin films using Auger electron spectroscopy. *Thin Solid Films*, volume 25(2):483–489, 1975. 101

[124] V. Guarnieri, L. Biazi, R. Marchiori, and A. Lago. Platinum metallization for MEMS application: Focus on coating adhesion for biomedical applications. *Biomatter*, volume 4(1):e28822, 2014. 101

[125] G. Gottstein. *Physical Foundations of Materials Science*. Springer Science & Business Media, 2013. 101

[126] R. Cahn and P. Haasen. *Physical Metallurgy*. Elsevier Science, 1996. ISBN 9780080538945. 101

[127] A. Katz, B. Weir, and W. Dautremont-Smith. Au/Pt/Ti contacts to p-$In_{0.53}Ga_{0.47}As$ and n-InP layers formed by a single metallization common step and rapid thermal processing. *Journal of Applied Physics*, volume 68(3):1123–1128, 1990. 101

[128] J. Zhang, J. Han, Y. Yin, L. Dong, and W. Niu. Study on the failure temperature of Ti/Pt/Au and Pt_5Si_2–Ti/Pt/Au metallization systems. *Journal of Semiconductors*, volume 38(9):096005, 2017. 101

[129] B. Lekitsch. *Development of Microfabricated Ion Traps for Scalable Microwave Quantum Technology*. Ph.D. thesis, University of Sussex, 2015. 101, 117

[130] P. H. Holloway. Gold/chromium metallizations for electronic devices. *Gold Bulletin*, volume 12(3):99–106, 1979. 101

[131] Y. Shacham-Diamond, A. Dedhia, D. Hoffstetter, and W. Oldham. Reliability of copper metallization on silicon-dioxide. In *Proceedings of the 8^{th} International VLSI Multilevel Interconnection Conference*, pp. 109–115. IEEE, 1991. 102

[132] E. O. Hammerstad and N. T. Høgskole. *Microstrip Handbook*. Trondheim: Norwegian Institute of Technology, 1975. 110, 132

[133] J. Baker-Jarvis and S. Kim. The interaction of radio-frequency fields with dielectric materials at macroscopic to mesoscopic scales. *Journal of Research of the National Institute of Standards and Technology*, volume 117:1, 2012. 111

[134] M. Niedermayr. *Cryogenic Surface Ion Traps*. Ph.D. thesis, Universität Innsbruck, 2015. 113

[135] W. Che, Y. F. Tang, J. Zhang, and Y. Chow. Formulas of dielectric and total attenuations of a microstrip line. *Radio Science*, volume 45(5), 2010. 115

[136] B. Simonovich. Practical method for modeling conductor surface roughness using close packing of equal spheres. In *Proceedings of the IEEE International Symposium on Electromagnetic Compatibility*. 2016. 115

[137] C. Xu, C. Reece, and M. Kelley. Analyzing surface roughness dependence of linear RF losses. In *Proceedings of the 26th International Linear Accelerator Conference*. 2013. 115

[138] D. J. Berkeland, J. D. Miller, J. C. Bergquist, W. M. Itano, and D. J. Wineland. Minimization of ion micromotion in a Paul trap. *Journal of Applied Physics*, volume 83(10):5025–5033, 1998. doi:10.1063/1.367318. 117

[139] J. Britton. *Microfabrication Techniques for Trapped Ion Quantum Information Processing*. Ph.D. thesis, Univeristy of Colorado, Boulder, 2008. 117

[140] K. Mouthaan, R. Tinti, M. De Kok, H. De Graaff, J. Tauritz, and J. Slotboom. Microwave modelling and measurement of the self-and mutual inductance of coupled bondwires. In *Proceedings of the Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 166–169. IEEE, 1997. 122

[141] A. Harm, K. Mouthaan, E. Aziz, and M. Versleijen. Modelig and simulation of hybrid RF circuits using a versatile compact bondwire model. In *Proceedings of the 28th European Microwave Conference*, volume 2, pp. 529–534. IEEE, 1998. 122

[142] K. Mouthaan. *Modelling of RF High Power Bipolar Transistors*. Delft University Press, 2001. 122

[143] T. A. Green. Gold electrodeposition for microelectronic, optoelectronic and microsystem applications. *Gold Bulletin*, volume 40(2):105–114, 2007. 124, 125, 126

[144] S. Dimitrijević, M. Rajčić-Vujasinović, and V. Trujić. Non-cyanide electrolytes for gold plating – A review. *International Journal of Electrochemical Science*, volume 8(5):6620–6646, 2013. 125

[145] E. Koukharenko, Z. Moktadir, M. Kraft, M. Abdelsalam, D. Bagnall, C. Vale, M. Jones, and E. A. Hinds. Microfabrication of gold wires for atom guides. *Sensors and Actuators A*, volume 115(2-3):600–607, 2004. 125, 126

[146] E. Papadopoulou, M. Meneghello, P. Marafini, R. P. Johnson, T. Brown, and P. N. Bartlett. The effect of temperature on electrochemically driven denaturation monitored by SERS. *Bioelectrochemistry*, volume 106:353–358, 2015. 125

[147] Z. Liu and A. C. West. Modeling of galvanostatic pulse and pulsed reverse electroplating of gold. *Electrochimica Acta*, volume 56(9):3328–3333, 2011. 126

[148] D. Mac Arthur. A study of gold reduction and oxidation in aqueous solutions. *Journal of The Electrochemical Society*, volume 119(6):672–677, 1972. 126

[149] J. Y. Park, G. H. Kim, K. W. Chung, and J. U. Bu. Electroplated RF MEMS capacitive switches. In *Proceedings of the 13th Annual International Conference on Micro Electro Mechanical Systems*, pp. 639–644. IEEE, 2000. 126

[150] A. J. Bard, L. R. Faulkner, J. Leddy, and C. G. Zoski. *Electrochemical Methods: Fundamentals and Applications*, volume 2. wiley New York, 1980. 127

[151] M. Z. Bazant. Theory of chemical kinetics and charge transfer based on nonequilibrium thermodynamics. *Accounts of Chemical Research*, volume 46(5):1144–1160, 2013. 128

[152] Y. Xie, X. Zhang, B. Ou, T. Chen, J. Zhang, C. Wu, W. Wu, and P. Chen. Creating equally

spaced linear ion string in a surface-electrode trap by feedback control. *Physical Review A*, volume 95:032341, 2017. doi:10.1103/PhysRevA.95.032341. 140

[153] Y. Ralchenko, A. Kramida, J. Reader, et al. NIST Atomic Spectra Database (version 5.5.3), [Online], 2018. 146, 147

[154] R. Williams and M. Woods. Mobile fluoride ions in SiO_2. *Journal of Applied Physics*, volume 46(2):695–698, 1975. 146

[155] M. A. Makeev and A.-L. Barabási. Ion-induced effective surface diffusion in ion sputtering. *Applied Physics Letters*, volume 71(19):2800–2802, 1997. 146

[156] Y.-D. Wu and C.-L. Wong. Substituent effect on the dissociation energy of the Si-H bond: A density functional study. *Journal of Organic Chemistry*, volume 60(4):821–828, 1995. 147

[157] A. Vijh and K. Dimoff. The effect of oxide surface layers on the breakdown voltage in metal-vacuum-metal sandwiches. *Journal of Materials Science*, volume 11(1):150–163, 1976. 148

[158] W. Y. Ng. *The Study of Cleaning Methods for Dynamic Random Access Memory (DRAM) Capacitor*. Master's thesis, National Chiao Tung University, 2010. 149

[159] H. Sinn, W. Kaminsky, and K. Pohlmann. DE4012397C1: Halogen hydride removal - by adding ammonia to pyrolysis gas in an agitated bed of pyrolysis reactor. Patent, 1990. 151

Appendix A

Detailed microfabrication processes

A.1 PECVD

A.1.1 PECVD in situ nitrous oxide clean

Tool description: OIPT SYS 100 PECVD Tool

Process gas: N_2O 500 sccm

Plasma source: 50 W RF (13.56 MHz)

Chamber pressure: 1000 mTorr

Sample table: Sample table heated to 350°C

Process details: Nitrous oxide plasma removes organic contaminants similarly to how an oxygen plasma does which is avoided due to its highly reactive nature with silane gas.

A.1.2 PECVD of silicon dioxide - recipe 1, conventional

Tool description: OIPT SYS 100 PECVD Tool

Process gas: SiH_4 10 sccm, N_2O 80 sccm, N_2 1000 sccm

Plasma source: 20 W RF (13.56 MHz)

Chamber pressure: 1000 mTorr

Sample table: Sample table heated to 350°C

Process details: Highly reactive silane gas constantly get absorbed and released from the hot sample surface. Process parameters were optimised by Dr Owain Clark for both low stress and high uniformity. Deposition rate is $\sim$ 20 nm/min.

A.1.3 PECVD of silicon dioxide - recipe 2, improved

Tool description: OIPT SYS 100 PECVD Tool

Process gas: SiH_4 4.2 sccm, N_2O 350 sccm, N_2 80 sccm

Plasma source: 20 W RF (13.56 MHz)

Chamber pressure: 1000 mTorr

Sample table: Sample table heated to 350°C

Process details: This optimised recipe guarantees a pinhole-free SiO_2 film with low stress. A 1 µm is deposited in $\sim$ 30 mins.

A.1.4 PECVD of silicon dioxide with TEOS - recipe 1, conventional TEOS

Tool description: OIPT SYS 100 PECVD Tool

Process gas: Ar carrier gas 500 sccm

Plasma source: 40 W RF (13.56 MHz)

Chamber pressure: 500 mTorr

Sample table: Sample table heated to 350°C

Process details: TEOS ($Si(OC_2H_5)_4$) is used as a precursor to silicon dioxide instead of silane. Carrier argon gas brings the TEOS vapour into the reaction chamber where at elevated temperature, TEOS converts to silicon dioxide.

A.1.5 PECVD of silicon dioxide with TEOS - recipe 2, LF only

Tool description: OIPT SYS 100 PECVD Tool

Process gas: Ar carrier gas 500 sccm

Plasma source: 50 W LF (50 kHz)

Chamber pressure: 1000 mTorr

Sample table: Sample table heated to 350°C

Process details: This recipe aims to show the effect of LF deposition. The resultant film is highly compressive.

A.1.6 PECVD of silicon dioxide with TEOS - recipe 3, improved TEOS

Tool description: OIPT SYS 100 PECVD Tool

Process gas: Ar (carrier gas) 500 sccm

Plasma source: 8 s of 40 W RF (13.56 MHz), 12 s of 40 W LF (50 kHz)

Chamber pressure: 500 mTorr

Sample table: Sample table heated to 350°C

Process details: This recipe uses an alternating combination of frequency sources to enhance the density of the deposited film.

A.1.7 PECVD of silicon nitride - recipe 1, conventional

Tool description: OIPT SYS 100 PECVD Tool

Process gas: SiH_4 12.5 sccm, NH_3 20 sccm, N_2 500 sccm

Plasma source: 20 W RF (13.56 MHz)

Chamber pressure: 875 mTorr

Sample table: Sample table heated to 350°C

Process details: Films produced with this recipe has little H-bond at a cost of more pinholes. A 17 min reaction gives 300 nm film.

A.1.8 PECVD of silicon nitride - recipe 2, improved

Tool description: OIPT SYS 100 PECVD Tool

Process gas: SiH_4 20 sccm, N_2 500 sccm, NH_3 35 sccm

Plasma source: 10 s of 20 W RF (13.56 MHz), 10 s of 30 W LF (50 kHz)

Chamber pressure: 750 mTorr

Sample table: Sample table heated to 350°C

Process details: Similar to the TEOS based SiO_2 recipe with alternating source (A.1.5), during an LF cycle, the deposited layer is densified. This process can produce a film with relatively low stress up to 200 nm in 15 mins.

A.2 CVD

A.2.1 Sputter deposition of titanium adhesion layer

Tool description: AJA International, Inc. ORION magnetron sputter

Process gas: Ar 10 sccm

Plasma source: 300 W DC

Chamber pressure: 3 mTorr

Sample distance to target: 200 mm

Process details: An 8 nm titanium adhesion layer is deposited in 60 s. Note that a clean chamber is desired for depositing such film as titanium is a getter material.

A.2.2 Sputter deposition of chromium adhesion layer

Tool description: AJA International, Inc. ORION magnetron sputter

Process gas: Ar 10 sccm

Plasma source: 250 W DC

Chamber pressure: 2 mTorr

Sample distance to target: 200 mm

Process details: A 65 nm film is deposited in 8 min. An adhesion layer of 8 nm is deposited in 1 min.

A.2.3 Sputter deposition of platinum diffusion barrier layer

Tool description: AJA International, Inc. ORION magnetron sputter

Process gas: Ar 10 sccm

Plasma source: 300 W DC

Chamber pressure: 3 mTorr

Sample distance to target: 200 mm

Process details: A 60 nm layer is deposited in 2 min.

A.2.4 Sputter deposition of gold layer

Process gas: Ar 10 sccm

Plasma source: 300 W DC

Chamber pressure: 3 mTorr

Sample distance to target: 200 mm

Process details: A 110 nm is deposited in 4min.

A.2.5 E-beam evaporation deposition of gold layer

Tool description: Leybold Optics Leybold Lab 700

Power: Soak stage 1 at 4%, soak stage 2 at 6%, depositing between 6% to 8%.

Chamber pressure: 10^{-6} Torr

Process details: Deposition rate measured with crystal thickness monitor is ~ 0.1 nm/s.

A.3 Dry etch

A.3.1 ICP pre-etch clean

Tool description: OIPT SYS 380 ICP RIE Tool

Process gas: Cl_2 50 sccm for 5 mins, then O_2 50 sccm for 5 mins

Plasma source: 800 W ICP (1.8-2.2 MHz)

Chamber pressure: 20 mTorr

Process details: This recipe uses Cl_2 gas to fully remove any metal residue. The O_2 passivates the chamber wall after the Cl_2 clean. This gives a constant initial chamber condition.

A.3.2 ICP etch of gold

Tool description: OIPT SYS 380 ICP RIE Tool

Process gas: Cl_2 20 sccm, Ar 10 sccm

Plasma source: 100 W RF (13.56 MHz), 800 W ICP (1.8-2.2 MHz)

Chamber pressure: 5 mTorr

Sample table: Carrier wafer cooled with helium flow, helium chiller set to 50°C.

Process details: Highly corrosive gas Cl_2 is used to chemically remove gold forming $AuCl_x$. This recipe gives an etch rate over 100 nm/min. When a slower etch is required, buffer gas such as N_2 can be introduced. This process also etches Pt and other metals at unknown etch rate. When etching non-noble metals, an extra argon bombardment step[1] should be executed before this to break its native oxide layer.

A.3.3 IBE gold etch

Tool description: OIPT Ionfab 300 Plus

Process gas: Ar 30 sccm

Chamber pressure and atom source parameters: 5 mTorr, VBEAM= 600 V, IBEAM= 2 mA, VACC= 301 V, PRF= 540 W

Sample table: Carrier wafer cooled with helium flow, helium pressure set to 25 mTorr resulting in a helium flow rate of about 23 sccm.

Process details: The physical bombardment of argon atoms breaks the bonds between metal atoms thus milling the film away. No chemical process is involved. A 200 nm Pt film was removed in 27 min. A 250 nm Cr/Pt/Au seed layer was removed in 35 min.

A.3.4 Oxide etch

Oxide etch recipe 1

Tool description: OIPT SYS 380 ICP RIE Tool

Process gas: Ar 150 sccm, C_4F_8 30 sccm, O_2 30 sccm

Plasma source: 500 W RF (13.56 MHz), 100 W ICP (1.8-2.2 MHz)

Chamber pressure: 150 mTorr

Sample table: Carrier wafer cooled with helium flow, helium chiller set to 10°C.

Oxide etch recipe 2

Tool description: OIPT SYS 380 ICP RIE Tool

Process gas: Ar 50 sccm, C_4F_8 30 sccm, O_2 20 sccm

[1] Argon bombardment step parameters: 200 W RF power, 800 W ICP power, Ar flow rate 10 sccm, HBr flow rate 20 sccm, Cl_2 flow rate 10 sccm, carrier wafer cooled to 40°C with helium flow.

Plasma source: 700 W RF (13.56 MHz), 100 W ICP (1.8-2.2 MHz)

Chamber pressure: 150 mTorr

Sample table: Carrier wafer cooled with helium flow, helium chiller set to 10°C.

Oxide etch recipe 3

Tool description: OIPT SYS 380 ICP RIE Tool

Process gas: Ar 150 sccm, C_4F_8 60 sccm, O_2 20 sccm

Plasma source: 700 W RF (13.56 MHz), 100 W ICP (1.8-2.2 MHz)

Chamber pressure: 200 mTorr

Sample table: Carrier wafer cooled with helium flow, helium chiller set to 10°C.

Oxide etch recipe 4

Tool description: OIPT SYS 380 ICP RIE Tool

Process gas: Ar 150 sccm, C_4F_8 30 sccm, O_2 30 sccm

Plasma source: 500 W RF (13.56 MHz), 100 W ICP (1.8-2.2 MHz)

Chamber pressure: 150 mTorr

Sample table: Carrier wafer cooled with helium flow, helium chiller set to 0°C.

Oxide etch recipe 5

Tool description: OIPT SYS 380 ICP RIE Tool

Process gas: Ar 150 sccm, C_4F_8 80 sccm, O_2 30 sccm

Plasma source: 500 W RF (13.56 MHz), 100 W ICP (1.8-2.2 MHz)

Chamber pressure: 150 mTorr

Sample table: Carrier wafer cooled with helium flow, helium chiller set to 0°C.

Oxide etch recipe 6

Tool description: OIPT SYS 380 ICP RIE Tool

Process gas: Ar 150 sccm, C_4F_8 30 sccm, O_2 30 sccm

Plasma source: 700 W RF (13.56 MHz), 100 W ICP (1.8-2.2 MHz)

Chamber pressure: 150 mTorr

Sample table: Carrier wafer cooled with helium flow, helium chiller set to 0°C.

Oxide etch recipe 7

Tool description: OIPT SYS 380 ICP RIE Tool

Process gas: Ar 150 sccm, C_4F_8 30 sccm, O_2 10 sccm, H_2 20 sccm

Plasma source: 700 W RF (13.56 MHz), 100 W ICP (1.8-2.2 MHz)

Chamber pressure: 150 mTorr

Sample table: Carrier wafer cooled with helium flow, helium chiller set to 0°C.

Oxide etch recipe 8

Tool description: OIPT SYS 380 ICP RIE Tool

Process gas: gas flow 1 (Ar 150 sccm, C_4F_8 30 sccm, O_2 10 sccm, H_2 20 sccm), gas flow 2 (Ar 150 sccm, C_4F_8 60 sccm, O_2 20 sccm)

Sample table: Carrier wafer cooled with helium flow, helium chiller set to 0°C.

Process details: This is a switched process between process A.3.4 and A.3.4. The chiller temperature, RF power and pressure are set to 0°C, 700 W and 150 mTorr respectively. Each cycle is consisted of 2s of gas flow 1 and 3s of gas flow 2.

Oxide etch recipe 9

Tool description: OIPT SYS 380 ICP RIE Tool

Process gas: gas flow 1 (Ar 150 sccm, C_4F_8 30 sccm, O_2 10 sccm, H_2 20 sccm), gas flow 2 (Ar 150 sccm, C_4F_8 60 sccm, O_2 20 sccm and SF_6 25 sccm)

Sample table: Carrier wafer cooled with helium flow, helium chiller set to 0°C.

Process details: This is a switched process between process A.3.4 and A.3.4. The chiller temperature, RF power and pressure are set to 0°C, 700 W and 150 mTorr respectively. Each cycle is consisted of 2s of gas flow 1 and 3s of gas flow 2.

Oxide etch polymer removal

Tool description: OIPT SYS 380 ICP RIE Tool

Process gas: Step 1: SF_6 50 sccm, 25 mTorr, step 2: 35 mTorr

Sample table: Carrier wafer cooled with helium flow, helium chiller set to 50°C.

Process details: This is a switching process consisted of 5s of step1 and 5s of step2.

Oxide etch oxygen ashing

Tool description: OIPT SYS 380 ICP RIE Tool

Process gas: NH_3 200 sccm O_2 100 sccm, 100 mTorr

Sample table: Carrier wafer cooled with helium flow, helium chiller set to 50°C.

Process details: This process aims to remove polymer from C_4F_8-heavy oxide etch.

Oxide etch residue removal

Tool description: OIPT SYS 380 ICP RIE Tool

Process gas: NH_3 200 sccm O_2 100 sccm, 100 mTorr

Sample table: Carrier wafer cooled with helium flow, helium chiller set to 50°C.

Process details: This process aims to remove polymer from C_4F_8-heavy oxide etch.

A.4 Wet etch

A.4.1 Wet etch of gold

There are two chemistries etching gold, iodine and aqua regia. As discussed in the chapters, the iodine etch is subject to Galvanic effect which creates undesired undercut near the interface with adhesion layer. Aqua regia however, purely harnesses the strong oxidizing nature of the etchant to remove gold which is more isotropic yet dangerous to operate.

Iodine gold etch

Prepare 1 gram of I_2 (solid) and 4 grams of KI (solid) in a glass container, then pour 40 ml DI water in the container and dissolve the solid by agitation. Submerge the sample in the solution to etch. Be careful on monitoring the etching process as the iodine solution is non-transparent. Rinse with DI water when expected etch depth is obtained. To store the etchant, keep it in a dry and cool place as heat and sunlight will trigger I_2 to decomposite.

Gentle iodine gold etch

Similar to the recipe above but use only 1 out 10 parts solution. Submerge the sample for 10s and quickly used DI water to rinse it clean.

A.4.2 NMP organic strip

N-Methyl-2-pyrrolidone (NMP) is a colourless organic liquid that dissolves a wide range of polymers. Thanks to its high solubility, a total strip of photoresist and other organic films is often done by bathing the substrate in hot NMP overnight. Typical temperature that the solution sits at is 100°C.

A.4.3 Silicon dioxide undercut etch

Hydrofluoric acid strongly etches SiO_2 but doesn't attack silicon, gold, chromium or copper. Increased etch rate is attainable with elevated temperatures and higher concentration. To remove SiO_2 layer buried underneath the supported structures, etch rate and etch profile must be carefully controlled.

A.4.4 RCA clean

The RCA clean is a standard set of wafer cleaning steps which are usually performed before high temperature processing. Operator can also use the first step (RCA-1) to remove metallic layers such as Titanium. Caution should be used as the RCA clean is designed as an organic solvent and while it is not as potent as HF or Piranha solution, nitrile gloves, goggles and a fume hood must be used.

Chemicals for RCA-1:

- 5 parts of DI water
- 1 parts of aqueous NH_4OH (ammonium hydroxide, 29% by weight of NH3)
- 1 parts aqueous H_2O_2 (hydrogen peroxide, 30%)

Place the dry shallow beaker on the beaker heater inside a fume cupboard. Prepare the solution and pour into the shallow beaker. Clamp the thermometer gently with the support stand and clamp, with the tip just below the surface of the solution. Place the beaker with the deionised water next to the heater inside the fume cupboard. Turn the heater on and set to a temperature of 225°C and wait for the solution to reach 80°C. Once the temperature is at 80°C submerge the substrates into the solution and start a timer for 10 minutes. The bubbles of oxygen will keep pushing the substrates to the surface, use the plastic tweezers to push them under and allow them to freely rotate if no substrate holder is available. Once the timer expires remove the substrates and place them in the deionised water beaker. Use QDR[2] to rinse the substrates if available. Empty the beaker, prepare the RCA-2 chemicals.

Chemicals for RCA-2:

- 6 parts of DI water
- 1 parts of aqueous HCl (hydrochloride, 27%)
- 1 parts aqueous H_2O_2 (hydrogen peroxide, 30%)

Put the DI water in a beakier, carefully add HCl in and heat it to 70°C. Once reached the temperature, remove it from hot plate and add H_2O_2. Bubbles should appear in 1 to 2 minutes indicating its ready to use. Soak the substrate in the solution for 10 minutes before removing it to rinse with DI water or use QDR.

A.5 Other processes

A.5.1 AZ 9260 4.7 μm Spin coating

Tool description: Brewer Science CEE 200 spin coater, Sawatec HP-401-Z hotplate

Dehydration: 10 min at 120°C in dehydration oven

Photoresist: MicroChemicals GmbH AZ 9260 Positive Photoresist

Spin profile: see table A.1.

Soft bake: 2 min at 120°C on hotplate

Process details: A 7s 500 rpm rotation step makes the photoresist evenly distributed on

[2]Quick Dump Rinse (QDR), a process that removes chemical residues after wet processes by cycling between overflow rinsing, spray rinsing and quick dump rinsing. All QDR processes used in this work guarantees a minimum DI water resistivity of 12 MΩ.

Table A.1: AZ 9260 4.7 μm spin profile

Step	Acceleration/rpm/s	Speed/rpm	Time/s
1	250	500	2
2	0	500	7
2	950	2400	2
2	0	2400	2
2	−950	500	60
2	0	500	2
3	−250	0	2

Table A.2: TI Prime spin profile

Step	Acceleration/rpm/s	Speed/rpm	Time/s
1	100	500	5
2	4000	4000	1
3	0	4000	30
4	-1000	100	2

the substrate surface, followed by a 2.4k rpm rotation which gives correct film thickness.

A.5.2 TI Prime coating

Tool description: Brewer Science CEE 200 spin coater, Sawatec HP-401-Z hotplate

Dehydration: 10 min at 120°C in dehydration oven

Photoresist: MicroChemicals GmbH TI Prime Adhesion Promoter

Spin profile: see table A.2.

Soft bake: 2 min at 120°C on hotplate

Process details: After spin coating, no residual drops should be visible. This recipe is modified from a recipe developed by Dr Kian Shen Kiang.

A.5.3 AZ 9260 4.7 μm Hard baking

Tool description: Sawatec HP-401-Z hotplate

Process details:

After soft bake, place the wafer with ca. 4.7 μm of photoresist film in an oven or a hot plate, follow the baking profile:

- 110°C, 1 min
- raise to 130°C in 1 min
- stay at 130°C for 1 min
- Cool down to room temperature in 30 mins

A gradual cooling down to room temperature is vitally important as an abrupt drop down of temperature will result in cracks.

Appendix B

Chip and mask designs

Unless stated otherwise, all masks presented below are 7 inches and all chips are 12 × 12 mm. This appendix includes the most essential but not all designs and masks used in the thesis.

B.1 Individual chip designs

All the chips are named in a systemic way with a format of 'AA00BB1'. 'AA' represents the type of chips, '00' the first two digits of the ion height in micron, 'BB' the designer and fabricator's initials or the fabrication facility and the last '1' represents the series number of the chip. For example, 'LN10FS1' is translated as the first type of the linear chips of 100 μm ion height designed and fabricated by **F**an in **S**outhampton Nanofabrication Centre. The followings are a selection of chips closely relative to the main contents of this thesis, the remaining chips can be found on the masks presented in the next section.
In this appendix, a selection of individual chips are attached including four linear ion traps (B.1, B.2, B.3 and B.4) and a sensor ion trap (B.5).

B.2 Individual mask designs

Mask B.6 and B.7 are chromium-glass masks[1]. Mask B.8 is a flexible thin-film mask[2].

[1]Fabrication service provided by Compugraphics International Limited.
[2]Fabrication service provided by Micro Lithography Services Ltd.

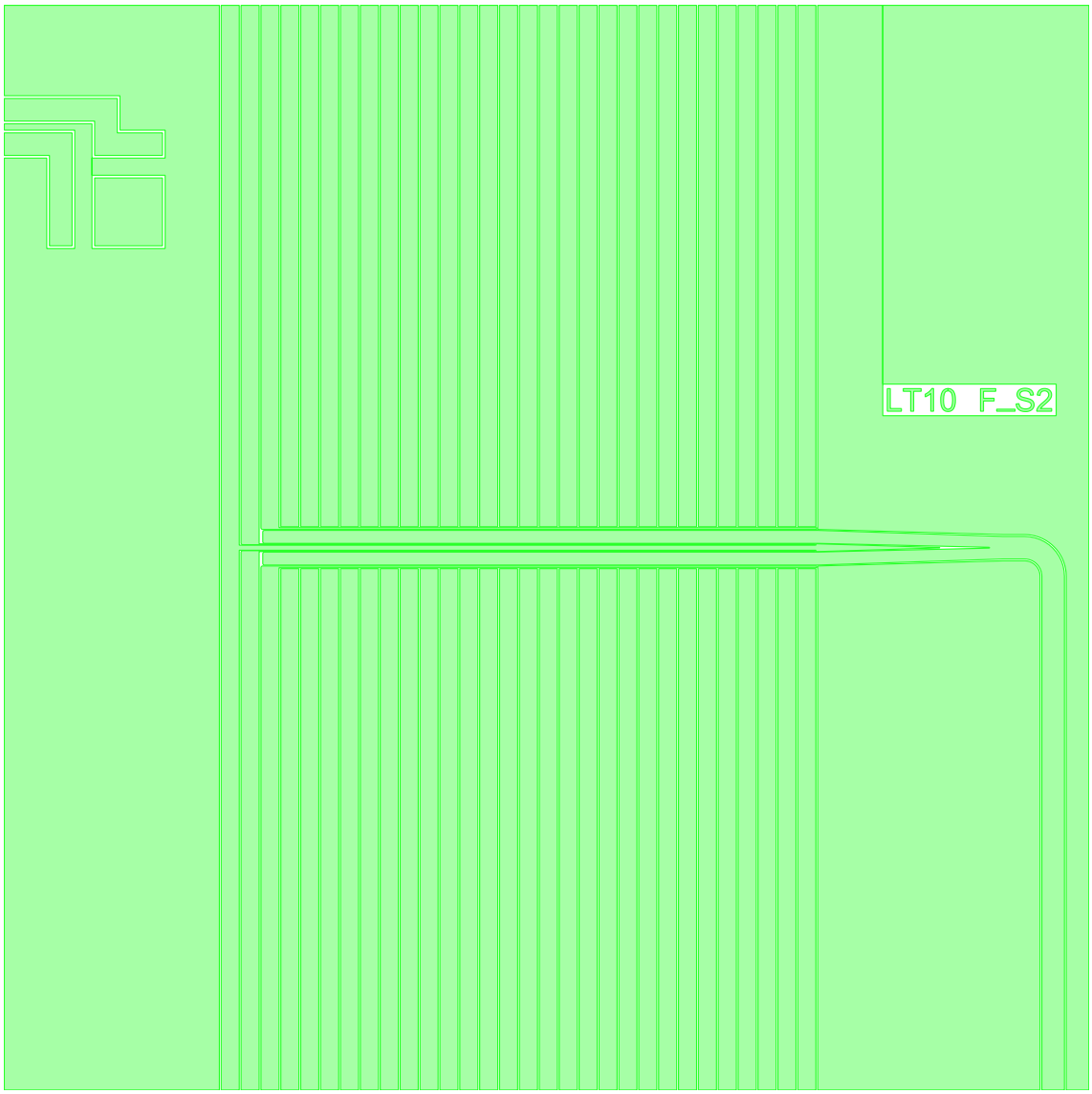

Figure B.1: Ion trap design LT10FFS2: **L**inear ion **T**rap, 100 μm ion height. The left top is a foot print for CX-1050-SD-HT-4L.

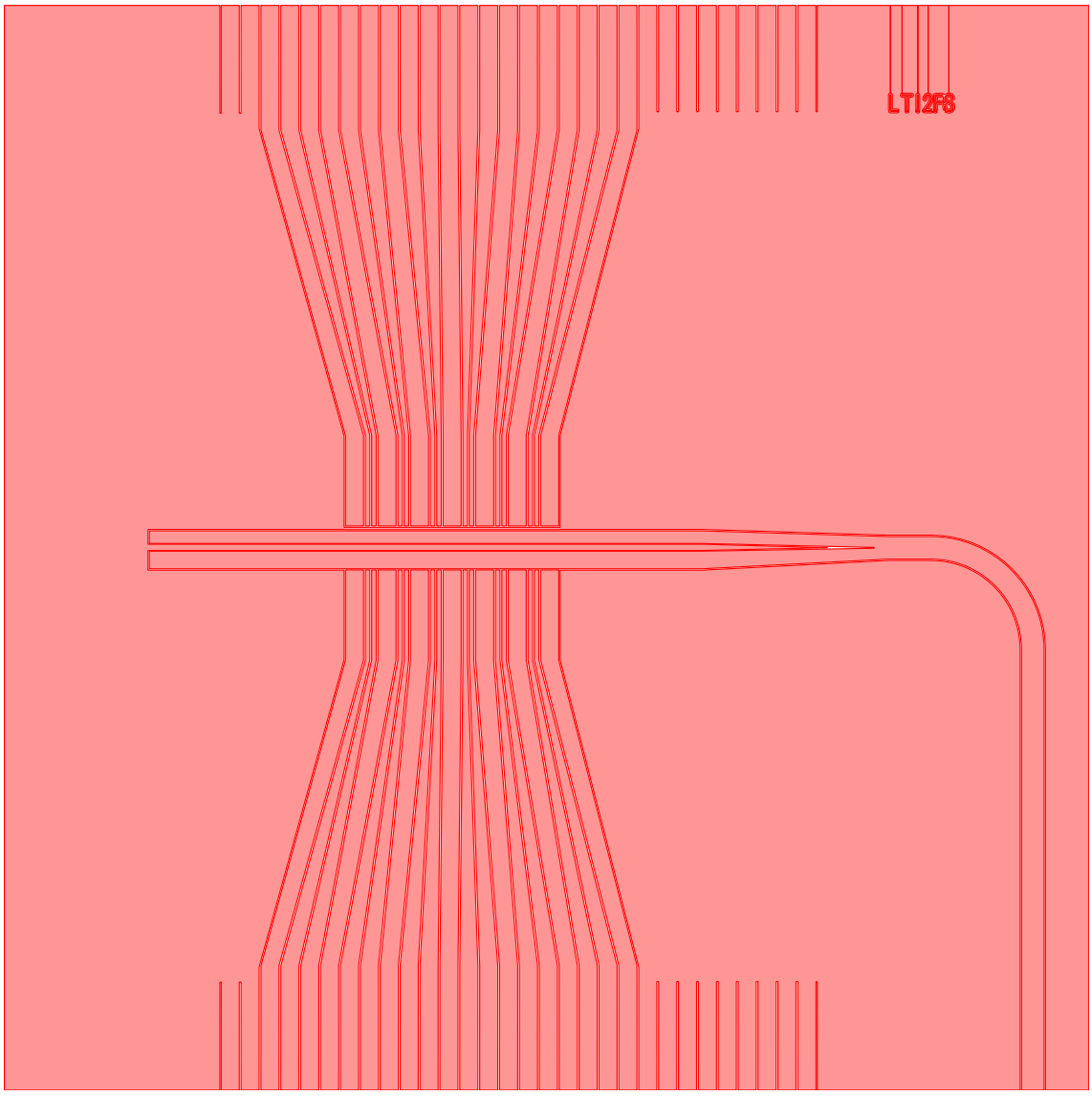

Figure B.2: Ion trap design LT12FS: **L**inear ion **T**rap, 125 μm ion height.

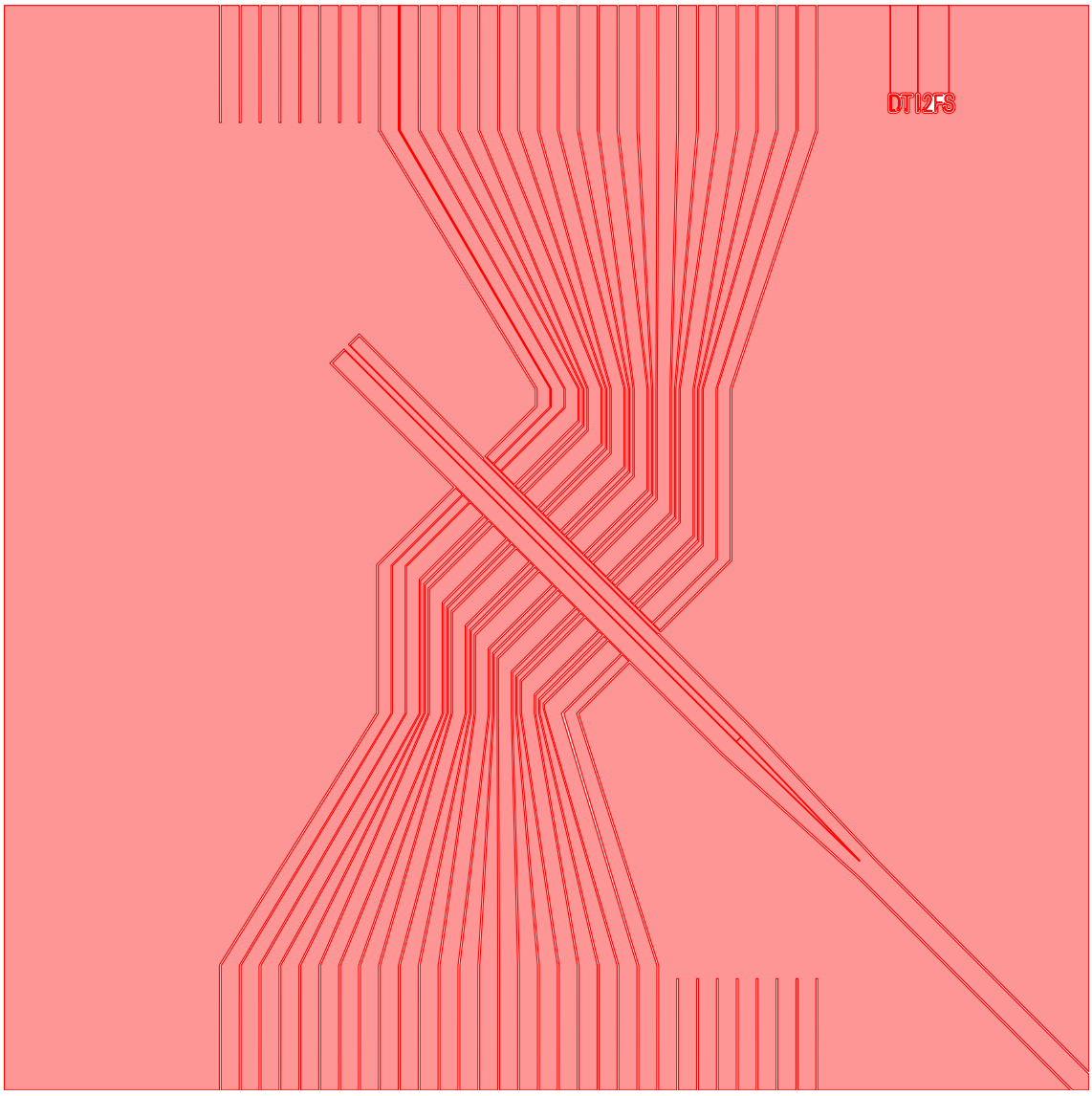

Figure B.3: Ion trap design DT12FS: **D**iagonal linear ion **T**rap, 125 μm ion height.

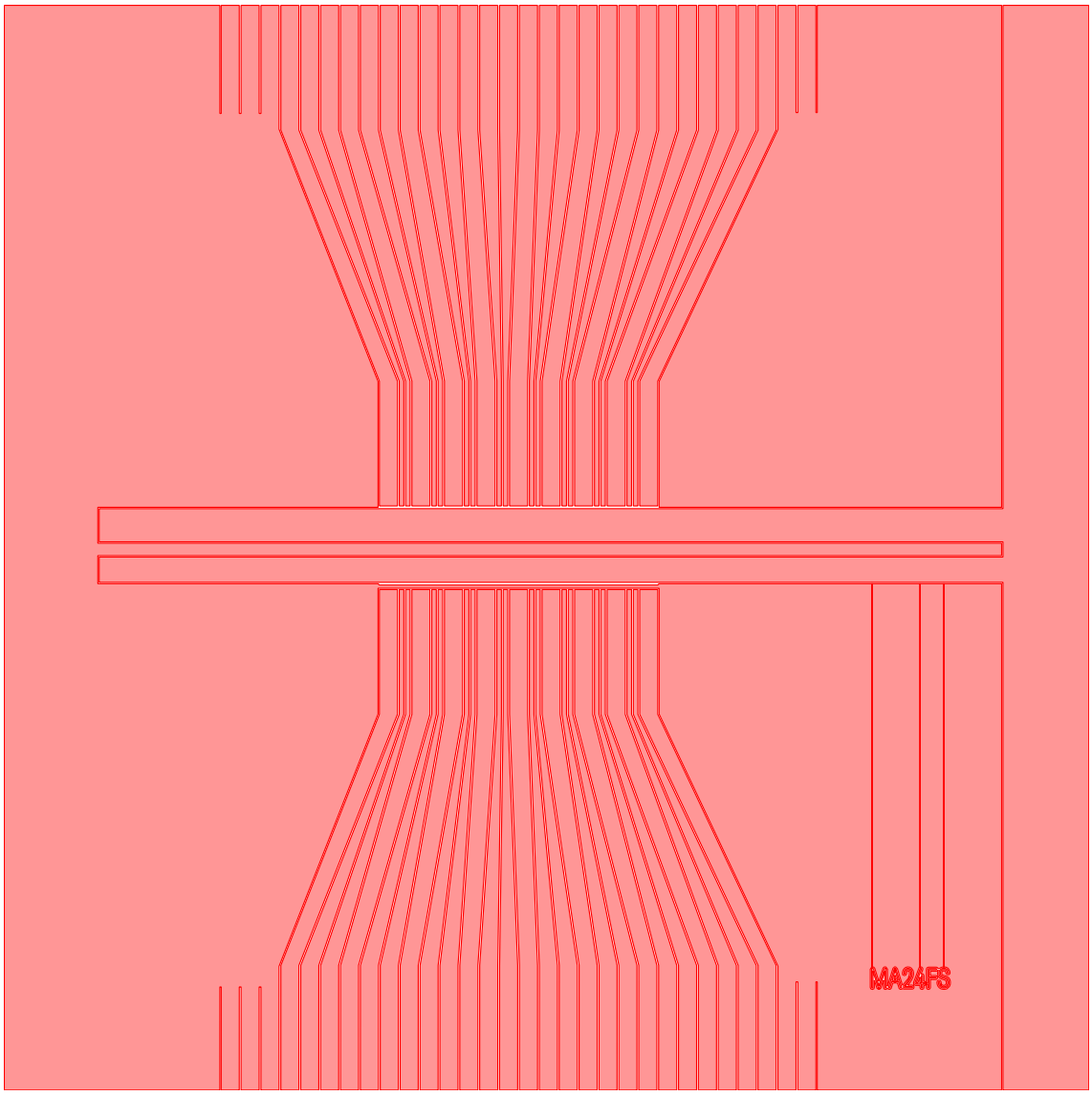

Figure B.4: Ion trap design MA24FS: '**M**other of **A**ll traps' linear ion trap, 240 µm ion height.

Figure B.5: Ion trap design SC14FAS1: **S**ensor ion trap **C**hip, is an ion trap with multiple linear regions, 140 μm ion height. Co-designed with Dr Altaf Nizamani.

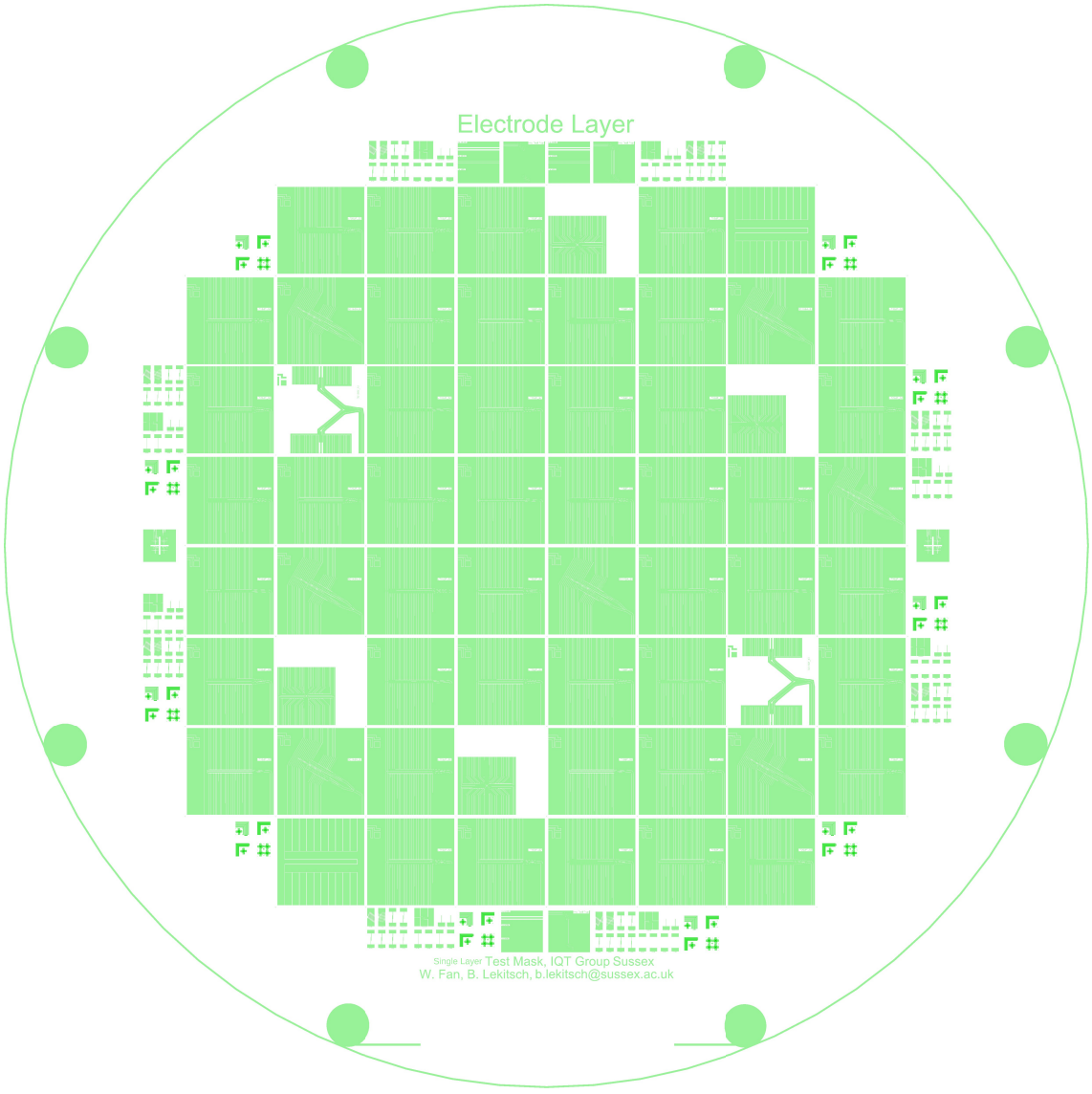

Figure B.6: Mask1, positive mask with electroplating contacts for ion traps.

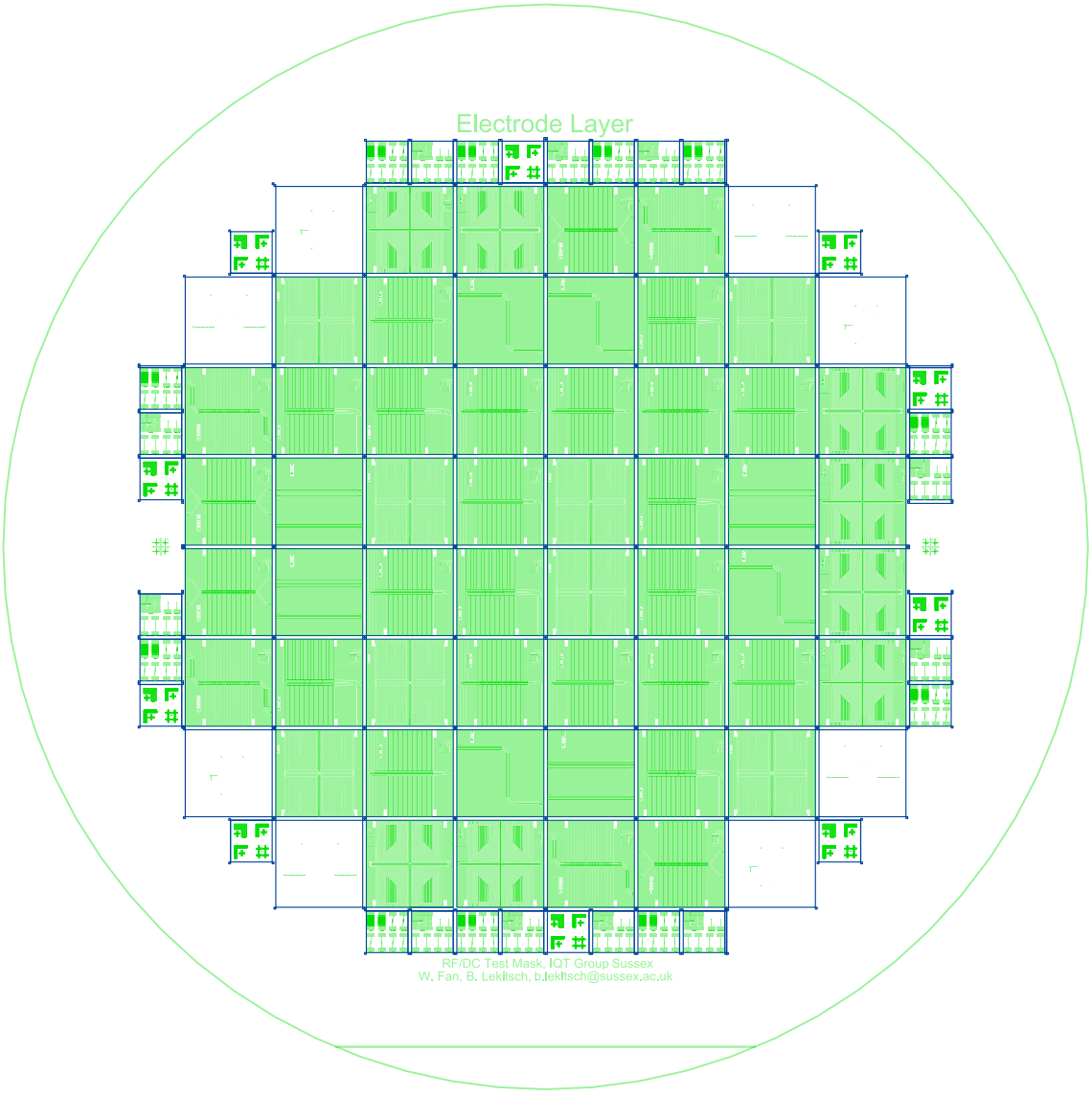

Figure B.7: Mask2, positive mask for ion traps and hybrid ring couplers.

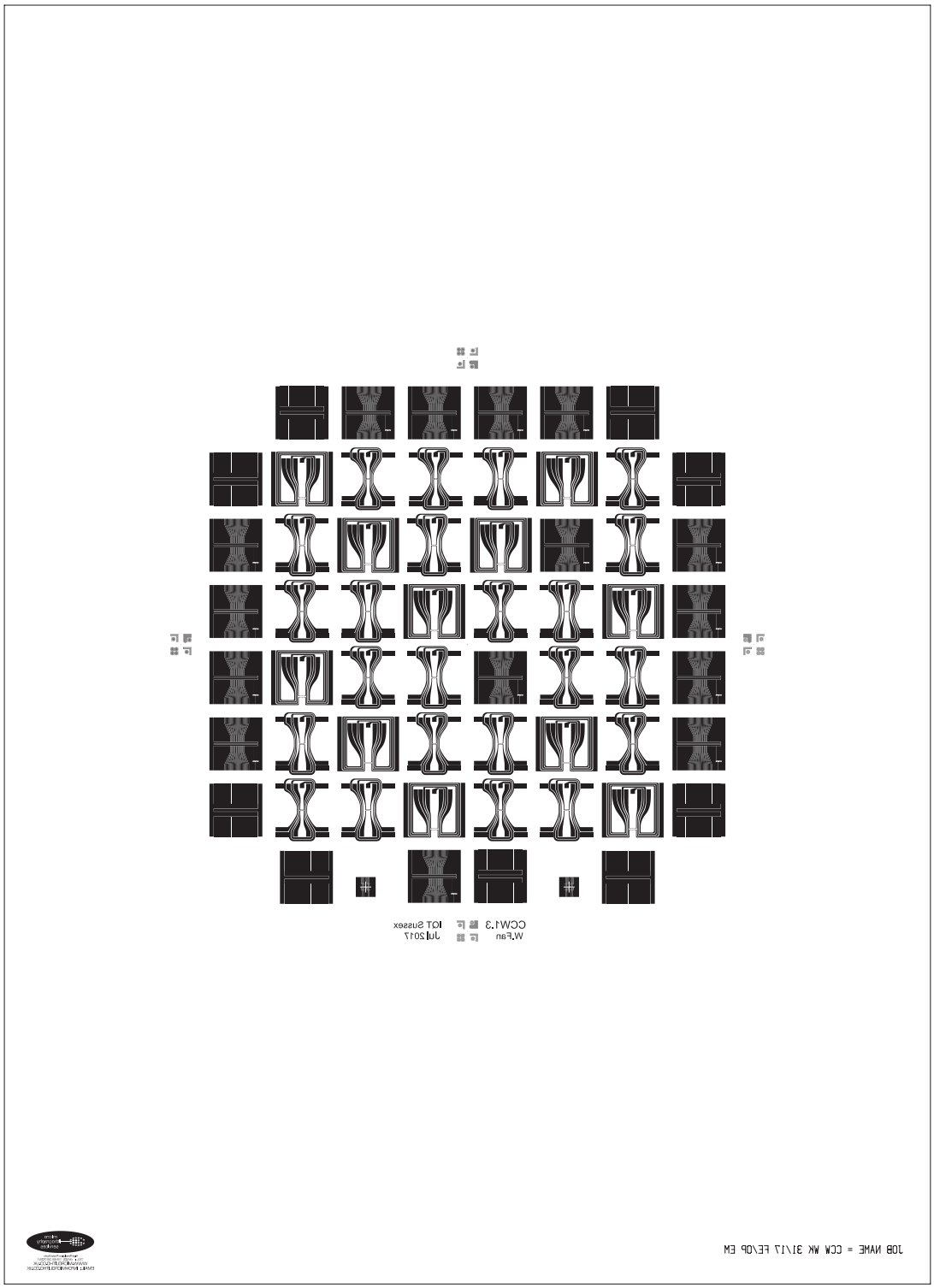

Figure B.8: Mask3, current carrying wires, positive mask.