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Flexible Sensors and Devices for Conformable Applications

*Design, Fabrication and Characterisation techniques
tuned for a flexible world*

Júlio César Beja Costa

Submitted for the degree of Doctor of Philosophy

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Declaration

I hereby declare that this thesis has not been and will not be submitted in whole or in part to another University for the award of any other degree.

Signature:

Júlio César Beja Costa

UNIVERSITY OF SUSSEX

JÚLIO CÉSAR BEJA COSTA, DOCTOR OF PHILOSOPHY

FLEXIBLE SENSORS AND DEVICES FOR CONFORMABLE APPLICATIONS

SUMMARY

Flexible electronics are considered a pathway towards more ubiquitous and discrete electronic devices. From brain sensors, to smart bandages and electronic skins, the potential of flexible electronics is endless and promises new and exciting applications. This thesis shows the work conducted on the characterisation and fabrication of flexible devices based on materials compatible with flexible substrates. By exploring the stability, resilience and versatility of such devices, it provides novel and useful insights into the limitations and potential of flexible electronics.

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Chapter 1

Introduction

1.1 Motivation

The barrier between people and their electronic devices is becoming thinner every day. Before home computers and telephones people would only rarely interact with relatively smart electronic devices, nowadays we can barely imagine living without a smartphone and internet access. Flexible electronics find their spotlight in this growing demand for ubiquitous electronics. At their most fundamental level, flexible devices tend to be cheaper to manufacture, can be fabricated over large areas, and are compatible with eco-friendly substrates. This means that even basic devices such as passive sensors can be readily produced and embedded in every day objects [1, 2]. In their most complex form, they can be used to produce brain/machine interfaces that are impossible to realise using rigid electronics [3], smart RFID tags at a fraction of the cost of standard ICs [4], or foldable smartphones and screens [5]. As a consequence of this growing interest, the field of printed and flexible sensors alone is expected to grow from \$3.6 Billion to \$7.6 Billion by 2027 [6].

However, contrarily to rigid electronics and Silicon, the field of flexible electronics does not have a champion semiconductor material. The vast number of available materials combined with their relative novelty leads to many unknowns. For example, there are not yet comprehensive studies on the long-term stability of some of the most utilised materials. Furthermore, while rigid ICs and other devices can be sold as parts and quickly soldered together to fabricate complex systems, flexible electronic devices need to be fabricated from scratch utilising specialised thin-film fabrication techniques. This, combined with other restraints that will become clearer in the following sections, means that there are still plenty of sensors and circuits to be realised in a flexible format. This thesis aims to study a subset of materials and flexible devices. More specifically, it discusses the long-term stability,

resilience to extreme environmental conditions and potential circuit/sensor applications of amorphous Indium-Gallium-Zinc-Oxide (a-IGZO) thin-film transistors. Thus, this work provides important considerations regarding the stability, limitations, and potential novel applications of this technology.

1.2 State-of-the-art¹

This section will discuss the state-of-the-art of flexible devices, circuits and sensors. It will start by providing a short historical perspective of the field of flexible electronics. This will be followed by an introduction to some of the most relevant materials and device architectures utilised in the development of flexible devices and circuits. Finally, an in-depth discussion of the material subset utilised in this thesis, as well as some examples of relevant sensors and circuits will be presented.

1.2.1 Introduction to Flexible Electronics

Partially flexible circuits are not new. For example, flexible printed circuit boards are fairly common and utilise standard rigid components soldered onto flexible boards made of Polyimide (PI). On the other hand, fully flexible electronic systems are rare and require for the entirety of the device, not only the substrate, to be mechanically flexible. The seeds of active flexible electronics can be traced back to 1968, when Dr. Brody and Dr. Page produced a Tellurium (Te) thin-film transistor (TFT) on a paper strip [9]. While inferior to Silicon (Si) metal-oxide-semiconductor field effect transistors (MOSFETs) in terms of raw performance, TFTs had the particularity of being possible to fabricate utilising coating techniques. For this reason, while the size of Silicon-based devices was limited by the size of the silicon crystals of only a few inches, TFTs could be fabricated over large substrates, which was essential for the development of flat-panel displays [9]. Their fabrication method also meant that these devices could be fabricated on substrates with low temperature budgets. These particularities set the trend for the scope of flexible electronics research. Instead of aiming to achieve raw performance comparable to Silicon, flexible electronics offer low-cost processing options, stability under mechanical bending and the potential to be implemented utilising fully biocompatible materials. Interestingly, Tellurium flexible TFTs achieving a hole mobility of $35 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ have recently been demonstrated on polyethylene terephthalate (PET) substrates [10]. These results are es-

¹This section includes components from selected sections of the review papers [7, 8], which the PhD applicant authored and co-authored.

pecially promising given the lack of high-mobility p-type semiconductors whose fabrication processes are compatible with flexible substrates. However, these devices still presented a relatively low On/Off current ratio (I_{on}/I_{off}) of 10^4 and the substrate had to be kept at -80°C during the Te evaporation. Shortly after Te, CdSe, hydrogenated amorphous silicon (a-Si:H) and low temperature polysilicon (LT p-Si) TFTs emerged [9, 11]. CdSe emerged as an n-type semiconductor compatible with flexible substrates, and recent devices based on this material demonstrated a field-effect mobility (μ_{FE}) of $10.1\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ with an I_{on}/I_{off} of 10^4 [12]. In comparison, a-Si offers a larger I_{on}/I_{off} of 10^7 with low Off currents of 10^{-12} A , resulting in lower power consumption [13]. However, this semiconductor presents a low μ_{FE} of $\approx 1\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$. LT p-Si is generally deposited by annealing and crystallising a-Si, films, resulting in high I_{on}/I_{off} with high μ_{FE} , at the expense of larger processing temperatures. More recently, to address the various aforementioned trade-offs, metal oxide TFTs [14], organic materials [15] and Silicon nanomembranes (SiNMs) [16, 17] have also been utilised to develop not only flexible electronic circuits, but also sensors. Compared to Te and CdSe, these new materials are less toxic, are more readily available, and can produce devices with overall better electrical performance. Organic materials can be deposited at room temperature (RT) and are ideal candidates for solution processed semiconductors, which results in a high compatibility with high-throughput industrial processes. However, they generally present low μ_{FE} of $1\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ to $10\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ [7]. SiNMs present mobility values of $\approx 800\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ but must be fabricated through a complicated transfer method since they are fabricated by gently thinning the top silicon layer in buried oxide Silicon wafers, followed by the etching of the SiO_2 layer to release the thin Si top layer. Regarding the performance of metal oxide semiconductors, section 1.2.3 discusses the properties of these materials in more detail. In addition to all the aforementioned materials, some exotic alternatives have also emerged, such as graphene, black phosphorus (BP) or transition metal dichalcogenides (TMDs) [7, 18, 19, 20]. These promise to offer very high mobility values but for now are still limited by the complexity of their fabrication processes. Table 1.1 shows a summary of the advantages and disadvantages of the aforementioned material groups for flexible electronics applications. In summary, a trend is observed towards the development of high-performance flexible electronics that are simple and cheap to fabricate. In this context, this thesis focus on the development and applications of metal-oxide based TFTs, and more specifically a-IGZO. This subset of materials was chosen since it offers a trade-off between performance, large-area process compatibility and cost. The next section discusses the design of flexible TFTs, including

more detailed considerations on the materials and architectures required for the development of such devices.

Semiconductor material	Industrial Scalability	μ_{FE} (cm ² V ⁻¹ s ⁻¹)	Carrier type	Processing T (�C)	Processing Cost
Metal oxide [21]	High	10 - 100	N	RT - 350	Low
Organic [22]	High	0.1 - 10	P	RT - 250	Low
a-Si [23]	High	1	N	150 - 300	Low
LT p-Si [24]	Average	50-100	N/P	250 - 350	Average
Si-NM [17]	Low	800	N/P	> 500	High
Te [10]	Average	35	P	-80 - RT	High
Graphene [19]	Low	> 10 000	N/P	> 400	High
BP [18]	Low	1000	N/P	> 300	High
TMD [20]	Low	200	N/P	> 400	High

Table 1.1: Main semiconductor materials compatible and tested for the fabrication of flexible electronics.

1.2.2 Flexible TFT design

This section discusses the important design elements when fabricating flexible TFTs. This includes the choice of materials and the device structure. Since this thesis is focused on the development of metal-oxide based TFTs, the description of the available materials and architectures is largely tailored towards this subset of materials.

Materials for Flexible TFTs

Thin-film transistors can be fabricated on flexible substrates to create bendable or even stretchable devices. A typical flexible TFT material stack includes the substrate, gate metal, gate insulator, semiconductor channel, source/drain contacts and passivation layer. Adhesion and barrier layers, as well as etch stop layers can also be found in some devices, if necessary [25]. These devices are fabricated by using either solution or vacuum-based thin-film deposition techniques that are typically limited to temperatures below 350  C due to the temperature budget of flexible substrates [21].

In typical applications, the semiconductor and substrate layers are the first to be chosen. Section 1.2.3 provides more details on some of the relevant metal oxide semiconductor materials compatible with flexible electronics, as well as their trade-offs. Generally,

a high I_{on}/I_{off} and a low threshold voltage (V_{th}) are desirable for low power consumption, a high carrier mobility allows faster devices, and a high transconductance (g_m) allows for higher intrinsic gains. After the semiconductor, the substrate is potentially the most important layer. Some of the important parameters to consider when choosing a substrate are its surface roughness, Young's modulus, glass transition temperature (T_g), thermal coefficient of expansion or transparency. Polyimide (PI) is commonly used as a substrate for high-performance electronics since this material presents a relatively high T_g of 360 °C, a small coefficient of thermal expansion of 3.4 ppm/K, surface roughness in the nanometer range and decent chemical stability [26]. However, PI is not as transparent or biocompatible as other materials such as PET and Parylene [27, 28]. At the same time, the T_g of the latter two materials is below 100 °C, with melting temperatures of approximately 280 °C [27, 28]. Other materials utilised as substrates for the development of flexible TFTs include polydimethylsiloxane (PDMS) [29], Polyethylene naphthalate (PEN) [30], or even paper [31], amongst many others.

In addition to the substrate and the semiconductor, choosing the gate and source/drain materials is also of importance. Most commonly, metal thin-films deposited through techniques such as DC sputtering, thermal evaporation or e-beam evaporation are chosen for this purpose. Gold thin-films are a common choice for the contact material due to their high conductivity and resistance to oxidation. However, in this case, titanium or chromium are generally required to increase the adhesion of gold to the substrate [32]. The most significant drawback of these materials is that they are not transparent, which limits the scope of their application. For applications that require transparency, ITO is typically used given its high transparency in the visible range (in excess of 80 %) and low electric resistivity ($1 \times 10^{-4} \Omega \text{ cm}$) [33]. Furthermore, the type of contact formed with the semiconductor material is an equally important factor. For example, while metals such as gold and nickel typically form an ohmic contact with a-IGZO, silver and platinum tend to form a Schottky barrier, depending on the oxygen content at the interface [34, 35]. It is important to note that while a Schottky barrier is not usually desirable in the design of TFTs, this phenomenon can be used to create interesting devices such as printed Schottky diodes [34] and high-intrinsic gain TFTs [35].

Equally important is the choice of the gate insulator. This is typically a thin dielectric material such as Al_2O_3 , SiO_2 or HfO_2 . This layer is important since the semiconductor/dielectric interface has a significant impact on the stability and performance of metal oxide devices [36, 37]. Al_2O_3 is commonly used in the fabrication of a-IGZO TFTs

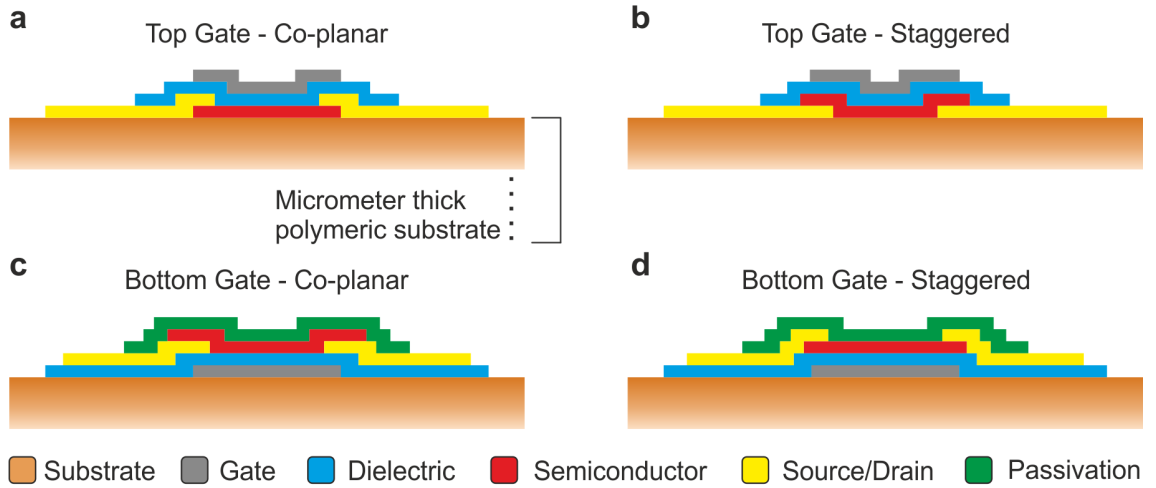


Figure 1.1: Main thin-film transistor device architectures. a) Top-gate co-planar; b) Top-gate staggered; c) Bottom-gate co-planar; d) Bottom-gate staggered

since it forms a high quality interface with this material and it can be deposited using atomic layer deposition (ALD) at room temperature while obtaining dense 2.5 g/cm^3 films with a dielectric constant above 7.5. Furthermore, it presents a breakdown voltage of approximately 3.7 MV/cm and a leakage current below $1 \times 10^{-7} \text{ A/cm}^2$ (5 V bias) [38, 7]. This material is also used as the passivation layer given its high quality interface with a-IGZO. However, $\text{TiO}_2/\text{Al}_2\text{O}_3$, $\text{HfO}_2/\text{Al}_2\text{O}_3$ and polymer/ Al_2O_3 multilayer stacks have demonstrated superior performance in terms of reliability when compared to single Al_2O_3 layers [39, 40, 41]. This indicates that the Al_2O_3 might not be enough to prevent degradation of flexible TFTs over long periods of storage time.

Flexible TFT structure

There are two common TFT architectures, top or bottom-gate. Top gate devices allow for semiconductor layers processed at higher temperatures since the semiconductor is either the first (co-planar fig.1.1a) or second (staggered fig.1.1b) layer to be deposited. For this reason, high temperature processing or semiconductor post-deposition treatments do not impact the remaining layers. In addition, top-gate TFTs do not require a specific passivation layer, since the deposition of the top dielectric and gate layers automatically shields the semiconductor from the external environment. However, controlling the properties of the semiconductor layer is inherently harder since the steps required to deposit and pattern the dielectric, gate and potentially contact layers have the potential to change the bulk of the semiconductor and the interface between the dielectric and the semiconductor [42]. This can have a negative impact especially in low temperature deposited amorph-

ous materials such as a-IGZO, since elements such as Oxygen and Hydrogen are known to be mobile inside this material and have a significant impact on the performance of the semiconductor [43, 44]. In contrast, while bottom-gate devices require a passivation layer, the semiconductor is not disturbed by as many fabrication steps, since both the gate and the dielectric have already been deposited and patterned when the semiconductor is deposited. In addition, the gate metal can shield the semiconductor channel from any surface charges in the substrate. The placement of the contacts also has an impact on the performance of the final devices. Co-planar architectures tend to have larger contact resistances since there is a confinement of the electric field on a very narrow region at the semiconductor/dielectric, leading to a contact-limited profile [45]. Staggered S/D contacts place the contacts in the opposite side of the semiconductor/dielectric interface and as such make use of a larger area of the S/D pads. In addition to the common device architectures described in this section, there are also other exotic device configurations such as multi-gate TFTs or vertical and quasi-vertical TFTs [8]. Details on the techniques, device structure and main methods used in this thesis can be found in the Methods sub-section in Chapter 2.

1.2.3 Amorphous Oxide Semiconductors for Flexible Electronics

The development of materials that can be processed at low-temperature and over large areas is attractive from both financial and environmental perspectives. This has resulted in a long list of metal oxide semiconductor materials that are compatible with the development of flexible electronic devices. This is because these materials can typically be deposited at low temperatures, which is one of the major limitations of flexible substrates.

Material	I_{on}/I_{off}	μ_{FE} (cm ² V ⁻¹ s ⁻¹)	Carrier	Processing T (°C)
a-InGaZnO [46]	10 ⁷	15	N	RT - 150
ZnO [47]	10 ⁸	13	N	RT - 150
InSnZnO [48]	10 ⁸	33	N	300
InSnO [49]	10 ⁸	26	N	200
InZnO [50]	10 ⁷	7	N	300
SnO [51]	10 ³	6	P	180
Cu _x O [52]	10 ²	5 ⁻⁴	P	300

Table 1.2: Properties of common metal oxide semiconductor materials utilised for the development of flexible transistors.

As presented in Table 1.2, metal oxide semiconductors are mainly n-type semiconductors. This is because the charge carrier transport relies on the overlap of spatially spread spherical ns orbitals belonging to the metal cations, corresponding to the conduction band minimum (CBM) [53]. Simultaneously, the valence band maximum (VBM) is comprised of highly localized oxygen orbitals, which results in a larger hole effective mass and in a poor hole mobility for p-type metal oxide semiconductors. For this reason, metal oxide semiconductors have mostly been confined to n-type devices [21, 54]. However, while a complimentary technology would be advantageous, metal oxides, and more specifically a-IGZO, offer a high mechanical stability when bent down to micrometre range radius [55], and can be deposited using low temperature techniques such as DC sputtering [56], RF sputtering [57], and solution methods [58, 59]. Of the aforementioned techniques, RF sputtering is the most common method employed for the deposition of a-IGZO thin-films. However, other methods are becoming more popular owing to their potential to fabricate films with higher charge carrier mobility and better step-covering properties [8]. These include ALD [47] and plasma-enhanced ALD (PEALD), [60] or pulsed DC magnetron sputtering (PDCMS) [61]. For example, flexible a-IGZO TFTs were fabricated on polyimide by depositing interlayers of In_2O_3 and GaZnO , resulting in devices with a μ_{FE} of $47.9 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ [60]. In addition, a-IGZO is easily patterned by utilising common microfabrication techniques such as photolithography combined with either lift-off or wet etching, depending on the application. Furthermore, solution processed a-IGZO is becoming the focus of increased attention due to the potential for industrial processes such as roll-to-roll manufacturing. However, while encouraging examples of inkjet printed IGZO are already present in literature [59], these still require relatively high annealing temperatures of up to 400°C .

In terms of their performance, flexible a-IGZO TFTs can be tuned to achieve an outstanding electron mobility (μ_{FE}) in excess of $70 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ [62], I_{on}/I_{off} above 10^{10} [63] and S of only 69 mV/dec [64]. However, while these performance parameters cannot be found in a single device, most standard high-quality a-IGZO TFTs combine an μ_{FE} of $15 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, threshold voltage (V_{th}) around 0 V , I_{on}/I_{off} of 10^7 and S below 200 mV/dec . These values represent a trade-off when comparing a-IGZO to other available metal oxide semiconductors such as ZnO or InSnZnO (ITZO). Table 1.2 displays the performance of common metal oxide semiconductors materials for a more facile comparison.

When considering high-frequency applications, metal oxide materials have also been utilised to fabricate flexible transistors operating with a f_{max} as high as 3.7 GHz and an f_t

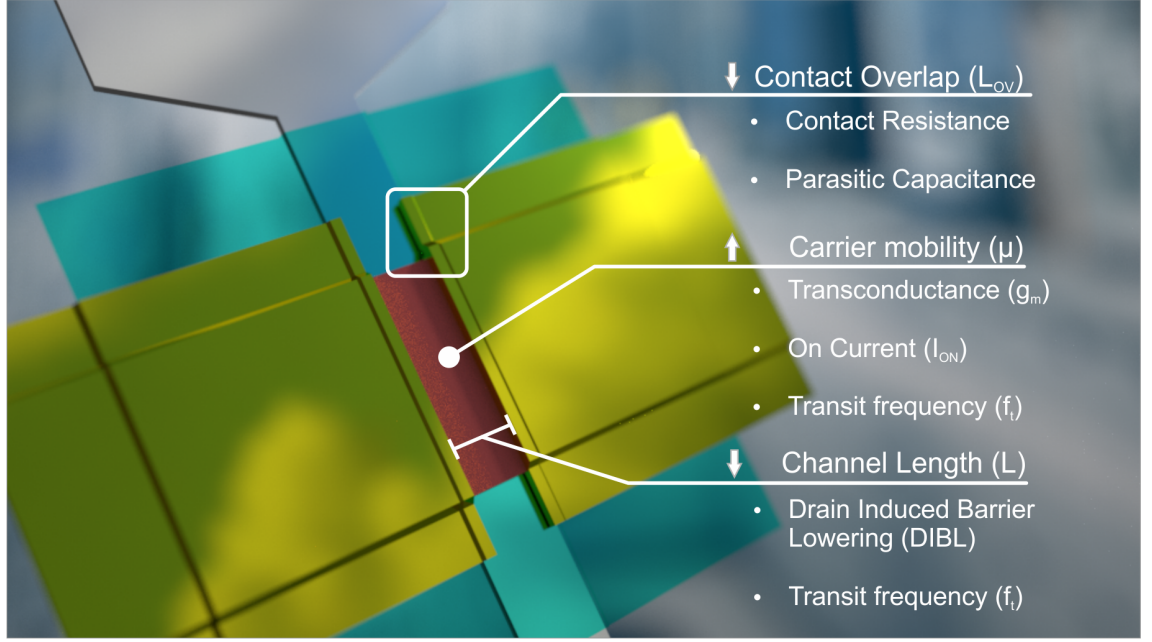


Figure 1.2: Illustration of a bottom gate staggered a-IGZO TFT. Some design parameters are highlighted along with their impact on the performance parameters of the device.

of 2.1 GHz [49]. This gigahertz operation was achieved by scaling down the channel length and thickness. However, it also required the use of a high-mobility InSnO (ITO) layer as thin as 5.6 nm and the usage of e-beam lithography, which is not compatible with large area manufacturing. More recently, a-IGZO has also been used to fabricate ultra-thin (3.6 nm) and short (38 nm) TFTs, which exhibited a μ_{FE} of $34.4 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and a S of 74.4 mV/dec [65]. However, in addition to having been fabricated on a rigid Si substrate the fabrication process still required e-beam lithography. Figure 1.2 displays some of the crucial parameters involved in improving the performance of existing flexible metal oxide TFTs for high-performance applications. The aforementioned reasons explain why metal oxides, and a-IGZO in particular, represent an attractive option for the development of high-performance flexible devices and circuits.

a-IGZO has already established itself as one of the leading contenders for the development of flexible thin-film transistors. For example, it has already been used in its crystalline form for the fabrication of LCD active matrixes by Sharp [66]. Simultaneously, its amorphous phase, with a significantly lower thermal budget, is emerging as a viable option for the development of smart tags and active cards. At the same time, given its relatively recent discovery - 2004 by Nomura et. al. [14], there are still many unanswered questions regarding its long-term stability or its resilience to adverse environmental conditions.

1.2.4 Flexible Electronic Circuits and Sensor Systems

The majority of commercially available flexible sensors are passive systems. Traditional force sensitive resistors fabricated on polymeric substrates are a good example of a common passive flexible sensor. These flexible sensors typically operate as simple signal acquisition elements controlled by a rigid circuit responsible for the whole signal processing and communication [67, 68, 30]. However, the reliance of traditional flexible sensors on rigid active components hinders their conformability. As such, it is important to devise flexible active elements to reduce their rigid footprint. In this context, flexible sensors should follow traditional rigid systems and incorporate not only the sensing elements but also on-site signal conditioning, power supply and signal communication. This could also result in devices with reduced noise levels since the flexible electronics could be placed closer to the signal source - e.g. brain-machine interfaces.

The advantages of a-IGZO over other semiconductors were presented in section 1.2.3. The presented performance parameters, combined with the fact that this material can be processed over large areas at temperatures below 150  C, result in an ideal candidate for the development of active flexible circuits. In reality, a plethora of examples of front-end conditioning circuits based on this material, such as voltage [69, 70], transimpedance [71], differential [57] and buffer amplifiers [72] have been demonstrated on flexible substrates. Complete flexible sensor systems such as magnetic sensors or resistively coupled electric potential sensors have also been demonstrated, showcasing the potential of these devices for the development of integrated flexible sensors [57, 70]. For example, a differential giant magnetoresistance (GMR) in a Wheatstone configuration combined with a flexible a-IGZO differential amplifier achieved a signal to noise ratio (SNR) of 56 dB. In addition, this device featured a TFT acting as an output stage and presented a total gain of 46 dB [57]. Regarding the electric potential sensor, Zulqarnain et al. [70] demonstrated a chopper amplifier implemented using a-IGZO for the on-site acquisition of a flexible heart rate sensor's signal. This device was operated with a minimal power consumption of only 0.052 mW and a noise level of 186.3  V. In comparison, similar systems built using a-Si had a power consumption of 11 mW [73]. Both systems required a resistively coupled interface i.e. wet electrodes placed in contact with the signal source. These examples highlight the interest of developing flexible based front-end conditioning circuits. Buffer amplifiers, coupled with voltage amplifiers and active filters have the potential to significantly increase the SNR of flexible sensors by placing the signal buffering, filtering and amplification as close to the signal source as possible. In comparison, when using rigid electronics, the

noise at the signal source can be further increased by any noise picked up during the transmission of the signal between the flexible sensor and the active rigid circuitry. In addition, interfacing flexible sensors using rigid elements is inherently complicated [74]. The rigid nature of contacts such as copper wires and metal clips damages the soft features of flexible sensors, leading to sheering, tearing and eventual failure of the contacts.

In addition to the front-end-conditioning of signals, flexible sensors can also incorporate power supplies, either in the form of a power transmission system e.g. using inductively couple coils [75] or in the form of self-powering options [76]. However, the vast majority of active flexible sensors in literature utilise external rigid power supplies. Power transmission utilising inductively coupled coils typically results in devices with larger areas due to the addition of the the coils to the substrate. Furthermore, the alignment of the coils in the power transmission system is crucial for the power efficiency of the system, and the misalignment between receiver and transmitter units is a well known issue in flexible systems [77]. At the same time, self-powering options are interesting since they allow for almost fully independent flexible sensors. However, these also require bespoke fabrication processes to integrate the power generating component as a part of the sensor, complicating their realisation [76]. This is an inherent issue of flexible electronics, in opposition to traditional rigid systems, modularity is highly complicated to achieve. These challenges extend to the signal transmission systems. Most flexible sensors are interfaced using metallic wires or clips, once again at the expense of reduced sensor durability. However, wireless communication systems on flexible substrates have already been developed, including NFC compatible systems [78] based on a-IGZO. These systems, while complex, promise to redefine the way in which flexible systems communicate. In summary, flexible circuits utilising metal oxides have been extensively studied and applied in various stages of flexible sensors. However, while this is true, currently available flexible sensors are not designed for long-term usage. For example, most biosensors still require resistively coupled interfaces to the signal source using e.g. wet electrodes, which results in a galvanic contact that can degrade over time. In addition, these sensor systems lack power and signal transmission capabilities. Moreover, most flexible sensor systems continue to be interfaced using traditional approaches such as copper wires. These constraints result in devices that are very dependant on external electronics, and which are only effective for short periods of time or as proofs-of-concept. In addition, the non-existence of a high-performance p-type metal oxide semiconductor fabricated at low temperatures and which demonstrates a stable response, μ_{FE} above $10\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, V_{th} around 0 V , and (I_{On}/I_{Off}) above 10^7 ,

further complicates the development of complex flexible circuits. At the same time, the first iterations of metal oxide based commercial products utilising active flexible circuits are already arriving, and the development of fully integrated systems is expected to increase as companies start building devices for specific applications, further pushing the boundaries of flexible electronics.

Chapter 2

Summary

This chapter provides an overview of this thesis as well as the main achievements that resulted from the PhDs applicant research work. To this end, the chapter starts by presenting the objectives of each main chapter, followed by the overall thesis outline, methods and overall research contribution.

2.1 Objectives

This thesis discusses the development and characterisation of flexible devices, sensors and circuits based on the amorphous oxide semiconductor a-IGZO. The first objective of this thesis is to understand the stability and resilience of a-IGZO based flexible transistors. To do this, it starts by discussing their practical longevity and evaluating the role of the passivation layer. This is followed by the study of the resilience of similar devices under extreme environmental conditions. The second main objective of this thesis is to understand how a-IGZO can be used to produce different flexible sensors and circuits. First, this thesis explores how this material can be used to easily fabricate low-cost and ubiquitous electronics. To do this, an almost entirely handwritten pressure sensor system is presented, including a printed diode based on a-IGZO. Second, a-IGZO is used to create a capacitive electric potential sensor. In this case, the objective is to show a flexible sensor capable of detecting electric potential signals through an encapsulation layer, eliminating a need for contact.

2.1.1 Stability and longevity of a-IGZO flexible transistors

As discussed in section [1.2.2](#), there is a plethora of available substrates, materials and fabrication techniques available for the realisation of flexible TFTs. However, while the

direct impacts of the various possible combinations in the immediate performance of the fabricated devices is well studied, there is still little knowledge regarding the long term performance of these same devices. In this context, this work aims to provide information into the fundamental practical longevity of one of the most well-known flexible TFTs used in the development of high-performance flexible electronic systems, a-IGZO TFTs. Here, the following research questions are discussed:

- What is the practical stability of a-IGZO TFTs?
- How effective is Al_2O_3 as a passivation layer?
- What are the main instability mechanisms present in a-IGZO TFTs after long-term storage?

2.1.2 Resilience of a-IGZO flexible transistors under extreme environmental conditions

Following the understanding of their baseline and long-term stability, the resilience of this technology for applications in extreme environments is assessed. This is motivated by the fact that flexible electronics are typically resilient and lightweight, which is advantageous for applications in extreme environments that require high mobility or have weight constraints. Examples of these are space missions, firefighting equipment or research gear in the Earth's poles. The produced research work aims to answer the following research questions:

- What are the effects of extreme environmental conditions such as cryogenic temperatures, high-energy electron irradiation and magnetic fields on otherwise stable flexible a-IGZO TFTs?
- Is there a compound degradation of a-IGZO TFTs after successive exposure to extreme environmental conditions?

2.1.3 Printed electronics on paper for cheap and ubiquitous flexible devices

Understanding the stability and performance of individual flexible TFTs is essential for the design of more complex systems. This was introduced in sections [1.2.4](#) and [1.2.2](#). As explained, a-IGZO can be deposited at low temperatures using large area compatible techniques, resulting in high-throughput and low-cost processes. In this context, it is

interesting to explore the limits of the low-cost applicability of this material by combining it with printing techniques and widely available materials such as graphite and metal inks. Furthermore, this thesis explores the formation of a Schottky contact between different metal inks and a-IGZO with the objective of producing partially printed diodes. This work aims to answer the following research questions:

- Can graphite, a-IGZO and metal inks be utilised to create electronic devices using a straightforward method?
- Can a-IGZO be used together with printed metals to create a Schottky diode?
- How to create easily customisable electronics that do not require specialised and expensive manufacturing equipment and facilities?

2.1.4 Towards a flexible electric potential sensor

Finally, as discussed in section 1.2.4, a-IGZO has tremendous potential to be implemented as the semiconductor in complex active circuits for the conditioning of flexible sensors. More specifically, this material could be used to fabricate one of the first flexible electric potential sensors able to measure signals through the substrate or encapsulation. This contrasts with the aforementioned systems that required a resistive coupling e.g. wet electrodes [70, 73]. This work then aims to answer the following research questions:

- How can one increase the input impedance of an a-IGZO based amplifier for capacitive applications?
- What are the current limitations of flexible electronics for the development of capacitively coupled electric potential sensors?

2.2 Thesis Outline

To address the research questions and complete the objectives presented in section 2.1 this thesis is divided into four separate research chapters corresponding to four peer-reviewed articles. Figure 2.1 provides a summary of the organisation of these chapters as well as the main research questions answered in each chapter. Chapter 3 presents a study regarding the long-term stability, or shelf-time, of a-IGZO based TFTs. To complement the knowledge acquired through Chapter 3, chapter 4 provides a new understanding on the resilience of these devices by studying the impacts of cryogenic temperatures, electron irradiation, magnetic fields and bending.

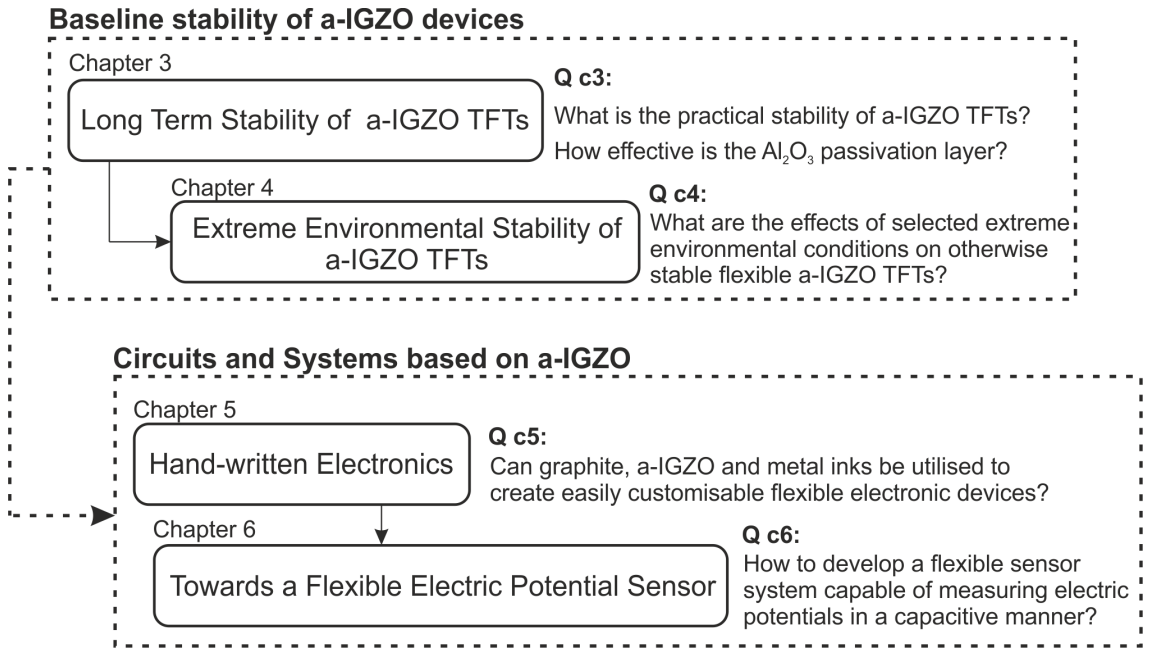


Figure 2.1: Schematic showing the organisation of the thesis and the main research questions for each chapter.

Following the two characterisation intensive chapters on the baseline stability of a-IGZO devices, chapter 5 demonstrates the work performed on the handwritten fabrication of devices, circuits and a pressure sensor system. Lastly, to explore the full potential of a-IGZO in high-performance flexible circuits, chapter 6 shows an active sensor system based on an a-IGZO buffer amplifier with a bootstrapped cascode input stage.

In summary, this thesis studies the impacts of various conditions, both standard and extreme, on a-IGZO TFTs, and broadens the scope of potential applications of these same flexible devices. In the end, a conclusion summarizing the contents of each chapter is presented, together with an overarching conclusion and outlook of the field of flexible electronics.

2.3 Research Articles

This section lists and presents the topics of the research articles incorporated in this thesis. In addition, it also contains a list of other research articles co-authored by the PhD applicant, some of which are highlighted in section 2.5 based on their relevance to the main work presented in this thesis.

Research articles included in the thesis**Chapter 3: Long-term aging of Al₂O₃ passivated and unpassivated flexible a-IGZO TFTs**

[1] - **Costa, Júlio C.**, Arash Pouryazdan, Giuseppe Cantarella, Luisa Petti, Christian Vogt, Alwin Daus, Stefan Knobelspies, Gerhard Troster and Niko Münzenrieder, "Long-term aging of Al₂O₃ passivated and unpassivated flexible a-IGZO TFTs". IEEE Transactions on Electron Devices (2020), vol. 67, 11, pages 4934 - 4939. DOI: 10.1109/TED.2020.3026613

Júlio C. Costa designed the characterisation, characterised and analysed the a-IGZO TFT devices after 80 months of storage. In addition, the author also re-analysed the data of the as-fabricated devices and wrote the research article.

Main topics

- Study the degradation of a-IGZO TFTs over 80 months of shelf-storage
- Understand the resilience to gate bias stress of aged devices
- Understand the impact of the passivation layer on the stability of such devices

[2] - **Chapter 4: Flexible IGZO TFTs and Their Suitability for Space Applications.**

Costa, Júlio C., Arash Pouryazdan, Julianna Panidi, Filippo Spina, Thomas D. Anthopoulos, Maciej O. Liedke, Christof Schneider, Andreas Wagner, and Niko Münzenrieder. "Flexible IGZO TFTs and Their Suitability for Space Applications." IEEE Journal of the Electron Devices Society 7 (2019): 1182-1190. DOI: 10.1109/JEDS.2019.2931614

Júlio C. Costa designed the experiments, characterised and analysed all data. With the exception of the electron irradiation, which took place in the Helmholtz-Zentrum Dresden-Rossendorf (HZDR), the author also performed all of the experiments and wrote the research article.

Main topics

- Understand the stability of a-IGZO TFTs in extreme environmental conditions

- Conditions included: electron irradiation, cryogenic temperatures, magnetic fields and bending

[3] - **Chapter 5: Hand-Drawn Resistors, Capacitors, Diodes, and Circuits for a Pressure Sensor System on Paper.**

Costa, Júlio C., Amir Wishahi, Arash Pouryazdan, Martin Nock, and Niko Münzenrieder. "Hand-Drawn Resistors, Capacitors, Diodes, and Circuits for a Pressure Sensor System on Paper." *Advanced Electronic Materials* 4, no. 5 (2018): 1700600. DOI: 10.1002/aelm.201700600

Júlio C. Costa designed the experiments, characterised and analysed all data, and wrote the research article. In addition, the author fabricated the resistors, capacitors and half-wave rectifiers. The sensor system, as well as the Schottky diode were also entirely fabricated by the thesis author.

Main topics

- Demonstrate a facile and low-cost method to fabricate electronic circuits
- Explore the Schottky barrier formed at the interface between a-IGZO and different metals to create printed diodes
- Demonstrate a sensor system almost entirely fabricated utilising an artisanal method

[4] - **Chapter 6: Flexible Bootstrapped Cascode System with Feedback for Capacitive Through Substrate Electric Potential Measurements with a 55 dB Relative Gain.**

Costa, Júlio C., Arash Pouryazdan, Robert J. Prance, Helen Prance, and Niko Münzenrieder. «Flexible Bootstrapped Cascode System with Feedback for Capacitive Through Substrate Electric Potential Measurements with a 55 dB Relative Gain” - Presented at IEDM 2020 and awaiting proceedings.

Júlio C. Costa designed the experiments, characterised and analysed all data, wrote the research article and performed the live presentation at IEDM 2020.

Main topics

- Demonstrate a device capable of measuring electric potentials through an encapsulating layer such as the substrate
- Study different biasing options to maximise the relative gain of the designed device

Review articles

In addition to the four main articles featured in this thesis. Júlio C. Costa also participated in the preparation of two large review articles in the field of flexible sensors and flexible transistors. Sections 1.2 and 2.4 are based on information written by the thesis author as part of these review articles.

[5] - **Costa, Júlio C.**, Filippo Spina, Pasindu Lugoda, Leonardo Garcia-Garcia, Daniel Roggen, and Niko Münzenrieder. "Flexible sensors—from materials to applications." *Technologies* 7, no. 2 (2019), 35. DOI: 10.3390/technologies7020035

Júlio C. Costa was responsible for the organisation of the chapters and management of the review content. In addition, the thesis author wrote the review section on materials for flexible sensors, as well the section on the flexible circuits. This review was featured in the cover of the respective journal edition and is show in appendix A.2.

[6] - Cantarella, Giuseppe, **Júlio Costa**, Tilo Meister, Koichi Ishida, Corrado Carta, Frank Ellinger, Paolo Luigi, Niko Münzenrieder and Luisa Petti, "Review of recent trends in metal oxide thin-film transistors for analog applications," *IOP, Flex. Print. Electron.* 5, 033001, (2020). DOI: 10.1088/2058-8585/aba79a

Júlio C. Costa wrote the section on high-performance flexible TFTs for analog applications.

Other research articles

The following articles include contributions from the author but are not included in this thesis.

[7] - Pouryazdan, Arash, **Júlio C. Costa**, Pasindu Lugoda, Robert J. Prance, Helen Prance and Niko Münzenrieder. "Flexible Micro-Scale Sensor Array for Non-Contact Electric Potential Imaging" In 2020 IEEE International Conference on Flexible and Printable Sensors and Systems (FLEPS). DOI: 10.1109/fleps49123.2020.9239593

[8] - Garcia-Garcia, Leonardo, **Júlio C. Costa**, Pasindu Lugoda, Daniel Roggen and Niko Münzenrieder, “Copper Wire Based Electrical Contacts for Direct Interfacing of Stretchable Sensors”, In 2020 IEEE Sensors. DOI: 10.1109/sensors47125.2020.9278749

[9] - Lugoda, Pasindu, **Júlio C. Costa**, Leonardo A. Garcia-Garcia, Arash Pouryazdan, Zygimantas Jocys, Filippo Spina, Jonathan Salvage, Daniel Roggen and Niko Münzenrieder “CocoStretch: Strain sensors based on natural coconut oil and carbon black filled elastomers” - Advanced Materials Technologies (2020), 2000780. DOI: 10.1002/admt.202000780

[10] - Lugoda, Pasindu, **Júlio C. Costa**, Arash Pouryazdan, Leonardo A. Garcia-Garcia, Daniel Roggen and Niko Münzenrieder “Evaluation of a Pseudo Zero-Potential Flexible Readout Circuit for Resistive Sensor Matrixes” ” In 2020 IEEE International Conference on Flexible and Printable Sensors and Systems (FLEPS). DOI: 10.1109/FLEPS49123.2020. 9239450

[11] - Lugoda, Pasindu, **Júlio C. Costa**, Carlos Oliveira, Leonardo A. Garcia-Garcia, Sanjula D. Wickramasinghe, Arash Pouryazdan, Daniel Roggen, Tilak Dias, and Niko Münzenrieder. ”Flexible Temperature Sensor Integration into E-Textiles Using Different Industrial Yarn Fabrication Processes.” Sensors 20, no. 1 (2020): 73. DOI: 10.3390/s20010073

[12] - Spina, Filippo, Arash Pouryazdan, **Júlio C. Costa**, Luis Ponce Cuspinera, and Niko Münzenrieder. ”Directly 3D-printed monolithic soft robotic gripper with liquid metal microchannels for tactile sensing.” Flexible and Printed Electronics 4, no. 3 (2019): 035001. DOI: 10.1088/2058-8585/ab3384

[13] - Spina, Filippo, **Júlio C. Costa**, and Niko Münzenrieder. ”Flexible IGZO thin-film transistors with liquid EGaln gate contacts.” In 2019 IEEE International Conference on Flexible and Printable Sensors and Systems (FLEPS), (2019). DOI: 10.1109/FLEPS.2019. 8792241

[14] - Münzenrieder, Niko, **Júlio Costa**, Luisa Petti, Giuseppe Cantarella, Tilo Meister, Koichi Ishida, Corrado Carta, and Frank Ellinger. ”Design of bendable high-frequency circuits based on short-channel InGaZnO TFTs.” In 2019 IEEE International Conference on Flexible and Printable Sensors and Systems (FLEPS), (2019). DOI: 10.1109/FLEPS.2019. 8792264

[15] - Pouryazdan, Arash, **Júlio C. Costa**, Robert J. Prance, Helen Prance, and Niko Münzenrieder. "Non-contact long range AC voltage measurement." In 2019 IEEE Sensors. DOI: 10.1109/sensors43011.2019.8956724

[16] - **Costa, Júlio C.**, Arash Pouryazdan, Julianna Panidi, Thomas Anthopoulos, Maciej O. Liedke, Christof Schneider, Andreas Wagner, and Niko Munzenrieder. "Low Temperature and Radiation Stability of Flexible IGZO TFTs and their Suitability for Space Applications." In 2018 48th European Solid-State Device Research Conference (ESSDERC), pp. 98-101. IEEE. DOI: 10.1109/ESSDERC.2018.8486889

[17] - bin Wan Zaidi, Wan Muhammad Hilmi, **Júlio Costa**, Arash Pouryazdan, Wan Fazlida Hanim Abdullah, and Niko Münzenrieder. "Flexible IGZO TFT SPICE model and design of active strain-compensation circuits for bendable active matrix arrays." IEEE Electron Device Letters 39, no. 9 (2018): 1314-1317. DOI: 10.1109/LED.2018.2854541

[18] - Münzenrieder, Niko, **Júlio Costa**, Giuseppe Cantarella, Christian Vogt, Luisa Petti, Alwin Daus, Stefan Knobelspies, and Gerhard Tröster. "Oxide thin-film electronics on carbon fiber reinforced polymer composite." IEEE Electron Device Letters 38, no. 8 (2017): 1043-1046. DOI: 10.1109/LED.2017.2720258

2.4 Methods¹

All the TFTs presented in this thesis follow a bottom-gate staggered architecture (Fig. 2.2). Generally, the process for the fabrication of these devices is initiated by the deposition of a SiN_x buffer layer between the polyimide substrate and the rest of the material stack. Here, SiN_x was deposited through Plasma Enhanced Chemical Vapour Deposition (PECVD) using an Oxford Instruments PECVD 80⁺ chamber. This deposition is followed by the deposition of the gate metal by techniques such as e-beam evaporation, filament thermal evaporation or DC sputtering. Here, the preferred technique was e-beam evaporation. This technique uses a controlled beam of electrons ejected by a filament in a vacuum chamber to heat and sublime metals placed in a crucible. It offers several advantages over other evaporation methods such as filament thermal evaporation at the expense of a slightly more complex and harder to optimise process. These advantages include the ability to deposit metals with very high melting points, such as Titanium, the ability to

¹This section was based on selected sections of the review papers [7, 8], which the PhD applicant authored and co-authored.

deposit alloys, or the ability to deposit metals that react with refractory metal boats, such as aluminium. The TFTs used on this work mainly utilised 35 nm thick Cr as the gate layer deposited using either a Univex 500 or a Plassys II e-beam evaporator. Furthermore, the gate metal features were patterned using wet-etch utilising a mixture of perchloric acid and ceric ammonium nitrate. For the patterning of the gate layers, standard positive photoresist AZ1518 from Microchemicals was patterned through photolithography utilising a gate mask. This mask differed for every device set. Wet-etch enables the formation of small and well defined features and is generally preferred when compared to other methods such as lift-off. However, wet etch can also easily damage any layers beneath the etched layer, and as such special care is required to prevent this. Following the deposition and patterning of the gate metal, the Al_2O_3 dielectric layer was fabricated by atomic layer deposition (ALD) at a temperature of 150 °C utilising water and Trimethylaluminum (TMA) as the precursors. Atomic layer deposition was chosen since it allows for the creation of very uniform and conformal coatings around irregular surfaces. This is important to ensure that the edges of the gate features on the bottom-gate TFTs were well insulated, thus decreasing any leakage current between the source-drain and the gate channel. The semiconductor a-IGZO was deposited through RF-sputtering at room temperature in a PVD Products magnetron sputtering chamber. This deposition was ran at 2 mtorr in a pure Ar atmosphere utilising a ceramic InGaZnO_4 target with an RF power of 75 W. Similarly to the gate layer, the semiconductor was patterned via wet etch, in this case via a $\text{HCl}:\text{H}_2\text{O}$ mixture. Before depositing the S/D contacts, vias were opened through the dielectric to the gate via wet etch utilising $\text{HNO}_3 : \text{H}_3\text{PO}_4 : \text{CH}_3\text{COOH} : \text{H}_2\text{O} = 1:25:5:5$. Finally, the S/D contacts were deposited by e-beam evaporation and patterned through lift-off. First, ma-N 1420 negative photoresist was deposited and patterned. Here, it is critical to slightly overdevelop the photoresist, since this will increase the undercut. This undercut is important since it reduces the chance of creating rough edges on the remaining metal track during lift-off. It is also advisable to deposit a photoresist thickness of at least 3 times the thickness of the subsequent metal layers. In this work, 10/60 nm Ti/Au S/D were deposited by e-beam evaporation (same process as for the gate). Because the thickness of the S/D is below 100 nm and the negative photoresist can be deposited with a thickness of $>1\text{ }\mu\text{m}$ the lift-off of this layer is easily viable and this process was chosen since it decreases the probability of damaging the semiconductor channel in comparison to both dry and wet etch. While processes such as wet and dry etch would allow for smaller gaps and devices, these could easily damage the surface of the semiconductor. For this

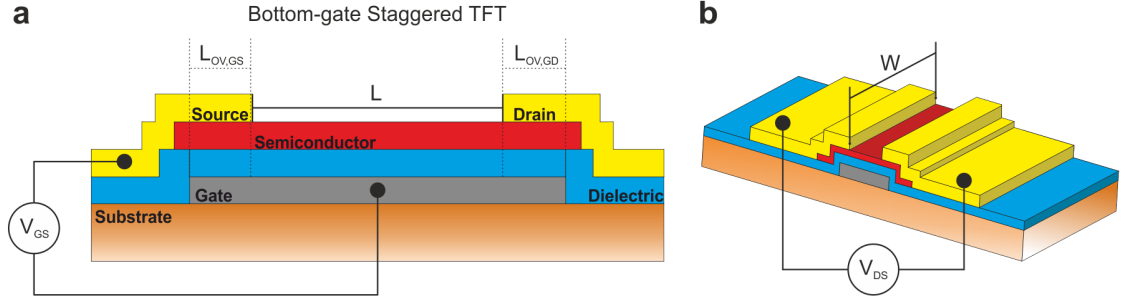


Figure 2.2: Schematic of a bottom-gate staggered TFT. a) Detailed schematic of the main layers and design parameters of a bottom-gate TFT. b) Bird's eye view of the top of bottom-gate TFT.

reason, it is common to find devices with etch-stop layers on top of the semiconductor precisely to protect the center of the channel during the wet etch of the S/D contacts. However, one of the challenges of utilising this layer involves the control of the effects of the additional deposition on the semiconductor channel [25]. Since the channel length of the devices utilised in this work is never below $8\text{ }\mu\text{m}$, lift-off offered a simpler and more effective approach. Finally, the devices were passivated utilising ALD deposited Al_2O_3 . Here, the deposition and vias to S/D and Gate layers were processed utilising the same methods as the gate dielectric. Chapter specific fabrication details are further given in the corresponding experimental sections.

Regarding the characterisation of the TFTs presented in this thesis, their DC performance is assessed by analysing their voltage-current characteristics and extracting various DC parameters. All the devices presented in this thesis were characterised in the dark. In addition, with the exception of the low temperature measurements in chapter 4, all transistors were characterised at room temperature and in standard atmosphere. Fig. 2.2 highlights some of the critical design parameters for a bottom-gate staggered TFT. The three most common current-voltage curves for TFTs are transfer and output curves, while C-V curves provide insights into the gate and overlap capacitance of the devices. Regarding the TFT transfer curves, these characterise the relation between the gate-source voltage and the drain current, allowing for the extraction of parameters such as the field-effect mobility (μ_{FE}), the threshold voltage (V_{th}), the ratio between the On and Off current (I_{On}/I_{Off}) or the subthreshold swing (S). Furthermore, depending on the applied voltage between the drain and source, the devices can be in the saturation ($V_{DS} \geq V_{GS} - V_{th}$) or linear regime ($V_{DS} \leq V_{GS} - V_{th}$). For the linear regime, the drain current can be approximated by the Shichman-Hodges model as [79]:

$$I_{D,lin} = \frac{W\mu C_{ox}}{L}(V_{GS} - V_{th})V_{DS} \quad for \quad V_{DS} \leq V_{GS} - V_{th}, \quad (2.1)$$

Here, W is the channel width, μ the charge carrier mobility, C_{ox} is the capacitance of the gate dielectric per unit area, L is the length of the semiconductor channel, and V_{GS} , V_{DS} and V_{th} are the gate-source, drain-source and threshold voltages, respectively. In the saturation regime the drain current can be approximated by:

$$I_{D,sat} = \frac{W\mu C_{ox}}{2L}(V_{GS} - V_{th})^2 \quad for \quad V_{DS} \geq V_{GS} - V_{th}. \quad (2.2)$$

Typically, W , L , and C_{ox} are previously defined fabrication parameters. As such, in order to extract the μ_{eff} , defined by μ in the saturation regime, one can apply a linear regression to the square root of I_D . The slope of the curve, i.e. its first derivative is then related to the μ_{eff} by equation 2.3. Its important to note that the while L is generally well defined and can be easily verified in simple planar devices, the W of devices is more prone to generate μ_{eff} quantification artifacts. This is especially true in devices where the semiconductor island extends outside the contact area, since this will then lead to a fringe conductivity that effectively increases the W of the devices. In this scenario, if one considers W as the width of the contacts, erroneously excluding the fringe conductivity, it will lead to an overestimation of the μ_{eff} . Furthermore, it can also be appropriate to utilise different models when working with devices which present e.g. considerable contact resistance [80]. Nevertheless, for most types of a-IGZO TFTs, and for comparative purposes, it is preferable to utilise the Shichman-Hodges FET model since it is widely accepted as an accurate model to extract parameters such as μ_{eff} and V_{th} [21]. Figure B.1 in chapter B shows an example of a linear fit on a standard device included in this work. This fitting yielded a R^2 value of 0.997, highlighting the good agreement between the model and the chosen TFT transfer curve profile.

$$\mu_{eff} = \frac{2L}{WC_{ox}} \left(\frac{d\sqrt{I_{D,sat}}}{dV_{GS}} \right)^2 \quad (2.3)$$

Together with μ_{eff} , the threshold voltage (V_{th}) of TFTs can also be assessed through the aforementioned linear regression. This value is generally taken from the linear extrapolation of $\sqrt{I_{D,sat}}$ vs. V_{GS} curve. This parameter corresponds to the V_{GS} point at which the channel becomes conductive. Furthermore, positive and negative V_{th} indicate enhancement and depletion type devices, respectively. These device types can serve different applications. Enhancement type devices are well suited for simple logic applications

that rely on Off-0 V and On-5 V states. In this case, high I_{ON}/I_{OFF} values are also required, whereas values $\geq 10^4$ are typically considered adequate for analog applications. At the same time, depletion type devices can be useful in applications such as current sources. V_{th} tends to be highly dependant on the fabrication parameters, since the doping of the semiconductor is influenced by factors such as Oxygen concentration during deposition, annealing temperatures and, in the case of sputtering, on the applied power and cleanliness of the chamber. Another parameter that is widely dependant on the fabrication process is the S of TFTs. This parameter indicates how fast a device shifts from the Off to the On state. Lower values are usually required and indicate a high quality semiconductor/dielectric interface. In contrast, high values are typically a result of trap states across the interface that become occupied/unoccupied slowly as the gate voltage increases. S is calculated by equation 2.4

$$S = \max \left(\frac{dV_{GS}}{d \log I_D} \right) \quad (2.4)$$

In addition to the parameters mentioned so far, the contact resistance (R_C) between the semiconductor and the source/drain electrodes is also of importance. This parameter is estimated using the transmission line method from the output curves of devices with different lengths. The contact resistance is especially important for short-channel TFTs, since the contact resistance can become a dominant factor and limit the driving current of the devices. This is generally observed in the transfer curve of TFTs by the appearance of a linear behavior when the device is in the saturation regime. Equally important is the overlap capacitance C_{ov} between the gate contact and the source/drain contacts as well as the semiconductor region. C_{ov} is calculated from the total gate capacitance $C_G = C_{GS} + C_{GD}$ extracted from the capacitance-voltage ($C - V$) characteristic curves [21]:

$$C_G = C_{ch} + C_{ov} = C_{ox}WL + C_{ov} = C_{ox}A_{ov,tot}, \quad (2.5)$$

Here, C_{ch} is the capacitance between the gate and the semiconductor channel, $A_{ov,tot}$ corresponds to the total overlap area between gate and the source, drain and semiconductor features. $A_{ov,tot}$ in particular depends on the channel length L . The total overlap $L_{ov,tot}$ between gate and source/drain contacts is given by:

$$L_{ov,tot} = L_{ov,GS} + L_{ov,GD}. \quad (2.6)$$

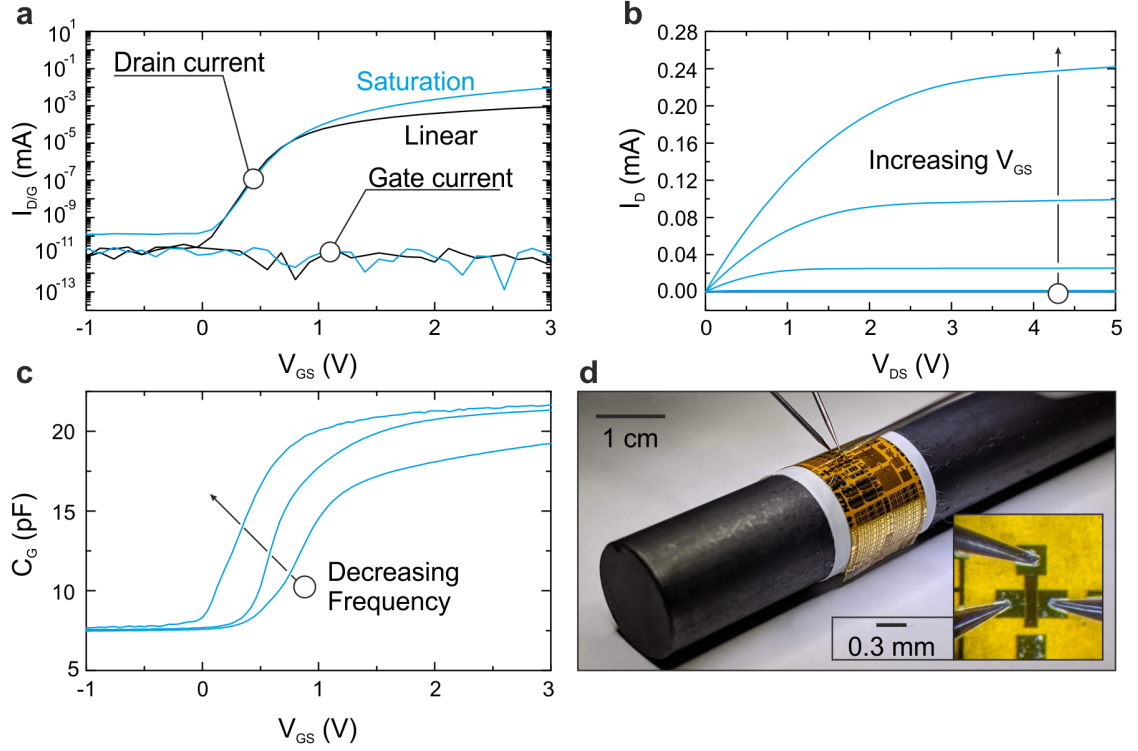


Figure 2.3: Representative curves of a typical a-IGZO flexible TFT. a) Transfer, b) output and c) capacitance curves obtained in the dark using a B1500 semiconductor parameter analyser. d) Micrographs of flexible a-IGZO devices. The transfer curves were extracted from [8]. The device represented in the TFT transfer and output curves has an oxide thickness of 25 nm, a channel length of 4 μm and width of 50 μm . Saturation and linear curves are extracted with $V_{DS} = 5\text{ V}$ and 0.1 V, respectively. These same values are utilised throughout the thesis.

The C_{ov} is an important parameter given that it limits the mobility, and hence the transconductance (g_m) of TFTs. The g_m corresponds to the relation between the change in V_{GS} and the resulting change in I_D . This value is calculated using equation 2.7 and is important for both the intrinsic gain and maximum frequency of operation of the TFT.

$$g_m = \frac{dI_D}{dV_{GS}} \quad (2.7)$$

All the aforementioned parameters are extracted from transfer, output and CV curves. These curves can be measured using specialised equipment such as parameter analysers. The characterisation of the devices presented in this work was carried out on a Keysight B1500 semiconductor parameter analyser. In addition, all devices were measured inside of a shielding box to minimise external noise sources. Figure 2.3 shows examples of transfer (fig. 2.3a), output (fig. 2.3b) and C-V (fig. 2.3c). In addition, figure 2.3d shows an

example of a set of flexible devices bent around a rod and connected to the parameter analyser through specialised probes. The inset shown in figure 2.3d presents a single device connected in the same manner.

2.5 Research Contribution

This section presents a summary of the PhD’s applicant research contribution to literature. In addition to the achievements from each main chapter, the work conducted by the PhD applicant on co-authored publications and which is of relevance to this thesis is also included. This summary includes achievements in the following topics: Stability and resilience of flexible TFTs and sensors; Alternative materials for the fabrication of flexible sensors; Novel flexible sensors and circuits for wearable applications.

2.5.1 Stability and resilience of flexible TFTs and sensors

On the stability and resilience of flexible TFTs and sensors, the work conducted in **Chapter 3** demonstrated that both passivated and unpassivated TFTs remain operational after 80 months of shelf-storage. However, contrarily to what was expected, the passivated devices appeared to be less stable under Positive Gate Bias Stress (PGBS). This is better exemplified by figures 2.4a and b. Figure 2.4a shows the transfer curves of a passivated a-IGZO flexible TFT before stress, after $V_{GS} = 10\text{ V}$ for 600 s stress, and after a recovery step of $V_{GS} = 0\text{ V}$ for 150 s. The same is shown for an unpassivated TFT in figure 2.4b. As demonstrated, a significant hump-effect was observed in the case of the passivated TFTs. This is explained by the formation of a back-channel caused by the degradation of the passivation layer. These results show that Al_2O_3 should not always be utilised as a standalone passivation layer in bottom-gate TFTs.

In terms of the resilience to extreme conditions of similar passivated a-IGZO TFTs, Chapter 4 demonstrates that these devices withstand high-energy 34.1 MeV electron irradiation with a density of $10^{12}\text{ e}^-/\text{cm}^2$. As shown in figure 2.5, the impact of high-energy electron irradiation on the performance of the TFTs is not significant. Furthermore, the flexible devices also remain operational at temperatures down to 78 K with an average decrease of 20 % for the μ_{FE} . This decrease, as well as the positive shift in V_{th} is most likely caused by the reduction in free charge carriers since a-IGZO is a thermally activated semiconductor material. It is also important to note that the bendability and circuit performance of a-IGZO TFTs is not affected by previous exposure to extreme conditions.

In addition to the previous two studies on the stability and resilience of flexible a-

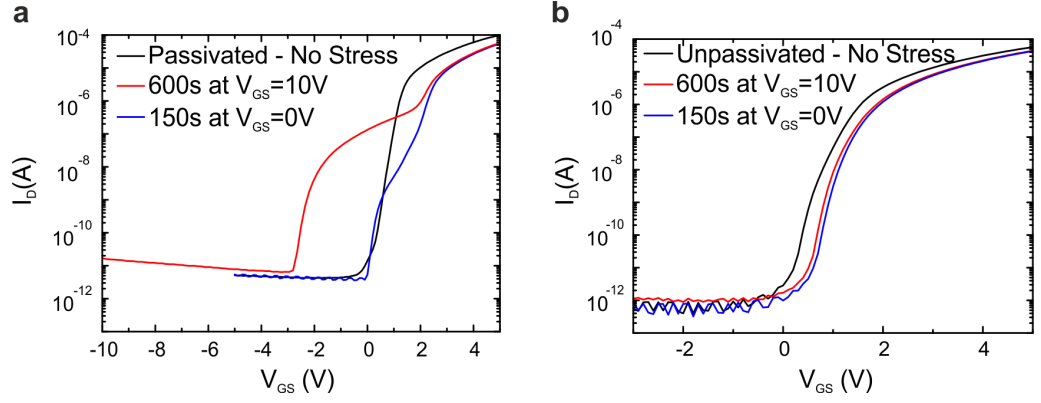


Figure 2.4: Positive gate bias stress and recovery of passivated (a) and unpassivated (b) flexible a-IGZO TFTs. The red curves correspond to the devices stressed with $V_{GS} = 10$ V for 600 s. The blue curves correspond to the relaxation step, where the devices were allowed to recover with $V_{GS} = 0$ V for 150 s before their transfer curve was measured again.

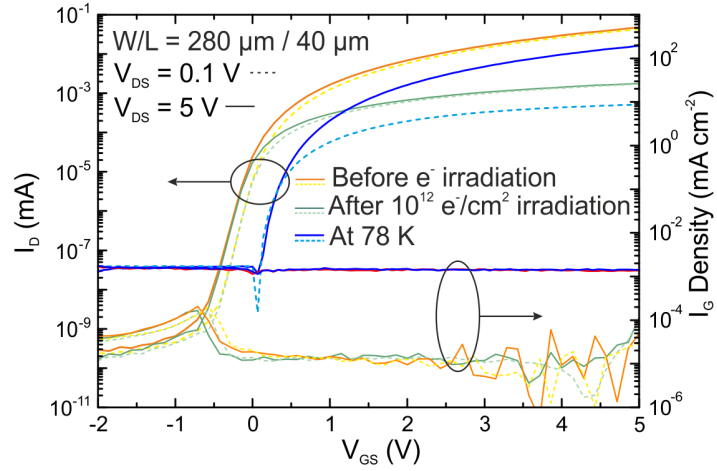


Figure 2.5: Evolution of the saturation and linear transfer curves for a transistor irradiated with the highest electron density, followed by exposure to 78 K. The increase in the leakage current is an artefact of the measurement setup and reflects the reduced current sensitivity of the source measurement unit utilised to characterise the TFTs at low T.

IGZO TFTs, the PhD applicant also worked on the study of the stability of rigid/flexible interfaces. In [74], the study of the stability of different types of copper wires for the addressing of stretchable strain sensors is presented. Figure 2.6 shows a representation of the performed test, as well as photographs of the individual contacts. In summary, the filament cable shown in figure 2.6 demonstrated the best all around performance. Using this type of contact, 50 cycles at 50% strain only led to a 10% drift in resistance with minimal hysteresis occurring on up to 75% strain. Furthermore, this type of contact was capable of withstanding a load of 1.47 N. In comparison, using the single wire resulted

in a rupture load of 0.34 N. This work highlights the importance of the contact choice for stretchable sensors. The rigid/soft interface is prone to break due to the mismatch between the mechanical properties of the two elements. In addition, hysteresis is also an issue since the stretchable material tends move in and out of contact with the wires or clips.

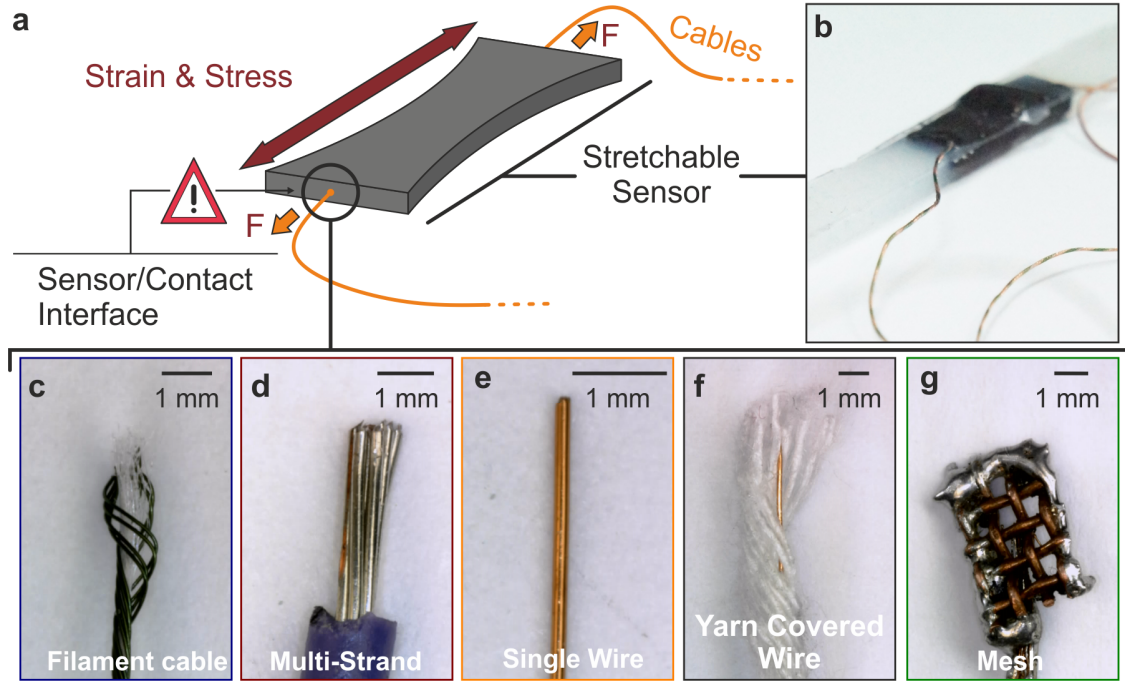


Figure 2.6: Different types of wires utilised to address a stretchable strain sensor. a) Schematic of the uniaxial strain applied to test the stability of each contact. b) Photograph of one of the studied sensors. c) Filament cable. d) Multi-strand cable. e) Single wire. f) Yarn covered wire. g) RFI electromagnetic shielding copper mesh with solder on the edges [74].

2.5.2 Alternative materials for the fabrication of flexible sensors

This section highlights the advances in the usage of alternative materials for the fabrication of flexible sensors. **Chapter 5** demonstrated the first handwritten Schottky diode on paper, which achieved a rectification ratio of 1:8. In addition, working circuits were fabricated by utilising standard graphite pencils, as well as Nickel (Ni) and Silver (Ag) pens. More importantly, a pressure sensor incorporating these materials, a handwritten Schottky diode and a rigid IC presented a linear behavior for applied pressures between 0.2 kPa and 1.2 kPa, with a sensitivity of 51 mV/kPa. This system is shown in fig. 2.7. This was also the first time that an off-the-shelf IC was embedded in a paper circuit utilising

handwritten metal tracks. This work shows that flexible sensors and basic circuits can be realised without the requirement for expensive and specialised manufacturing facilities.



Figure 2.7: Representation of the various devices fabricated using handwritten deposition of graphite and metal inks, as well as RF sputtered a-IGZO, on paper.

Another interesting material that can be utilised in the fabrication of stretchable sensors is coconut oil. In [81] the authors demonstrate that coconut oil can be utilised to disperse carbon black nanoparticles, allowing for the fabrication of a stretchable conductive material that uses Ecoflex as a structural matrix. In this application, coconut oil substitutes harmful solvents such as heptane or chloroform. Scanning electron microscope analysis indicates that the Ecoflex/Coconut oil mixture cures to form a porous structure filled with a conductive blend of coconut oil and carbon black (Figure 2.8). The semi-liquid nature of this sensor then results in devices with low hysteresis. More accurately, the sensors demonstrate a hysteresis of only 2.41 % at 200 % strain for 250 stretch/release cycles [81]. This work proved that coconut oil can effectively be used on the fabrication of stretchable sensors, leading to devices that are less harmful to nature. This work was featured as one of the covers of the respective journal edition (Fig. A.3) [81].

2.5.3 Novel flexible sensors and circuits for wearable applications

This section discusses two types of novel flexible sensors. First, in [82], the authors demonstrate a flexible resistive temperature sensor embedded inside a textile yarn. This is the first example of a fully flexible sensor embedded inside a yarn. This promises to combine the high-area fabrication and low-cost aspects of flexible sensors with high-throughput textile production. This smart yarn was then embedded in a sleeve and used to mon-

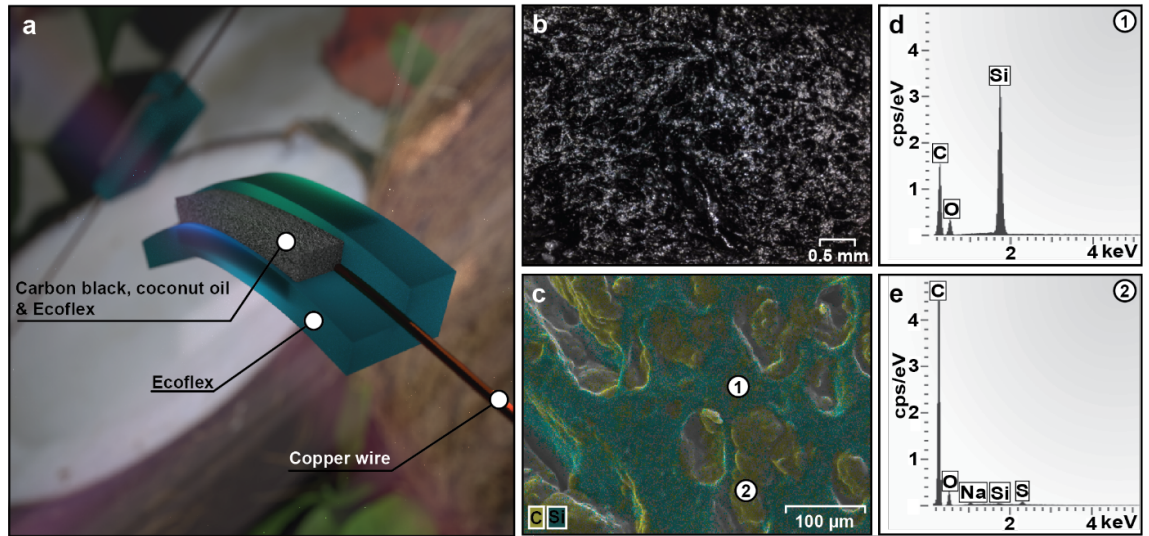


Figure 2.8: Stretchable strain sensor based on Ecoflex, Carbon Black and Coconut oil. a) Representation of the presented stretchable strain sensor. b) - e) SEM analysis of a cured Ecoflex/Carbon Black/Coconut oil based stretchable strain sensor. The green areas correspond to Silicon rich regions. The porous areas, in yellow, are rich in Carbon, indicating the presence of carbon black and coconut oil without Ecoflex [81].

itor a user’s physical activity by measuring the skin’s temperature. Figure 2.9 shows a representation, as well as photos, of the described smart-yarn. This sensor presented a sensitivity of $2.65 \times 10^{-3}/^{\circ}\text{C}$ when uncovered, compared to $2.58 \times 10^{-3}/^{\circ}\text{C}$ when covered utilising a double-cover yarn. Such sensors could be utilised for smart-wear applications such as smart socks capable of detection of early signs of diabetes-related foot ulcers or infection-monitoring bandages.

Finally, **Chapter 6** demonstrates a flexible sensor capable of measuring electric potentials through the thickest encapsulation yet in a flexible electric potential sensor - 50 μm thick polyimide (fig. 2.10). This showed that a bootstrapped cascode buffer amplifier with an active biasing element powered by the sensor’s feedback can effectively increase the input impedance of flexible electric potential sensors. Furthermore, the flexible electric potential sensor exhibited a relative gain of up to 55 dB with a power consumption of only 145 μW . This sensor represents a significant step towards the development of flexible electric potential sensors with potential applications in brain/machine interfaces, implant ECG sensors or smart health patches.

In summary, the work presented in this thesis provides important considerations regarding the stability of passivated and unpassivated flexible a-IGZO TFTs. It establishes that Al_2O_3 is not sufficient as a standalone passivation layer for most applications since

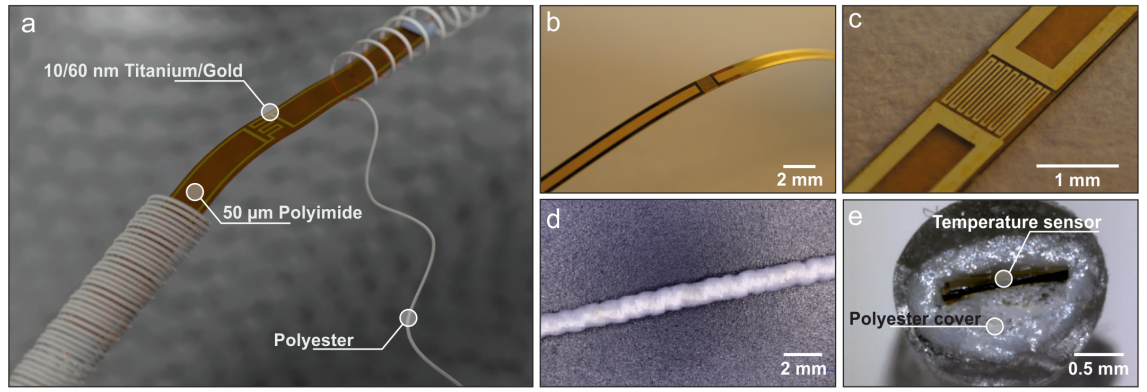


Figure 2.9: Flexible temperature sensor embedded in a textile yarn. a) Representation of the flexible sensor inside the polyester textile yarn. b) and c) Stand-alone flexible temperature sensor. c) Textile covered flexible temperature sensor. d) Cross-section of the smart-yarn.

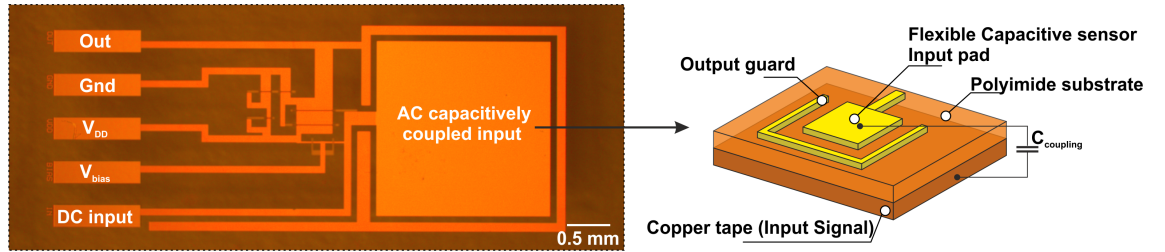


Figure 2.10: A flexible bootstrapped cascode buffer amplifier with an active biasing element for the through-substrate measurement of electric potentials.

there are indications that it degrades over time. This work also proved the resilience of a-IGZO when exposed to extreme environmental conditions, opening the path for various applications. Regarding the interface between stretchable electronics and rigid readout circuits, it is shown that the choice of the type of wire has a significant impact in the performance of the sensor. This work also demonstrates that thin-film sensors can be embedded inside yarns to create smart-textiles, and that a-IGZO can be combined with metal inks and graphite to create Schottky diodes and whole pressure sensor systems. Each of these devices advanced their respective fields by providing insights on how to make flexible electronics more accessible, affordable and customisable. Finally, a flexible capacitive electric potential sensor is demonstrated. Such a device could be utilised to measure biopotentials as a completely inert implant owing to the fact that it can be completely encapsulated. As a whole, this work provides insights on the durability and potential of flexible electronics, as well as some of the pressing challenges of moving this research topic to the real-world applications.

Chapter 3

Long Term Stability of amorphous InGaZnO Thin-Film-Transistors

Chapter 3 discusses the stability of passivated and unpassivated a-IGZO TFTs over long periods of storage under standard environmental conditions. This study is important due to the commercial potential of such devices and the necessity for their stable performance over time. This chapter has been published in IEEE Transactions in Electron Devices and corresponds to reference [83].

3.1 Introduction

Recent developments in flexible electronic technologies have opened the path towards truly unobtrusive and conformable electronics. This is important for the growing market of wearable devices since these allow for the development of electronic devices with new form factors for applications on curved and irregular surfaces [21, 84]. Among the available flexible technologies, amorphous oxide semiconductors have been widely researched due to a combination of advantages over other alternatives such as organic materials and amorphous-Si [14]. These advantages include higher mobility ($>10\text{ cm}^2/(\text{V s})$), large area fabrication compatibility, low temperature processing and stability under bending stress [85, 32, 86, 87]. The potential of amorphous Indium Gallium Zinc Oxide (a-IGZO) for the fabrication of large area and high density flexible electronics has already been shown through the development of active matrix displays, as well as highly conformable devices such as flexible biosensors, analog amplifiers and logic gates [88, 55, 89, 90, 91, 7]. Due to the usage of a-IGZO in commercial electronics [92], the study of its stability is of paramount importance. The impacts of illumination, humidity, positive and negative gate bias stress,

as well as bending, on a IGZO transistors have been extensively studied [93, 94, 95, 96, 97, 98, 99]. In this work, we study the impact of long term storage (80 months) under standard environmental conditions – room temperature, dark and exposed to air, on the performance of Al_2O_3 passivated and unpassivated flexible a IGZO thin film transistors (TFTs). This study is important since it offers a new perspective on the practical durability of potential a IGZO based products as well as on the performance of Al_2O_3 as a passivation layer over large periods of time. This is particularly important given that Al_2O_3 has been shown to be sensitive to corrosion by water and degrades after only 5 minutes when stored in a 38 °C and 90 % relative humidity (RH) environment [39, 40, 100]. In this work, the devices were exposed to standard environmental conditions, which typically equate to 25 °C and 40 % RH, for 80 months. After this period, the threshold voltage (V_{th}), field-effect mobility (μ_{FE}) and sub threshold swing (S) of the unpassivated transistors increased by 0.91 V, 23 % and 258 mV/dec, respectively. The same parameters changed by -0.03 V, 6.8 % and 114 mV/dec for the passivated devices, respectively. When exposed to positive gate bias stress (PGBS) immediately after fabrication, the passivated a-IGZO transistors showed a higher stability than their unpassivated counterparts. In contrast, after 80 months of storage, the transfer curves of passivated devices show an always On profile even for short PGBS times. In addition, both passivated and unpassivated devices demonstrate the appearance of a hump effect on their transfer curves after positive gate bias stress, although this effect is more pronounced on the passivated devices [101, 102].

3.2 Device fabrication

All a-IGZO TFTs were fabricated on a free standing 50 μm thick polyimide foil (Fig. 3.1). The fabrication details can be found in [32]. Here, we used 25 nm thick Al_2O_3 as the gate insulator. Al_2O_3 was always deposited through Atomic Layer Deposition at 150 °C to optimize TFT performance and minimize thermal stress on the substrate. The semiconductor channel consisted of RF-sputtered 15 nm thick a-IGZO deposited at room temperature. After contact deposition, this concluded the fabrication of the unpassivated devices (Fig. 3.1a). In the case of the passivated TFTs (Fig. 3.1b), a final 25 nm thick Al_2O_3 passivation layer was deposited since this material forms a low defect density interface with a-IGZO, acts as an efficient gas barrier, and promotes the stability of the devices [103, 104]. No annealing step was performed on the final devices. Fig. 3.1c shows a photograph of the transistors measured in this work. All devices were characterized in the dark using an HP4156A parameter analyser after fabrication and a Keysight B1500A

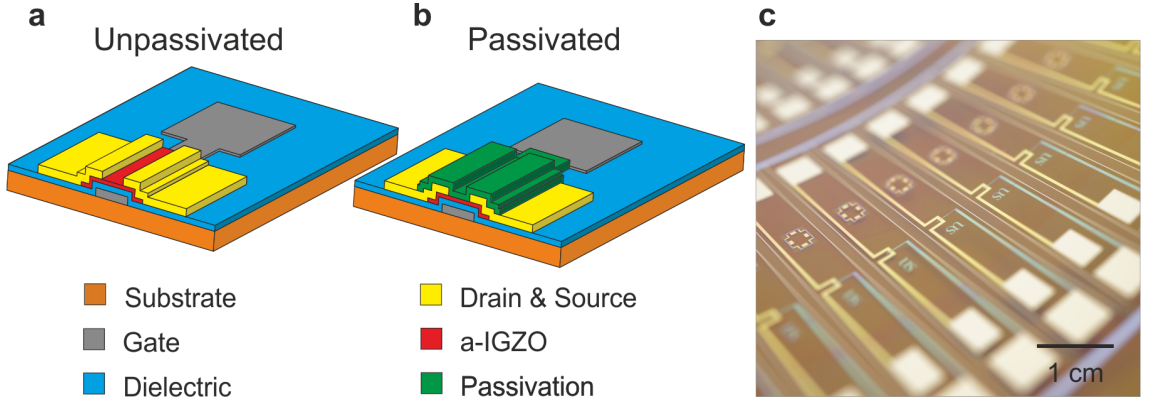


Figure 3.1: Structure of the passivated and unpassivated devices. Unpassivated (a) and passivated (b) staggered bottom gate amorphous InGaZnO thin film transistors. The only difference between devices is the Al_2O_3 passivation layer (green). c) Image of a substrate containing passivated InGaZnO thin film transistors. The passivated devices have seven different W/L ratios ranging from $280\text{ }\mu\text{m} / 215\text{ }\mu\text{m}$ ($6 \times 10^{-2}\text{ mm}^2$ WxL) to $500\text{ }\mu\text{m} / 10\text{ }\mu\text{m}$ ($5 \times 10^{-3}\text{ mm}^2$ WxL). The unpassivated devices have a W/L ratio of $280\text{ }\mu\text{m} / 115\text{ }\mu\text{m}$ ($3.2 \times 10^{-2}\text{ mm}^2$ WxL).

parameter analyser after 80 months. The V_{th} and μ_{FE} were extracted from the saturation regime of normalised and averaged transfer curves using the Shichman Hodges model [79]. The I_{ON}/I_{OFF} and S were extracted by calculating the $I_{D_{Max}}/I_{D_{Min}}$ ratio and taking the inverse of the maximum derivative of $\log(I_D)$ over V_{GS} , respectively.

3.3 Aging effects

To assess the impact of long term storage, the performance of various passivated and unpassivated TFTs was initially measured by extracting their transfer curves. Figure 3.2 shows the averaged transfer and output curves obtained from a total of 61 individual transistors. The shaded areas on the linear plots represent the standard deviation calculated during the averaging process. The corresponding performance parameters extracted from the saturation regions are given in Table 3.1. As shown in Fig. 3.2, the transistors remain operational after long term storage. Fig. 3.2a shows the evolution of the transfer curve of the passivated devices, whereas the same curves for the unpassivated TFTs are shown in Fig. 3.2c. Regarding the passivated devices, all their parameters remained virtually constant except for an increase in S . In contrast, both the V_{th} and μ_{FE} , as well as the S , increased for the unpassivated TFTs. Additionally, the maximum I_{ON}/I_{OFF} of the unpassivated devices is observed to have increased over time. However, this is most prob-

Parameter	Passivated		Unpassivated	
	Original	80 m. after	Original	80 m. after
V_{th} (V)	0.27	0.24	0.43	1.34
μ_{FE} (cm ² V ⁻¹ s ⁻¹)	11.8	11	7.7	10
I_{ON}/I_{OFF}	2×10^7	1×10^7	5×10^6	1×10^7
S (mV/dec)	131	245	115	373

Table 3.1: Parameter comparison after fabrication and after 80 months on shelf storage.

ably a result of the larger I_D at higher V_{GS} rather than an improvement of the channel, since the Off current is seen to be lower for the unpassivated devices immediately after fabrication.

While the relatively smaller parameter variation of the passivated devices indicates a larger stability over long periods of storage, a small hump was observed on the stored passivated TFTs' linear regime transfer curve and hints at a further degradation of these devices. The same was not evident in the unpassivated devices. This effect was absent on the saturation regime and did not significantly affect the On regime of the devices, as can be seen in the linear plot of the passivated devices shown in Fig. 3.2b. This effect does not seem to be explained by previously reported effects such as the accumulation of charges on the interface of the channel edges [105, 106]. On the other hand, Yang et.al [101] attributed a similar effect to hole trapping on the SiO_x etch stop layer of a IGZO TFTs when PGBS was applied at 75 °C, indicating that the layer deposited at the back of the channel can contribute to this effect. In this work, the hump effect is observed to be more severe for passivated devices when exposed to positive gate bias stress, hinting that the Al₂O₃ passivation layer plays a role in this degradation phenomenon. Here, all devices had active islands that extended a minimum of 75 µm outside the source/drain contacts. This effect might be related to the corrosion of Al₂O₃ due to the humidity present in the air, since it has been shown that Al₂O₃ is prone to degrade when exposed to water [39]. This degradation could be studied by investigating the density of OH bonds in the Al₂O₃ through FT-IR because the corrosion of Al₂O₃ typically results in the formation of OH groups [107]. However, since this characterization was not performed at the time of fabrication, it would not be possible to verify its evolution. Regarding the unpassivated devices, their saturation curve showed a linear behaviour instead of the expected quadratic relation between I_D and V_{GS} for V_{GS} values between 2 V and 3.5 V. This is shown in Fig. 3.2d and is possibly a result of the degradation of the drain/source contacts over the long

storage time period.

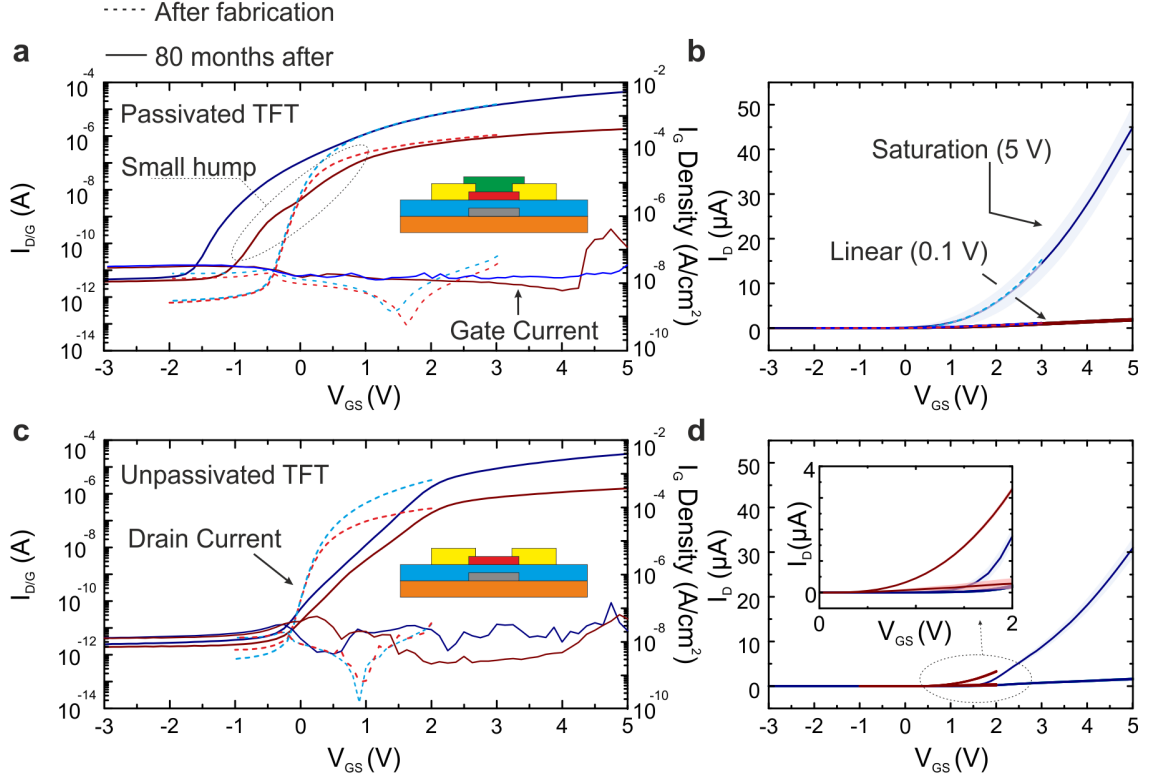


Figure 3.2: TFT characteristics obtained by averaging and normalizing the measurements from 45 passivated and 16 unpassivated devices. a) Transfer characteristic of 7 passivated TFTs measured after fabrication, and 38 devices after 80 months of shelf storage. b) Linear scale of (a). c) Transfer characteristics of 4 unpassivated TFTs measured after fabrication, and 12 TFTs after 80 months of shelf storage. d) Linear scale of (c). The shaded areas indicate the standard deviation of the individual measurements. The passivated devices have seven different W/L ratios: 280 μm / 215 μm , 280 μm / 115 μm , 280 μm / 75 μm , 280 μm / 35 μm , 280 μm / 15 μm , 280 μm / 10 μm and 500 μm / 10 μm . The unpassivated devices have a W/L ratio of 280 / 115. Here, V_{DS} in saturation (blue curves) = 5 V and V_{DS} linear (red curves) = 0.1 V. The corresponding fittings based on the Shichman-Hodges FET model can be found in C.1.

3.4 Positive Gate Bias Stress

To study the stability of these devices, the results of PGBS measurements of both passivated and unpassivated TFTs after fabrication were compared to their performance under PGBS after 80 months of storage. All measurements were conducted in the dark. Electrical fields ranging from 4×10^7 V/m ($V_{GS} = 1$ V) to 6×10^8 V/m ($V_{GS} = 15$ V) were

applied for a period of 600 s. Figures 3.3 and 3.4 show the transfer curves obtained for both unpassivated and passivated devices before and after PGBS with various electrical fields. New devices were used for each PGBS electric field measurement. In addition, to avoid effects caused by dimension mismatches between the passivated and unpassivated TFTs, all the stressed devices had a W/L ratio of 280/115 μm . The effects of PGBS on unpassivated TFTs immediately after fabrication are shown in Figs. 3.3a and 3.3b. These graphics show that the unpassivated devices exhibited a relatively stable response for small $4 \times 10^7 \text{ V/m}$ electric fields. However, for higher electrical fields ($2 \times 10^8 \text{ V/m}$), these devices exhibited an extreme negative V_{th} shift. In addition, for fields larger than $2 \times 10^8 \text{ V/m}$, the large negative shift did not allow the devices to turn Off at reasonable V_{GS} , and as such no measurements are shown. For comparison, the effects of PGBS on unpassivated devices after 80 months of storage are shown in Figs. 3.3c and 3.3d1. Contrarily to what was observed after fabrication, the unpassivated devices remained operational after both small and large electric fields when stressed after being 80 months of long term storage. On the other hand, a hump effect is observed on their characteristics after large electric fields PGBS ($4 \times 10^8 \text{ V/m}$) and its effect is highlighted in the linear plot of the same transfer curves (Fig. 3.3d2).

Regarding the passivated TFTs, Figs. 3.4a and 3.4b show that immediately after fabrication these devices showed a relatively stable response to PGBS. $4 \times 10^7 \text{ V/m}$ and $4 \times 10^8 \text{ V/m}$ stress electric fields resulted in small positive and negative V_{th} shifts, respectively. These asymmetric shifts can be attributed to electron trapping at low stress electric fields - leading to the initial positive threshold voltage sweep, and to the doping of the channel by hydrogen ions released by the impact ionization of OH bonds at the semiconductor/dielectric interface at higher stress voltages - negative shift. This is similar to the results presented in the next section regarding time dependent PGBS. Curiously, contrarily to the unpassivated TFTs, the passivated devices became less stable over time. After 80 months of storage both low - $4 \times 10^7 \text{ V/m}$ in Fig. 3.4c, and high - $4 \times 10^8 \text{ V/m}$ in Fig. 3.4d1, stress electric fields led to the appearance of a hump effect. In the worst case scenario, the hump effect led to a negative threshold voltage shift that reached a maximum of 7 V. In addition, two separate μ_{FE} regions were observed on the transfer characteristics of the passivated transistors stressed with gate fields above $4 \times 10^8 \text{ V/m}$ after 80 months of storage. For V_{GS} between -4 V and 2 V a low-mobility region can be observed. This is followed by a higher mobility region for V_{GS} between 2.5 V and 5 V . These two distinct mobility zones are observed in the device's transfer curve as the hump

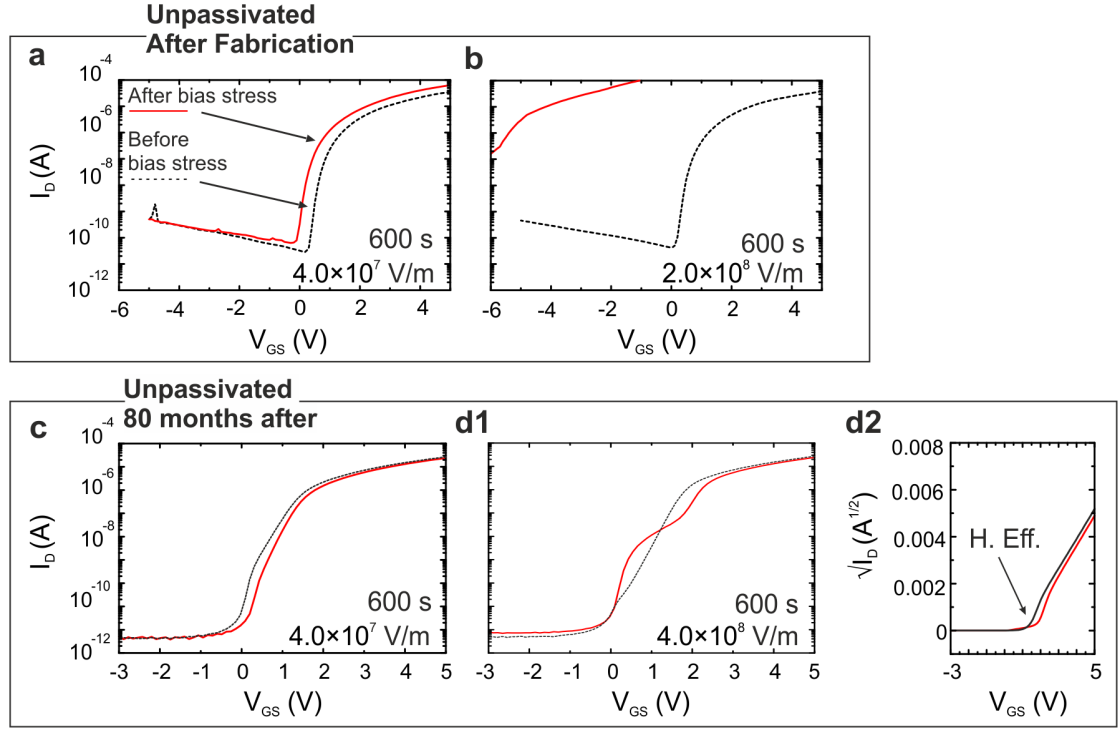


Figure 3.3: Positive gate bias stress representative transfer curves for unpassivated a-IGZO TFTs immediately after fabrication and after 80 months of shelf storage. All transfer curves were extracted with a constant $V_{DS} = 5$ V and the stress time was 600 s. a) and b) Effects of 4×10^7 V/m and 2×10^8 V/m PGBS on an unpassivated device immediately after fabrication. c) and d1) 4×10^7 V/m and 4×10^8 V/m PGBS applied on an unpassivated device after 80 months – d2) shows the linear scale of d1. For each PGBS electric field measurement a new device was used.

effect and are highlighted as μ_{FE} (1) and μ_{FE} (2) on the respective linear plot in Fig. 3.4d2. These two regions can be the result from a double-channel effect.

3.5 Time Dependent PGBS

To study the time dependent shift of the devices' transfer curves during PGBS, a gate voltage of 10 V was applied for up to 50 000 s (\approx .13.9 h) on both passivated and unpassivated transistors – figs. 3.5a and 3.5b, respectively. Representative transfer curves over the PGBS time are shown in figs. 3.5c and 3.5d. The transfer curves' shift was determined using the constant current method, which does not consider the hump effect because it only represents the shift of the V_{GS} value at which I_D was 4×10^{-6} A for a $V_{DS} = 5$ V. This value was chosen since it typically corresponded to the middle point of the hump effect observed in our measurements. It was thus the most reliable method to extract information

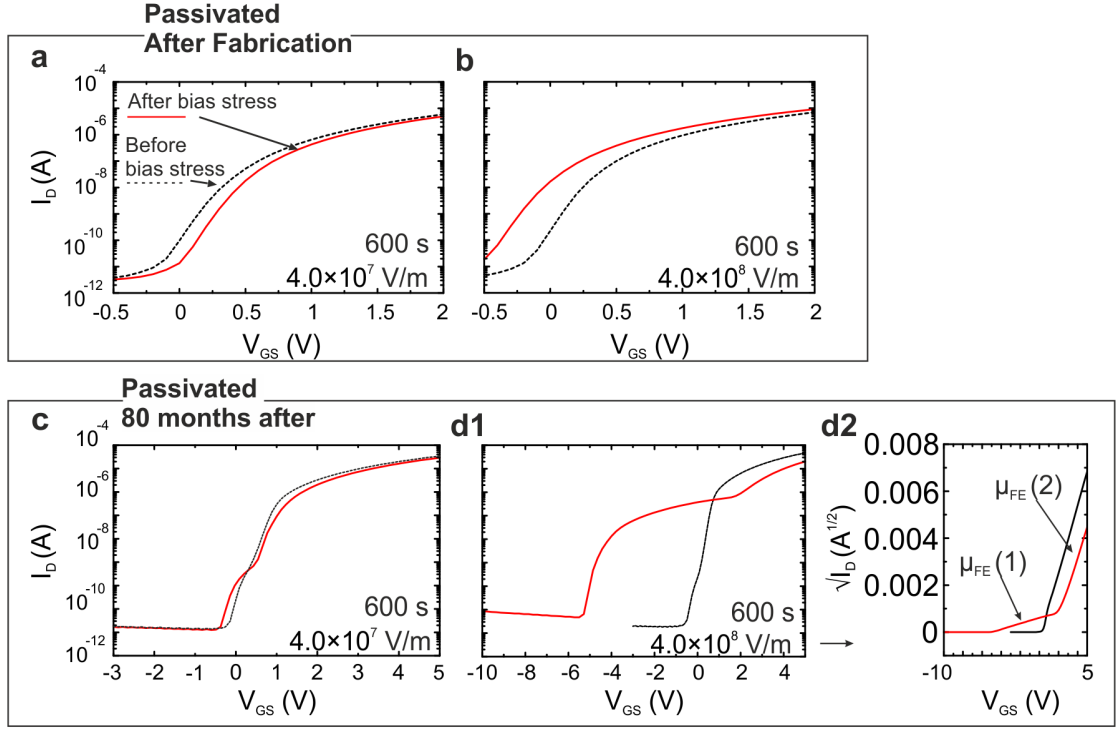


Figure 3.4: Positive gate bias stress representative transfer curves for passivated a-IGZO TFTs immediately after fabrication and after 80 months of shelf storage. All transfer curves were extracted with a constant $V_{DS} = 5$ V and the stress time was 600 s. a) and b) 4×10^7 V/m and 4×10^8 V/m PGBS applied on a passivated device immediately after fabrication. g) and d1) 4×10^7 V/m and 4×10^8 V/m PGBS applied on a passivated device after 80 months - d2) shows the linear scale of d1. For each PGBS electric field measurement a new device was used.

regarding the shift of the transfer curves, as other methods, such as extracting it at the point of maximum transconductance, would only yield information about the shift of the fully On state. Furthermore, while this method allowed the extraction of an approximated value of V_{th} for the unpassivated devices due to the absence of a pronounced hump effect, the same is not true for the passivated TFTs. For this reason, the transfer curve shift for the passivated TFTs is described as $V_{GS}@I_D=4\mu A$ to clarify that this does not represent the real V_{th} due to the acute distortion of their transfer curves. Both unpassivated and passivated transistors present initially positive V_{th} and $V_{GS}@I_D=4\mu A$ shifts, respectively. This initial increase follows a known stretched exponential trend as presented in Equation 3.1, accounting for the trapping of the electrons at the semiconductor/dielectric interface [98, 108, 109]. Here, ΔV_{+Max} is the maximum positive threshold voltage shift for an infinite stress time, τ represents the characteristic trapping time of carriers and β represents

the fitting coefficient [109]:

$$\Delta V_{th}(t) = \Delta V_{+Max} \left\{ 1 - e^{-\left(\frac{t}{\tau}\right)^\beta} \right\} \quad (3.1)$$

As the stress time increases, both $V_{GS}@I_D=4\mu A$ (passivated) and V_{th} (unpassivated) devices starts to shift in the negative direction. This phenomenon has been attributed to e^- doping of the semiconductor layer caused by hydrogen diffusion originating from the Al_2O_3 gate dielectric. Hydrogen is created through the severing of the OH bonds at the semiconductor/dielectric interface by electrons injected into the dielectric due to the gate biasing stress, and then drift and react with oxygen vacancies in the semiconductor to generate free carriers [110, 111, 112]. ALD Al_2O_3 thin films are known to contain trapped hydrogen. Helium elastic recoil detection (He-ERD) measurements of our TFTs showed a hydrogen content of 7% (H/O ratio) in the Al_2O_3 [113]. The presence of hydrogen and its drift into the semiconductor can help explain the observed parameter shifts. Previous work conducted by Chang et. al. proposed a modified equation which took into account the breakage of AlO-H bonds by the high energy channel electrons and the subsequent drift of the hydrogen atoms [111]:

$$\Delta V_{th}(t) = \Delta V_{-Max} \left\{ \frac{1}{1 + \left(\frac{t}{\tau_H}\right)^{-\alpha}} \right\} \quad (3.2)$$

In Equation 3.2, ΔV_{-Max} is the maximum negative threshold voltage shift for an infinite stress time, τ_H represents the characteristic time of hydrogen release and α is inversely proportional to the spread of the dissociation energy (σ) of the AlO-H bonds ($\alpha = kT/\sigma$). In the case of the unpassivated devices, the threshold voltage shift could be fitted across the entire time span using an equation resulting from the sum of (1) and (2) [36]. This results on a ΔV_{+Max} , τ and β of 0.3 V, 2.5×10^3 s and 0.31, respectively, as well as a ΔV_{-Max} , τ_H and α of -1.2 V, 3.2×10^4 s and 1.16, respectively. This leads to a spread of the dissociation energy of 0.022 eV. These parameters are similar to results obtained from other bottom gate top contact a-IGZO TFTs and σ is about 5 times smaller than the values reported by Chang et al [111].

While the dissociation energy is a result of a parametric fit and as such can be liable to fluctuation, the usage of the same gate stress voltage as [111], associated with a behavior that closely follows the electron trap-Hydrogen release model, as can be seen from the fitting in Fig. 3.5b, indicates that the electrons injected into the gate dielectric during gate stress may have sufficient energy to break the OH bonds. Regarding the passivated devices, an aggravation of the hump effect was observed over the PGBS time. Addition-

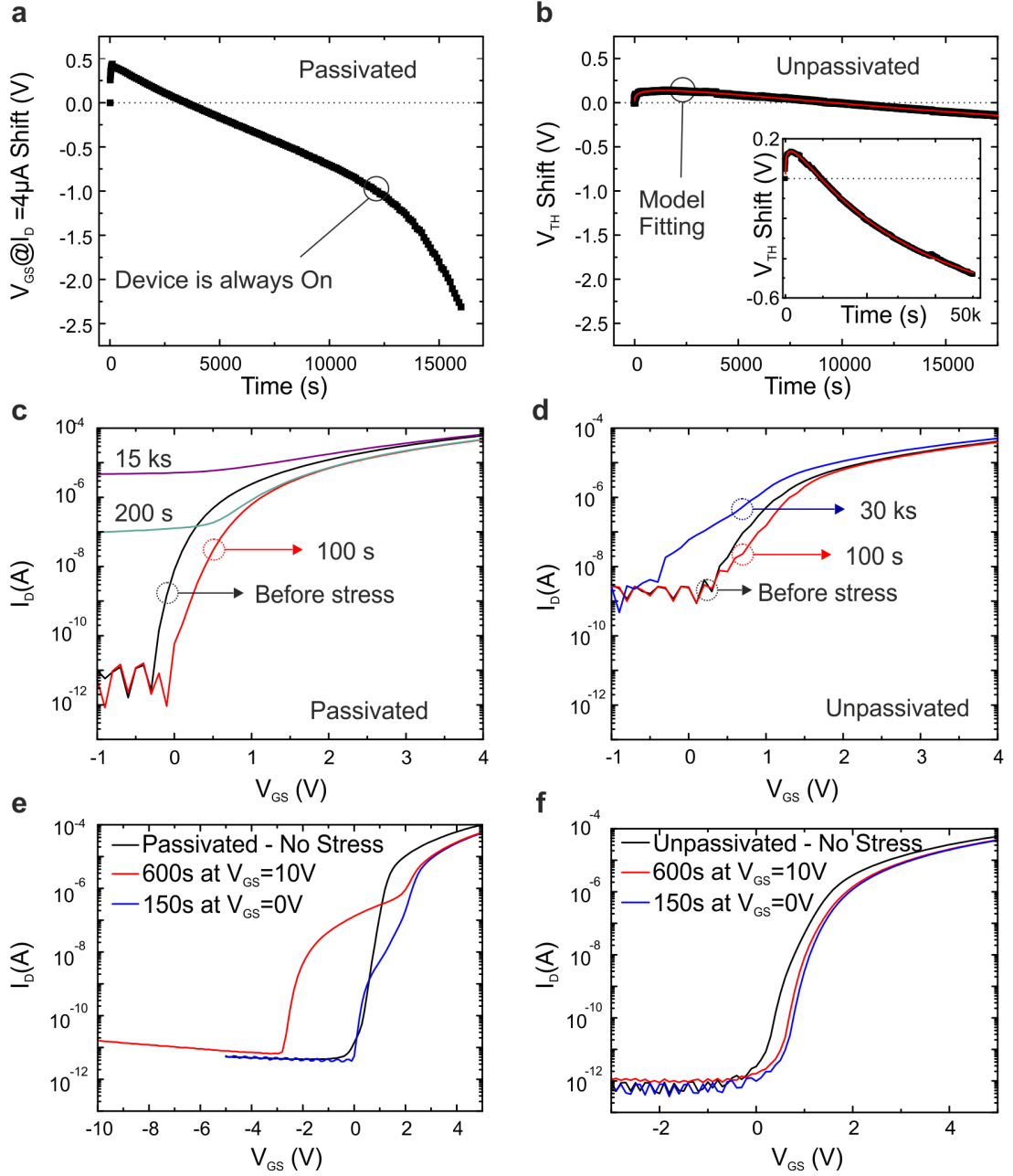


Figure 3.5: PGBS over a 50 000 s period with a gate voltage of 10 V (4×10^8 V/m). Each measurement was performed using a V_{GS} sweep from -1 V to 4 V and a $V_{DS} = 5$ V. a) and b) $V_{GS}@I_D=4\mu\text{A}$ and V_{th} over the PGBS time for a passivated and unpassivated device, respectively. Inset of b) V_{th} shift over the PGBS full time span for the unpassivated device. c) and d) Representative transfer curves of a passivated and unpassivated 280 μm / 115 μm TFT, respectively. e) and f) Stress and recovery at $V_{GS} = 0$ V of a passivated and unpassivated TFT.

ally, after a relatively short time, a fast transition to an always On state is clearly seen in fig. 3.5c. The same was not observed on the unpassivated devices (fig. 3.5d). After this

point, the fitting using the sum of Eq. 3.1 and 3.2 was not possible because the transfer curves ceased to demonstrate clear On and Off states in the sweeping range. Furthermore, while the sum of Eq. 3.1 and 3.2 could describe the behavior of $V_{GS}@I_D=4\mu A$ up to 5 ks stress times, the distortion of the curve due to the hump effect complicates the meaningful and reliable extraction of the fitting parameters. After 1.6×10^4 s no measurements are shown for the passivated devices since they did not turn off anymore. It is worth mentioning that although the subthreshold swing of the devices degraded over time, the initial positive shift observed for both passivated and unpassivated TFTs under PGBS presents a similar behavior to newly fabricated devices, which indicates that the dielectric was not significantly affected. Furthermore, while a 0 V V_{GS} for 150 s recovery step was seen to mitigate the hump effect on passivated devices stressed for 600 s with a $V_{GS} = 10$ V, this effect persisted. These results can be seen in fig. 3.5e. Unpassivated devices exposed to the same conditions demonstrated a higher stability and a smaller effect by the recovery step (fig. 4f). Both devices also showed a reduction in I_D at $V_{GS}=V_{DS}= 5$ V even after the recovery step, this is probably due to a lingering positive threshold voltage shift caused by the longer time that is required for the dielectric trapped charges to recover.

The presented results indicate that while hydrogen doping competes with electron trapping for the resulting threshold voltage shift on both types of devices, there is an additional instability mechanism caused by the passivation layer, potentially through the creation of a back-channel. In addition, the attenuation of the left shift of the passivated TFTs' hump effect after the recovery step as seen in Fig. 3.5e suggests that this is due to the formation of trap states. These results suggest that while Al_2O_3 is an excellent dielectric and passivation material after deposition, there is some degradation of its stability over time. Given the importance and ubiquitous usage of Al_2O_3 as a gate dielectric/passivation layer, future work should look into the density of states (DOS) of the semiconductor film in order to further clarify the origin of this hump effect [114]. The DOS measurements could be done in conjunction with the fabrication of a secondary back-gate in the passivated devices which would serve to analyse the presence and influence of the back-channel. Increasing the temperature of the Al_2O_3 deposition up to 250  C typically results in denser, higher quality films with optimal properties. This could lead to an improved resistance to water corrosion by reducing the diffusion of water into the Al_2O_3 film. Nevertheless, 250  C is too high for most flexible substrates. On the other hand, TiO_2/Al_2O_3 , HfO_2/Al_2O_3 and polymer/ Al_2O_3 multilayer stacks have also demonstrated superior performance in terms of reliability when compared to single Al_2O_3 layers [39, 40, 41]. These approaches could be

implemented to develop a-IGZO devices and circuits stable over longer shelf time storage periods.

3.6 Conclusion

In this work, the electrical characteristics of passivated and unpassivated a-IGZO TFTs characterized immediately after fabrication and after 80 months of shelf storage were compared to evaluate the long term stability of these devices. It was found that both passivated and unpassivated devices are affected by instabilities related to long term environment exposure. The Passivated TFTs demonstrate a more stable response under transient biasing conditions such as when extracting their transfer curve. In contrast, the baseline parameters of the unpassivated TFTs, namely the V_{th} and the S presented larger variations over the 80 months periods. However, contrarily to what was expected, the aged devices passivated with an Al_2O_3 layer were less resistant to the influence of positive gate bias stress. The more distinct degradation was evident by the appearance of an acute hump effect after PGBS of the passivated devices when compared to their unpassivated counterparts. The presented data indicates that the hump effect is related to the passivation layer. These results indicate that over long periods of time, while interface between Al_2O_3 and a-IGZO deteriorates. Nevertheless, Al_2O_3 is still effective as a capping layer, evidenced by the reduced parameter variation over the 80 months period. This is particularly important given that such effects could be highly disruptive for long term operation instead of long term storage scenarios, so new passivation alternatives should be investigated to prevent the degradation of such systems over long periods of time.

Chapter 4

Stability of amorphous InGaZnO Thin-Film-Transistors under Extreme Environmental Conditions

Chapter 4 discusses the resilience of a-IGZO TFTs under extreme environmental conditions. The effects of high-energy electron irradiation, cryogenic temperatures, magnetic fields and bending on flexible a-IGZO TFTs are studied. This work provides insights on the potential of this technology for applications that require both resilient and lightweight electronics, such as space applications. Part of the contents of this chapter were presented at ESSDERC/ESSIRC 2018 [115] and later as an extended version corresponding to this chapter in IEEE Journal of the Electron Devices Society [116].

4.1 Introduction

The development of electronic devices for space applications is a widely researched topic since the beginning of the space age. Due to the extreme conditions present outside the Earth's atmosphere, specialized electronic equipment and shielding are required to make these devices capable of withstanding conditions such as large temperature variations, or constant doses of radiation. As an example, special considerations have to be taken when developing instrumentation for the International Space Station, as it regularly passes through the South Atlantic Anomaly (SAA) [117]. This area is characterised by an increase in radiation and energized charged particles due to the weak local geomagnetic field - in

particular, the flux of energized electrons (energies up to 5 MeV) can reach $10^6 \text{ e}^-/\text{cm}^2\text{s}$ [118, 119]. The interaction between these electrons and electronic systems causes failures due to ionization effects and atomic displacements in the bulk of semiconductors, which has been prevented by the implementation of bulky shielding structures. As space travels become more common and more sensors are used to ensure the astronauts' safety, the development of lightweight and robust electronic devices is required. In this context, flexible electronics are a viable option for the development of future space suits. Fig. 4.1 shows a vision for spacesuit integrated textile electronics. Various materials compatible with thin film technologies have been tested for space applications, including organic semiconductors such as pentacene and hydrogenated amorphous silicon (a-Si:H). However, organic materials were observed to be unstable in conditions similar to the ones found in space [120]. Simultaneously, a-Si:H presents a stable response under outer space conditions but has a relatively low mobility ($\approx 1 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$) [121]. For these reasons, alternative materials compatible with flexible technologies should be studied for space applications. Amorphous oxide materials such as Indium Gallium Zinc Oxide (a-IGZO) [14] are adequate candidates for the development of conformable and lightweight, yet high performance, sensor systems [21]. Additionally, its amorphous phase improves its radiation hardness since there is no crystalline structure to be damaged. To apply this semiconductor to space wearable applications, its suitability and stability must be assessed. While the electric stability of amorphous oxide semiconductor devices represents an open research question, this topic is also widely studied by numerous groups [122, 123]. Similarly, the mechanical stability of a-IGZO has already been extensively studied by demonstrating outstanding bending stability down to $25 \mu\text{m}$ bending radii [34, 88, 55, 91]. However, additional potential deterioration mechanisms including low temperature, magnetic field and electron irradiation stress are equally important for space applications.

Previously, it was shown that rigid a-IGZO transistors continue to operate after being exposed to relatively low energetic electron irradiation (0.8 MeV , $10^{14} \text{ e}^-/\text{cm}^2$) [124]. Nevertheless, the employed bulky and rigid substrates can shield and interact with the semiconductor channel [125, 126]. Simultaneously, the electrons in the SAA are more energetic. Hence, these results cannot be used to predict the response of devices on thin flexible polymeric substrates. Furthermore, in order to preserve conformability, flexible a-IGZO TFT based systems cannot be shielded with bulky glass or lead encapsulations. Similarly, it is known that a-IGZO can function at low temperatures, more specifically, a-IGZO TFTs on glass were shown to remain operational down to 10 K [127]. However,

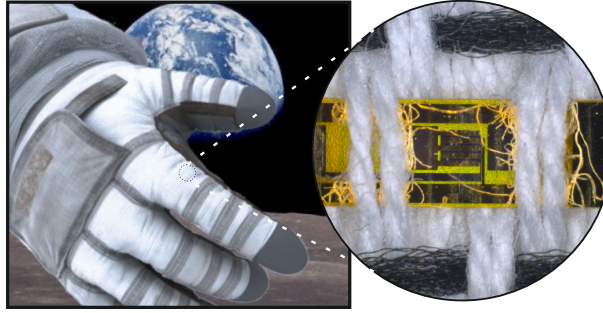


Figure 4.1: Concept of an a-IGZO circuit incorporated into a spacesuit. This material could be used for the development of unobtrusive sensor systems that measure e.g. temperature and radiation.

due to the larger thermal expansion of deformable polymer foils (20×10^{-6}) [128] compared to rigid substrates such as glass (-1×10^{-6}) [129] at cryogenic temperatures, it is necessary to characterize the temperature stability of flexible a-IGZO thin film transistors (TFTs) [130]. In addition, a-IGZO TFTs on glass have also been shown to present a magnetoresistive effect [131]. This effect was attributed to the properties of the employed gate insulator materials. More specifically, it was proposed that using SiO_x or SiN_x led to a magnetoresistive effect arising from the paramagnetic and diamagnetic properties of oxygen and nitrogen, respectively [131]. Al_2O_3 is another dielectric which is commonly employed as a gate insulator in a-IGZO TFTs due to the high-quality interface between the two materials. However, until now it was not clear if Al_2O_3 has the same effect as SiN_x or SiO_x . Therefore, in this work, we assess the performance of flexible a-IGZO TFTs that use Al_2O_3 as the gate insulator under various magnetic fields.

Here, the effects of four separate stressing conditions on the electrical characteristics of flexible a-IGZO transistors are assessed. Initially, they are characterised before and after exposure to electrons with an energy of 34.1 MeV and electron fluences spanning 6 orders of magnitude. Afterwards, the devices were characterised at temperatures down to 78 K, which is below the minimum temperature measured for shaded objects in Low Earth Orbit (LEO) [132]. The operation of these devices when exposed to magnetic fields up to 11 mT was then studied, and finally the same devices were tested under bending stress. It is demonstrated that these flexible devices remained fully operational and were not significantly affected after being irradiated by 34.1 MeV electrons with an electron density of $10^{12} \text{ e}^-/\text{cm}^2$, followed by the exposure to 78 K and also under the influence of magnetic fields. These measurements simulate a 278 h spacewalk above the South Atlantic Anomaly,

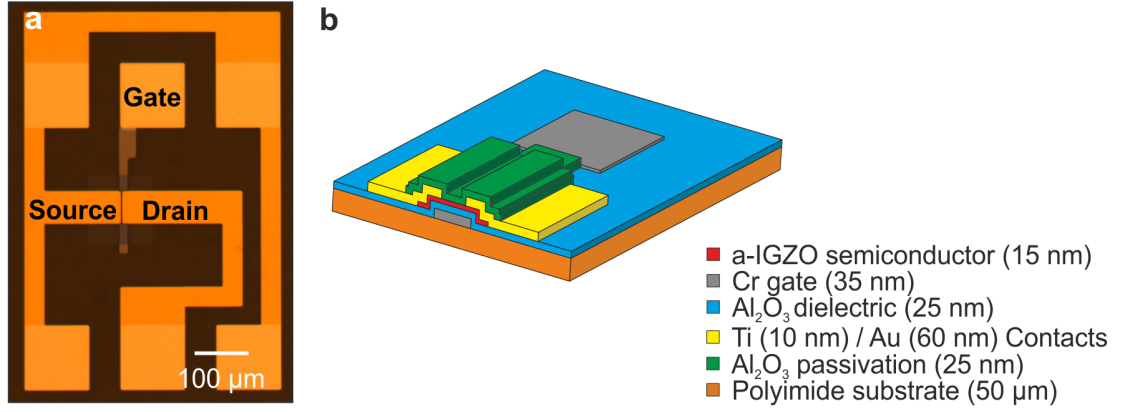


Figure 4.2: a-IGZO TFT stack structure studied under extreme environmental conditions. a) Micrograph of the transistors studied in this work. b) Schematic of the staggered bottom gate transistors.

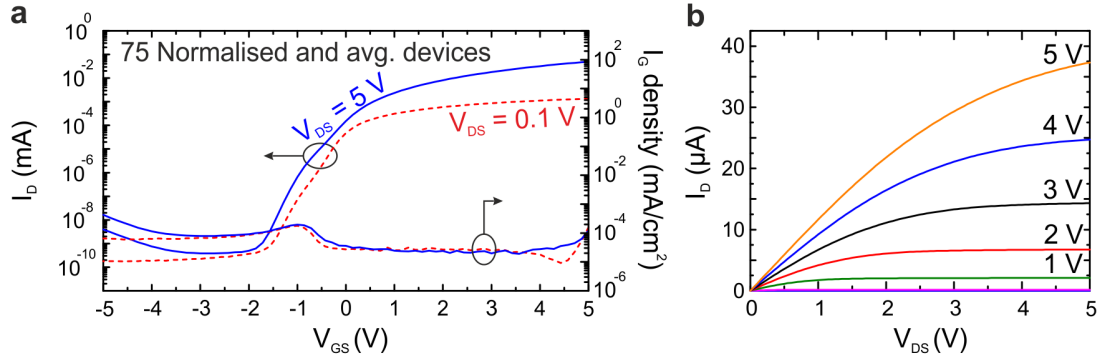


Figure 4.3: TFT characteristics before irradiation, low temperature treatment and magnetic field exposure. a) Saturation ($V_{DS} = 5$ V) and Linear transfer ($V_{DS} = 0.1$ V) curves. b) Output curves for Gate Source voltages (V_{GS}) ranging from 0 V to 5 V

which is sufficiently longer than typical spacewalks. Finally, the operation of a flexible Cascode amplifier is demonstrated after the sample was exposed to the aforementioned conditions. The demonstration of this circuit indicates that more complex circuits and systems based on flexible a-IGZO TFTs have the potential to be implemented in space applications.

4.2 Device fabrication

Fig. 4.2a shows a micrograph of a representative transistor sample characterised here. The IGZO TFTs were fabricated on a free standing 50  m thick polyimide foil (Fig. 4.2b) using conventional UV lithography [133]. To improve adhesion and to prevent outgassing of the

substrate, a 50 nm thick silicon nitride layer was deposited on both sides of the substrate using plasma enhanced chemical vapor deposition. The gate consists of a 35 nm-thick Cr layer deposited through e-beam evaporation. The 25 nm-thick Al_2O_3 gate insulator layer was deposited through atomic layer deposition (ALD) at a temperature of 150  C. This represents the highest process temperature involved into the fabrication process. Afterwards, a 15 nm-thick amorphous IGZO layer was deposited by radio frequency magnetron sputtering at room temperature. The gate, gate insulator, and semiconductor layers were structured by wet etching. The drain and source contacts were fabricated in a lift-off process by depositing 10 nm of titanium and 60 nm of gold through e-beam evaporation. The subsequent ALD deposition and structuring of an additional 25 nm-thick Al_2O_3 layer passivated the transistors and concluded the fabrication process.

4.3 Baseline Transistor Performance

The devices were measured using a Keysight B1500A parameter analyser. Electron irradiation was performed at a direct-beam end-station at the superconducting electron LINAC ELBE [134] at Helmholtz-Zentrum Dresden-Rossendorf (HZDR) in standard atmosphere. The electron fluence calibration has been performed by measuring the electric current in a Faraday cup and the dose rate in an ionization chamber Roos model 34001 [135]. We assume an error of the fluence measurement of max. $\pm 10\%$. Furthermore, the penetration depth for high energy electrons is in the range of centimetres, and as such the 25 nm-thick Al_2O_3 passivation layer is not able to effectively shield the semiconductor channel [136]. Electrical characterisation of the devices at low temperatures was carried out under vacuum (1×10^{-5} mbar) at temperatures varying from 78 K to 310 K using a cryogenic probe station (Janis Research, ST-500) and an Agilent B2902A source measure unit. The low temperature measurements were conducted in vacuum as even in inert atmospheres the residual air humidity would condense on the surface of the devices and hinder their proper characterisation. In addition, all measurements were conducted in the dark, using transistors originating from the same substrate. Performance parameters were extracted from the saturation regime using the Shichman-Hodges model [79].

Fig. 4.3 shows the normalised and averaged transfer and output curves of 75 individual TFTs. From the saturation transfer curve (Fig. 4.3a), an average threshold voltage (V_{th}) of 0 V, a field effect mobility (μ_{FE}) of $12 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, a subthreshold swing (S) of 233 mV/dec, a I_{ON}/I_{OFF} ratio $>10^7$, and a maximum transconductance g_m ($V_{GS} = 5 \text{ V}$) of 18 μS , were extracted. The gate current of these devices was typically $<10^{-11} \text{ A}$. These

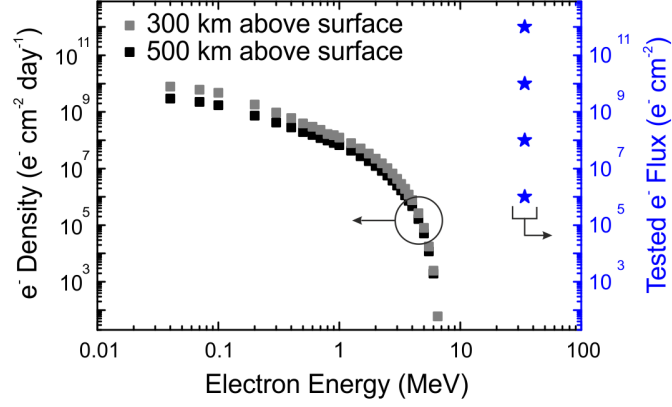


Figure 4.4: Trapped electron density at 300 km and 500 km above Earth’s surface as extracted from [119], and electron fluxes tested.

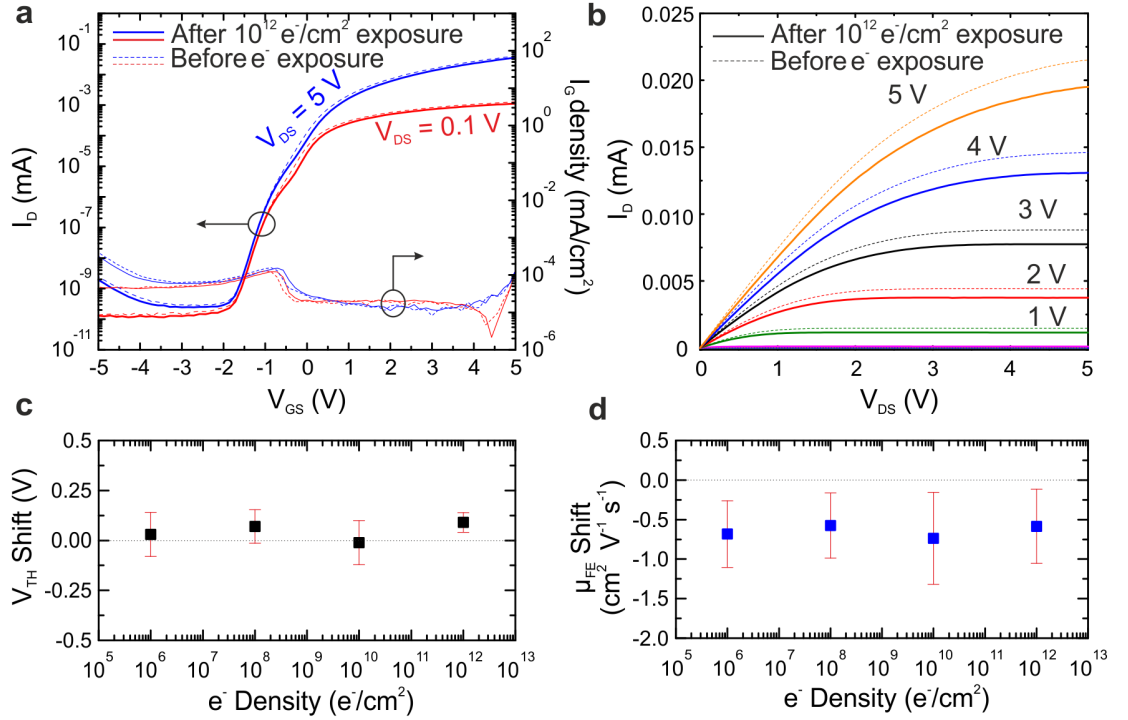


Figure 4.5: Impact of electron irradiation. a,b) Averaged transfer and output curves from 25 a-IGZO TFTs exposed to electron irradiation with a density of $10^{12} \text{ e}^-/\text{cm}^2$. c,d) Evolution of the V_{th} and the μ_{FE} for all electron irradiation densities.

values are in agreement with other high quality state of the art flexible a-IGZO TFTs [21].

4.4 Electron Irradiation Effects

The TFTs were exposed to electron irradiation with fluence ranging from $10^6 \text{ e}^-/\text{cm}^2$ to $10^{12} \text{ e}^-/\text{cm}^2$. Fig. 4.4 shows the typical trapped electron densities at 300 km and 500 km

for electron energies ranging from 0.04 eV to 6.5 eV. In Fig. 4.4 the star-shaped points indicate the energy and densities used in this work, which exceed both the density and energies typically existent in LEO. Fig. 4.5a presents the averaged transfer curves from the same 25 transistors measured before and after exposure to electron irradiation at $10^{12} \text{ e}^-/\text{cm}^2$. The gate current is normalized. From these measurements, a V_{th} shift of $+(0.09 \pm 0.05) \text{ V}$ was observed, whereas the μ_{FE} decreased by $(-5 \pm 6) \%$. The variation of S was observed to be negligible. The I_{ON}/I_{OFF} ratio and the gate current were virtually unaffected by the electron irradiation, remaining at 10^7 and $<10^{-11} \text{ A}$, indicating that the Al_2O_3 gate insulator was not damaged. Fig. 4.5b shows the averaged output curves for the same transistors, reflecting the decrease in the maximum I_D due to the increase of V_{th} and the decrease of μ_{FE} . Electron irradiation has no impact on the quality of the drain and source contacts, given that no current crowding effects are observed for low V_{DS} [137]. The evolutions of both the V_{th} and μ_{FE} are shown in Figs. 4.5c and 4.5d, respectively, with increasing electron irradiation. Parameter extraction was performed before and after irradiation on the same set of transistors (25 TFTs for each electron irradiation density). The threshold voltage is demonstrated to be virtually independent of the electron irradiation, whereas the mobility decreases after irradiation. The shift in V_{th} is significantly smaller than the 1 V V_{th} shift observed for top-gate Al_2O_3 (200 nm) gate dielectric rigid a-IGZO TFTs exposed to 0.8 MeV electrons with a fluence of $10^{14} \text{ e}^-/\text{cm}^2$ [124] and can be explained by the reduced interaction of the electrons with the low-density polymer substrate. Additionally, it is observed that the shift's magnitude of the mobility is independent of the irradiation fluence. These results indicate that the impacts on both V_{th} and μ_{FE} are independent of the electron fluence. Future work should look at the impacts of higher energy electron irradiation given that in this work it was fixed at 34.1 MeV. Regardless, the observed decrease of both I_D and μ_{FE} , as well as the increase of V_{th} can be explained by the formation of both oxygen interstitial and zinc vacancy acceptor defects, caused by the exposition to high energy electrons, as well as by charge trapping at the gate/dielectric without any damage to dielectric material [138, 139]. Finally, it is important to note that the small distortion in the transfer curves observed at approx. 0 V V_{GS} is a result of the averaging of devices with different geometries, and not a result of any damage to the material stack.

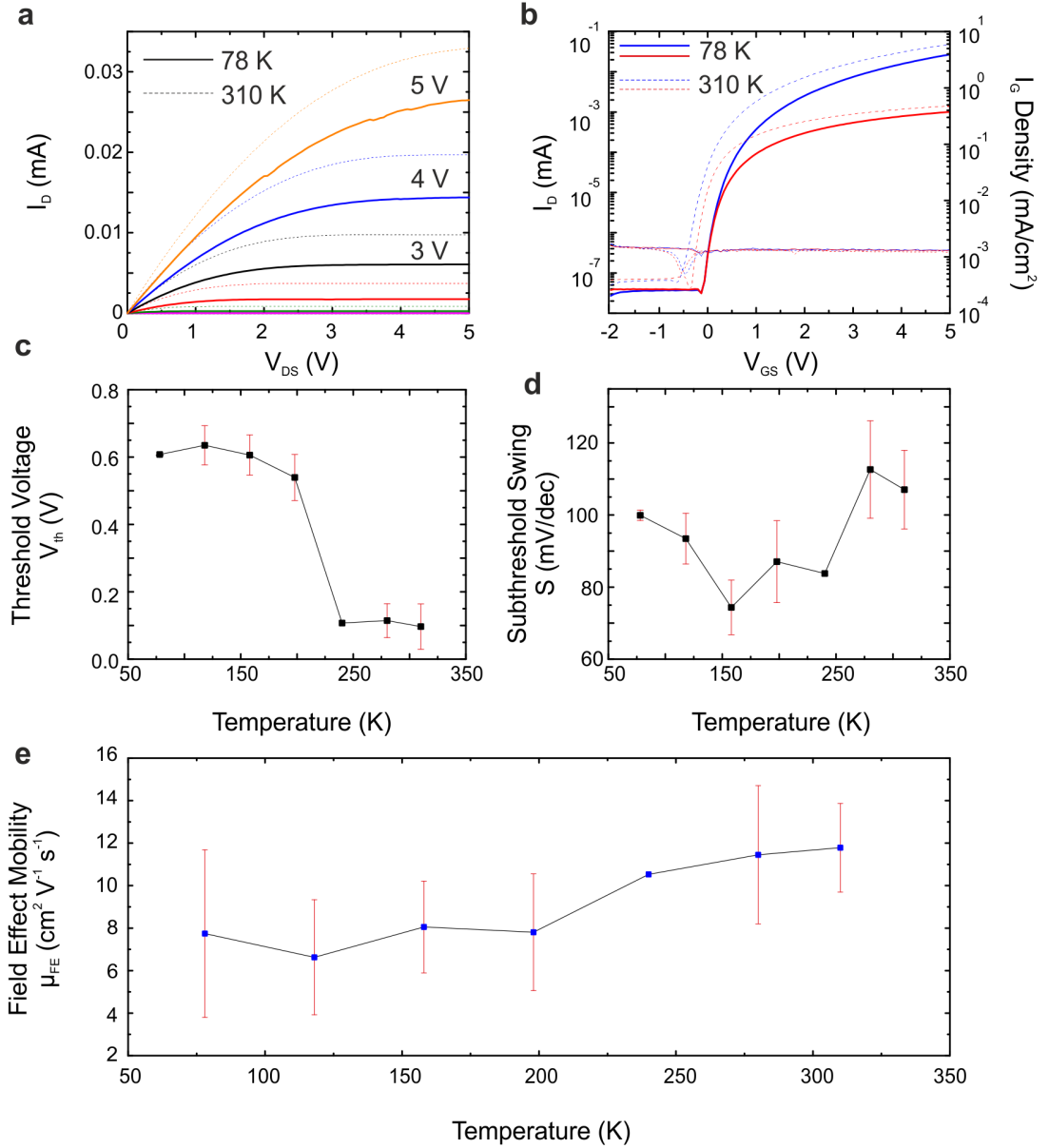


Figure 4.6: Low temperature measurements from a total of 16 transistors. a) Output curves at 78 K and 310 K. b) Transfer curves. c,d,e) V_{th} , S and μ_{FE} variation for temperatures from 78 K to 310 K.

4.5 Low Temperature Measurements

Next, the impact of low temperature on flexible a-IGZO transistors was investigated. Fig. 4.6 shows the averaged performance variation of the characterised transistors. Characteristic curves were extracted from 16 transistors. The reduced number of measurements is because the temperature-induced expansion of the polyimide substrate complicated reliable contacting of the devices, and different transistors had to be measured for each temperature. Fig. 4.6a shows the averaged output curves for the measured transistors,

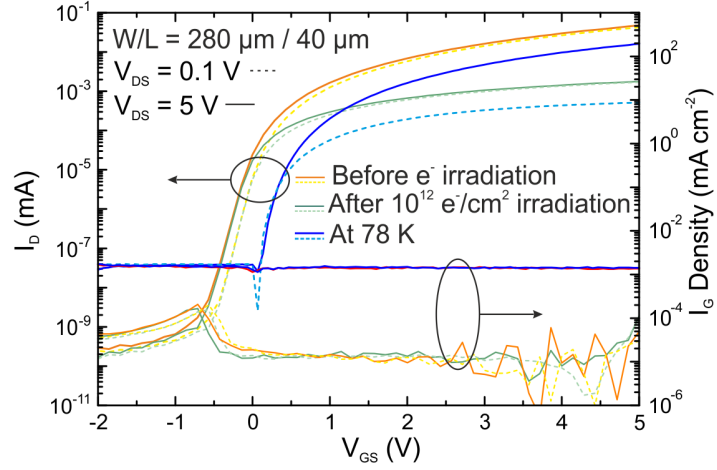


Figure 4.7: Evolution of the saturation and linear transfer curves for a transistor irradiated with the highest electron density, followed by exposure to 78 K.

where a decrease of the drain current is observed for 78 K in comparison to the values observed at 310 K. This is explained by the decrease of the thermal energy available for the thermal activation of electrons trapped in defect sites. As it was observed for the irradiated transistors, no current crowding effect is visible for low V_{DS} values. An average V_{th} of 0.6 V with minimal error was extracted from the measured TFTs at 78 K (Fig. 4.6b), corresponding to a positive shift of (0.51 ± 0.07) V when compared to the (0.09 ± 0.07) V extracted from the same devices at room temperature. The evolution of V_{th} , S and μ_{FE} are presented in Figs. 4.6c, 4.6d and 4.6e, respectively. V_{th} increases for lower temperatures, whereas the subthreshold swing and μ_{FE} decrease for the same interval. The performance of the devices was observed to recover as the temperature returned to 310 K. Previous studies on rigid TFTs have presented similar trends for V_{th} , and μ_{FE} due to the thermal activated profile of a-IGZO [127]. In addition, measurements down to 10 K on rigid a-IGZO TFTs demonstrated that the subthreshold swing increased for temperatures below 80 K [127], which was attributed to a change from band conduction to variable range hopping [140]. It is interesting to note that no correlation was observed between V_{th} and the subthreshold swing. In fact, the subthreshold swing remains comparatively stable down to 78 K. It is possible that an increase of the subthreshold swing would be observed for lower temperatures, as reported in [127].

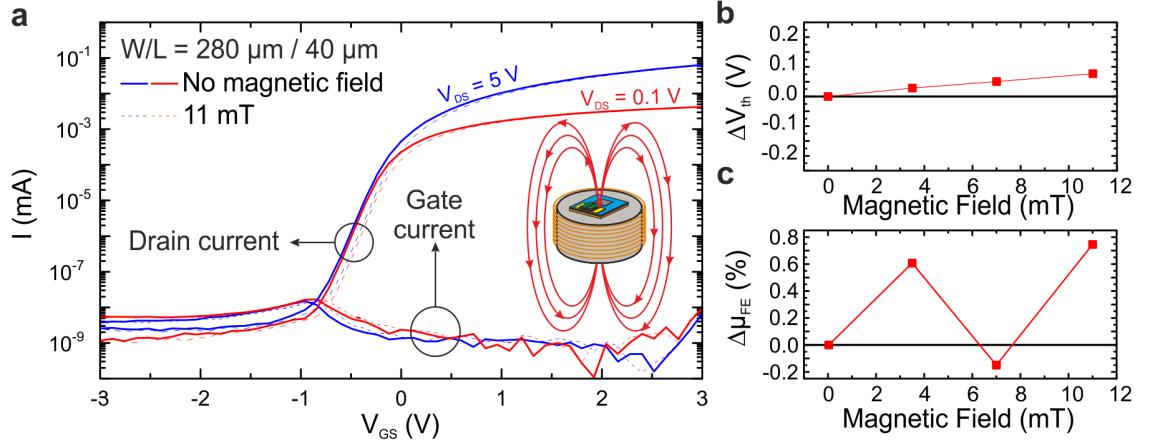


Figure 4.8: Magnetic field effect on a-IGZO flexible TFTs. a) Transfer curves measured at 0 mT (full line) and 11 mT (dashed line). b,c) V_{th} and μ_{FE} shift for a device measured under various magnetic fields. d) Schematic of the setup used to apply the magnetic field.

4.6 Combined irradiation and temperature

The combined influence of radiation and low temperatures was investigated, Fig. 4.7 presents the transfer curve evolution of a TFT that was irradiated with $10^{12} \text{ e}^-/\text{cm}^2$ and afterwards cooled down from 310 K to 78 K. As can be seen, in comparison with the devices that were not exposed to electron irradiation, such as the ones on Fig. 4.6b, the parameter shifts are only slightly affected by the applied electron irradiation. The irradiated sample exhibited V_{th} , μ_{FE} and S shifts of +0.38 V, $-5.95 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and +30 mV/dec, after being cooled down to 78 K. The same parameters shifted by +0.13 V, $-5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and 21 mV/dec for the non irradiated sample. The irradiated sample presents larger parameter shifts at low temperatures. Although these differences are small and could be related to intrinsic performance variations of the samples, the measurement indicates that a combined radiation-temperature effect in flexible a-IGZO TFTs has to be considered for space applications. This combined effect can be caused by an increased number of defects in the irradiated transistors, as high energy electron irradiation has been shown to create acceptor defects on a-IGZO TFTs [124]. The thermally activated occupation and de-occupation of these traps then changes the low temperature behaviour of the TFTs.

4.7 Magnetic Field Effects

In addition to the effects of electron irradiation and low temperatures, it is also important to study the influence of magnetic fields on the properties of the devices. Fig. 4.8a

shows the transfer characteristics of a flexible a-IGZO TFT measured at 0 mT and under an 11 mT magnetic field. For comparison, the magnetic field at an altitude of 300 km above the Earth’s crust does not typically exceed 20 nT [141]. It has previously been demonstrated that IGZO TFTs can be sensitive to magnetic fields [131]. This sensitivity has nonetheless been correlated with the employed gate insulator. Aoki et al. [131] characterised a-IGZO TFTs on glass with both SiN_x and SiO_x gate insulators, which resulted in conventional (resistance increase) and inverse magnetoresistive effects, respectively. Figs. 4.8b and 4.8c show the V_{th} and μ_{FE} of an a-IGZO TFT with Al₂O₃ gate insulator for various magnetic fields. The magnetic field is applied perpendicularly to the direction of the channel (Fig. 4.8d). This field was generated using a coil wrapped around a ferromagnetic core, and the magnetic field was measured using a Redcliffe 102 Hall magnetometer. The devices were placed on the surface of the ferrite core and in order to exclude the effects of temperature, the core’s surface temperature was monitored during the measurements and was not allowed to exceed room temperature (RT) + 1 °C. All measurements were conducted in the dark and in a standard atmosphere. Although a 0.08 V positive shift is observed for the V_{th} , this effect was also observed for devices measured repeatedly under a 0 mT magnetic field. Given that the μ_{FE} was not significantly affected by the magnetic field, the V_{th} shift is most probably related with gate bias stressing of the devices. These results show that flexible a-IGZO TFTs can operate under magnetic fields 10⁶ times larger than the ones found in LEO [141].

4.8 Device Bendability

Assessing the flexibility of these devices is important given the desired application in flexible sensors. For this reason, the TFTs were tested under bending at various radii after exposure to electron irradiation, low temperature and magnetic fields. Fig. 4.9 shows the resulting transfer characteristics under 12.5 mm, 7.5 mm and 5 mm bending radii, corresponding to tensile strains of 0.22 %, 0.35 % and 0.52 % calculated from [142]. The devices were attached to rods as shown in Fig. 4.9c to apply strain parallel to the TFT channel. The transfer curve of the devices shifted in the negative direction with decreasing bending radii, and the exact V_{th} is captured in Fig 4.9b. Re-flattening the device resulted in a gradual recovery of the transfer curve [143], however, bending to smaller radii causes cracks and permanently damages the devices. In addition, no significant increase of the gate leakage current was measured for all bending radii, indicating that the dielectric layer was not significantly affected by the bending stress. This negative shift is in line

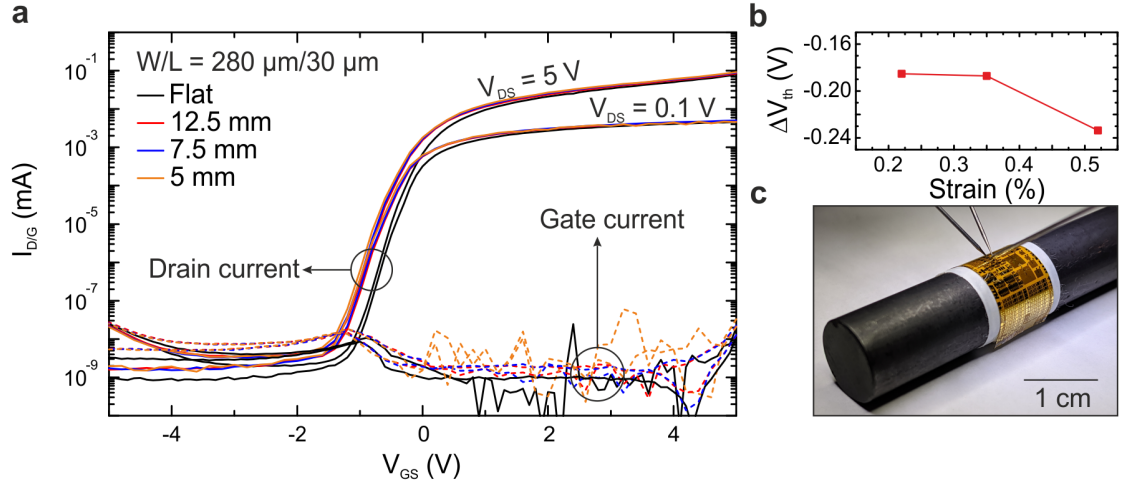


Figure 4.9: Effects of mechanical bending on a-IGZO flexible TFTs. a) Transfer curves measured for a flat device and for three different bending radii, 12.5 mm, 7.5 mm and 5 mm. Threshold voltage shift for the various bending radii. c) Photograph of bent substrate with measured samples.

with the effect of tensile strain on non irradiated a-IGZO TFTs. These results illustrate the flexibility of the devices studied in this work.

4.9 Integrated Amplifier

In addition to individual TFTs, the functionality of an integrated circuit was investigated after it was exposed to an electron irradiation of $10^{12} \text{ e}^-/\text{cm}^2$, temperatures as low as 78 K, and magnetic flux densities up to 11 mT. These represent the most extreme conditions discussed here. Fig. 4.10a shows a micrograph of the tested voltage amplifier fabricated using three IGZO TFTs, and Fig. 4.10b shows a representative amplified signal at a frequency of 100 Hz. In addition, Fig. 4.10c displays the corresponding circuit schematic which also indicates the TFT dimensions, input, bias, and supply voltages, as well as the loading effect of the characterisation equipment. The employed Cascode topology based on standard NMOS design principle utilizes an active load and represents a tradeoff between circuit complexity and performance. This is because the Cascode reduces the Miller effect and hence the negative impact of parasitic overlap capacitance, unavoidable if circuits are fabricated on free-standing flexible substrates [69]. Such amplifiers are essential for the conditioning of a variety of sensors.

Figs. 4.10b and 4.10d prove that the circuit is fully functional. After, irradiation, temperature and B-field stress, the Cascode circuit provides an average low frequency

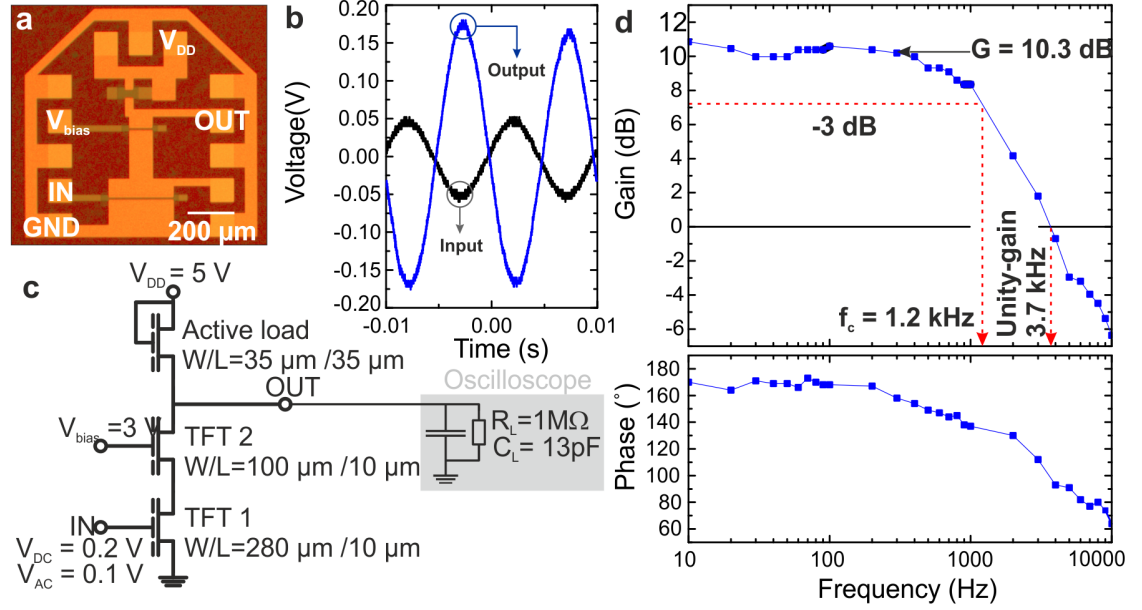


Figure 4.10: Flexible a-IGZO Cascode amplifier. a) Micrograph of the integrated circuit. b) Representative input and output voltages at $f = 100$ Hz. c) Circuit schematic showing the individual TFT dimensions, output load, as well as bias and input voltages. d) Bode plot measured after the circuit was exposed to electron irradiation ($10^{12} \text{ e}^-/\text{cm}^2$), low temperatures (78 K), and magnetic fields (11 mT).

voltage gain of 10.3 dB, a -3 dB cutoff frequency of 1.2 kHz, and a unity gain frequency of 3.7 kHz. This results in a gain bandwidth product (GBWP) of 3.6 kHz. Furthermore the Cascode architecture also results in power consumption of only $62.5 \mu\text{W}$. Commercial rigid amplifiers such as the OPA277 tested using temperatures down to 73 K have a GBWP of 1 MHz [144]. However, in comparison, flexible amplifier systems using pentacene TFTs show maximum GBWP of 2 kHz and their reliability has not been tested after they've been exposed to conditions similar to the ones found in space [145].

4.10 Conclusion

The suitability of flexible a-IGZO TFTs was assessed for the development of electronic devices for conformable and lightweight space applications. Electron irradiation followed by low temperature treatment down to 78 K were conducted to simulate the harsh environment found in Low Earth Orbit. Trap creation caused by electron irradiation induces a positive V_{th} shift and a decrease of the μ_{FE} for electron irradiation densities up to $10^{12} \text{ e}^-/\text{cm}^2$ and electron energy of 34.1 MeV. Nonetheless, the variation of the electron irradiation fluence did not influence the magnitude of these shifts. Subsequent low

temperature measurements down to 78 K resulted in an average decrease of 20 % for the μ_{FE} , accompanied by a positive V_{th} shift and a decrease of the subthreshold swing that reached a minimum of 66.5 mV/dec. It was also demonstrated that the temperature induced parameter shifts are slightly influenced by previous electron irradiation. Regarding the magnetic field impact on the performance of the TFTs, no visible variation was observed. Finally, a Cascode amplifier was shown to be operational after the sample had been irradiated and exposed to low temperatures and magnetic fields that exceeded the conditions found in Low Earth Orbit. These results show that a-IGZO TFTs fabricated on flexible polyimide substrates are a viable option for the development of lightweight and unobtrusive devices for space applications, such as smart textiles for space suits.

Chapter 5

An Handwritten pressure sensor based on solution processed Silver and Nickel inks, and a Diode on paper

Chapter 5 presents the fabrication of resistors, capacitors, diodes and circuits on paper using a manual printing technique. The presented methods showcase a simple, yet effective, method to fabricate devices using low-cost materials and techniques that are widely available. This chapter was published in *Advanced Electronic Materials* [34] and featured in the cover page of the 5/2018 edition of the same journal. The cover page is shown in the appendix figure A.1. Please note that figures 5.2, 5.3 and 5.4 are found at the end of this chapter due to their large size.

5.1 Introduction

As electronic systems become embedded into the whole spectrum of human activities, new approaches are required to make customized electronics cheaper and easier to produce. Paper, one of the most ubiquitous materials in history, has already been utilized as substrate and dielectric in devices such as thin film transistors [146, 147, 148], point-of-care sensors [149, 150], or supercapacitors [151, 152]. These led to flexible, biodegradable and recyclable electronics, but still relied on complex fabrication techniques which generally require vacuum, elevated temperatures and expensive machinery [153, 154, 155]. Due to the natural compatibility between paper substrates and pen/pencil based deposition techniques,

hand drawn layers provides a more immediate approach to deposit and structure materials. In this respect, conductive inks have been developed using solutions containing silver [156], metallic nanowires [157], indium gallium alloys [158] or carbon nanotubes [159]. In addition, inks containing semiconductors such as zinc oxide [160] or poly-3-octylthiophene [161] have been developed. These materials have been used for the development of electrocardiogram sensors [162], antennas [163], displays [164], and transistors [165, 166, 167]. Nevertheless, the complex synthesis required to produce such inks limits their widespread use. Graphite, on the other hand, is an abundant and cheap material, and lead pencils have been used to write on paper since the 16th century [168]. More importantly, due to the bulk structure of graphite, which consists of disorganized clusters of stacked graphene sheets connected by Van der Waals bonds, graphite is an electrically conductive material. Hence, commercially available pencils can be used to fabricate pencil-written electronic components, circuits, and sensors [169, 170, 171, 172, 173]. In this work, the complexity and functionality of hand written electronics is moved to a new level through the development of a complete pressure sensor system which also features the first hand written Schottky diode on paper. The presented system is based on a pen and pencil-written half-wave rectifier, as well as a low pass filter and percolation force sensitive resistor. It also includes an off the shelf operational amplifier biased using hand written passive components. The amplifier acts as a sensor conditioning circuit and improves the signal to noise ratio of the device. The realization of the system relied on a detailed characterization of the discrete components to evaluate and define the fabrication parameters. Pencils containing different graphite to clay ratios allow for the fabrication of thin film resistors with varied sheet resistances. Changing resistance values is easily achieved by either removing or adding graphite layers to or from the existing structures, making the prototyping process faster. Graphite paper graphite parallel plate capacitors demonstrate capacitance values as high as 141 pF/cm²; this is three times larger than similar existing paper capacitors [174]. Hand written Schottky diodes on paper exhibiting rectification ratios of 1:8 were also fabricated and studied. All hand written devices are used to realize circuits including rectifiers and filters for frequencies up to 13.56 MHz. Finally, all presented devices and circuits were tested under tensile and compressive stress. Bending radii down to 100 μ m, (corresponding to complete folding and strain of 50 %) were applied while the devices remained fully functional. The results demonstrate the potential of the presented technique for the development of complex, flexible hand written electronic systems, broadening the scope of inexpensive, eco-friendly and readily available electronics.

5.2 Pressure Sensor System

The potential of the presented hand written electronics is demonstrated through the fabrication of a fully integrated pressure sensor system (Figure 5.1a). The output signal of this system exhibits a linear behavior for applied pressures between 0.2 kPa and 1.2 kPa, with a sensitivity of 51 mV/kPa. This is comparable to other percolation and strain based flexible pressure sensors, with the added advantage of a simple and inexpensive fabrication process (Figure 5.1b) [175]. Liao et al. [176] developed a highly sensitive graphite strain sensor with a gauge factor of 536.6, nevertheless, the conversion of strain to pressure is complicated due to variables such as dimension of the device and elastic modulus of the paper substrate. Liana et al. [177] fabricated a strain sensor that featured an optical readout system which required a mixture of copper particles, polydimethylsiloxane and carbon paste to operate. In comparison, the techniques demonstrated here can be used to develop pencil/pen written biodegradable electronic scales, accelerometers and resistive touch user interfaces in a straightforward manner, with key applications in fast device prototyping, as well as in teaching environments where commercial electronic development tools are too costly. The structure layout for the pressure sensor system is shown in Figure 5.1c and the circuit schematic is presented in Figure 5.1d. The system is constituted by three sub systems: rectification and high pass filtering to remove the negative component of the AC input signal and the high frequency background noise (Figure 5.1e); this is followed by the modulation of the signal's amplitude in a voltage divider made from a pencil written 21 k  resistor and the force sensing resistor (FSR) (Figure 5.1f); lastly, the sensor's output signal is amplified (Figure 5.1g) to recover the signal from attenuation caused by the first two stages. Two hand-drawn graphite resistors of 4 k  and 40 k  provide a voltage gain of 11 when used in a non-inverting configuration with the off-the-shelf operational amplifier. The FSR consists of two stacked graphite contacts separated by a ring-shaped paper spacer. The bottom contact is fabricated by drawing two interdigitated graphite tracks; these graphite tracks are separated by a 2 mm gap to ensure that no resistive contact exists between the two sections when no pressure is applied. The top contact consists of a drawn graphite filled circle which bridges both bottom contacts when pressure is applied. In contrast to strain sensors, where the resistance variation originates from the bending of a resistive film, the resistance variation in percolation FSR originates from the increase in conductivity as both the top and bottom layers are pushed together, and the contact area between different graphite clusters increases (Figure 5.1f). The sensor system was tested by measuring the averaged output signal for various applied pressures, as

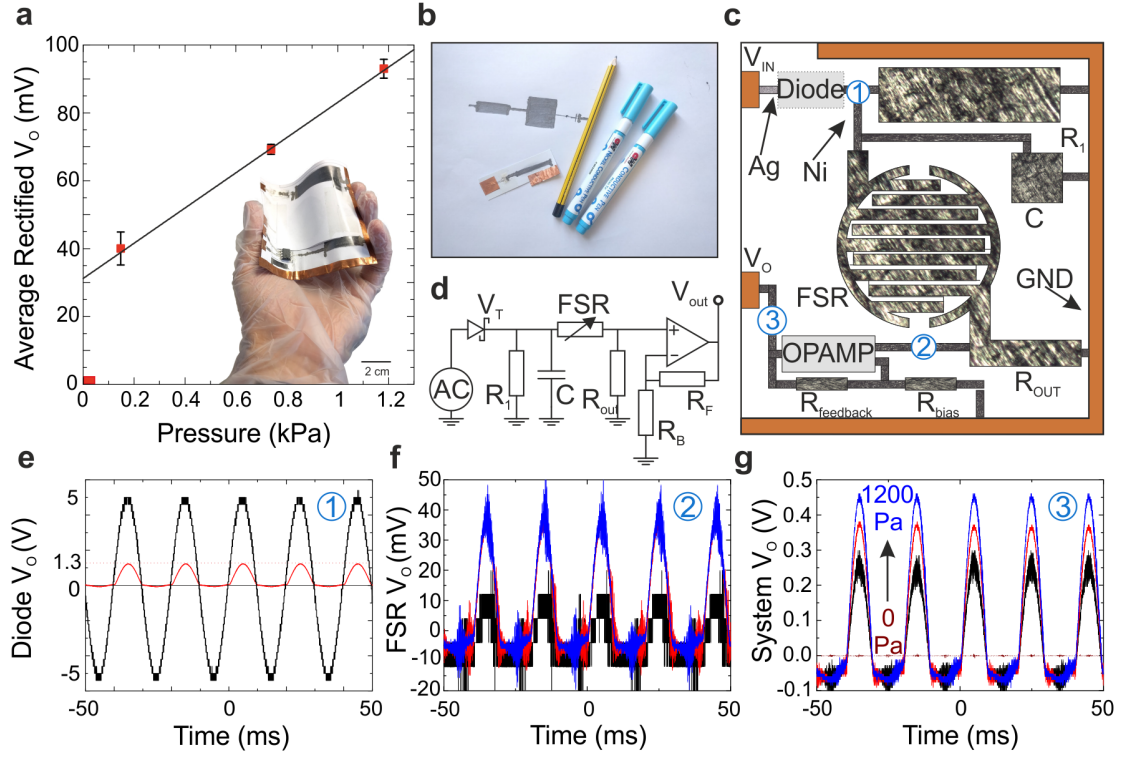


Figure 5.1: Pressure sensor system. a) Output signal of an integrated pressure sensor system fabricated on paper. This system presents a sensitivity of 51 mV/kPa for pressures up to 1.2 kPa. b) Pencil and pen-written devices on a paper substrate. The simplicity of this technique facilitates the development of electronic prototypes. c) Full design of the pressure sensor. This device used a pen-written half-wave rectifier to eliminate the negative component of a 10 V peak to peak AC signal, which was then modulated by the pressure applied to a pencil-written force sensitive resistor (FSR). The FSR is integrated into a voltage divider and its output signal is amplified using an off the shelf amplifier whose gain of 11 was defined by two hand-written resistors. d) Full circuit schematic of the system, including values of all elements. Intermediate signals from the half-wave rectifier (e), pressure sensing voltage divider (f) and amplifier (g).

shown in Figure 5.1a. The half-wave rectifier simplifies the readout process by eliminating the negative peaks of the sensor output. The small error obtained (less than plus minus 12 %), combined with the obtained linearity and sensitivity showcase the capabilities of the presented techniques. In addition to the pressure sensor system, other modalities such as humidity, strain and temperature can be detected using this technology. The latter is demonstrated in supplementary Figure D.1. A pencil written temperature sensor exhibits a linear behavior in temperature ranges from 50 °C to 140 °C, with a sensitivity of $7.7 \times 10^{-4} (\Omega/\Omega_0)/^\circ\text{C}$.

5.3 Single Components

Figure 5.2a presents the layout of the three basic hand written electronic devices used to realize the described sensor system. Figure 5.2b shows the relation between conductance and width to length (W/L) ratio for resistors fabricated with two different types of commercial pencils (graphite contents of $(92.5 \pm 2.5) \%$ and $(72.5 \pm 2.5) \%$). The sheet resistance of the resistors fabricated through this technique was evaluated using a set of 30 devices for both pencil types. Resistors made from pencils with higher graphite to clay ratio exhibited a sheet resistance of $(500 \pm 31) \Omega/\square$, while an average value of $(7.7 \pm 0.4) \text{ k}\Omega/\square$ was obtained for the resistors fabricated using the lower graphite to clay ratio pencils. These values were extracted from the inverse of the specific conductance for each pencil type in 5.2b. More specifically, $(92.5 \pm 2.5) \%$ presented a specific conductance of 2 mS, whereas resistors fabricated using $(72.5 \pm 2.5) \%$ pencils presented a 0.13 mS specific conductance. Given their superior reliability and conductivity, higher graphite content pencils are preferable for the fabrication of electronic devices. In addition, the current-to-voltage characteristics of resistors with different W/L ratios demonstrates their linearity (Figure 5.2c). The parallel plate capacitors were fabricated using high graphite content pencils (92.5 %) with two distinct contact types, namely compact and sparse. These classifications relate to the density of the graphite films. Sparse film deposition was performed by dragging the pencil on the paper once, whereas compact graphite films were the result of 10 repeated depositions to ensure a continuous layer – Figure D.2 and b show that the sparse layers cover only 45 % of the paper area, which leads to highly resistive contacts ($>1 \text{ M}\Omega$). Figure 5.2d presents the specific capacitance extracted from a total of 50 samples. The average specific capacitance for compact graphite capacitors is $(117 \pm 4) \text{ pF}/\text{cm}^2$, and sparse graphite capacitors exhibit a value of $(20 \pm 5) \text{ pF}/\text{cm}^2$. Furthermore, the frequency dependency of compact capacitors is not significant for frequencies from 1 kHz to 10 MHz. In contrast, sparse graphite capacitors exhibit a drop of capacitance by two orders of magnitude in the same frequency interval (Figure D.3). This decrease in capacitance is explained by the parasitic resistance of the structures. This parasitic resistance, in combination with the capacitance, creates a low-pass filter that attenuates high frequency signals. The last component required for the fabrication of the sensor system is a diode. Diodes were manufactured by deposition of Ag and Ni contacts on a IGZO coated paper using conductive ink pens. Optical imaging of both coated and uncoated area is shown in Supplementary Figure D.2, while insets e, f, g and h show AFM micrographs of the substrate. Figure 5.2e shows the IV characteristics of an Ag-Ni diode

fabricated on paper before and after annealing. The device exhibits a turn on voltage of 0.6 V and a rectification ratio of 1:8. Without annealing, the fabricated diodes have an almost ohmic behavior. Nevertheless, as shown in Figure 5.2f, annealing at 150  C for 10 min under ambient conditions results in an increase of the current rectification ratio from 1:1.25 to 1:4.5 for forward and reverse bias voltages of 1 V and -1 V. Annealing for an additional period of 60 min led to a further increase of the rectification ratio to 1:8. At the same time, the maximum On current decreases after the 60 min annealing step. Previously, the formation of AgO_x at the interface of silver and a-IGZO has been correlated with the formation of a Schottky barrier, as the mismatch in the work function of a-IGZO (4.5 eV) and silver (4.26 eV to 4.74 eV) is not enough to explain this effect. The measurements indicate that longer annealing times increase the thickness of interfacial non conductive AgO_x , and improve the rectification ratio [178]. a-IGZO was chosen as it can be deposited at room temperature, and remains operational when bent to radii down to 25 μm . Furthermore, a-IGZO is a common semiconductor material used for the development of flexible analog electronic systems [55, 21]. For instance, a-IGZO has been employed in the fabrication of flexible Schottky diodes using vacuum based manufacturing techniques. These demonstrated high frequency operation up to 2.45 GHz [179] and rectification ratios up to 10^7 [180].

5.4 Pen/pencil written circuits

The presented single components are suitable for the development of a variety of circuits. To characterize the sub systems of the pressure sensor system, individual low, high and band-pass filters, as well as a half-wave rectifier, were fabricated. Figure 3a shows 1st order low and high pass filters on paper. These filters were fabricated by drawing a resistor and a capacitor in series. Figures 5.3b and 5.3c, show the frequency response for two low-pass filters with -3 dB cut off frequencies of 3 kHz and 60 kHz. Figures 5.3d and 5.3e show the response of two corresponding high-pass filters exhibiting cut-off frequencies of 7 kHz and 60 kHz. These filters present the typical behavior of low and high pass filters, and exhibit a signal attenuation of roughly equal to 15 dB/dec beyond the cut off frequency. By adding or removing graphite layers to/from the resistors, the RC time constant of the filters can be tuned, enabling accurate control of the cut-off frequency. Following the fabrication of single pole filters, a band-pass filter for 13.56 MHz aimed for RFID applications was developed (Figure 5.3f). This circuit was designed to be compatible with applications such as electronic ticketing and garment tracking, as inexpensive and biodegradable circuits are

desirable for both applications. The output signal of a half-wave rectifier consisting of a pen-written diode and pencil-written resistor is shown in Supplementary Figure D.4. The attenuation of the input signal by a factor of 11 is caused by the 70 k  output resistor. This value is smaller than the diode’s forward resistance of 750 k  at 5 V bias voltage. In addition to the fabrication of hand-written electronic devices, the possibility of using paper as a carrier substrate for off the shelf components was evaluated. Here, a customized printed circuit board (PCB) was fabricated to interface and to bias a voltage amplifier (Figure 5.3g). A commercially available off the shelf operational amplifier was fixed to a sheet of paper using a Ni pen. The Ni acted as adhesive and Ohmic contact between the amplifier and the pencil/pen written components. The design of this system can be found in Figure D.5. Using the non inverting configuration shown in Figure 5.3h, two graphite resistors, of 3.1 k  and 362  , were used to define the voltage gain of the amplifier circuit. As shown in Figure 5.3i, this amplifier exhibits a gain of 19.5 dB and a -3 dB cut-off frequency of 30 kHz. This device can thus be implemented to condition the output signal of a variety of sensor systems. It also demonstrates the potential of paper PCBs to be used as an alternative substrate to conventional fiber glass circuit boards. Such fabrication process is ideal for disposable or prototyping applications, as it does not require specialized and often costly equipment such as PCB milling machines or etching.

5.5 Bending Stress

Typically, flexible devices suffer from strain related effects. Due to this, the behavior of all the electronic components and circuits was tested for various bending radii, ranging from 5 mm to 100  m. The results indicate that resistors exhibit almost no variation in their resistance for tensile and compressive bending down to 0.1 mm, equivalent to strain of 50 % (Figure 5.4a). The strain was calculated using an equation adapted from previous reports on thin film bending [181, 182]. These bending radius corresponds to complete folding. While re-flattening after tensile folding has minor effects, re-flattening after compressive folding results in a resistance increase of two orders of magnitude. This is because tensile cracks created by the extension of graphite, allows for both edges of the crack to come into contact after re-flattening. Contrarily, compressive cracks are generated by the formation of excess material across the folding line, which delaminates from the surface. In the case of capacitors (Figure 5.4b), as the graphite electrodes were drawn on both sides of the paper, no difference exists between tensile and compressive bending. Capacitors with compact graphite contacts show a stable performance for all bending radii.

In contrast, the sparse capacitors demonstrated a decrease of 25 % of the capacitance when re-flattened after undergoing complete folding. To characterize the stability of the diodes, a bending radius of 5 mm (1 % strain) was applied and their IV curves were studied (Figure 5.4c). The On current of the diodes was found to decrease by 23 % during the bending cycle, which is explained by the low adhesion of the nickel and silver contacts to the a-IGZO coated paper, resulting in the delamination of the metal layers. Nevertheless, when re-flattened, the On current increased to 83 % of its original value. For bending radii below 5 mm, the a-IGZO diodes cease to function. The rectification ratio remained constant after the device had been bent and re-flattened. As shown in Figure D.6, the AC response of a half wave rectifier bent to a radius of 5 mm followed the DC behavior of single diodes. The maximum output signal dropped by 18 %, followed by a recovery to 91 % of the input signal after re-flattening. The low and high pass filters did not show any performance variation when undergoing bending (1 % strain), and did not suffer from long-term variations after being re-flattened; mirroring the behavior of the individual components (Figure 5.4d,e). The strain applied to these devices should never surpassed 1 % as a loss of function is observed otherwise. The band-pass filter transmission level decreased from -6 dB to -10 dB when re-flattened after undergoing bending to a radius of 5 mm (1 % strain), but did not show any shift in the cut-off frequencies (Figure 5.4f). The results reported, validate the fabricated hand-written components and circuits for the implementation in flexible electronics.

5.6 Conclusion

In this work, pencils and conductive pens were used to fabricate a pressure sensor system on paper. The complete pressure sensor system exhibits a linear behavior for pressures up to 1.2 kPa and a sensitivity of 51 mV/kPa. The techniques used to fabricate this system demonstrate the possibility to develop devices such as biodegradable tags, biometric sensors, and novel flexible human machine interface systems. Additionally, the fabrication of the first hand-written Schottky diode and half-wave rectifier was reported. A maximum rectification ratio of 1:8 was obtained for the presented Ag/a-IGZO/Ni hand written diodes, a value that remained constant even when the devices were subjected to a strain of 1 % and subsequently re-flattened. The rectifying properties of these devices were shown to be related to temperature treatment and AgO_x formation at the interface. The behavior of all devices and circuits was studied under bending. Resistors, capacitors and RC filters showed no significant performance variation when bent down to radii of 100 μ m. The

presented work demonstrated the versatility of using commonly available materials and writing tools for the fabrication of circuits on paper substrates. Considering the advantages of hand-written electronics, and the electrical and mechanical performances achieved, this work is a major step towards the development of more complex hand-written circuits as a flexible and eco-friendly alternative to standard electronics.

5.7 Experimental Section

5.7.1 Single Components

Standard printer paper with a thickness of 100 μm was used as a substrate for the fabrication of all devices and circuits. B9 ($(92.5 \pm 2.5) \%$ graphite content) and HB ($(72.5 \pm 2.5) \%$) commercially available pencils from Faber-Castell[®] were used for the deposition of graphite films. Nickel and silver deposition was achieved using Circuitworks[®] Nickel Conductive CW2000 and Conductive Micro Tip CW2200 pens from Chemtronics[®], respectively. Amorphous Indium Gallium Zinc Oxide (In:Ga:Zn = 1:1:1) was deposited through standard room temperature RF sputtering [183]. Diodes were fabricated on 1 cm^2 to 4 cm^2 a-IGZO coated paper samples using silver and nickel metal inks. The annealing of these devices was performed on a hotplate under ambient conditions. The annealing temperature was 150 °C.

5.7.2 Pressure Sensor System

The pressure sensor system was fabricated on a 100 cm^2 paper substrate. The rectifying stage of this circuit consisted of a diode connected in series with a parallel combination of a resistor and capacitor. The diode was fabricated through the deposition of two 2 mm \times 6 mm parallel Ag and Ni contacts on a 1 cm \times 1.5 cm a-IGZO coated paper, which was fixed to the main substrate using commercial tape. The Ag terminal of the diode was directly connected to the input of the system. The Ni terminal was connected to the low pass filter made from a 46 k Ω hand written resistor and a 550 pF hand drawn capacitor (both 1.5 cm \times 5 cm). Both devices were fabricated using a 92.5 % graphite content pencil and a compact graphite profile. The output of this resistor was inputted to the FSR. The fabrication of the graphite force sensitive resistor followed a 3 layer design. The bottom layer consisted of two asymmetrical groups of graphite tracks, designed to create an interdigitated structure where no contact existed between the two contacts. This structure was fabricated using a B9 (92.5 % graphite content) pencil and exhibited an Off

resistance of 23 M Ω . A paper layer was used as a spacer between the bottom and top contacts. This spacer layer determined the sensor's active area. In this case, a 6 cm \times 5 cm sheet of paper with a 4 cm diameter hole, corresponding to a total active area of 12.6 cm², was fabricated. The top contact was fabricated using a B9 pencil to deposit a continuous graphite layer. The output consisted of a 0.7 cm \times 3 cm 21 k Ω resistor fabricated using a 92.5 % graphite content pencil. Finally, the signal was amplified using an OP177 connected in a non inverting configuration to two resistors of 0.5 cm \times 1.6 cm (40 k Ω after being tuned) and 0.6 cm \times 1 cm (4 k Ω). Copper tape was used on all devices to improve the contact between circuits and the instrumentation.

5.7.3 Pen/Pencil Written Circuits

Low and high pass filters were fabricated through the hand-written deposition of a resistor and a capacitor in series using a B9 type pencil. The components were connected using low resistive Ni ink. The band-pass filter was fabricated by connecting a low-pass filter and a high-pass filter. The employed 480 pF capacitors were fabricated by depositing compact graphite films on opposite sides of the paper substrate using 92.5 % graphite content pencils.

5.7.4 Bending Stress

Bending measurements were carried out in ambient conditions. All samples were bent using stainless steel rods with radii between 5 mm and 0.5 mm. Complete folding of the paper was achieved manually. The resistors, capacitors, and RC filters were bent perpendicularly to the current direction. The diodes and half-wave rectifiers were bent parallel to the diode's channel. The samples were fixed to the stainless-steel rods using standard adhesive without influencing the bending radii.

5.7.5 Characterization

All AC signals were generated using a Philips PM5139 function generator. AC signals were measured using a Rhode&Schwarz RTM2032 Oscilloscope. Resistances were measured using a 117 True RMS Multimeter from Fluke, whereas capacitances were measured using an HP4274A multi-frequency LCR meter. The diodes' current to voltage response before and after annealing was characterized using a Keysight B1500A parameter analyser.

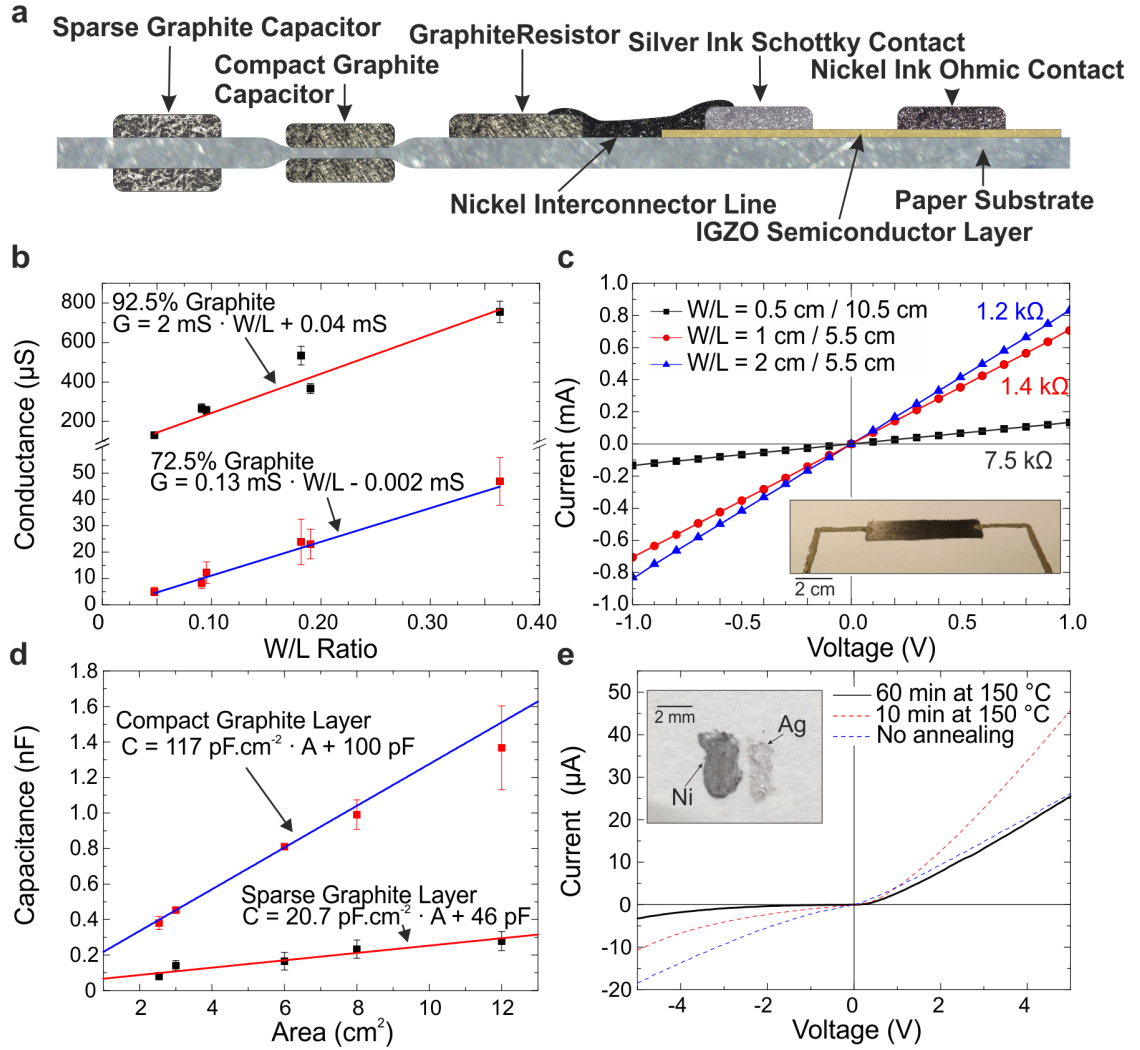


Figure 5.2: Hand written single components. a) Layout of the main components. Graphite films were drawn using $(92.5 \pm 2.5)\%$ and $(72.5 \pm 2.5)\%$ graphite content pencils. Ohmic contacts between different structures were achieved through pen-written Ni tracks. Silver and nickel metallic inks were used to deposit Schottky and Ohmic contacts on a paper substrate coated with a-IGZO. b) Conductance as a function of the width to length ratio of graphite resistors fabricated using pencils with graphite contents of 92.5 % (30 samples) and 72.5 % (30 samples). The specific conductance value for high and low graphite to clay ratio resistors is $(500 \pm 31) \Omega/\square$, and $(7.7 \pm 0.4) \text{ k}\Omega/\square$, respectively. c) IV measurements for three different W/L ratio resistors. The linear behavior indicates an Ohmic contact between nickel and graphite. d) Capacitance of capacitors manufactured from sparse and compact graphite layers. e) IV curve of a Schottky diode fabricated through pen-written Ag and Ni contacts on a-IGZO coated paper. The turn on voltage is 0.6 V. The increase of the rectification ratio after annealing is attributed to the formation of AgO_x at the interface between Ag and a-IGZO.

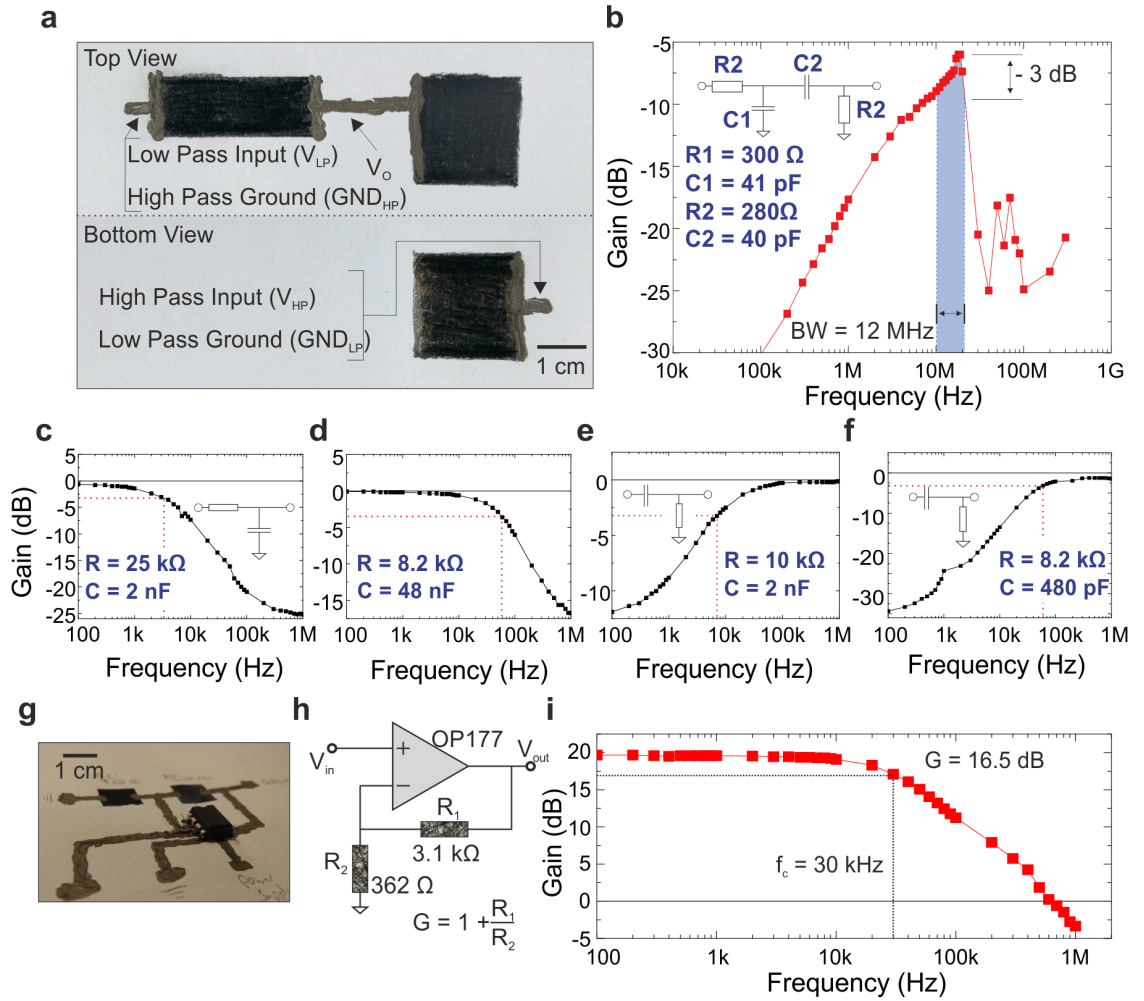


Figure 5.3: Hand written circuits. a) Layout of frequency filters. These devices were developed using graphite and Ni conductive pens. The Top view shows a resistor and one contact of a capacitor, the bottom view shows the opposite side of the paper substrate and hence the second contact of the capacitor. Top view - pictures of the side of the paper where the resistors and tracks were drawn, bottom view - opposite side of the paper. b) and c) 3 kHz and 60 kHz low pass filters. d) and e) 7 kHz and 60 kHz high pass filters. f) 13.56 MHz band pass filter. The blue area indicates the bandwidth of the device (12 MHz). g) Integration of the rigid amplifier on the paper substrate. The amplifier circuit is fixed on paper using the Ni metal ink. h) Schematic of the circuit. This circuit consisted of two resistors of $3.1 \text{ k}\Omega$ and 362Ω that connected to the amplifier in a non inverting configuration. i) Bode plot for this system showing a cut-off frequency of 30 kHz and a gain of 16.5 dB

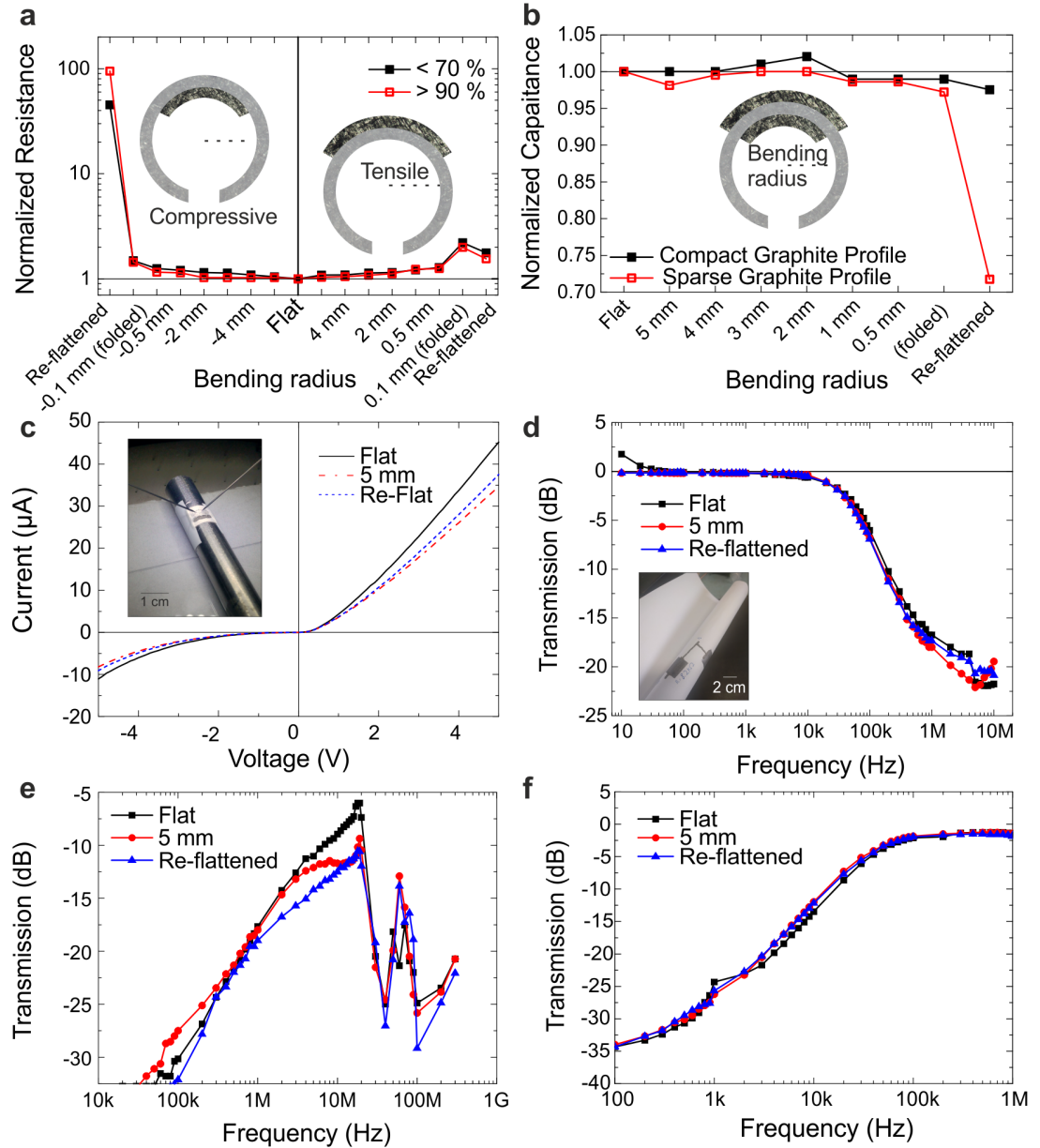


Figure 5.4: Hand-written components and circuits under bending stress. a) Variation of the normalized resistance of resistors down to radii of 0.1 mm (complete folding), and subsequent re flattening. b) Response of hand-written capacitors to bending. c) IV characteristic of a hand written Ag/a-IGZO/Ni Schottky diode measure while flat bend to a radius of 5 mm and re-flattened. The On current of the device decreases by 23% when bent, but recovered to 83% of the initial value after re-flattening. Since the Off current behaves similar, the rectification ratio remained nearly constant. Low (d), band (e) and high (f) pass filters tested under the same bending conditions as the diodes. Both the low and the high pass filters show no performance variation. The band-pass filter shows a decrease in the transmission of the input signal of -4 dB while the cutoff frequencies stay constant.

Chapter 6

Towards the development of a flexible Electric Potential Sensor

Chapter 6 discusses the development and characterisation of an encapsulated electric potential sensor based on an a-IGZO TFT bootstrapped cascode buffer amplifier. Here, it is demonstrated that the devised system can detect electric fields through the thick 50 μm polyimide substrate using a fully capacitive, and hence non-contact, coupling. The presented approach can be implemented in other systems to enable the capacitive measurement of electric fields with lower frequencies. This chapter was presented at IEDM 2020 and is currently waiting for the release of the proceedings.

6.1 Introduction

There is an increasing focus on the development of flexible, unobtrusive and ubiquitous sensors. This has been largely motivated by the advantages of such devices for the growing IoT, wearable and health tracking markets. In this context, flexible sensors that can measure electric potentials with high accuracy, minimum noise and minimum signal drift can find applications in e.g. neonatal health monitoring [184]. However, these are mostly based on resistively coupled sensors which typically require conductive gels to reduce the contact resistance between the signal source and the sensor [185]. On the other hand, flexible capacitive sensors do not require conductive gels and enable the development of devices encapsulated with materials that can be biocompatible and corrosion resistant [186]. However, capacitive sensors also require an ultra-high input resistance and ultra low input capacitance, which is not easily achievable with flexible thin film transistors (TFTs). This is necessary to prevent the attenuation of the input signal due to the weak coupling

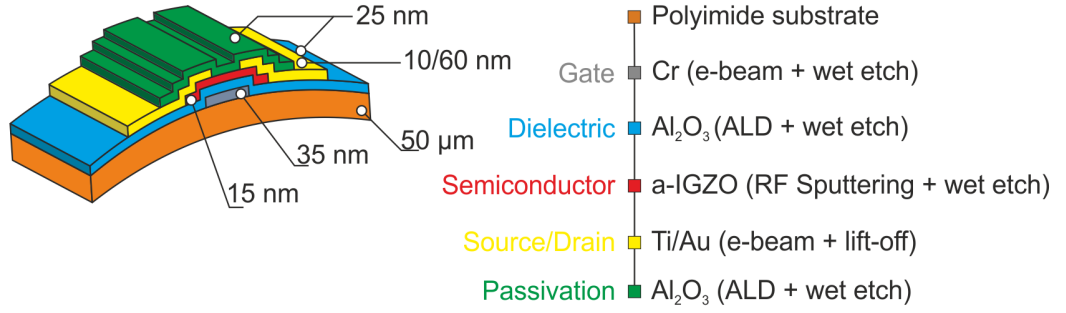


Figure 6.1: Layer structure of the utilized passivated a-IGZO bottom gate, top contact thin film transistors. All devices were fabricated with a maximum temperature of 150  C.

between the source and the sensor. Here, we show an encapsulated flexible capacitive sensor fabricated using amorphous InGaNZnO (a-IGZO) TFTs. a-IGZO was chosen as it can be fabricated at low temperatures and presents a good trade off between electrical performance and process ease when compared to other flexible semiconductors [14]. The developed capacitive sensor is achieved by implementing a source follower buffer with a bootstrapped cascode configuration. The implemented cascode configuration is used to increase the input impedance (Z_{IN}) of the sensor system [187]. Furthermore, by adding a bias element to bias the input transistor, we demonstrate a further increase in Z_{IN} . Here, the objective is not to add any gain to the measurements, since this can be added afterwards [69], but to reduce the attenuation of the input signal by virtually increasing the input impedance of the capacitive sensor.

6.2 Thin-film transistor technology

All devices were fabricated on a free standing 50  m thick polyimide foil with a bottom gate, inverted staggered, configuration. The fabrication steps are summarized in Fig. 6.1. No annealing step was performed on the final devices. Representative transfer, output and CV curves of the devices are shown in Fig. 6.2a,b and c, respectively. These devices presented V_{TH} , μ_{FE} , I_{ON}/I_{OFF} , S and C_{ON} of 0.2 V, 11 cm²V⁻¹s⁻¹, 10¹⁷, 120 mV/dec and 4 nF/mm² (1 kHz) [69]. Fig. 6.2d shows the impact of bending on a representative TFT. For the maximum strain of 0.6 %, corresponding to a 4 mm bending radius, V_{TH} decreased by less than 0.1 V.

6.3 Flexible capacitive sensor circuit design

The capacitive sensor presented in this work consists of a novel flexible bootstrapped cascode input stage with an active impedance biasing element entirely fabricated using a-IGZO technology. In Fig. 6.3, transistors T1 and T2 have a W/L of 410/10 μm , T3 and T4 have a W/L of 112/10 μm , T5 has a W/L of 40/10 μm , and T6 and T7 have a W/L of 10/8 μm . A representative photograph of the final system attached to a user's finger is shown in Fig. 6.3a. Fig. 6.3b shows a micrograph of the full circuit. Including the input pad, this system occupied an area of 13.8 mm². A major feature of this system is that it is completely encapsulated while still being able to measure AC signals through thin insulating materials, as is pictured in Fig. 6.3c. Fig. 6.3c also illustrates the presence of the output guard. The purpose of this element is to surround the input pad by an element connected to the output of the sensor. Given the source follower configuration, the input of the device should follow the input signal and as such the voltage difference between the input pad and the output guard should be minimal, which results in a decrease of the parasitic capacitance of the input pad. Regarding the circuit blocks shown in 6.3d, the biasing element/cascode buffer combination works as a high input impedance signal buffer and the current mirror acts as a stabilization element. Here, the two main blocks of the circuit are:

- Cascode input stage (T1, T2, T3)
- Active bias element (T6, T7)

The cascode input stage follows a standard source follower configuration with an ideal voltage gain (V/V) of 1. The purpose of this stage is to provide a high input impedance interface in order to reduce the attenuation of the input signal. In the Cascode input stage, the capacitance between the input TFT's (T2) gate and S/D terminals is minimised when compared to a standard voltage amplifier based on unipolar amorphous metal oxides. This is because the drain and source of T2 both follow the gate terminal. Figure 6.4a illustrates the operation of this circuit. In comparison, an inverter amplifier would have the drain voltage increase with a decrease in gate voltage, and vice versa. This seesaw effect would result in a larger potential across the Gate-Drain equivalent to the gain of the amplifier, which in turn would increase the parasitic capacitance of the input stage. As shown in Figure 6.5, the coupling capacitance $C_{coupling}$ forms a voltage divider with the input capacitance C_{IN} and a high pass filter with the input impedance R_{IN} . For this reason, it is imperative to decrease C_{IN} (ideally to atto-Farad range) and increase

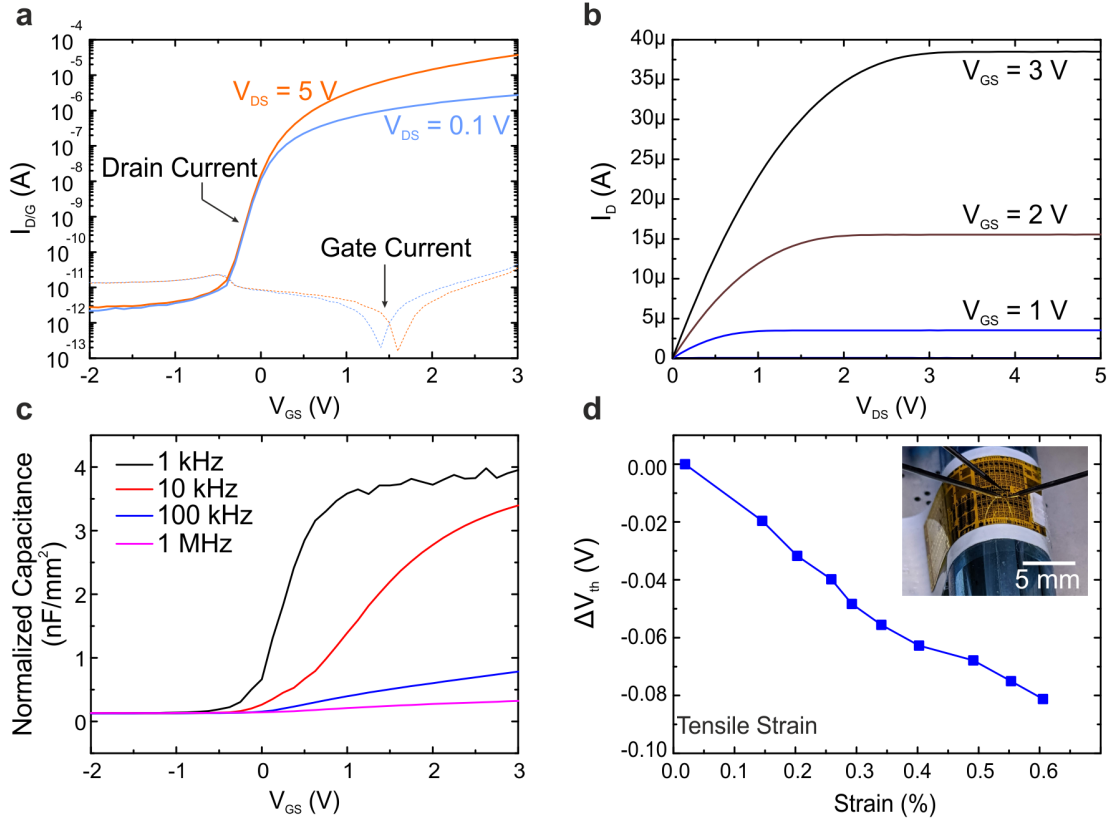


Figure 6.2: Single TFT device performance. a) Representative transfer curve of one of the fabricated a-IGZO TFTs. W/L ratio is $280 \mu\text{m}/115 \mu\text{m}$. b) Representative output curve of one of the fabricated a-IGZO TFTs. W/L ratio is $280 \mu\text{m}/115 \mu\text{m}$. c) Representative CV gate capacitance of one of the fabricated a-IGZO TFTs. d) Effects of tensile strain on the threshold voltage of a representative TFT.

R_{IN} (ideally to tera-Ohm range) in order to reduce the attenuation of the input signal. Reducing C_{IN} and increasing R_{IN} is equivalent to increasing the overall input impedance Z_{IN} . However, when Z_{IN} is very high, even small values of gate leakage current can result in large accumulated charges which lead to drift in the output signal. This signal eventually saturates the output and the signal becomes independent of any changes in the input. For this reason, it is necessary to add a high impedance path to ground for this AC current to flow. Here, we used T6 and T7 as two back to back diode connected TFTs to provide a high impedance path to ground. An exemplification of the exact current path is shown in Figure 6.4b.

6.4 Flexible capacitive sensor characterization

A 5 V_{pk-pk} input signal was applied from beneath the 50 μm thick polyimide substrate by placing the flexible capacitive sensor on top of a copper tape connected to a Philips PM5139 function generator. Given that the input pad has a 4 mm^2 area and considering a relative dielectric constant of 3 for polyimide results in a 2.12 pF coupling capacitance ($C_{Coupling}$). The output of the system was then connected to an external SIM910 processing unit that buffered the output. The output signal was measured using a Rhode&Schwarz RTM2032 Oscilloscope. V_{DD} was set to 3 V for all measurements. To study the effect of different V_{bias} values on the input impedance of the sensor, four main configurations were implemented: positive V_{bias} of 1.5 V, negative V_{bias} of -1.5 V, grounded V_{bias} , and feedback bias i.e. by returning the output of the sensor to V_{bias} . The setup used for the latter is shown in Fig. 6.5. In this case, the output of the sensor was summed to an external voltage of 1.6 V before being fed into the V_{bias} . This offset voltage was chosen as it was seen to maximize the output's amplitude. The capacitive sensor system was also characterized without the bias element by gently removing the connections, resulting in a floating input TFT. This concluded the setup required for capacitively coupled signals. In addition, the circuit was characterized using a resistively coupled input signal. Finally, the sensor was also characterized with both V_{DD} and V_{bias} off to ensure that the acquired signals are not a result of a direct coupling between the input and the output. The power consumption of this sensor was measured to be 145 μW .

6.5 Results and Discussion

In order to assess the ideal performance of our sensor, Fig. 6.6a and Fig 6.6b show the Bode plots when the input signal was DC coupled to the input pad. Here, the signal was attenuated by 3.4 dB when using the feedback bias method. Fig. 6.6c and Fig.6.6d, show the magnitude and phase when the signals were AC coupled to the input signal through the polyimide substrate. The resulting performance and the impact of the different biasing schemes on the capacitive sensor system is summarized in Table 6.1. The input resistance and capacitance were calculated by considering that the $C_{Coupling}$ (2.12 pF) and the input capacitance (C_{IN}) formed a capacitor voltage divider, and that the C_{IN} and the input resistance (R_{IN}) both formed a high pass filter that resulted in the lower 3 dB cut off frequency observed for each graph in Fig. 6.6c. Fig. 6.6e shows the difference between the magnitude of the output signal using the different biasing options and the values

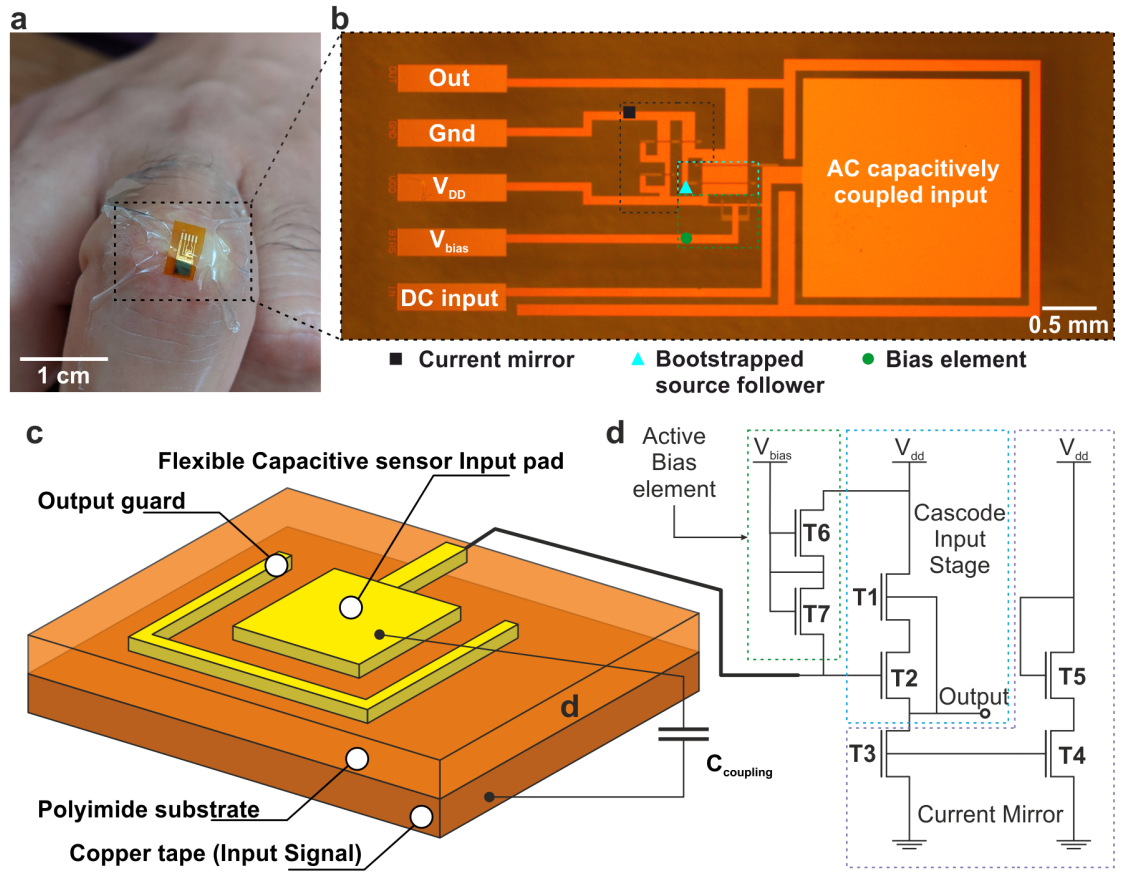


Figure 6.3: A flexible capacitive sensor system enables non contact measurement of AC signals. a) Photograph of a representative system attached to a user’s finger. b) Optical micrograph of the final device. c) Schematic illustrating the capacitive nature of the measurement. d) Circuit schematic of the fabricated flexible capacitive sensor system.

obtained when the system was Off. In the case of the feedback biasing technique, the relative gain is as high as 55 dB, showing that the presented approach effectively increases the input impedance of the system. When characterizing the system in an Off state, the capacitive sensor attenuated the input signal by 49 dB as a result of its high C_{IN} and low R_{IN} of 767 pF and 5.6 k Ω , respectively, which followed a similar behavior when the system was On and the active impedance element was biased with a negative V_{bias} . Using a positive or grounded V_{bias} decreased C_{IN} by more than 6 times and increased R_{IN} by 12 times. However, by using the feedback bias, a significant increase of the magnitude at low frequencies was observed. This is a result of the significant increase in R_{IN} to 2.9 M Ω , a factor of 518 times larger than when the system was off. At the same time, C_{IN} remained relatively constant for both the positive and feedback biasing. This C_{IN} is influenced by the gate capacitance of the input TFT and the bootstrapping topology in parallel with the feedback element capacitance. As such, C_{IN} can be improved by tuning

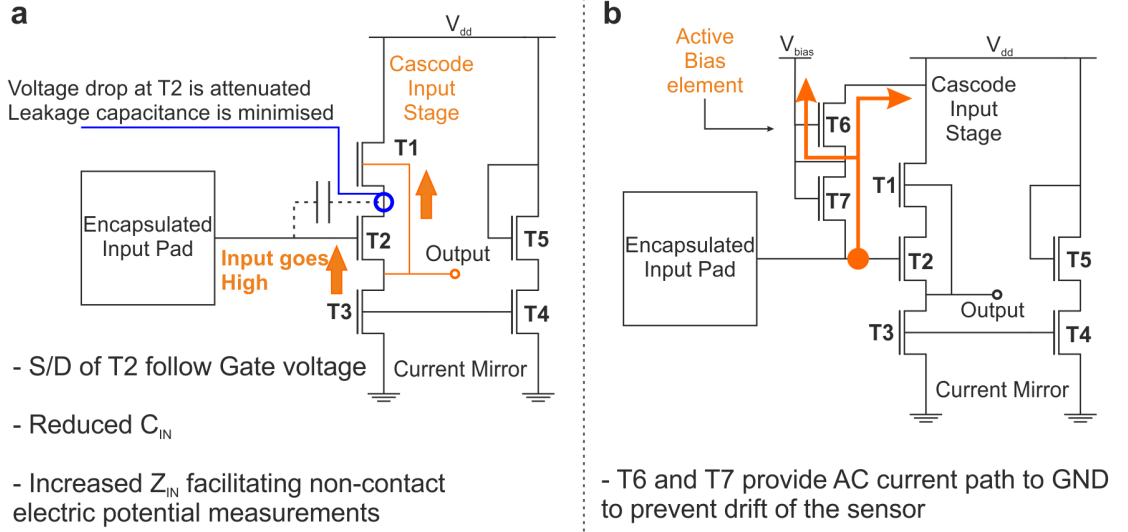


Figure 6.4: Detailed schematic of the operation of the two main components of the flexible capacitive sensor. a,b) Operation of the cascode input stage and AC current path to ground, respectively.

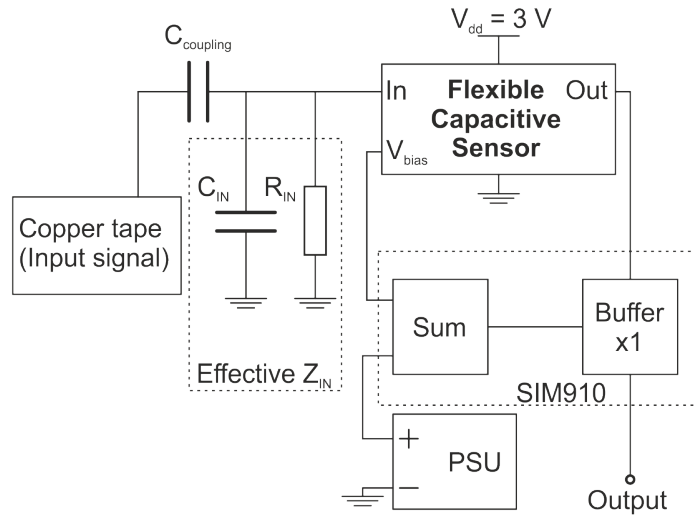


Figure 6.5: Characterization setup utilized to quantify the performance of the developed system. The effective Z_{IN} is visualized. The devices were characterized in the dark and at room temperature.

the device dimensions using e.g. a self-aligned topology to decrease C_{IN} . For the floating input TFT, the capacitance increased to 530 pF, while the resistance remained relatively low, at 811 k Ω . The noise performance of this system was also characterized and is shown in Fig. 6.6f. When On, the system presents a $1/f$ noise typical in a IGZO TFTs. Here, the corner frequency is approximately 37 kHz with $100 \mu V / \sqrt{Hz}$ at 100 Hz. When Off, the noise quickly decreases to lower values. Fig. 6.7a shows examples of 27 kHz signals

measured using the flexible capacitive sensor. This frequency value was chosen as it was observed to be a point where all biasing options showed a relatively high magnitude of the output vs. input signal. At lower frequencies only the feedback bias option yielded values that were not overwhelmed by the $1/f$ noise. The measurement of a 3 kHz AC signal using this method is also shown in Fig. 6.7b. Measurements at lower frequencies of 40 Hz and 60 Hz are also shown in Fig. 6.7c and d, respectively. Finally, to demonstrate the dynamic performance of the presented sensors, we used 3 kHz and 20 Hz arbitrary waveforms as the input signal. As shown in Fig. 6.7e and Fig. 6.7f, the output closely matched the input signal. These results indicate that the presented combination between a bootstrapped cascode and a bias element significantly improves the performance of a capacitively coupled flexible sensor. The input resistance increased and the lower corner frequency dropped from 18 kHz to 450 Hz, compared to using a static positive bias voltage to control the bias element.

6.6 Conclusion

We implemented a bootstrapped cascode buffer with a bias element that significantly improves the performance of flexible capacitive sensors. By using the output of the presented sensor to bias the cascode input stage through an active impedance element, we obtained a relative gain of 55 dB at frequencies as low as 100 Hz. In addition, the system presented a maximum noise of $100 \mu\text{V}/\sqrt{\text{Hz}}$ at this frequency. This improvement was attributed to an increase in the system's input resistance from 68 k Ω when using a static positive V_{bias} of 1.5 V to 2.9 M Ω when using the feedback biasing method. These results show that this method can significantly improve the performance of capacitively coupled AC probes.

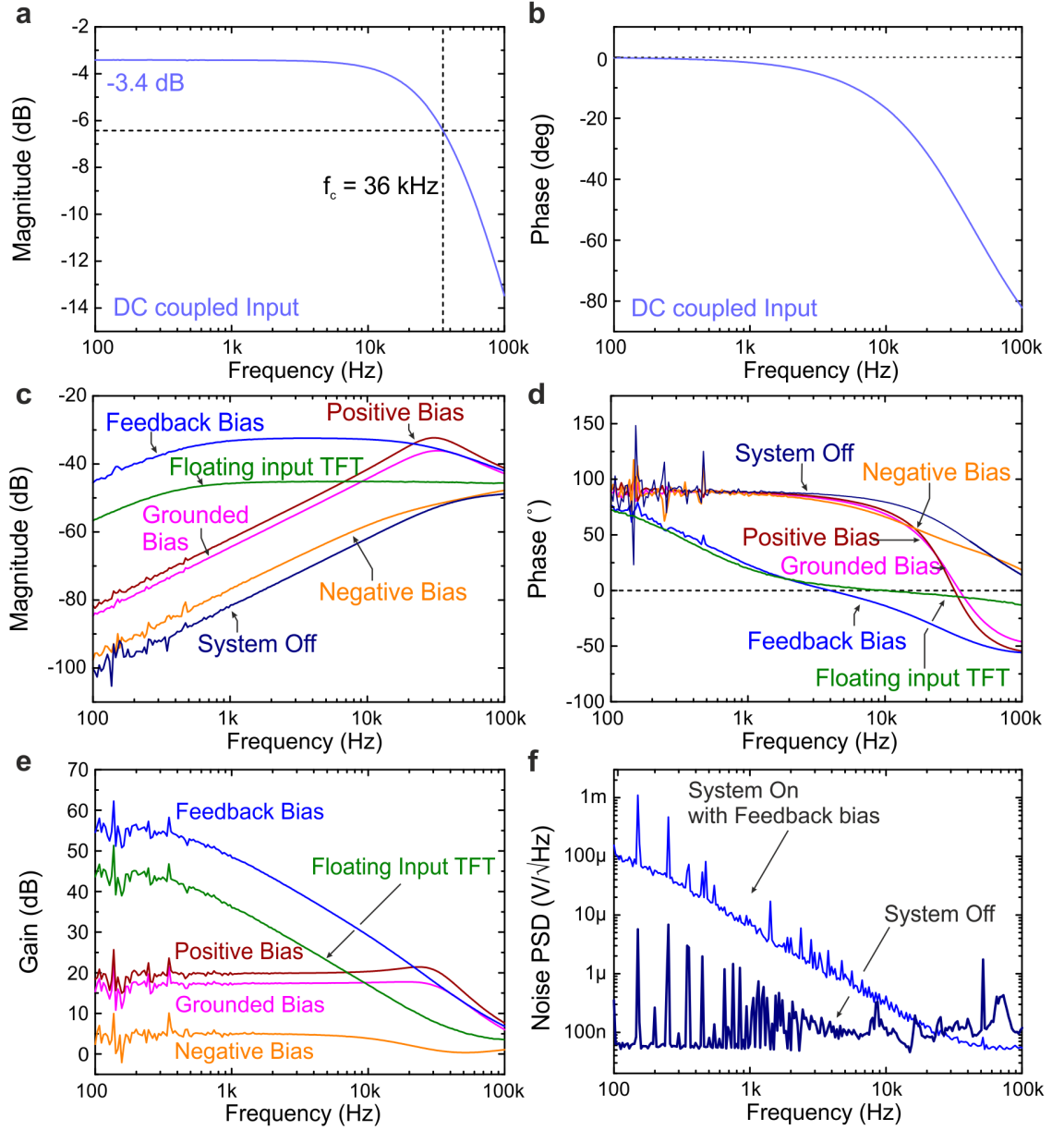


Figure 6.6: System performance. a) Magnitude and b) phase Bode plots for the DC coupled input signal. Here, the signal had a 200 mV_{pk-pk} amplitude. c) Magnitude of the output vs. input signal for a capacitively coupled 5 V_{pk-pk} input signal. Four different biasing options are shown, together with the values obtained when the system was Off and when the input TFT's gate was floating. d) Phase of the output vs. input signal for a capacitively coupled 5 V_{pk-pk} input signal. e) Relative gain of the system obtained by calculating the difference between the magnitude values obtained using the different biasing options and the system in the Off state. f) Power spectral density of the noise for the system on the On and Off states. In the On state the noise is dominated by $1/f$ noise with a 37 kHz corner frequency.

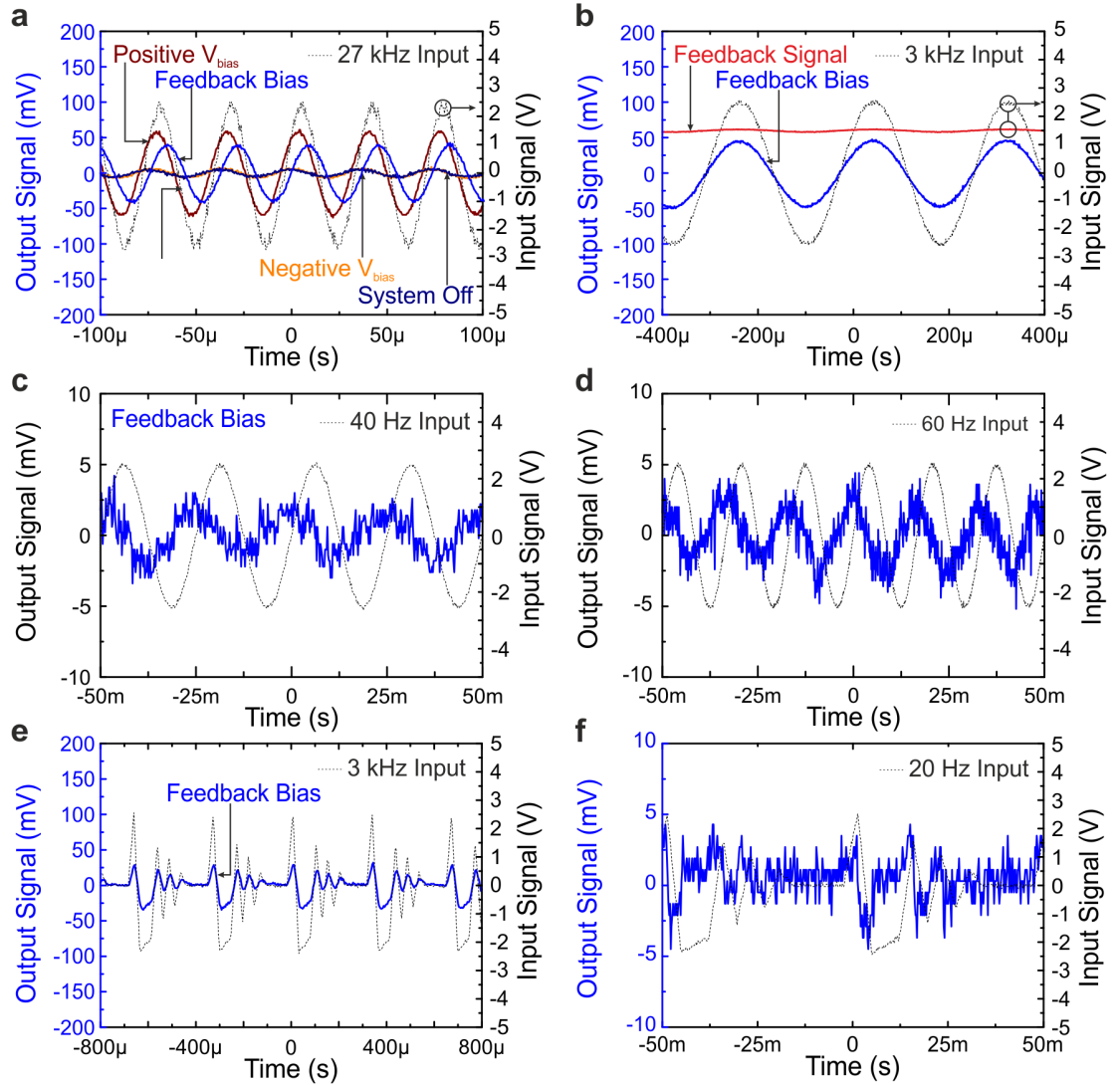


Figure 6.7: Signal acquisition at various frequencies using the encapsulated flexible electric potential sensor. a) Representative 27 kHz signals acquired using the different biasing options. b) Representative 3 kHz signal acquired using the feedback biasing. The feedback signal is also shown. The through substrate capacitively coupled input signal is also shown. Representative c) 40 Hz and d) 60 Hz signals acquired using the feedback biasing method. These measurements illustrate the lower frequency limit of the capacitive sensor system. e) Acquisition of an arbitrary 3 kHz signal using the developed system with the feedback biasing option. f) Acquisition of an arbitrary 20 Hz signal using the developed system with the feedback biasing option.

	R_{IN} (k Ω)	C_{IN} (pF)	Lower f_c (kHz)	Magnitude at f_c (dB)	Bandwidth (kHz)
Bias Feedback	2990	124	0.45	-35.5	0.45 - 32
Positive Bias	68	123	19	-35.4	19 - 50
Negative Bias	4.6	822	42	-51.8	N/A
Grounded Bias	47	186	18	-39	18 - 60
System Off	5.6	767	37	-51.2	N/A
DC coupling	N/A	N/A	0.1	N/A	0.1 - 36
Floating input	811	530	370	-48	0.37 - N/A

Table 6.1: Summary of the performance parameters obtained from the respective Bode plots obtained from the different biasing options.

Chapter 7

Conclusion

Chapter 3 shows that passivating flexible TFTs using a stand-alone layer of Al_2O_3 is not as effective as previously expected. The formation of a hump effect under low gate biasing stress conditions indicates that the passivation can have a role on the degradation mechanisms of a-IGZO TFTs over long periods of time. New passivation materials, and potentially new passivation techniques, should be explored in order to extend the lifetime of such devices. Chapter 4 demonstrates that a-IGZO TFTs built on flexible substrates remain operational down to 78 K and withstand electron irradiation doses of up to $10^{12} \text{ e}^-/\text{cm}^2$ with an electron energy of 34.1 MeV. The resilience demonstrated by these devices extends the potential applications of flexible TFTs to extreme environments, such as the ones found in Low Earth Orbit. Furthermore, the lightweight aspect of flexible electronics could be a further advantage for such applications. Additional studies are required to understand how other high energy particles can influence the performance of a-IGZO TFTs. In chapter 5, an handwritten pressure sensor and testing circuits demonstrate how a simple technique can effectively create electronic devices. Furthermore, this chapter also presents the first partially handwritten diode in literature. The presented principle can be extended to fabricate printed devices with smaller dimensions and different contact materials to further improve the Schottky barrier. Chapter 6 demonstrates a flexible buffer amplifier in a cascode configuration. This device was capable of measuring electric potentials through the 50 μm polyimide substrate. By leveraging the circuit topology and using the device's output as the bias of an input impedance control element, fully capacitive and encapsulated measurements were possible with a relative gain of 55 dB. This approach expands upon the work previously conducted in the University of Sussex on the development of non-contact electric potential sensors. The proposed approach can be improved to allow devices with even larger relative gains and lower noise levels.

Overall this thesis expands the knowledge regarding the stability and resilience of flexible a-IGZO TFTs. In addition, it demonstrated the potential of this technology for the development of various types of sensors. The stability and versatility of this TFT technology confirms its potential for the development of implants or other forms of long-term wearable sensors. While there is no metal-oxide complimentary technology with appropriate performance, the circuits developed to compensate this are shown to be effective enough for the fabrication of active sensors operating at the low frequencies that are relevant in most bio-signals. For applications that require high-frequency operation, devices with shorter channels or new semiconductor materials are required, but this should not be immediately necessary for the development of flexible sensors. In summary, this technology is expected to see a significant increase in customer applications due to its compatibility with large-area production techniques, excellent electrical performance and reliable operation.

7.1 Outlook for flexible electronics

The field of flexible electronics is growing, and with it new and interesting challenges. As of now, most flexible sensors, transistors or other types of flexible devices and systems are only yet available in a lab setting. Some of the challenges that currently need to be addressed in this field are the lack of functional modularity and the lack of an obvious flexible champion material. In typical rigid devices, modular ICs and components are brought together into a board to fabricate an end-product. However, this is not easily done in flexible electronics. One of the reasons for this is that there is not yet a reliable and ubiquitous protocol regarding how to contact flexible devices utilising rigid connectors, let alone a way to connect individual flexible components to each other. With regards to the materials, there is not a clear winner for the spot of best flexible semiconductor. In flexible electronics, each material group, such as organic semiconductors, flexible Si or metal oxides, offers their own set of advantages without really having a definite winning quality. In contrast, Si is one of the most abundant materials on the Earth's crust and allows for both high electron and hole mobility, which made it an obvious choice for the large-scale production of electronic devices. For this reason, hybrid solutions including various type of semiconductor materials in a single flexible substrate are becoming increasingly popular. Finally, there is not yet a flexible sensor or other type of device that has been regarded as a significant improvement over other alternatives. Foldable phones or screens for example are still considered a curiosity with a large price tag, and while flexible brain

sensors and RFID tag already exist, their benefits are not yet clear. However, it is expected that similarly to other technologies and products, flexible electronics will slowly emerge in bespoke applications and then make their way into mainstream applications.

Appendix A

Cover Pages

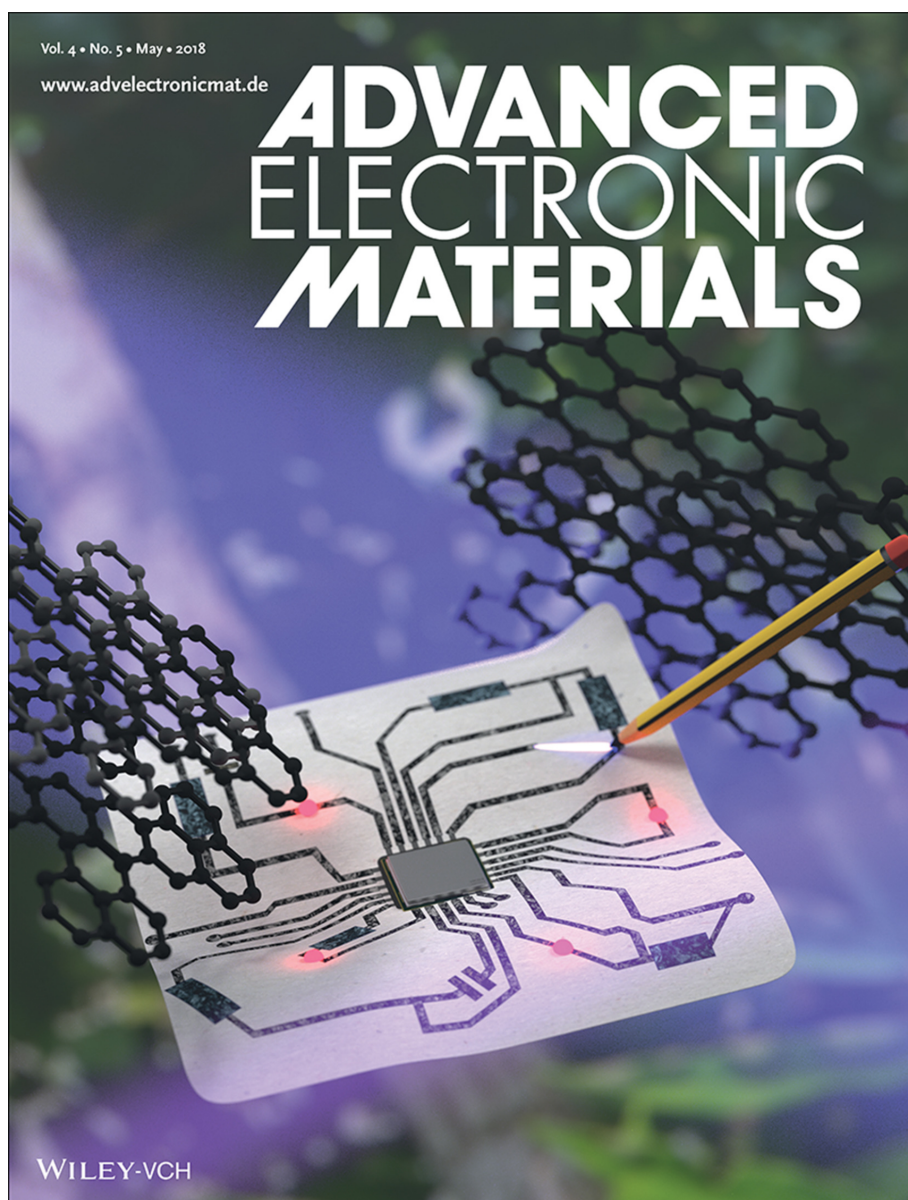


Figure A.1: Cover page on Advanced Electronic Materials 5/2018. [34]

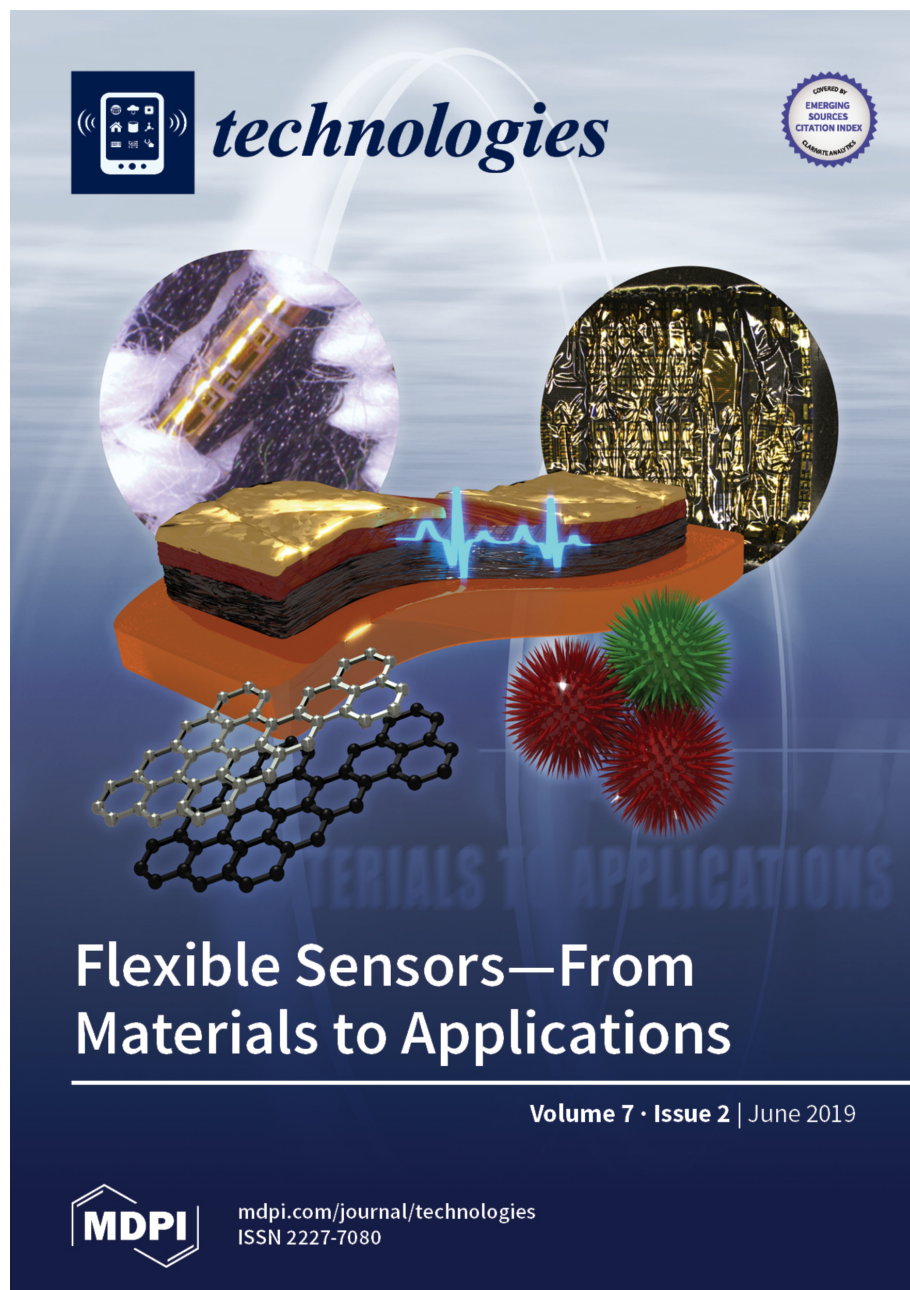


Figure A.2: Cover page on MDPI Technologies Vol. 7 Issue 2 2019. [7]



Figure A.3: Cover page on Advanced Materials Technologies Vol. 6 Issue 2 February 2021.

[81]

Appendix B

Supplementary Info to chapter 2

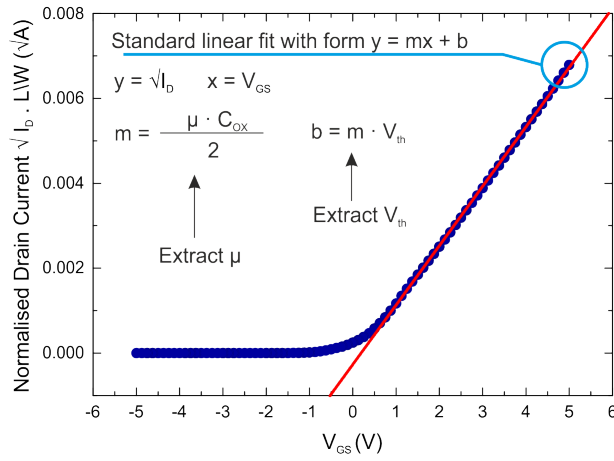


Figure B.1: Example of a linear fitting applied in the ON state of an amorphous InGaZnO TFT with dimensions $W = 280 \mu\text{m}$ and $L = 75 \mu\text{m}$. As shown, the model shows a good agreement with the linear profile of the square root of the drain current for a normalised transfer curve, with a $R^2 = 0.997$.

Appendix C

Supplementary Info to chapter 3

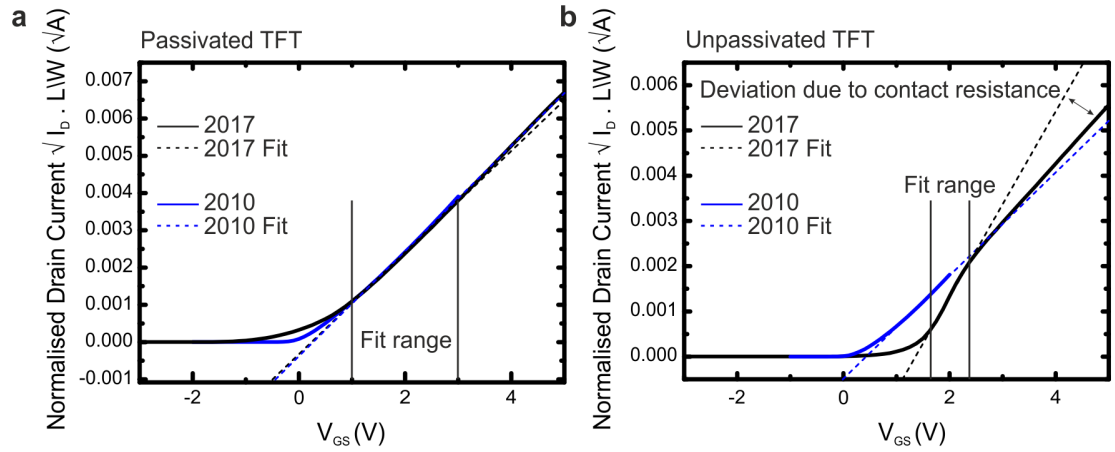


Figure C.1: Fitting of the square root, normalised, saturation curves of passivated and unpassivated TFTs for pristine and aged devices. a) Passivated TFTs. b) Unpassivated TFTs. The fitting ranges were modified in order to have comparable results for aged and pristine devices. In the case of the aged TFTs the fitting excludes the component which includes significant contribution from contact resistance. Here, the R_2 was never smaller than 0.99.

Appendix D

Supplementary information to chapter 5

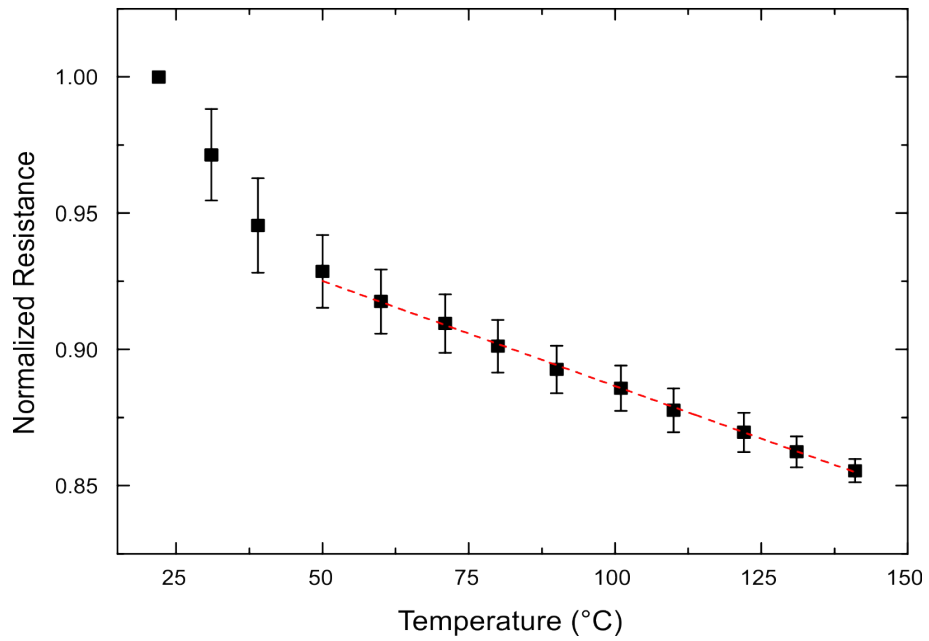


Figure D.1: Alternative pencil-written sensor. The thermoresistive behavior of the drawn graphite films was studied to develop a temperature sensor. As graphite has semiconductor properties, its resistance decreases with the increase in temperature. Here, two consecutive rising and decreasing temperature cycles are shown. The resistor was annealed at 180 °C for 10 min before the measurements. This sensor shows a linear behavior for the range of 50 °C to 140 °C, and a sensitivity of $7.7 \times 10^{-4} (\Omega/\Omega_0)/^\circ\text{C}$, where (Ω_0) was used to normalize the data and represents the initial resistance value.

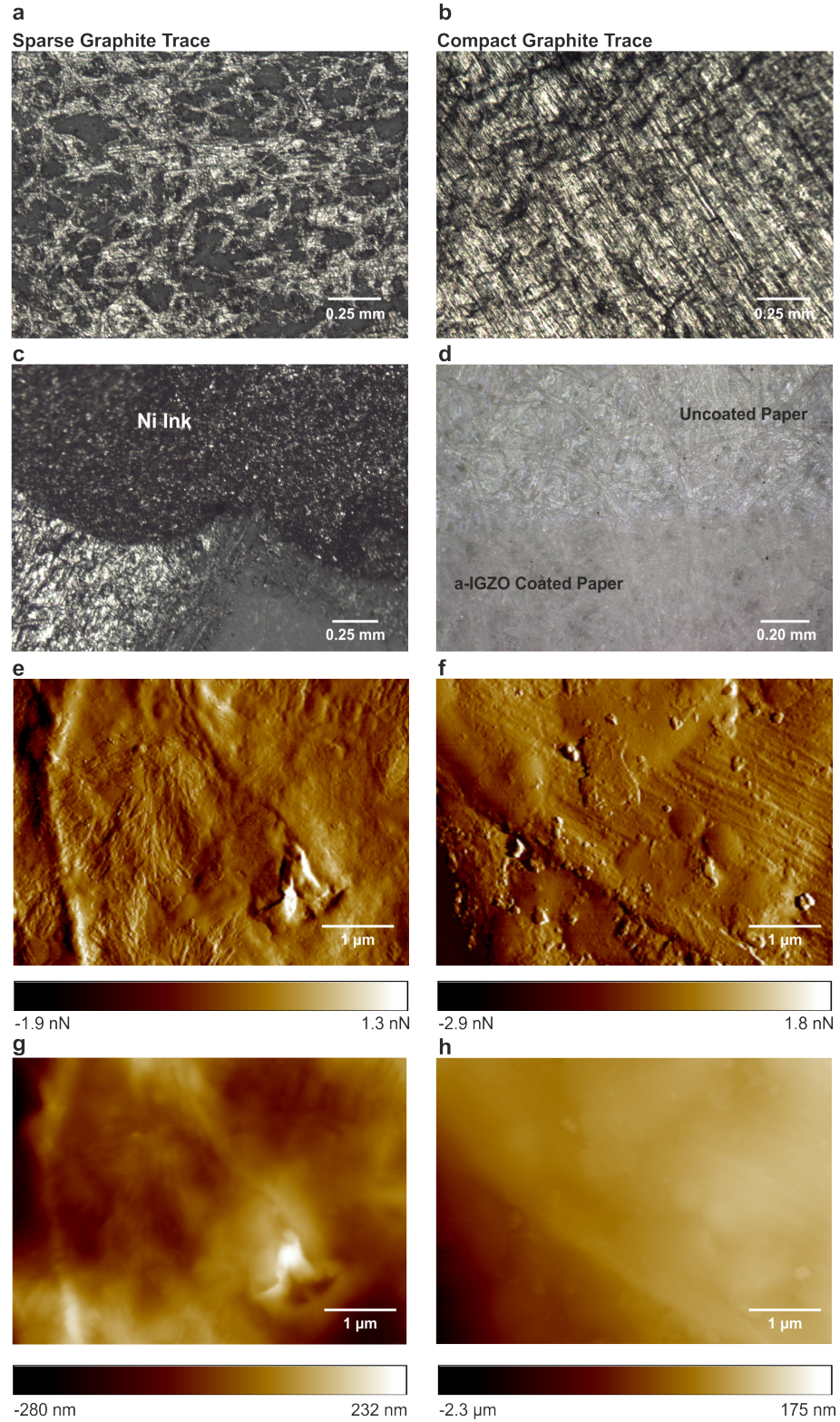


Figure D.2: Optical and AFM images of the samples' surface. a) Sparse graphite contacts show only 45 % coated area, whereas compact graphite contacts show a continuous graphite layer (b). c) Interface between Ni ink, graphite and paper. d) Optical imaging of the separation between the a-IGZO coated paper (darkened area on the bottom) and the uncoated paper (top). e) and f) AFM peak force error imaging of coated areas of the paper. g) and h) AFM height maps of the same areas examined in (e) and (f).

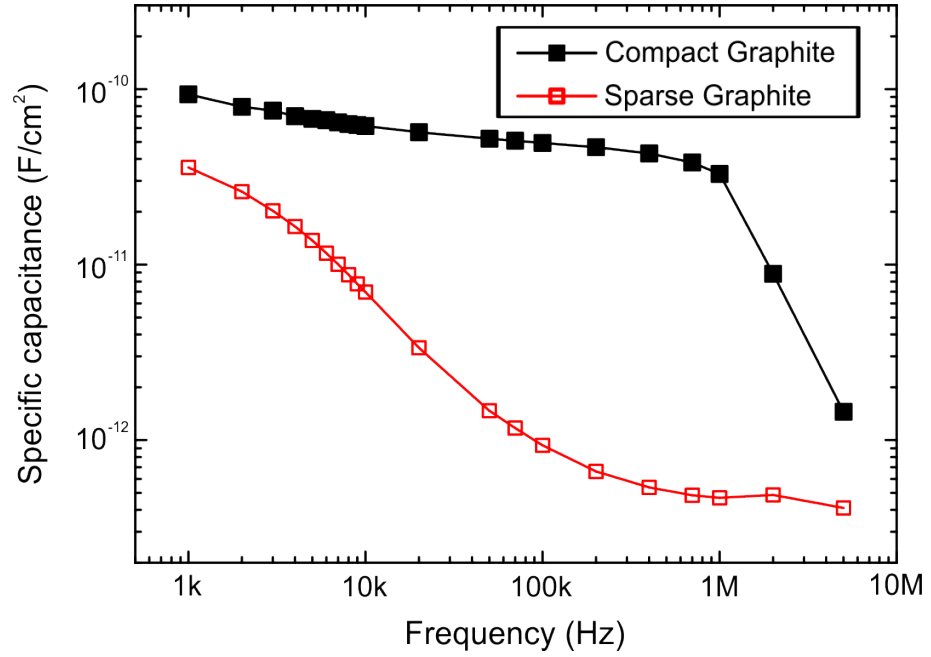


Figure D.3: Specific capacitance as a function of frequency for sparse and compact graphite capacitors. Sparse graphite capacitors present a larger sensitivity to the increase of frequency. This is due to the higher resistivity ($>1\text{ M}\Omega$ compared to $1\text{ k}\Omega$) of sparse graphite capacitor plates when compared to their compact graphite counterparts.

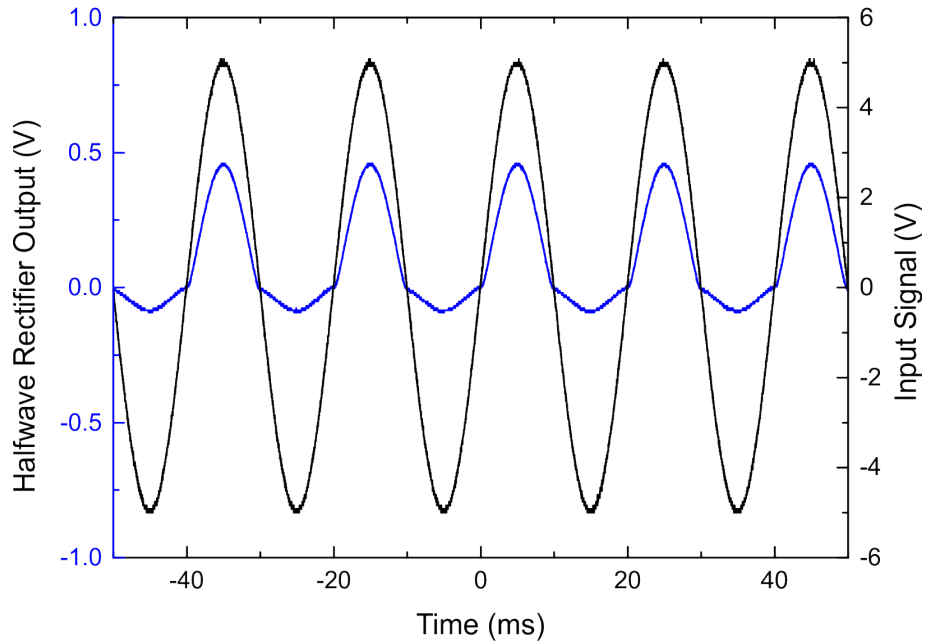


Figure D.4: Rectified 10 V peak to peak 50 Hz signal using a pen written Schottky rectifier. The observed attenuation results from the difference in resistance between the output resistor of $70\text{ k}\Omega$, and the diode ($750\text{ k}\Omega$). This device presents a current rectification ratio of 1:5, matching the values obtained for the single diodes.

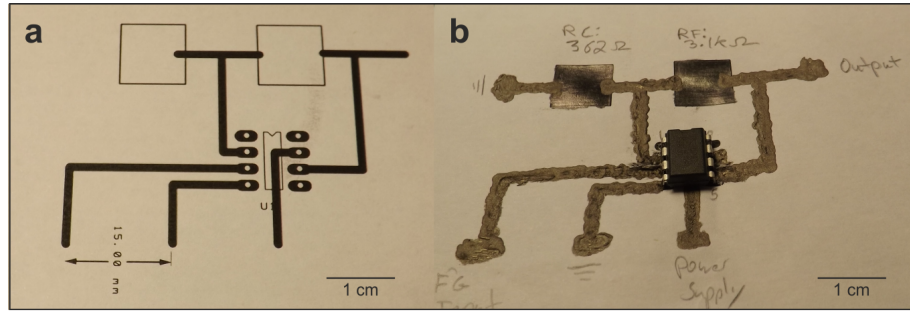


Figure D.5: Paper PCB schematic used for the fabrication of a non-inverting amplifier based on handwritten graphite resistors, an off-the-shelf amplifier IC, and nickel interconnecting lines. a) The layout schematic indicates the areas to fill with graphite, as well as the position of the pins of the voltage amplifier. The black lines indicate where to draw the Ni connecting tracks. b) This amplifier exhibits a gain of 19.5 dB, and a cut-off frequency of 30 kHz.

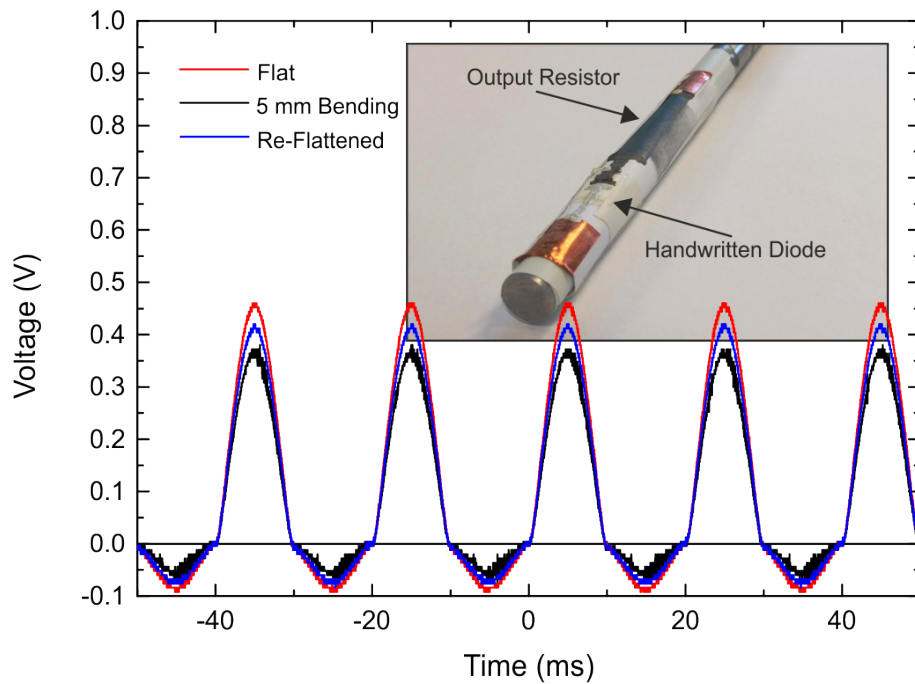


Figure D.6: Electrical response of the half-wave rectifier under bending stress. This device presents similar results as single diodes when rectifying a 50 Hz 10 V peak to peak signal. When bent to a radius of 5 mm, both the On and Off current decrease by 23 %, resulting in a constant rectification ratio. When re-flattened, the On and Off current reverted to 88 % of their initial values.

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